ELECTRICAL AND FLUIDIC INTERCONNECT DESIGN AND TECHNOLOGY FOR 3D ICS

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ELECTRICAL AND FLUIDIC INTERCONNECT DESIGN AND TECHNOLOGY FOR 3D ICS

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SUMMARY

For decades, advances in device scaling has proven to be critical in improving the performance and productivity of 2D systems. In this thesis, we explore how advances in technology have pushed functional integration to such a high-level that interconnection and packaging issues represent real barriers to further progress. While three-dimensional (3D) integration offers to be a potential contender to overcome the barriers of increased energy consumption due to interconnects and bandwidth limitations, there are certain challenges that must be overcome before systems can be successfully stacked. Cooling and power delivery are among these key challenges in the integration of high performance 3D ICs. To address these challenges, microchannel heat sinks for inter-stratum cooling and through-silicon vias (TSVs) for signaling and power delivery between stacked ICs were explored. Novel integration schemes to integrate these fluidic and electrical interconnects in conventional CMOS processes were also explored. Compact physical modeling was utilized to understand the tradeoffs involved in the integration of electrical and microfluidic interconnects in a 3D IC stack. These concepts were demonstrated experimentally by showing different CMOS compatible methods of fabricating microchannels and integration of high aspect ratio ($\sim$20:1) and high density (200,000/cm^2) electrical TSVs in the fins of the microchannels for signaling and power delivery. A novel mesh process for bottom up plating of high aspect ratio TSVs is also shown in this work. Fluidic reliability measurements are shown to demonstrate the feasibility of this technology. This work also demonstrates the design and fabrication of a 3D testbed which consists of a 2 chip stack with microchannel cooling on each level. Preliminary testing of the stack along with interlayer electro-fluidic I/Os has also been demonstrated.

CHAPTER I

INTRODUCTION

The rapid growth and transformation of the electronics industry is based on the evolution of integrated circuit (IC) technology to provide improvements in cost per function, size, and performance. Gordon Moore, in 1965, observed that the total number of devices (per unit area) on a chip doubled every 12 months [64]. He predicted that this trend will continue in the 70's, but will slow in the 80's, where the total number of devices will double every 24 months [63]. His empirical observation is called ***Moore's Law***. A graph indicating the transistor count per die over the years is shown in Figure 1.

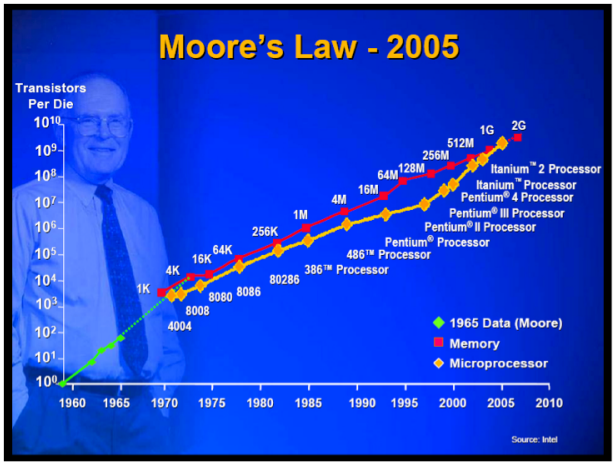


Figure 1: Transistor count over technology generations as predicted by Moore's Law [32].

In 1974, Robert Dennard and his team reported the mathematical insight into the optimal way to scale transistors for generations to come. The scaling principles described by Dennard were quickly adopted by the semiconductor industry as the road map for providing systematic and predictable transistor improvements [9]. Dennard's paper summarized the transistor or circuit performance changes under ideal scaling

Table 1: Scaling Results for Circuit Performance [23].

Device or Circuit Performance	**Scaling Factor**
Device dimension t_{ox}, L, W	$1/\kappa$
Doping concentration N_d	κ
Voltage V	$1/\kappa$
Current I	$1/\kappa$
Capacitance $\epsilon A/t$	$1/\kappa$
Delay time CV/I	$1/\kappa$
Power dissipation CV^2	$1/\kappa^2$
Power density VI/A	1

conditions, where κ is unit less scaling factor, as shown in Table 1. If all dimensions, voltages, and doping levels were scaled by κ, the circuit delay was decreased by κ and the power/circuit decreased by κ^2. Further, the power/unit area of silicon remained constant. As a result, as the device size reduced, transistors switched faster and consumed lesser power.

Despite the several advantages offered by scaling, the physical limits of silicon devices and interconnects are fast approaching. Several secondary effects that were neglected earlier, now pose a serious threat to system performance. The following sections cover the challenges and possible solutions to combat these issues.

1.1 Issues with Device Scaling

A central CMOS scaling problem is managing the conflicting requirements of reducing the transistor area, the dynamic power, and the off-state power consumption, while increasing the circuit performance [69]. Below are some critical issues that need to be addressed at the transistor level to improve system-level performance [5, 47]:

1. The aggressive scaling of gate oxide has forced it to reach thicknesses in the order of a few atomic layers. This has resulted in an increase in the gate tunneling current, leading to large leakage and consequently heat generation.

2. The reduction in threshold voltage, V_{th}, increases the device off current. As devices scale down, leakage power has a larger share in the total power consumed. Figure 2 details the increasing contribution of passive power to the total power. As seen, it accounts for around 5%-10% of power budget at 180nm, 20%-25% at 130nm and 35%-60% at 65nm.

3. As the FET channel length is scaled below a critical value, the subthreshold power rolls up exponentially. This reduces the transistor current drive and switching speed.

4. As devices scale down, the control of critical dimensions becomes difficult and tolerance demands increase. This in turn affects the manufacturing yield and cost of production.

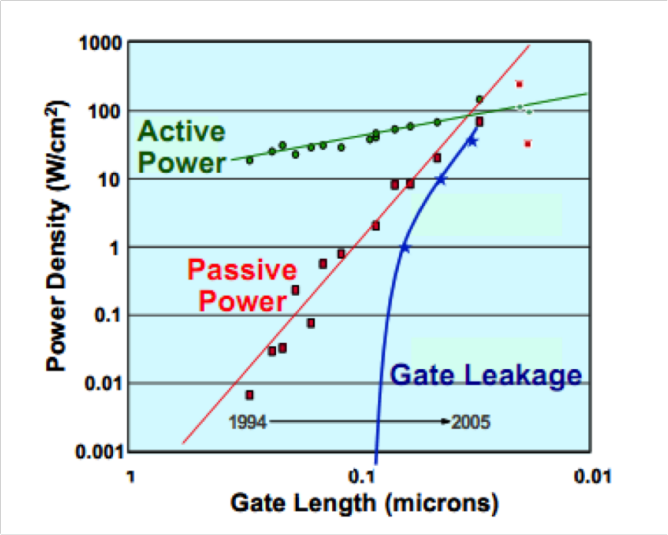


Figure 2: Contribution of passive power to the total power [17].

In order to combat the issues with device scaling, a number of new technologies have evolved to keep device scaling on track as predicted by *Moore's law*. Mobility enhancement techniques such as stress engineering have been attractive for performance enhancements beyond those derived from pure scaling. These include strained-silicon growth, use of SiGe source drains [62, 9], and dual-stress liner [66]. However, most

Table 2: Scaling of interconnects [23].

Parameter	**Scaling Factor**
Line resistance, $RL{=}\rho L/W_t$	κ
Normalized voltage drop, IRL/V	κ
Line response time, RLC	1
Line current density, I/A	κ

of the stress elements utilized since 90nm node are geometry dependent and do not scale well with shrinking pitch. In 2007, high-k dielectrics and metal gates in MOSFETs replaced the SiO_2 dielectric and polysilicon gates [61]. This provided more than 20% improvement in transistor switching speed and reduced transistor gate leakage by more than tenfold [1]. However, additional enhancements beyond high-k/metal gate technology will be needed to further augment gate length scaling and to provide sufficient short-channel control. In spite of improvements in materials and processes, transistors have already reached nanoscale dimensions, and given the aggressive pace of Moore‘s law it seems possible that transistors may hit physical scaling limits within the next ten years [69].

1.2 On-chip Interconnect Scaling Implications

To meet the demands of a technology node, interconnect cross-sectional dimensions are scaled at the same rate as gate dimensions. The scaling of interconnects as described by Dennard is seen in Table 2. In contrast to scaled transistors that improve performance and reduce cost, scaled interconnects increase latency and energy dissipation leading to performance degradation [60]. As a result, the performance of an IC is increasingly being limited by the on-chip interconnects rather than transistors.

These constraints have been addressed by adding more metal layers, changing to interconnect materials that are more conductive (such as Cu), and using low-k dielectrics to reduce resistance and capacitance per unit length, which in turn improves

interconnect speed. However, the ITRS low-k dielectric roadmap implementation has been delayed due to several technical challenges. In addition, Cu resistivity increases with continued scaling due to grain boundary and interface electron scattering [4]. Clearly, delay caused by interconnects is no longer negligible and interconnect performance plays a big role in the overall system performance, seen in Figure 3.

Furthermore, signal integrity issues due to scaling increase as cross talk noise between the interconnects increases as shown in [81]. Scaling also adversely affects reliability of interconnects due to electromigration issues. For the same current density, the electromigration performance is expected to degrade with scaling due to the increased relative importance of Cu-interface effects [58].

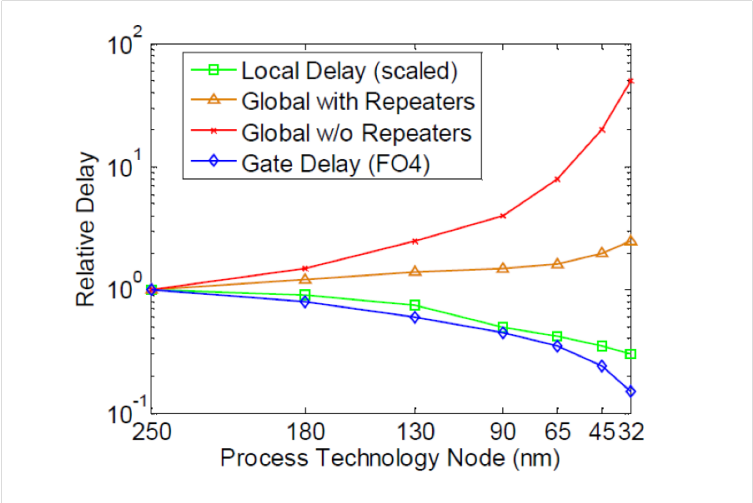


Figure 3: Comparison of delay due to gate and interconnects [4].

1.3 Progress in Ancillary Technologies

So far, scaling and its implications on system performance based on monolithic nanoelectronic silicon technology which includes devices and on-chip interconnects were discussed. However, the total system performance also depends on ancillary supporting technologies such as power delivery system, heat removal, and off chip signaling. Figure 4 highlights current silicon ancillary technologies.

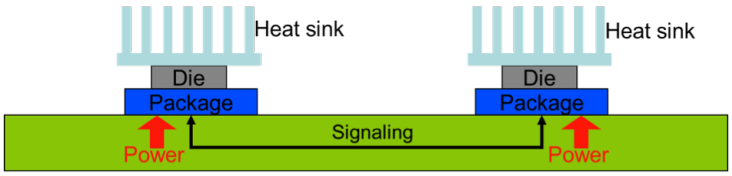


Figure 4: Current ancillary technologies for Silicon [6].

The progress of silicon technology beyond the 45nm node has been a great challenge. This is because the performance of systems has struggled to reach the intrinsic limits of each particular generation of technology. A major reason for this failure is that the capabilities of ancillary or supporting technologies, such as cooling, power delivery, and signaling, that are significant for overall system performance have not been explored at the same pace as the monolithic nanosilicon technology [5]. These critical issues are described in detailed below.

Heat removal challenges: Power dissipation has increased consistently over the different generations of microprocessors as shown in Figure 5. In order to function reliably, an adequate cooling solution is needed. Historically, air-cooling has been used to remove the heat generated from high performance chips. However, as the feature size of a silicon transistor has been decreasing, the demand to attain a smaller junction-to-ambient thermal resistance (R_{ja}) has resulted in the thermal I/O (heat sink) to scale bigger. The lowest attainable thermal resistance from an air-cooled heat sink, after using the best available materials for all the thermal interconnects between the silicon die and the ambient, is approx. 0.5 °C/W [5]. The ITRS roadmap has projected that the R_{ja} requirement for cooling future high performance ICs will be <0.2 °C/W, which shows that the heat removal demands cannot be satisfied by existing air-cooling solutions [4].

Power delivery: The primary objective of the power delivery network is to distribute power efficiently to all transistors on a chip while maintaining an acceptable

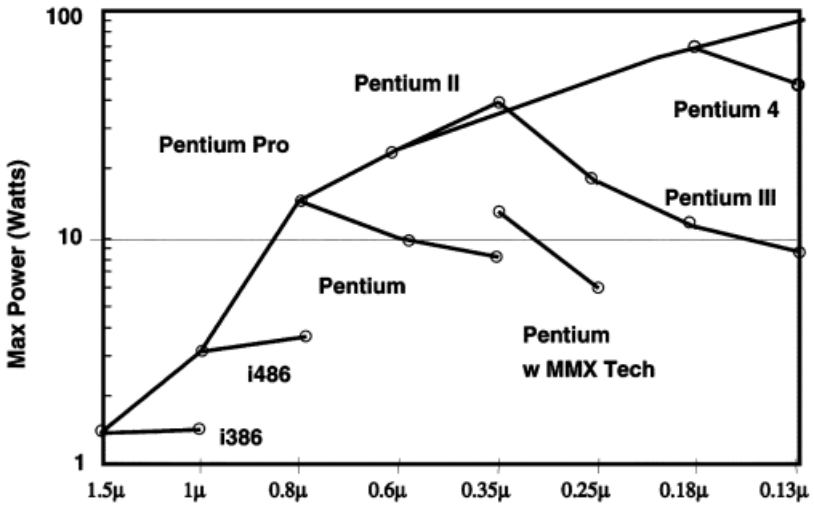


Figure 5: Maximum power dissipation of several microprocessors [11].

level of power-supply noise. With increasing power dissipaiton and decreasing supply voltage, the supply current has increased, reaching a value greater than 100A for some microprocessors [5]. It is a challenge to efficiently deliver such high currents from an off-chip DC-DC converter to transistors on the integrated circuit through parasitics of the packaging and on-chip interconnects. The empirical acceptable power-supply noise is typically 10% to 15% of the supply voltage. As supply voltage continues to scale, logic circuits become increasingly sensitive to power-supply noise. Excessive supply noise can severely degrade the performance of the system by introducing gate delay variation, logic failures, false switching, and signal integrity challenges [80].

Signaling: Another metric to improve the speed of modern day computing is the increase in clock frequency. Clock frequencies peaked a few years ago and have remained quite flat since then [51]. Chip designers realized that it is no longer worth the cost in terms of power consumed and heat dissipated to increase the clock frequency. Intel has termed this the *speed/performance tradeoff* and it is the motivation for transitioning to multicore processors which integrate multiple cores onto a single chip [70]. As the multicore processor performance improves, it requires higher bandwidth and low-latency memory [35].

1.4 Three Dimensional System Integration

To keep up with ever increasing system integration demands, it is imperative that developments in silicon ancillary technologies be accelerated. To this end, 3D system integration ushers a new era of technology convergence between on-chip interconnects and packaging [49]. 3D integration consists of stacking and vertically interconnecting several layers of active circuits. 3D system integration is a strong candidate for overcoming the barriers in interconnect scaling, thereby offering an opportunity to continue performance improvements using CMOS technology by enabling increased circuit functionality and new 3D architectures. 3D integration may be used either to partition a single chip into multiple strata to reduce on-chip global interconnect length [38] and/or to stack chips that are homogenous or heterogeneous. An example of 3D stacking of homogenous chips is memory chips, while an example of heterogeneous chip stacking is memory and multicore microprocessor chips [5].

Although 3D stacking has been used for low-power applications, high-performance 3D stacked microprocessors have not been feasible largely due to thermal and power delivery challenges. The central idea behind this thesis is to address these challenges and eventually demonstrate a practical and CMOS integrated solution for a stacked system of high performance ICs.

CHAPTER II

3D SYSTEM INTEGRATION REVIEW

The reduction of interconnect delay and power consumption are of paramount importance for deep-sub-micron designs. 3D integration is an emerging technology that can form highly integrated systems by vertically stacking and connecting various disparate technologies, and functional components together [57]. The potential benefits of 3D integration can vary depending on the approach. The following are the main advantages of 3D system integration:

Interconnect wire length reduction: Technology scaling has proven to improve microprocessor performance in terms of size and switching speed [21, 75]. However, on the flip side, global interconnect wire delay is not synchronous with device scaling [68, 59, 10, 76]. As the interconnect scaling continues, RC delay plays a more dominant role in determining the system performance. Thus, interconnect delay is a severe bottleneck to improving system performance. This leads to 3D ICs being a viable solution. 3D ICs can be fabricated using short vertical interconnections called *Through Silicon Vias (TSVs)*, which are of the order of a few microns in length compared to present global interconnects which are orders of magnitude higher. It has been shown that when a 2D- SoC is converted to a 3D- SoC, wiring length of the global interconnects reduces by a factor of the square root of the number of layers used [37]. With 3D integration, the circuit-to-circuit interconnect length reduces and the interconnect density increases. Figure 6 below shows that when a 2D system-on-chip consisting of several blocks is converted to a 3D system, the interconnect length between the different blocks reduces from a few millimeters to a few microns. Reduction of wire

length due to 3D integration results in two major advantages [87]. (1) Latency improvement: This can be achieved by reducing the length of the average interconnect and the critical path; (2) Power reduction: As seen in the previous chapter, the interconnect power consumption plays an increasingly significant role in the total power consumed as scaling continues. The lengthy interconnections between chips are analogous to transmission lines that are prone to inductance and capacitance and noise due to cross-talk between signals. Energy consumed in interconnect circuits is of the order of 10-25 pJ per bit, due to the use of sophisticated processing techniques. In contrast, 3D interconnects are shorter and simpler with lumped capacitance at the end, that result in significantly lesser energy consumption (less than 1pJ per bit) [12]. Therefore, 3D integration technologies can provide high bandwidth at much lower power and energy.

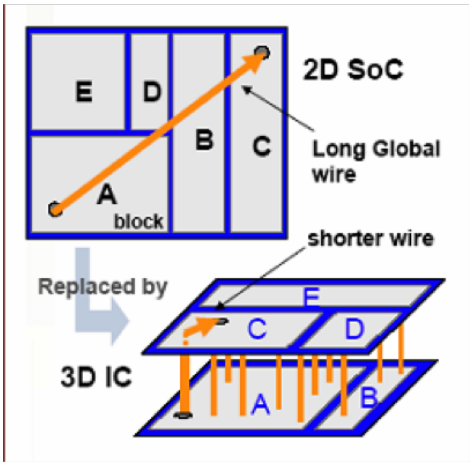
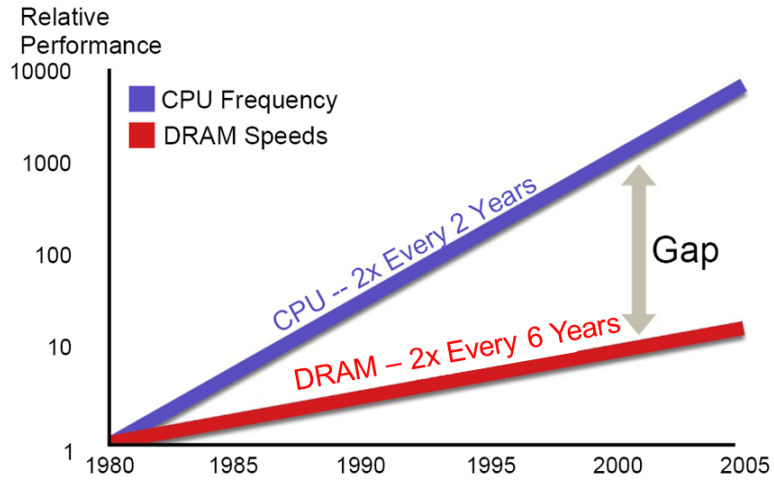


Figure 6: Interconnect length reduction from 2D to 3D systems [29].

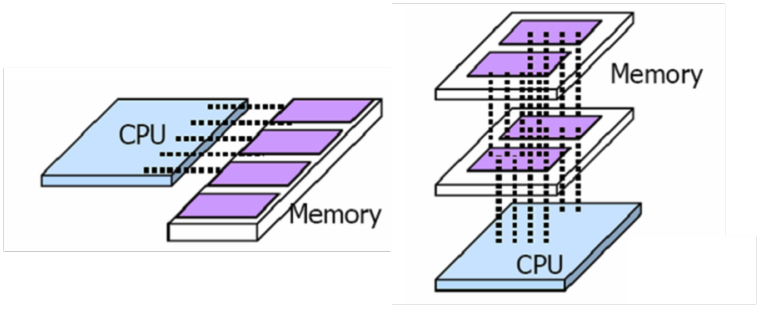
Memory Bandwidth Improvement: The rate of improvement in microprocessor speed exceeds in comparison to DRAM memory. Due to this, the microprocessor technology has increased in speed (with a rate of 60%/year), while the access time to DRAM memory has only improved at 10%/year [14]. See Figure 7(a).

Hence computer designers are faced with a challenge due to the Processor - Memory Performance gap, which now is a major obstacle to improved computer system

performance, also termed as the *memory wall* problem. Due to the growing memory access latencies, which is measured in processor cycles, a request that misses in the cache, may require several cycles to satisfy. This leads to system speed being dominated by memory performance. Thus, the problem is reducing the average memory access time [71]. A large off- chip bandwidth is needed to reduce the latency of the system which connects processor and memory in a system.



(a)



(b)

Figure 7: (a) Processor-memory mismatch causes system performance bottlenecks [2], and (b) Processor-memory stacking [51].

To reduce latency, the critical path also needs to be shortened. On a conventional 2D chip, the memory and logic units reside at the opposite ends. In comparison, a 3D chip can have logic and memory stacked together, which can significantly reduce the critical path as shown in Figure 7(b) [51]. Furthermore, the bandwidth between the CPU and DRAM improves dramatically with TSVs that can fetch hundreds to

thousands of bits at once. Power consumption also drops because the large capacitive loads due to off-chip accesses are removed [53].

Heterogeneous Integration: 3D integration technologies can prove to be a feasible and cost-effective approach for integrating heterogenous technologies to realize future microprocessors targeted at the *More than Moore* technologies projected by ITRS [87]. As 3D comprises of horizontal and vertical stacking, the different types of components can be fabricated separately, and layers can be implemented with different technologies. Some examples include digital CMOS, SiGe, RF BiCMOS, MEMS, Silicon-on-insulator (SOI), and future silicon technology as illustrated in Figure 8 [15]. A major advantage is that the different technologies can be optimized independently in terms of technology and specifications.

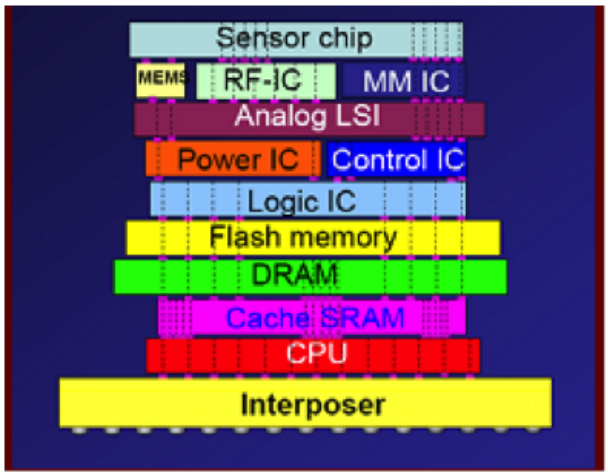


Figure 8: Heterogeneous integration of systems [15].

Small Form factor: 3D systems also result in higher packing density and smaller footprint due to the addition of a third dimension to the conventional two dimensional layout, and potentially lowers the cost design. Thus, from the above discussion, we can see that 3D integration has the ability to address the convergence of *Moore's Law* and *more than Moore*, and it offers a path for higher performance, higher density, higher functionality, smaller form factor, and potential cost reduction.

2.1 Overview of available 3D Technologies

There are three categories of 3D stacking technologies, summarized in Figure 9: first, technologies that do not require TSVs (Figure 9(a)-(c)); second, technologies that do require TSVs (Figure 9(d)-(e)); and third, technologies that consist of monolithic 3D systems that make use of systems that make use of semiconductor crystallization to form active levels that are vertically stacked (with on-chip interconnects possibly between). A combination of all these technologies is possible [6].

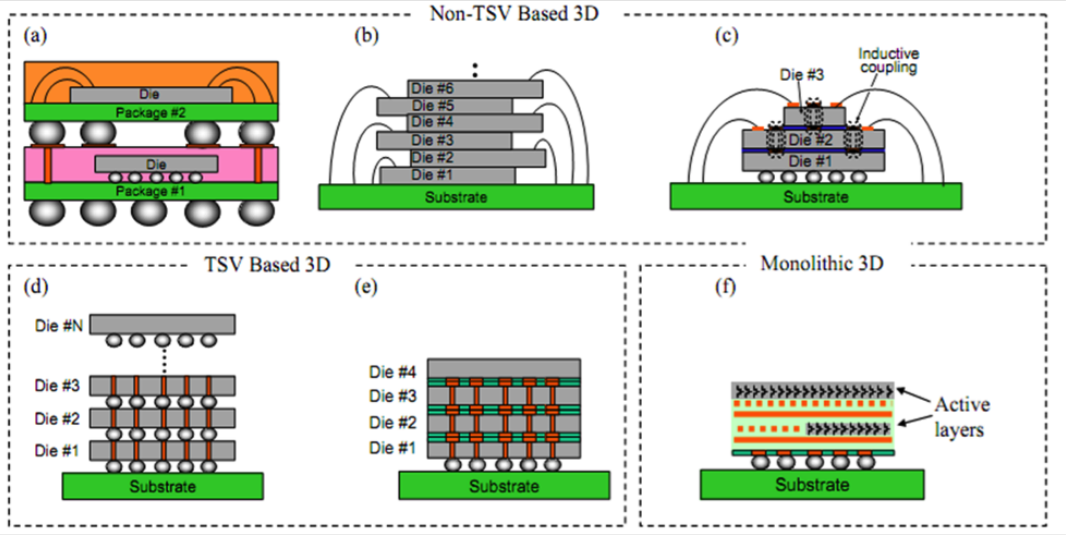


Figure 9: Overview of 3D technologies [6].

2.1.1 Non-TSV based 3D technology

The non-TSV 3D systems consist of a wide range of integration methodologies. Figure 9(a) demonstrates the stacking of fully packaged dice. These systems typically use solder balls to stack different subsystems (typically PCBs) containing individual packaged dies and/or components. A wide variety of assembly techniques can be used such as wire bonding, flip-chip, and underfill materials [22]. This is also defined as *3D System-in-Package (3D-SIP)* and is realized by interconnecting traditional pins of the die in the third dimension [7]. The available 3D-interconnectivity between two layers is typically only 2-5/mm along the perimeter of the device or 4-9/mm^2 when

area array packages are used [22]. Although this may offer the advantages of being low cost, simplest to adopt, fastest to market, and modest form-factor reduction, the overhead in interconnect length and low-density interconnects between the two dice do not enable one to fully exploit the advantages of 3D integration [22]. Figure 9(b) illustrates the most common method to stack memory dice, which is based on the use of wire bonds. Due to the adverse effect of wire bond length, low density, and peripheral limited pad location for signaling and power delivery, this approach is suitable for low-power and low-frequency chips. Figure 9(c) illustrates the use of wireless signal interconnection between different levels using inductive coupling [34]. This approach is quite elegant for low-power chips that require high-data rate signaling (without the need for TSVs). Power delivery, however, requires use of wire bonds for top dice in the stack, which are not applicable for high-performance/power chips. It is important to note that all non-TSV approaches rely on stacking at the die/package level (die-on-wafer possible for inductive coupling and wire bond), and thus do not utilize wafer-scale bonding. This may serve to impose limits on economic gains from 3D integration due to cost of the serial assembly process.

2.1.2 TSV based 3D technology

Figure 9(d) shows bonding of dice with C4 bumps and TSVs. The key advantages of TSV based 3D technology include the reduction in interconnect length and the increase in interconnect density. As this technology is best suited for die-level bonding, it faces the same economic issues described above. Figure 9(e) illustrates 3D stacking based on thin-film bonding (metal-metal, oxide bonding or adhesive bonding). A summary of the different bonding techniques available for 3D are as shown in the Figure 10 [55].

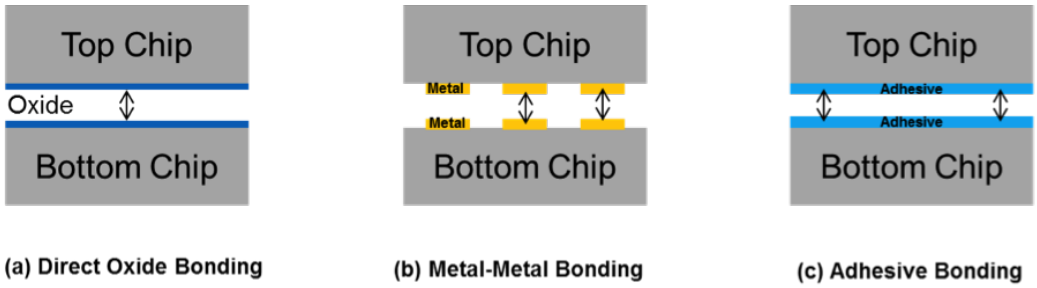


Figure 10: Various bonding techniques available for 3D [55].

2.1.3 Monolithic 3D Approach

Monolithic 3D techniques are based on a purely semiconductor manufacturing (non-packaging) approach to 3D integration. This approach involves sequential device process. The frontend processing (to build the device layer) is repeated on a single wafer to build multiple active device layers before the backend processing builds interconnects among devices. The main enabler to this approach is the ability to deposit an amorphous semiconductor film (Si or Ge) on a wafer during the IC manufacturing process and crystallize to form a single-crystal film using a number of techniques [28, 84]. Ultimately, this approach may offer the most integrated system with least interconnects possible but may not provide chip-size areas for device fabrication in the stack. It will be difficult to implement circuit integration with mixed technologies. An example of such monolithic 3D integration is shown in Figure 11 [16].

2.2 Challenges faced in implementing 3D ICs

Although 3D integration is regarded as one of the most promising technologies to relieve bottlenecks such as interconnect scaling, and memory bandwidth, there are several challenges in the implementation of this new paradigm shift.

Thermal Challenges: 3D integrated processors inevitably cause higher power density and lower thermal conductivity due to the close proximity of heat generating dies making the existing thermal hotspots even severe. The cooling issue is already

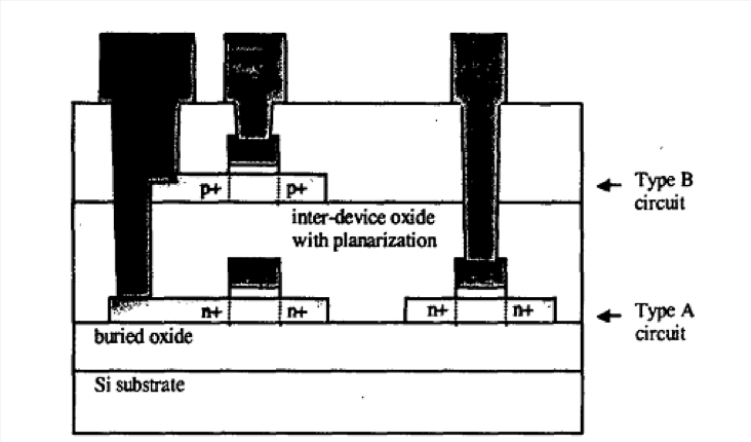


Figure 11: Schematic of monolithic 3D integration [16].

plaguing 2D IC systems, and this problem is exacerbated in 3D systems where heat flux from chips in the stack has to travel through a longer conductive path (larger thermal resistance) in order to be dissipated through the heat sink. As a first order approximation, a n-tier 3D chip would generate n times the power density as compared to 2D chip having identical characteristics [88]. Without efficient cooling, 3D ICs would suffer from severe performance degradations that include (1) increase in transistor leakage current, leading to increases in static power dissipation; (2) increase in the electrical resistance of on-chip interconnects that increases RC delay and I^2R losses and decreases bandwidth; (3) decrease in electromigration mean time to failure; and (4) degraded device reliability and decreases in carrier mobility [5]. Therefore advanced thermal management schemes have to be developed to fully exploit the advantages of 3D systems.

Power Delivery and Signaling Challenges: Power delivery to a 3D stack of high power chips presents many challenges. It requires careful and appropriate resource allocation at the package level, die level, and intrastratal interconnect level. In order to deliver power and allow signaling in a 3D stack, reliable interlayer connections are required. As discussed above, spacers and wirebonds can be used for inter layer electrical connection; however, these approaches may not be suitable for high

performance due to the high RC delay caused in the wire bonds. Wirebonds also limit the density of interlayer interconnects as they are limited to the periphery of the chip. They also impact the signaling characteristics as they introduce parasitic inductance, capacitance, and resistance. The other alternative is *TSVs*. The reason for TSVs to be an attractive choice is that the signals are transmitted directly from the lower layers to the upper layers through the TSVs, which have the shortest path, leading to the smallest RC delay. Furthermore, a high density of TSVs can be fabricated in a given chip as their placement is not limited to the periphery of the chip.

2.3 Solutions to Challenges

No approach discussed thus far addresses the simultaneous cooling and power delivery needs of stacked high performance ICs. As discussed in the previous chapter, after using the best materials, the typical junction-to-ambient thermal resistance (R_{ja}) of conventional air-cooled heat sinks has been larger than 0.5 °C/W [5]. The scaling of conventional air-cooled thermal interconnects cannot meet ITRS-projected power dissipation at the end of the roadmap in 2018, which demands an R_{ja} of 0.2 °C/W [4]. Hence, novel cooling solutions are required to address the cooling needs of 3D ICs. An example includes single-phase or two-phase liquid cooling system. As illustrated in Figure 12, the heat transfer coefficient of single phase microchannel cooling is orders of magnitude higher than conventional air cooling [31].

A monolithic integrated microchannel heat sink eliminates the need for *thermal interface materials (TIMs)* and represents the highest level of process integration possible for liquid cooling [20]. As demonstrated by Tuckerman and Pease, in 1981, the chip junction-to-ambient thermal resistance can be as low as 0.09 °C/W and that a power density as high as 790W/cm^2 can be rejected when a microchannel heat sink is directly integrated into a Si chip [83]. Moreover, an integrated microchannel

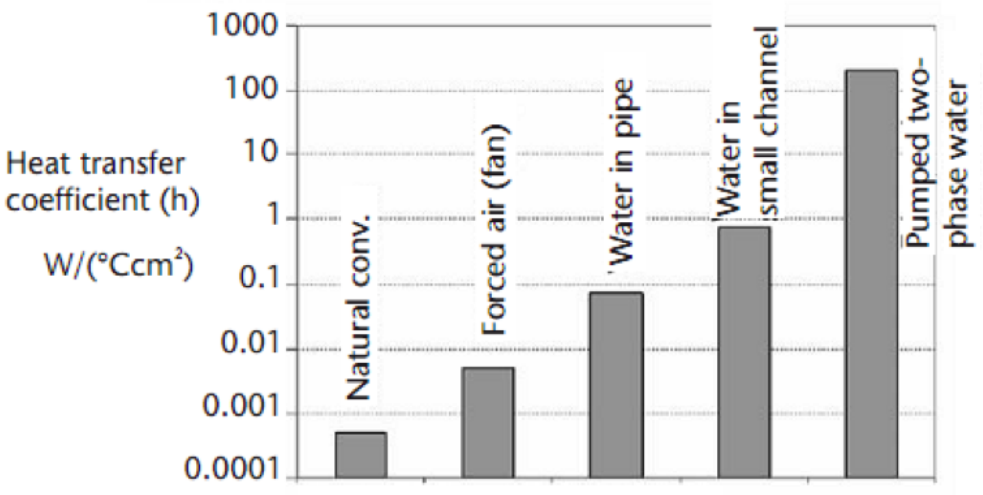


Figure 12: Heat transfer coefficient of single phase microchannel cooling versus conventional air cooling [31].

heat sink can largely reduce the IC package footprint and volume to leverage form-factor and performance requirements of multichip and 3-D chip stacks. Due to these benefits, microfluidic cooling has recently received increasing interest [93, 36, 54, 46]. To date, there have been several studies that have focused on the characterization of microchannel dimensions or thermofluidic properties [8, 44, 39, 30]. However, integration issues with CMOS, reliable interstrata connections, and fluid delivery still remain a challenge. Integration and performance tradeoff with vertical electrical interconnects is also not clear and requires deeper investigation. This thesis aims to address some of the challenges.

2.4 Proposed 3D System

Figure 13 shows a proposed microfluidic network cooling scheme that can be used for cooling high-performance 3D chip stacks. Each silicon die of the 3D stack contains the following features: (1) an integrated microchannel heat sink, (2) through-silicon electrical (copper) vias (TSEV) and through-silicon fluidic vias (TSFV), the latter used for fluidic routing in the 3D stack, and (3) solder bumps (electrical I/Os) and microscale fluidic I/Os on the side of the chip opposite to the microchannel heat sink.

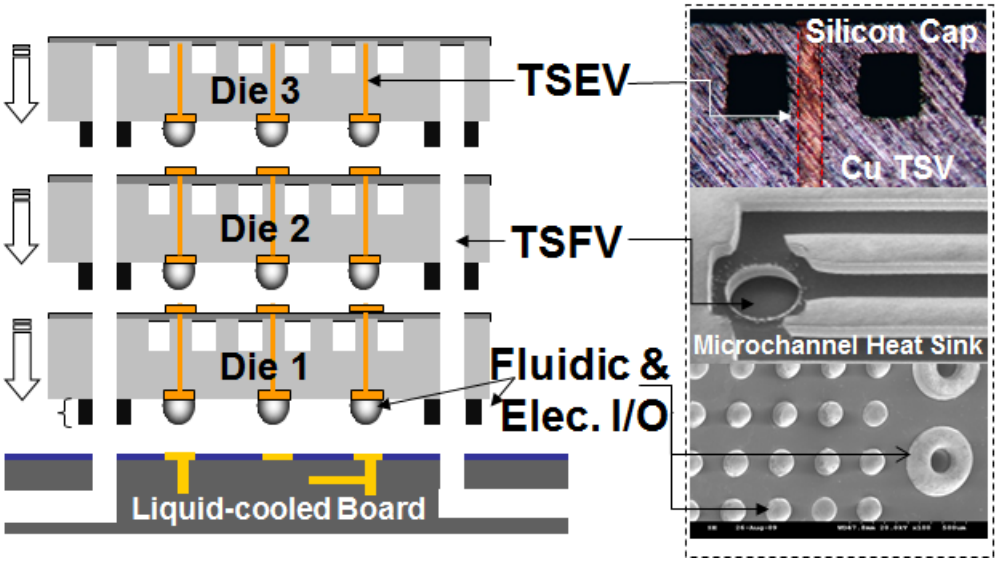


Figure 13: Schematic of proposed 3D system.

In Chapter III, the various schemes for integrating microchannel heat sinks and TSVs and the tradeoffs involved in their integration will be discussed. Chapter IV discusses the fabrication technology for integrated microchannel heat sinks and TSVs. In Chapter V, the design and fabrication of a 3D liquid cooled test bed is discussed along with some preliminary testing results.

CHAPTER III

INTEGRATION AND MODELING OF FLUIDIC AND ELECTRICAL I/OS

In the previous chapter, a three dimensional liquid cooled system was proposed which consisted of microchannel cooling and TSVs integrated in each layer for interlayer electrical connections. One of the most important aspects of the proposed system is the integration of fluidic and electrical interconnects in the same die. However, this integration consists of many tradeoffs, design considerations, and fabrication issues which must be considered for successful implementation, and will be discussed shortly. This chapter will cover technology for integrating microchannels and TSVs with conventional CMOS. It will also cover modeling, which demonstrates the performance tradeoffs involved in integrating TSVs and microchannels in a 3D stack.

3.1 Integration schemes for microchannels and TSVs

In this section, different approaches on how electrical (TSVs) and fluidic (microchannels) components can be integrated into conventional CMOS processing will be discussed. The major steps in microchip fabrication process include front-end-of-line (FEOL) processing, back-end-of-line (BEOL) processing, and semiconductor packaging. FEOL is the first portion of IC fabrication where the individual components such as transistors, capacitors, resistors, etc. are patterned on a semiconductor. FEOL includes all fabrication steps until the deposition of metal interconnect layers. BEOL is the second portion of IC fabrication where these individual components get interconnected with wiring on the chip. This includes metal contacts, dielectrics, and bonding pads for chip-to-package connections. After BEOL, the backend processing

takes place which consists of wafer test and characterization, die separation, IC packaging, and other tests. Figure 14 shows the first two steps of FEOL and BEOL, and the respective temperature constraints.

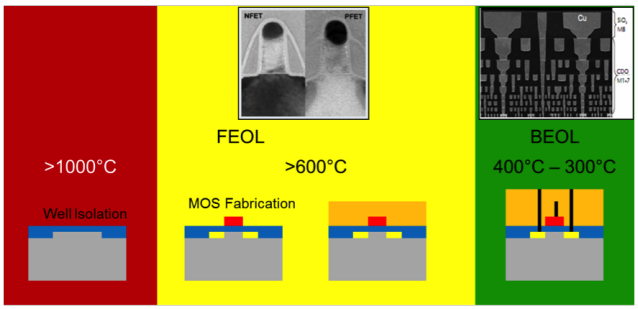


Figure 14: Illustration of steps in IC processing [65].

Based on the temperature and material constraints, the following are potential integration schemes for microchannel and TSV integration:

Homogeneous Approach: In this approach, after FEOL and BEOL processing, microchannel heat sinks are etched on the back side of the wafers which are subsequently capped using a CMOS compatible bonding method such as a sacrificial polymer process [19] or low temperature Si-Si direct bonding process discussed in chapter IV. Once the microchannels are enclosed and sealed, TSVs are etched in the fins of the microchannels, and appropriate sidewall isolation such as SiO_2 or Si_3N_4 is deposited. Finally, the TSVs are filled with a conductive material such as copper (with suitable barrier) or tungsten. Figure 15(a) demonstrates the concept of the homogeneous approach. Details of TSV fabrication will be covered in Chapter IV.

The homogeneous approach is conducive provided the processes following BEOL processing are CMOS compatible. This technique is thermally superior because of the high proximity of microchannels to the active circuitry and the absence of any thermal interface material (TIM) in the conductive path between the microchannel heat sink and the heat source. This approach is electrically better due to the absence of any contact resistance. A potential drawback of this technique arises from process

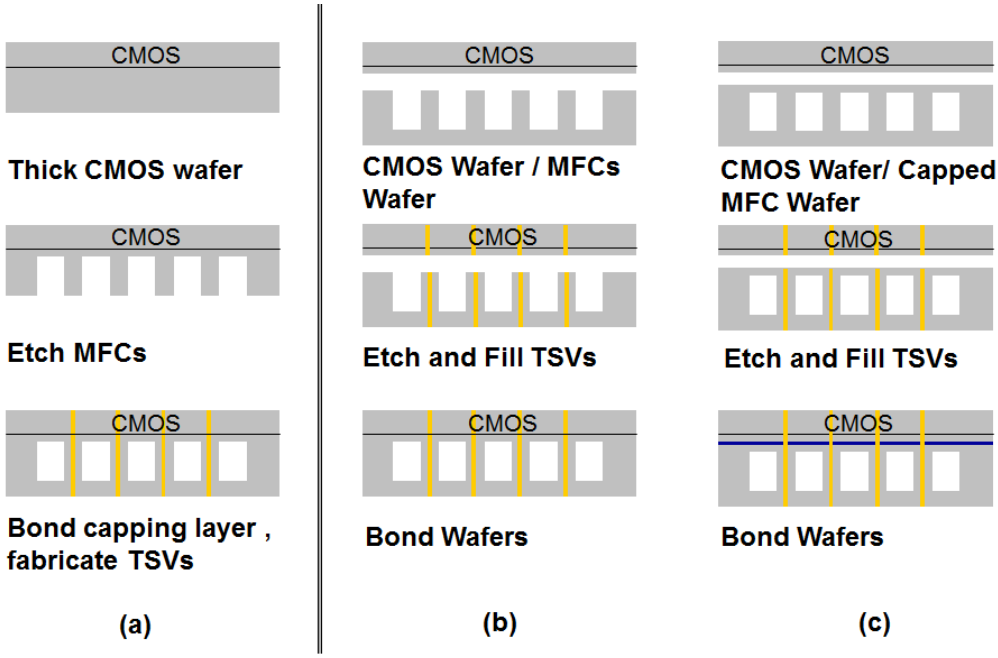


Figure 15: (a) Homogeneous approach and (b), (c) heterogeneous approaches.

integration issue such as materials and temperature compatibility. It also necessitates fabrication of high aspect ratio TSVs which increases process complexity. The capping process of the microchannels must be done using a low temperature process, that does not exceed the maximum allowable process temperature for BEOL (<450 °C).

Heterogeneous Approach: In this approach, microchannels and TSVs are fabricated on a new wafer that can be bonded in a number of ways to another wafer containing active circuitry and TSVs. There are two types of heterogeneous techniques, as discussed below: In the first method (Figure 15(b)), the two wafers are mechanically and electrically bonded using an appropriate CMOS compatible technique [78]. A popular bonding approach which enables both mechanical and electrical interconnection is shown by Ziptronix as shown in Figure 16 [3]. This approach is called the Direct Bond Interface (DBI) and can achieve over 100,000,000 electrical connections per square centimeter [3]. It is relatively more flexible than the homogeneous approach. The processes involved in fabricating microchannels and high aspect ratio TSVs need not be compatible with CMOS. It eliminates the need for fabricating

high aspect ratio TSVs in CMOS wafers which can cause some process and material issues. This approach also segregates the TSV fabrication process into two components, i.e. TSVs in the CMOS wafer and TSVs in the microfluidic channel (MFC) wafer. The advantages of this segregation will be discussed in the section below describing the *heterogeneous TSV approach*. The bonding process in this approach must be CMOS compatible to protect the underlying circuitry on the capping wafer. Precise alignment during bonding is required as both the bonding wafers have features on them. The electrical bonding of TSVs needs to be precise, as high density TSVs will be required to fulfill the power delivery and signaling requirements of a 3D stack.

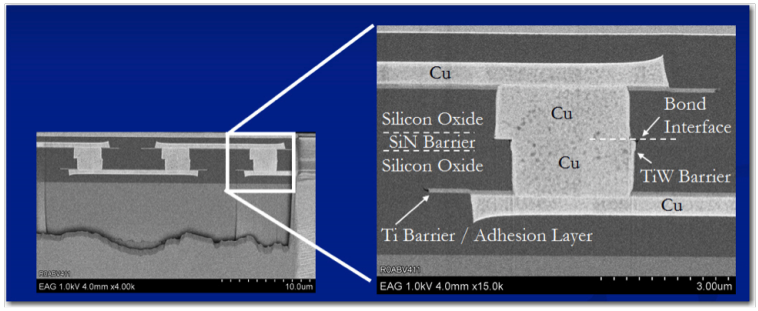


Figure 16: Direct Bond Interface by Ziptronix [3].

In the second approach (Figure 15(c)), wafers are fabricated with microchannels and capped using bonding techniques compatible with TSV fabrication. Once capped, electrical TSVs are fabricated in the wafer, which is then attached to a wafer with active circuitry using a hybrid bonding process demonstrated by [78, 3]. The main advantage of this process is that the two wafers can be fabricated independently of each other (even in separate foundries), thereby eliminating the added complexity of making compatible microchannel heat sinks and TSVs in the same processing stage. However, the addition of the bonding layer increases R_{ja}.

The heterogeneous approach of microchannel and TSV integration also enables the possibility of having a *heterogeneous TSV approach*. To understand the need for this technology, let us consider the homogeneous integration scheme. For example, if

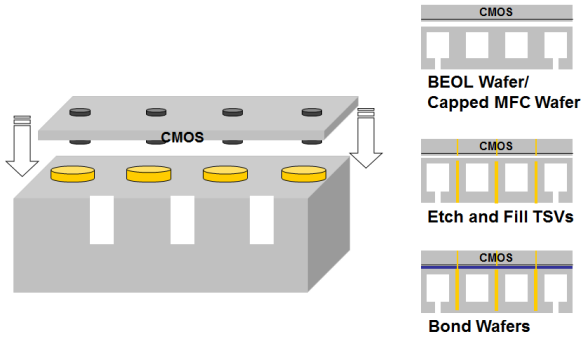


Figure 17: Heterogeneous TSV Approach.

the TSV aspect ratio is limited to 20:1, and the total thickness of the CMOS + MFC wafer is 400μm, then the diameter of the TSV is 20μm. Considering a 1cm X 1cm chip containing 1,000,000 TSVs/ cm^2, this amounts to 12.5% of silicon area. These large diameter TSVs occupy valuable silicon real-estate which would have been used for CMOS circuitry. If the diameter is made smaller to CMOS interconnect dimensions such as 1-2μm (0.125% Si area occupied), then the aspect ratio requirements would be >200:1. Aspect ratio is a major limiting factor in the fabrication of TSVs. This will be further discussed in the fabrication tradeoffs section in Chapter IV. Since the channel wafers and CMOS wafers are fabricated independently in the heterogeneous scheme, the diameter as well as material for TSVs in both wafers can be different. The CMOS wafer can have smaller diameter TSVs fabricated and thereby have additional room for circuitry. Another advantage of this approach is that the two layers can have different materials for TSVs. Currently, Cu, W, and highly doped polysilicon are the most promising candidate materials for TSV filling. Among them, Cu is superior in conductivity (almost 2 times greater than W) and has the ability of filling big structures, which makes it widely accepted in 3D integration [89]. However, note that the thermal coefficient of expansion (CTE) for Cu is about 4 times greater than that of W and more than 6 times that of Si (see Table 3). This would cause reliability issues. Due to the large CTE mismatch, Cu will cause fissures in the Si over a large number of thermal cycles. Study about the thermo-mechanical stress originating

Table 3: Electrical and thermal properties of Si, SiO_2, Cu, and W [25].

Material	**Si**	**SiO_2**	**Cu**	**W**
Electrical resistivity (nΩm at 20 C)	Semiconductor	Insulator	17	53
CTE (10^{-6} m/m-K)	2.6	Varies	16.5	4.5
Thermal conductivity (W/m-K) at 300 K	149	10	401	173

from CTE mismatch in the CMOS wafers due to smaller diameter TSVs is reported in detail by [56] and [77].

Due to the possibility of having different size as well as material used in the CMOS wafer and microfluidic channel wafer, it is termed as heterogeneous TSV approach. From the advantages discussed above, this method has the potential to be a strong contender in the overall integration scheme choice. Further study is needed to explore the fabrication issues involved with this method as well as electrical and mechanical modeling of such hybrid TSV structures.

3.2 Modeling and Design of MFC and TSV Integrations

In this section, the modeling and design of microchannel heat sink performance and TSV density will be discussed. For this analysis, the chip size was assumed to be 1cm (L) X 1cm (W). Figure 18(a) shows the overall chip top view.

Figure 18(b) illustrates a cross-sectional schematic of a microchannel heat sink containing an area-array distribution of TSVs per microchannel (Si) wall. The width of the microchannel wall (W_w) can be expressed as a function of TSV parameters by the following equation:

$$W_w = 20\mu m + P_{TSV}(N_{TSV} - 1) + D_{TSV} \quad (1)$$

where P_{TSV} is the TSV pitch, W_w is the =microchannel wall width, N_{TSV} is the number of TSV columns per microchannel wall (N_{TSV}>1), and D_{TSV} is the diameter of TSV. The first term in the equation is constant and is used to indicate the clearance

between the edge of the microchannel wall and the first and last TSV. In this analysis, this was assumed to be 20μm. It is also assumed that:

$$P_{TSV} = 1.5D_{TSV} \tag{2}$$

The total number of TSVs ($N_{totalTSVs}$) that can be routed through the chip (only through the microchannel wall, in this study) can be expressed as:

$$N_{totalTSVs} = N_{TSVcolumn}(n+1)L/P_{TSV} \tag{3}$$

where n is the total number of microchannels, which can be expressed as

$$n = (W - W_w)/(W_w + W_c) \tag{4}$$

The set of equations used to model the thermal resistance and pressure drop in a microchannel heat sink is shown in Figure 19, which models heat flow in the microchannel wall in one-dimension.

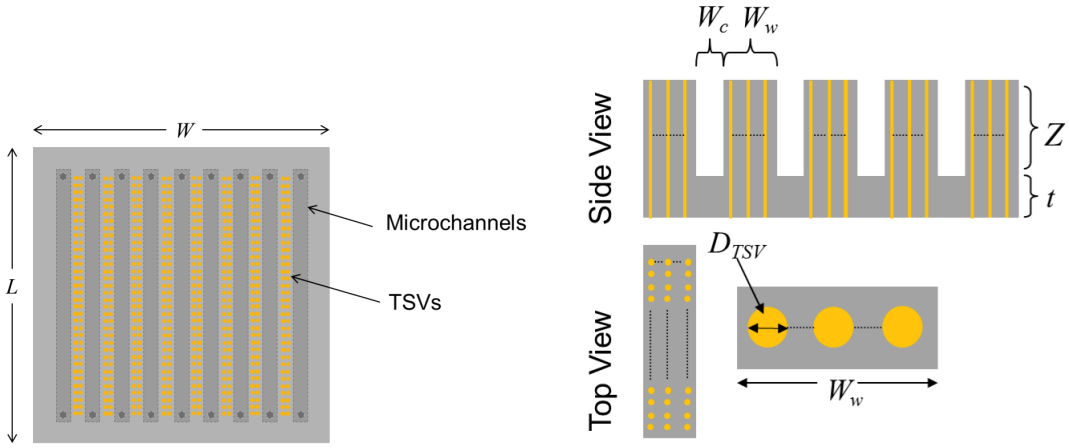


Figure 18: Schematic illustration of a microchannel heat sink with TSVs.

Figure 20 illustrates microchannel heat sink thermal resistance and pressure drop as a function of TSV diameter, number of TSV columns per wall, and microchannel thickness. As can it can be seen from the graph, there are numerous performance

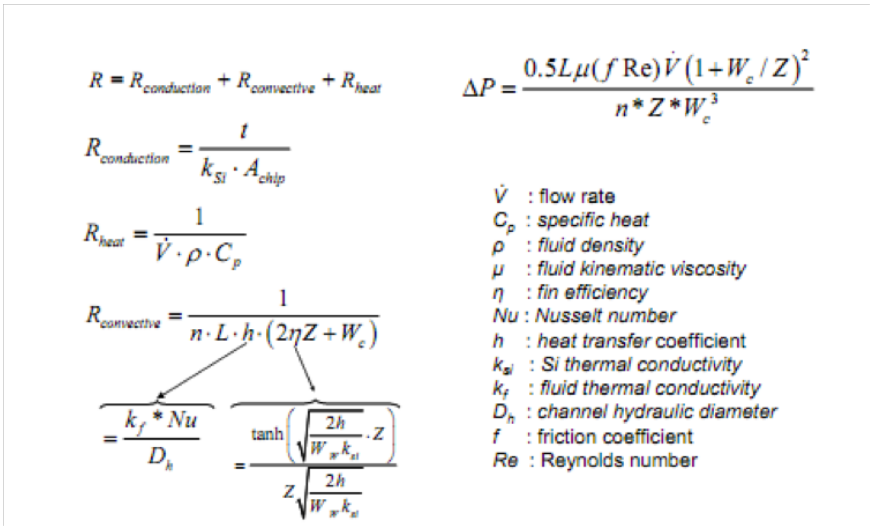


Figure 19: Set of equations used to calculate thermal resistance (R) and pressure drop (ΔP) in a microchannel heat sink [83, 18].

tradeoffs involved when integrating electrical and fluidic interconnects in the 3D stack. From a cooling perspective, having deep microchannels is beneficial to reduce the pressure drop and thermal resistance. However from an electrical perspective having maximum number of TSVs is beneficial to exploit fully, the advantages of 3D ICs. From the analysis we observe the following:

- As the number of TSV columns per wall increases (electrically better), the thermal resistance and pressure drop increase (cooling suffers). This occurs because as the number of TSV columns increases, the wall width increases, which lead to a smaller number of total microchannels (for fixed channel width and fixed chip dimension). This has the consequence of decreasing the overall surface area in contact with the fluid (increases thermal resistance) and decreases the total number of microchannels available (increases pressure drop because the variable n in the P equation shown in Figure 19 decreases).

- As the diameter of the TSV increases, both thermal resistance and pressure drop increase for the same arguments presented above. Increasing the diameter has fabrication benefits discussed in the next section.

- As channel thickness reduces, thermal resistance and pressure drop reduces as well which will result in diminished cooling capability. However, with reduced thickness aspect ratio requirements of TSVs reduces which has benefits discussed in the next section.

Nevertheless, these values of thermal resistance are much lower than for air-cooled heat sinks. In all cases, the value of junction-to-ambient thermal resistance is lower than current state of the art air-cooled heat sinks [5], and they meet the ITRS projections of approximately 0.2 °C/W which will be needed to cool future high performance ICs [4]. In Figure 20, we assume that high aspect ratio vias can be formed into the silicon however there are certain fabrication constraints which are considered in the next section. The total number of TSVs possible to route are also shown in the figure for each of the six curves.

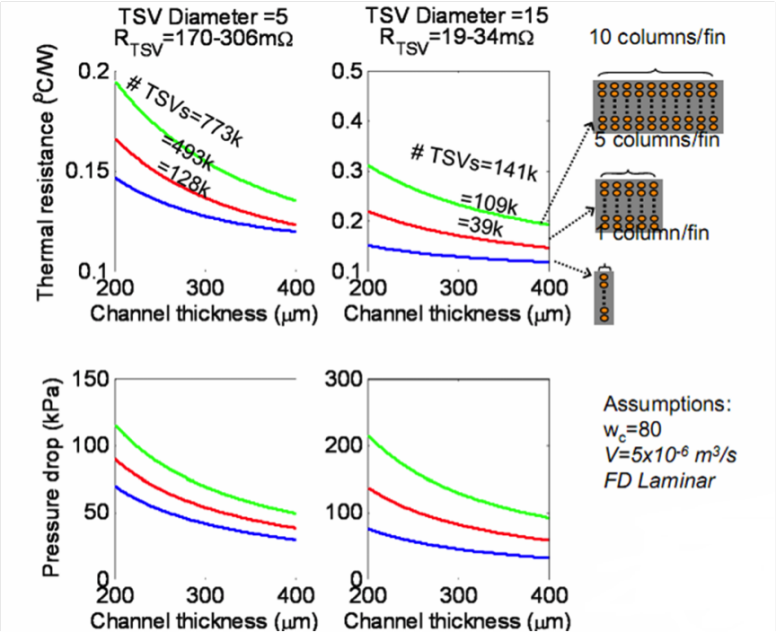


Figure 20: Thermal resistance and pressure drop in a microchannel heat sink as a function of TSV diameter, number of TSV columns per wall and channel thickness [6].

The heterogeneous approach described in the previous section is also modeled using the same assumptions described above. In this case, we assume a TSV diameter of

5μm and the bonding interface between the CMOS chip and channel wafer is assumed to be SiO_2. The modeling is based on the assumption that thermal conductivity of the bonding interface is a weighted average of the thermal conductivities of SiO_2 and Cu and that the TSVs are distributed evenly. The number of TSV columns per channel fin is varied from 5 to 20 along with the bonding interface thickness (1-10μm) in order to quantify the effect of bonding. Figure 21 illustrates the result of this first order modeling.

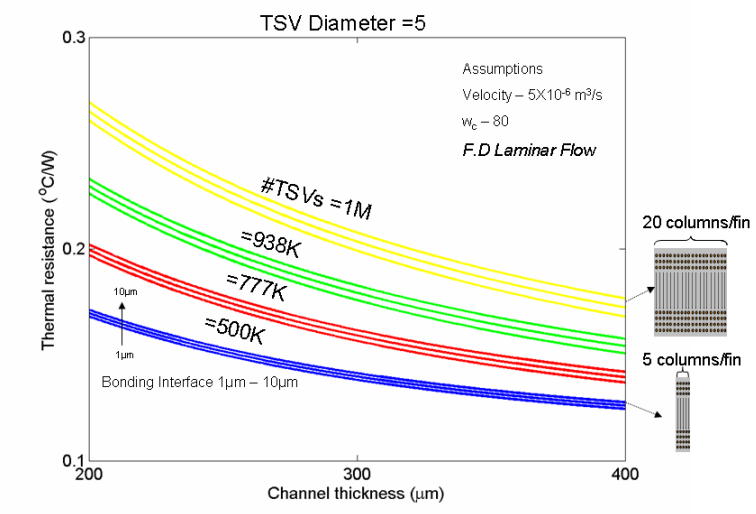


Figure 21: Thermal resistance of microchannel heat sink as a function of number of TSV columns per channel wall, channel thickness and thickness of bonding interface.

In this chapter, we reported various integration schemes for TSVs and microchannels. The selection of the integration scheme depends on the application, material and temperature constraints as well as the available fabrication technology. Based on the advantages discussed above, we believe that the heterogeneous scheme is a potential candidate for such integration and our fabrication techniques are based on it. From the modeling results, we see that there are clearly tradeoffs to be considered while integrating TSVs and microchannels. So far we have considered performance tradeoffs. There are some fabrication tradeoffs too which will be elaborated in the following chapter.

CHAPTER IV

FABRICATION OF FLUIDIC AND ELECTRICAL I/OS

In the previous chapter, we discussed the various integration schemes and modeled the tradeoff between the geometry of the microchannel heat sink, which fundamentally defines its performance and the number of TSVs that can be routed through it. In this chapter, fabrication details, integration results and testing of integrated microchannels and TSVs will be discussed. A novel fabrication technique for high density, high aspect ratio TSVs for future high performance ICs will also be reported.

In the previous chapter, we assumed that high aspect ratio high density TSVs can be fabricated with microchannels. However, each step of TSV fabrication, which includes via etching, via isolation, and via filling is aspect ratio limited [40, 90, 74, 82]. This is one primary reason why most conventional 3D systems have wafer thinning as a process step [42]. This necessitates fabrication of TSVs in strata having thicknesses ranging from 5-20μm. However, in our case, thinning is not an option. For microchannels to be an effective heat sink the minimum depth of the microchannels must be 200μm - 300μm and hence, the thickness of the stack must be at least 350μm (considering the extra thickness of the capping layer). Ideally, one would want small diameter TSVs (1-5μm) to be fabricated in thick wafers so as to ease handling issues, enable deep microchannels, and reduce the real estate occupied by TSVs.

Based on the advantages discussed in the previous chapter, we choose a heterogeneous approach to integrate microchannels and TSVs in a wafer where they are fabricated independently and then bonded using techniques discussed in chapter III. This fabrication process specifically discusses the non-CMOS component of the strata, i.e. a thick wafer containing microchannels and electrical TSVs.

The schematic in Figure 22 shows the fabrication process for integrating microfluidic cooling channels and electrical TSVs for a 3D IC stack.

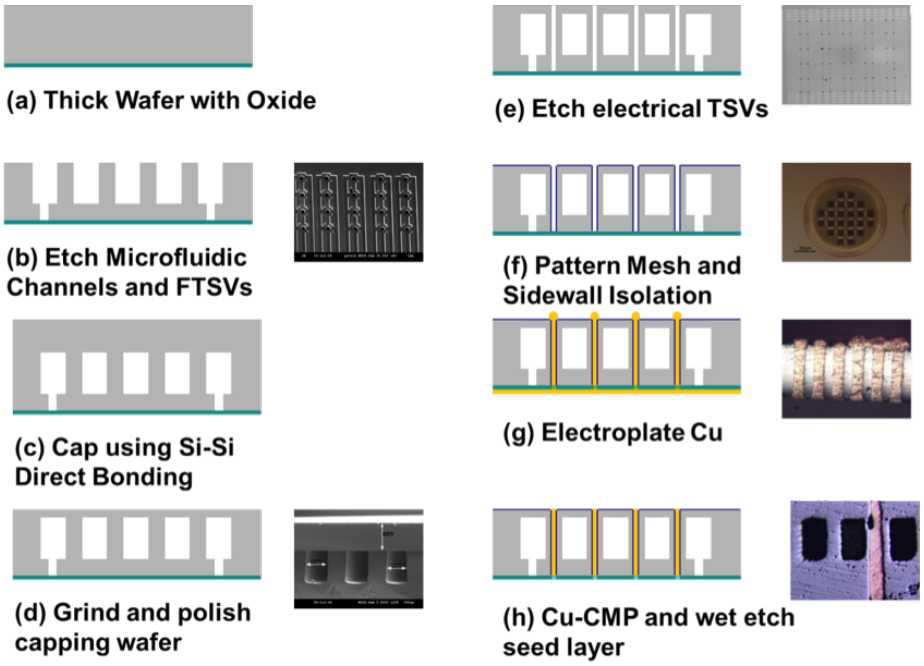


Figure 22: Schematic of wafer-level integration of microchannels, through-silicon uidic vias, and electrical through-silicon vias to enable 3D system integration using liquid cooling.

We begin by taking a blank 400μm double side polished (DSP) P-type wafer with a resistivity of 1-20Ω-cm. The next step is to deposit a 2μm thick PECVD layer of SiO_2 on the backside of the wafer (Figure 22(a)). This SiO_2 layer acts as the etch stop layer during subsequent etching of the microchannels (100μm width) and fluidic through-silicon vias (FTSVs) (100μm diameter). The etching is a two step process: first, FTSVs are patterned and etched to about 150μm using Bosch processing in an ICP; second, the microchannels are aligned with the partially etched FTSVs, and both of them are etched till a point when the FTSVs are visible on the back side of the wafer (Figure 22(b)). Careful control of etching is required so as to not punch through the 2μm etch stop layer.

4.1 Bonding Techniques

Wafer bonding is a technique of joining two substrates by bringing their surfaces in contact [24]. After etching microchannels and FTSVs, the MFC wafer must be capped in order to seal the microchannels and allow fluid flow through them (Figure 22(c)). There are several ways to bond a capping wafer to the microchannels. An adhesive bonding technique and a low temperature plasma enhanced bonding method were explored.

4.1.1 Adhesive Bonding

Bonding using the adhesive method requires an intermediate layer such as SU-8. This technique enables bonding of silicon at low temperatures and is less dependent on substrate material, particles, roughness, and planarity of the bonding surfaces [92]. Bond quality evaluation and leakage tests have been performed in literature [52], and the bond strength is sufficient for microfluidic applications. The process flow for adhesive bonding is shown in Figure 23. Microchem SU-8 2025 was used for the purpose of demonstration of adhesive bonding. SU-8 2025 is spun on a DSP blanket silicon wafer at 3000 rpm (@ 1000 rps) for 60s. This yields an SU-8 layer of 15μm-20μm. The wafer is placed on a hotplate heated to 150 °C and a wafer with microchannels is placed over it. A force of 2kg was applied uniformly to remove any air bubbles between the 2 wafers. The sample was then cured on a hotplate at 150 °C for 4 hrs. The result of the bonding is as shown in Figure 24. The main advantage of bonding microchannels using the adhesive method is the inherent tolerance in terms of wafer thickness variation, micro-cracks, and other particles, as compared to direct silicon bonding. The drawback of this process is that it necessitates the use of low temperature processes post bonding due to the presence of SU-8. Although this technique was explored, it is not the focus of our capping process. We used the direct

bonding approach discussed in the next section for capping microchannels.

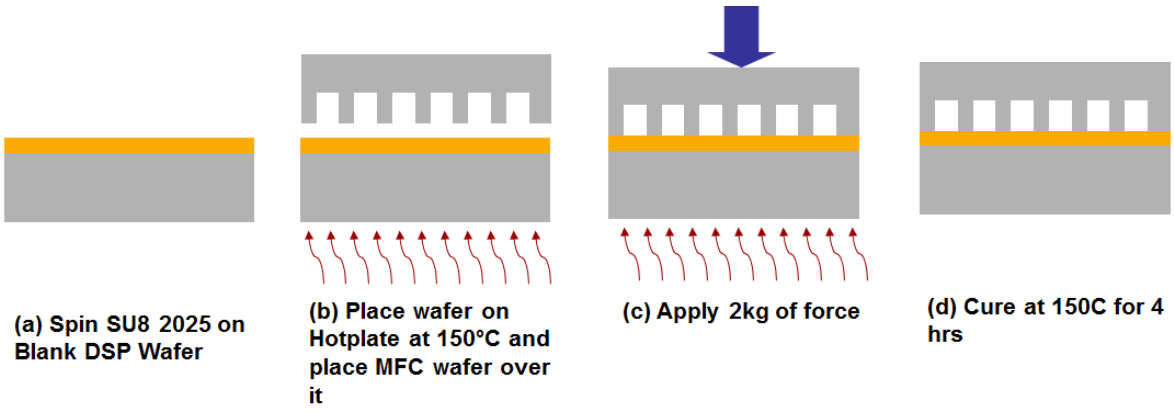


Figure 23: Process steps for adhesive bonding.

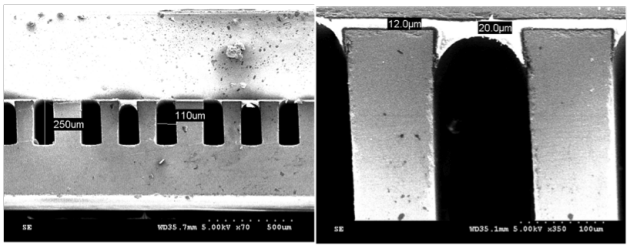


Figure 24: Adhesive bonding using SU-8 layer.

4.1.2 Plasma Enhanced Direct Bonding

Direct bonding is based on molecular bonds established between molecules from the surfaces of two bonding substrates [24]. Typically, the process consists of two main steps: a room temperature step in which weak adhesion is established between the substrates, and a high temperature annealing step where the weak bonds are converted to strong permanent bonds. It is generally assumed that adhesion forces (van der waals forces, electrostatic coulomb forces, capillary forces or hydrogen bridge bonds) are the primary bonding forces. The measured interface energy is low and is about 0.1 J/m^2 for bonded hydrophilic wafers. An increase of the interface energy by a factor of 10 or more is obtained by a subsequent annealing at elevated temperatures which transforms hydrogen bridge bonds across the interface via the reactions shown

in Figure 25 [73].

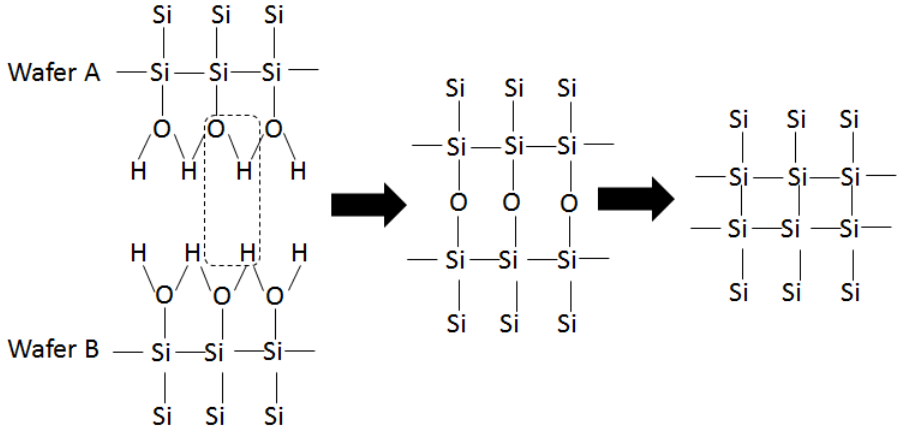


Figure 25: Hydrophilic bonding process .

The thermal step is the main limitation for wafer bonding applications. Traditionally standard silicon direct bonding requires temperatures in excess of 1000 °C which is the main limiting factor for applications that need low temperature processing. Hence, surface conditions must be realized during low-temperature annealing which results in interface forces comparable to those generated at high temperatures. For hydrophilic surfaces, the interface energy is equivalent to the number of silanol groups (Si-OH) at the initial surface. Therefore, an activation of the surfaces by an increasing density of silanol groups would also increase the interface energy. This activation can be achieved using plasma treatment. It has been reported that strong hydrophilic bonding with Si can be achieved at a low annealing temperature <400 °C, by exposing wafers to a low pressure plasma prior to the bonding [26, 79]. Low temperature plasma-activated Si-Si direct bonding approach was implemented for capping microchannels. The surface preparation methods developed for low temperature processes are based on surface chemical activation resulting in different types of bonds at room temperature which amounts to lower annealing temperature and time [24]. The following are the fabrication steps for wafer to wafer bonding.

Surface Preparation: The MFC wafer and a 400μm blank capping wafer are

dipped in a RCA-1 solution. RCA-1 consists of H_2O, NH_4OH, H_2O_2 in the ratio 5:1:1 respectively. RCA -1 attacks any organic impurities which may be on the surface of the wafers and makes the surface hydrophilic.

Plasma Activation: After RCA cleaning, the wafer surface is treated with O_2 plasma in a Reactive Ion Etch (RIE) system and bonded at room temperature and in atmosphere. During the plasma activation process, an oxidation takes place on the surface due to the bombardment with oxygen ions, which additionally will assist in the breaking of surface bonds. This not only cleans the surface but also forms a large number of free bonds. The damaged surface layer presumably accommodates a high concentration of OH groups resulting in high bond strength [79]. Table 4 refers to the plasma activation conditions.

Bonding: Immediately after plasma treatment, the wafers are rinsed with DI water for 3 min. Due to the rinse, the open dangling bonds of Si on the surface after plasma exposure become terminated with hydroxyl ions which contributes to the bonding process. Bonding is carried out by hand in room temperature. Since microchannels are capped using a blank silicon wafer, there are no alignment issues while bonding.

Annealing: Bonding is followed by a thermal annealing step at 400 °C for 12 hours which provides the energy needed to transform the weak reversible bonds into strong permanent bonds. The bonded wafers were tested by destructive tests such as crack test and dicing. When the wafers were diced, the bonded interface was observed under the SEM as shown in Figure 26. Bonded wafers were also examined under the IR microscope for voids and cracks. A consistent yield of 70-80% was achieved using this bonding technique.

4.2 Thinning of Capping Layer

The capping wafer on bonded and annealed samples was thinned down by back grinding and polishing to a thickness of 100μm (Figure 22(d)). The need for thinning the

Table 4: Conditions for plasma activation.

Parameter	**Value**
Cloud Position, W	50
Ctune Position, W	50
Process Pressure, mT	90
RF Setpoint, W	100
O_2 Flow, $sccm$	90
Process Time, min	1

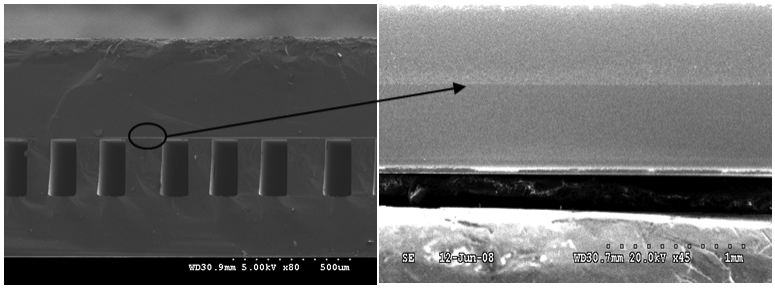


Figure 26: Bonding interface of microchannel heat sink.

capping layer arises from the fact that TSVs are to be integrated after the bonding process. Without thinning, the total thickness (800μm) would require fabrication of a very high aspect ratio (>15:1) TSV (assuming a diameter 50μm), and hence this puts a constraint on the maximum thickness of the capped microchannels. Capping wafers were thinned to 25μm however 100μm was chosen to maximize yield and maintain the mechanical integrity of the stack. Shown in Figure 27 is a graph of TSV diameter versus stack thickness for different aspect ratio values. As the wafer thickness increases, the TSV diameter increases. This increases the capacitance of TSVs which in turn affects the electrical performance of the system. Increasing the diameter of the TSVs also amounts to lower number of TSVs being fabricated in a unit area and lesser area available for active circuitry. Hence thinning of the capping layer is important.

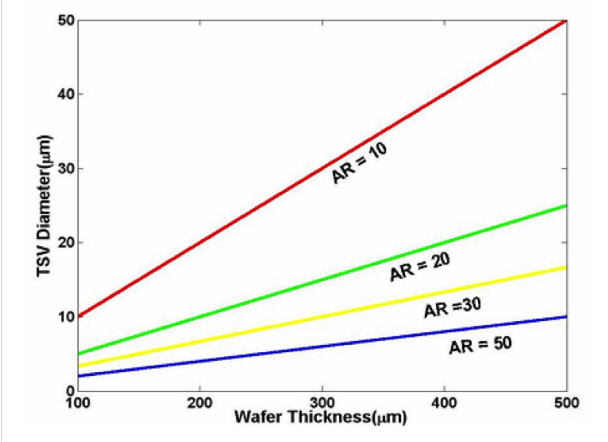


Figure 27: TSV diameter as a function of wafer thickness and aspect ratio.

4.3 TSV Fabrication background

After microchannel fabrication, TSVs are fabricated in order to form vertical interconnections. The steps involved in TSV fabrication are:

Via formation: Vias can be etched by laser ablation [48], DRIE using bosch process [13] or wet etching [27].

Via lining dielectric: The silicon via sidewall needs to be passivated to prevent shorting of TSV metal to silicon. Silicon dioxide and polymer annular rings are commonly used via lining dielectric.

Via filling: This determines the conductive material used to fill the vias such as W, Cu, polysilicon or conductive polymer. The choice of deposition method depends on the type of material used. For example, CVD is chosen for W while electroplating is the preferred method of Cu filling. The selection of technology, process integration, and via fill material depends on the system requirements such as via size, via density, aspect ratio and so on. In this work, we project via sizes of diameters 10-50μm in 300-400μm thick wafers. This amounts to aspect ratios ranging from 30:1 to 8:1. Cu is the material of choice for this application due to cost, superior conductivity and ease of fabrication [89]. There are several ways [41] in which Cu TSVs can be fabricated. Two main processes are discussed below.

4.3.1 Super-fill Process

In this method, TSVs are etched using DRIE. After sidewall isolation, a seed layer is applied by CVD (e.g Cu) or an adequate sputtering process (Ti:Cu). Metal is then filled in the TSV using Cu electroplating. Cu will also be deposited on the wafer front side during plating, which will be removed by a CMP step. Depending on the via size and depth, a wafer thinning step is required from the backside to expose the metalized vias. This is also called the super-fill process and is described in [45, 41].Schematic of this process is shown in Figure 28(a)

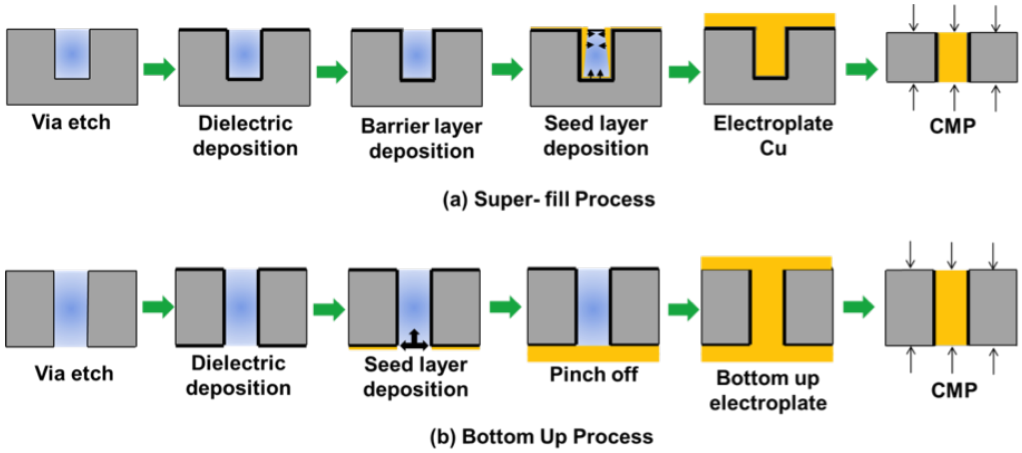


Figure 28: Cu via filling methodologies.

An issue with this process is that it requires mechanical polishing on both sides of the wafer. Another issue with this method is that it cannot be used for very high aspect ratio TSVs. From our literature search, we have found the maximum aspect ratio for this method to be 8:1. The limitation arises from the fact that there is a need for a conformal seed layer deposition on the sidewalls of the TSVs. As the aspect ratio of the via increases and via diameter reduces, the seed layer deposition becomes increasing non-conformal leading to voids in the filling process. As seen in Figure 29, as the aspect ratio increases, the via filling ratio reduces. This shows that there is a clear dependence of via fabrication on aspect ratio. Via etching parameters have to also be carefully controlled to reduce the scalloping on the sidewalls. If the

scalloping increases, then the conformity of the sidewall seed layer reduces thereby reducing the fill factor.

Due to these reasons, this process was not used for integrating TSVs in microchannels. As already discussed, microchannel wafers are thick (at least 300μm) and to fabricate TSVs (diameter 10-50μm) would require aspect ratios in the ranging from 30:1 to 6:1 which would not be feasible using this process.

4.3.2 Bottom up Process

Another method to fabricate TSVs, also known as the *bottom up* TSV process, is as shown in Figure 28 (b). Vias are etched all the way through followed by dielectric deposition. A seed layer is then deposited on the bottom and electroplated on that side until the seed layer around the circumference of the via is closed-up. Using this newly electroplated pinched-off seed layer, the TSVs are filled using *bottom up* electroplating of Cu. A demonstration of fabrication of TSVs in thick wafers using this technique is shown in [50, 91, 72, 67].

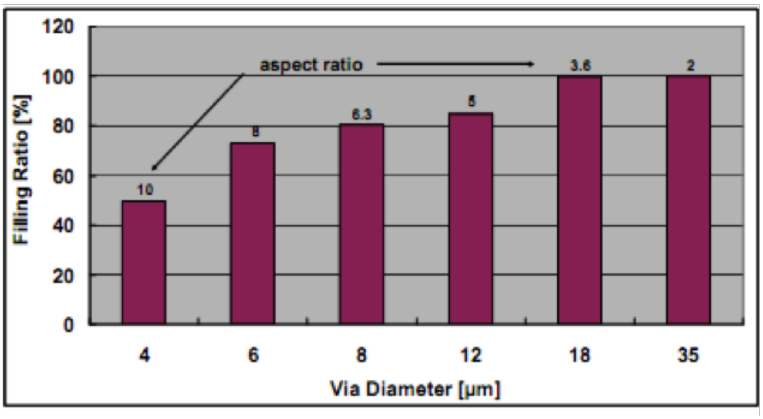


Figure 29: Via filling ratio in dependence of via diameter and via depth (aspect ratio) for sputtered TiW/Cu seed layer [85].

The advantage of the bottom up TSV process is that it is independent of the DRIE angle as well as the scalloping effect that occurs during etching. This process also allows for higher aspect ratios as compared to the super-fill approach due to the fact

that no conformal seed layer is needed for electroplating. Due to these advantages, the bottom up process is the technique that was chosen to fabricate TSVs with microchannels.

There is however one disadvantage to the conventional bottom up process. Since the pinching process requires pinching-off the entire via diameter, it takes an unrealistic amount of electroplating time (few hours for 50μm). During pinch off, a thick copper layer is formed requiring two CMP steps to planarize the wafer: first, on the top to remove any over plated Cu after TSV fabrication, and second, to remove the excess copper on the back side which has electroplated during the pinch-off process. This increases process complexity and reduces yield. In order to reduce time needed for pinch-off and eliminate the need for a CMP step on the bottom side, novel bottom up electroplating process known as the *mesh process*, was desmonstrated. The details of the mesh process are discussed in the next section.

4.3.3 Mesh Process for TSV fabrication

Once the wafers are bonded and thinned, TSVs (50μm diameter) are patterned on the fins of the microchannels using backside alignment. In order for TSVs to be patterned, alignment marks were created on the back of the wafer using positive resist (Shipley 1827).

Figure 30 shows the alignment mark creation on the back of the wafer using positive resist.

(a) (b)

Figure 30: (a) Alignment mark creation for backside alignment, and (b) Alignment with FTSVs seen through oxide layer.

Table 5: Recipe for mesh oxide etching.

Parameter	**Value**
Cloud Position, W	50
Ctune Position, W	50
Process Pressure, mT	12
RF Setpoint, W	350
O2 Flow, $sccm$	6
Ar Flow, $sccm$	20
CHF3 Flow, $sccm$	40
Etch rate, $min/\mu m$	45

Once patterned, TSVs are etched using the Bosch process in an ICP till the vias reach the oxide etch stop layer (Figure 22(e)). TSV diameters ranging from 25-80μm have been explored. However for this first prototype a diameter of 50μm was selected. It is imperative that the etching be controlled towards the end as the oxide layer is needed for further processing.

A mesh is then patterned on the silicon dioxide membrane as shown in the Figure 31(a). The mesh pattern is aligned with the vias visible through the oxide. The exposed oxide is etched using RIE using the following recipe: (Figure 31(b)). After the mesh formation, a sidewall isolation of SiO_2 (1μm) is grown using thermal oxidation (Figure 22(f)). Low temperature processes such as PECVD oxide can also be used for sidewall insulation; however since we are using the heterogeneous integration scheme, there is no temperature constraint for sidewall isolation. Following via sidewall isolation, a seed layer of Ti (300 $\mathring{A}$) and Cu (2000$\mathring{A}$) is deposited on top of this dielectric mesh using e-beam evaporation followed by bottom-up electroplating process.

There are two steps involved in the bottom-up electroplating process. In the first step, the capping side of the wafer is covered by a non-conductive tape, and copper is plated on mesh. The electroplating is continued until the mesh opening pinches off. In the pinch-off process, copper tends to be plated at the corners of the mesh openings as shown in Figure 31(c). This results in faster pinch-off times as compared

to using the conventional electroplating process on vias without mesh patterns.

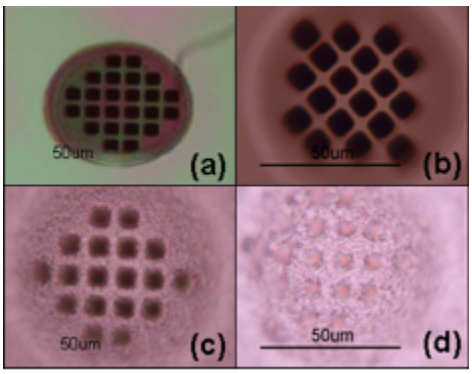


Figure 31: Mesh fabrication for faster pinch off times (a) Mesh patterning (b) Etching of mesh (c) Seed layer deposition (d) Pinch-off.

The pinched-off mesh opening are shown in Figure 31(d). Once the vias are pinched off, the second step is through via electroplating to fill the vias using topside electroplating. The tape on the front-side of the wafer is now removed, and the bottom side of the wafer is then sealed with the non-conductive tape. Electroplating is performed at the bottom of the vias where the sealed copper mesh serves as the seed layer (Figure 22(g)). After plating copper in the rest of the vias, the tape is removed and the over-plated copper on the front side is removed by conventional Chemical Mechanical Polishing (CMP) process using the iCue 5001 copper slurry, while the copper seed layer on the back side of the wafer is removed by wet etching (Figure22(h)).

Figure 32 shows a schematic that summarizes TSV fabrication using the mesh process. Figure 33 shows SEM and optical images of TSVs fabricated using this process.

4.4 Results of Integration

Shown in Figure 34 are X-ray and optical images of integrated microchannels and TSVs. The chip size is 10mm X 10mm and 51 microchannels are fabricated in a given chip. The depth of the microchannels is about 150μm and width is 100μm.

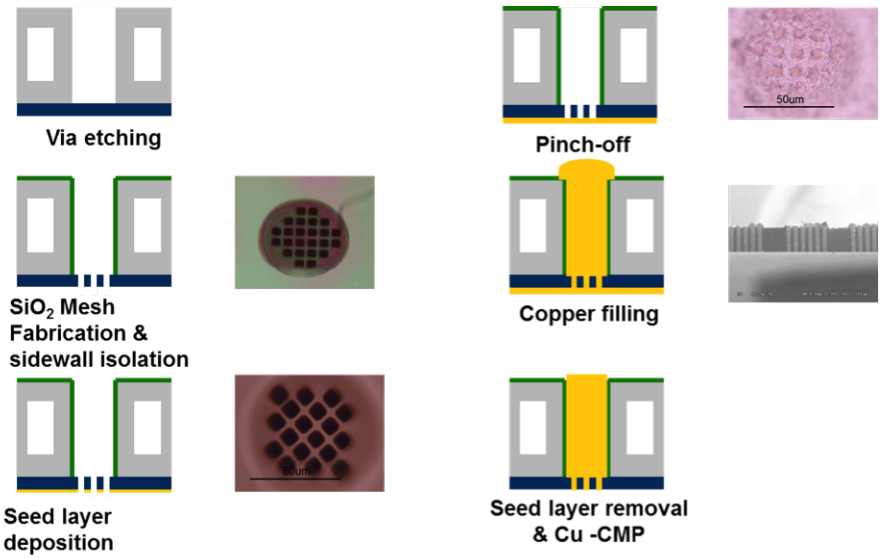


Figure 32: Schematic of TSV fabrication in microchannels using mesh process.

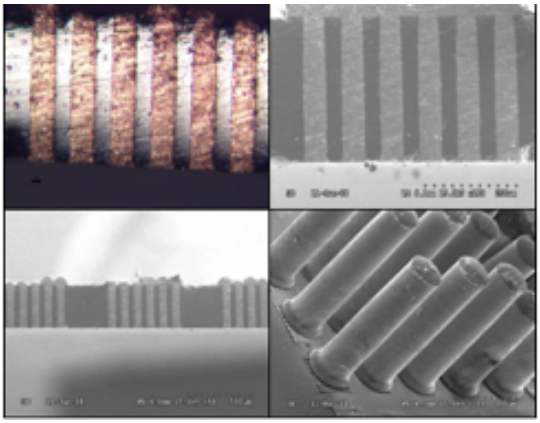


Figure 33: Results of bottom-up electroplating of TSVs.

Electrical through vias with a diameter of 50μm and a height of 500μm have been integrated with the microchannels. No voids or seams were observed when the TSVs were inspected in the SEM, X-Ray microscope, and optical microscope. We have thus demonstrated a wafer level batch fabrication technique for integrating TSVs and microchannels. Figure 35 shows how TSVs and MFCs are embedded in the heterogeneous integration scheme proposed in Chapter III.

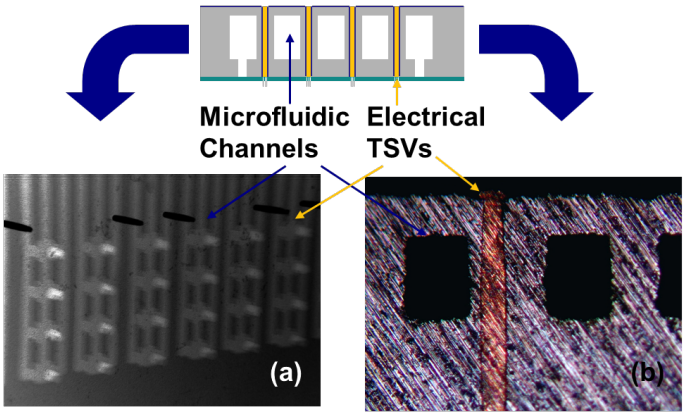


Figure 34: (a) X-Ray Image of Microchannels and TSVs integrated on a single Chip. (b) Cross-sectional optical image of integrated microchannel heat sink and electrical through-silicon vias.

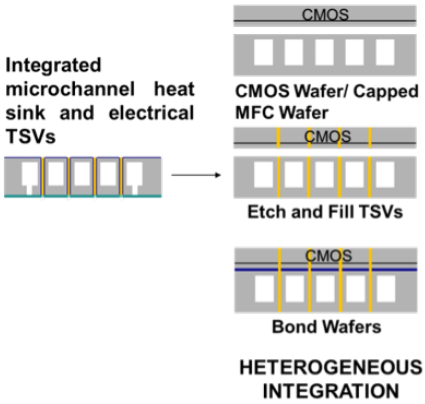


Figure 35: Integration with heterogenous scheme.

4.5 Hydraulic Testing

Hydraulic testing was performed on these samples with TSVs and microchannels. To our knowledge, this has been a first time for any group to report the testing of microchannels integrated with TSVs. Fluidic reliability tests have been performed on these samples by passing DI water through the microchannels using the setup shown in Figure 36. Flow rates ranging from 20ml/min to 200ml/min have been tested with no mechanical failure. We also measured the differential pressure drop of these microchannels for different flow rates. An aluminum manifold was attached to the vias using epoxy. Due to the epoxy application process, some vias are clogged with epoxy hence we have a higher pressure drop than what is expected. The result of this testing is as shown in Figure 37. As it can be seen the pressure drop values are close to calculated values when 50% of the vias are open.

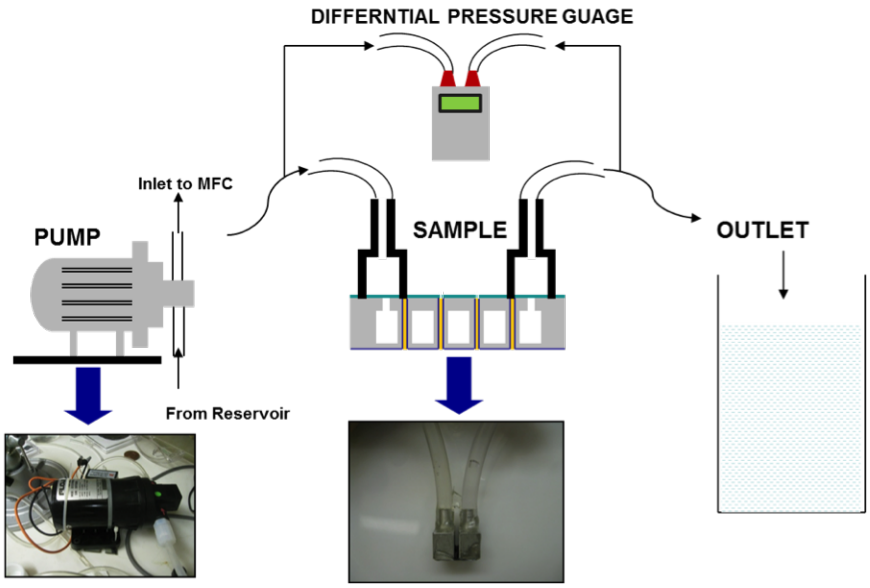


Figure 36: Experimental setup for reliability and pressure drop measurements.

4.6 High Density TSV Fabrication

Having demonstrated the ability to fabricate TSVs and microchannels reliably in thick silicon wafers, high density, high aspect ratio TSVs were explored. Based on

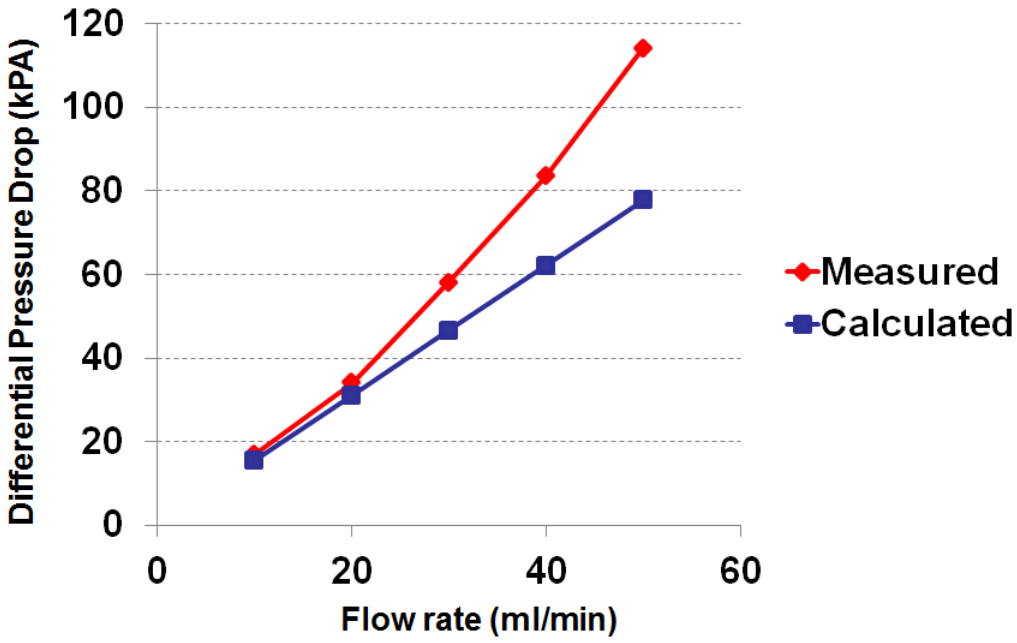


Figure 37: Hydraulic pressure drop vs Flow rate measurements.

the modeling results in the previous chapter, there is a clear need for fabricating high density TSVs. The number of TSVs required in a 3D system is a complex issue dealing with design, architectural specifications, level of folding, etc. 3D can be implemented at the lowest possible level (transistor level) requiring highest via density or at a high level requiring least via density. There is a trade-off involved in terms of area efficiency as shown in Figure 38. As the number of TSVs increase, the area available for active silicon reduces.

The fabrication process for high density, high aspect ratio TSVs is as shown in Figure 40. Due to aspect ratio constraints of etching, several novel techniques were explored in order to fabricate these structures successfully. As a first attempt, we have fabricated 10μm diameter TSVs with a pitch of 15μm in 200μm thick double side polished wafers. The mask design is as shown in Figure 39. As it can be seen this TSV design is compatible with microchannel structures.

Due to the high aspect ratio of the TSVs, a very thick ($> 20\mu$m) photoresist mask is required in an ICP machine in order to etch these TSVs. Hence the approach that

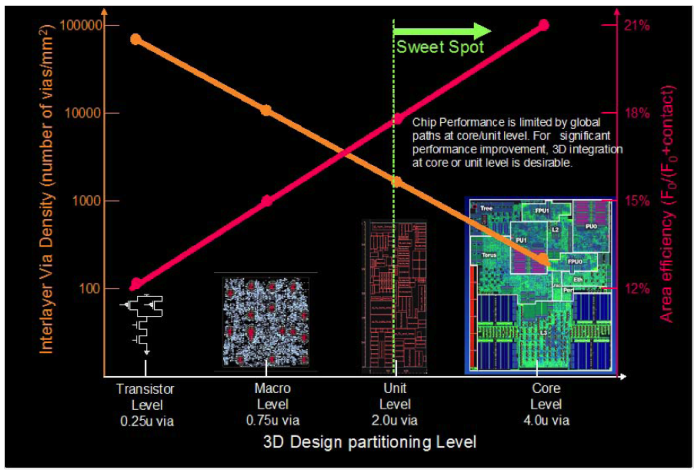


Figure 38: Via density vs Area Efficiency tradeoff (Source IBM)

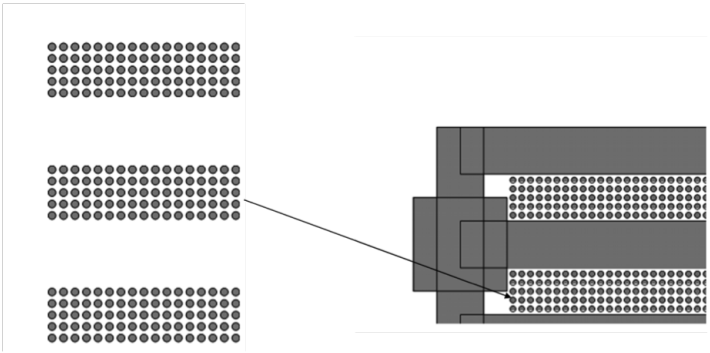


Figure 39: Mask design for high density, high aspect ratio TSV.

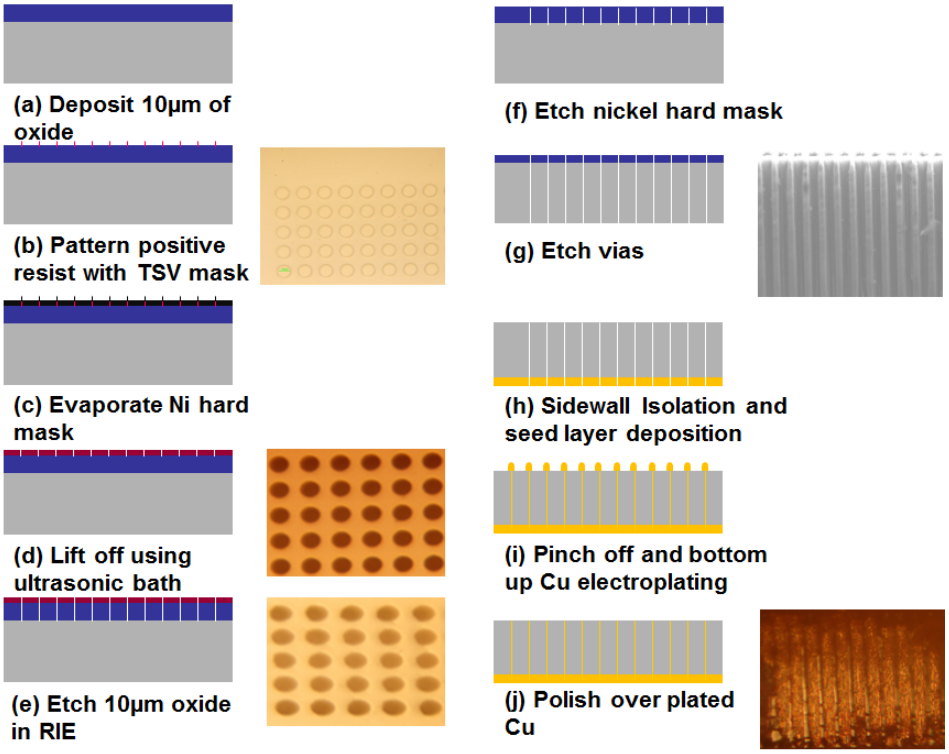


Figure 40: Schematic of high density, high aspect ratio TSV fabrication.

was used in the previous section cannot be used effectively. Due to the dimensions and density, we developed a process of using a thick oxide film as an etch mask for the TSVs. The first step of the process is deposition of a thick oxide layer (10-14μm) which will subsequently act as the mask for TSV etching.

In order to use the oxide as a mask for TSV etching, it must be patterned. A nickel hard mask technique was developed to pattern the oxide mask. The reason for the choice of hard mask is due to selectivity of photoresist to oxide during oxide etching. Photoresist (NR-5 8000) has a selectivity of 1:1 in the RIE machines in our cleanroom facility and hence, there is a challenge in patterning thick resist with our desired dimensions. Using the TSV mask, positive resist was patterned on the wafer as shown in Figure 40(b).

A thin layer of Ti/Ni (300$\mathring{A}$/5000$\mathring{A}$) was deposited on the surface (Figure 40(c)). The wafers were then dipped in acetone for the lift-off process. The positive resist

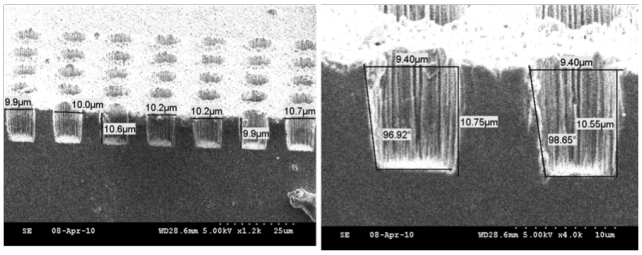


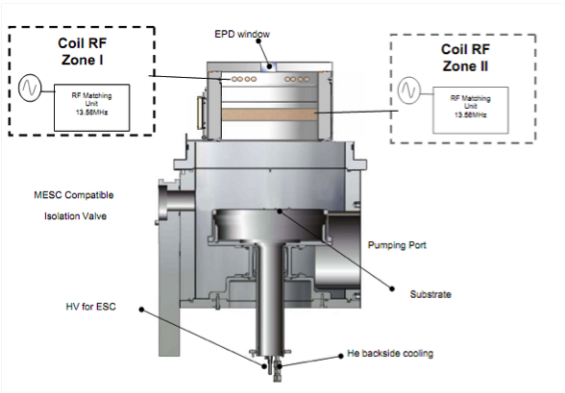
Figure 41: Cross-sectional images of 10μm oxide mask.

lifts off in acetone and subsequently, the TSV pattern is transferred onto the nickel layer as shown in Figure 40(d). The exposed oxide was etched in Plasma therm ICP machine.

As it can be seen in the cross sectional images (Figure 41), the sidewalls of the oxide mask are fairly perpendicular. This is important to ensure that the sidewalls of the TSV remain straight during silicon etching. The top view of the wafer after the oxide etching is as shown in Figure 40(e). Using this process, we could achieve a selectivity of 30:1 for oxide to nickel etching. The remaining nickel layer is etched off using a piranha bath.

In order to etch these high aspect ratio TSVs, the STS Pegasus (Figure 42) was selected instead of using conventional tools (STS ICP), since it has improved etch rates, etch uniformity, selectivity and was suitable for high aspect ratio TSVs.

(a)



(b)

Figure 42: STS Pegasus in the MiRC cleanroom.

Table 6: Etch recipe for high density, high aspect ratio TSVs.

Parameter	**Start value**	**End value**
Passivation, *seconds*	2	2
Etch, *seconds*	2.4	3.4
Main Pressure: Passivation, mT	20	20
Main Pressure: Etch, mT	16	18
C_4F_8 flow, *sccm*	150	150
SF_6 flow, *sccm*	250	175
13.56 MHz Coil, W	220	220
380 kHZ Platen, W	90	90
LF Pulse Generator Duty Cycle	70	70
Platen Chiller $^\circ C$	0	0
Etch rate $s/\mu m$	40	40

The power handling capacity and plasma generation area is higher for the Pegasus when compared to conventional ASE tools. It produces a neutral high radical density in the center of the wafer and a uniform ion density across the whole wafer surface which improves etch depth uniformity. It also has advanced substrate cooling and passivation phase enhancements which further contributes to uniform etching and high etch rate [33]. The recipe described in Table 6 was used in the Pegasus for etching.

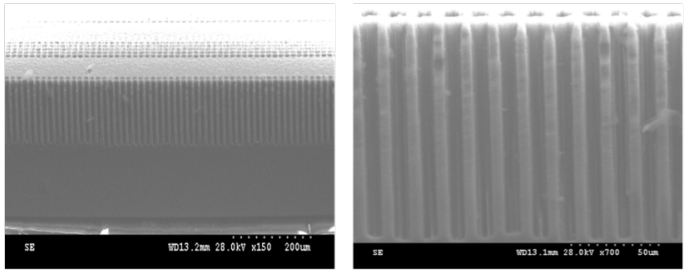


Figure 43: Etching of high aspect ratio TSVs using STS Pegasus.

Etching results are shown in Figure 43. After etching, we grow a 200nm thick thermal oxide for side wall isolation(Figure 40(h)). This sidewall isolation can also be performed using low temperature processes such as PECVD. Following sidewall isolation, a Ti/Cu seed layer ($300\mathring{A}/1000\mathring{A}$) is sputtered on the backside of the

vias. As the TSV diameter is small (10μm), a mesh process described in the previous section was not required as the pinch-off time is in the order of few minutes. Pinch-off for10μm TSVs took about 15-20mins at 20mA dc current in a copper plating bath. The pinch-off process for the 10μm TSV is shown in Figure 44.

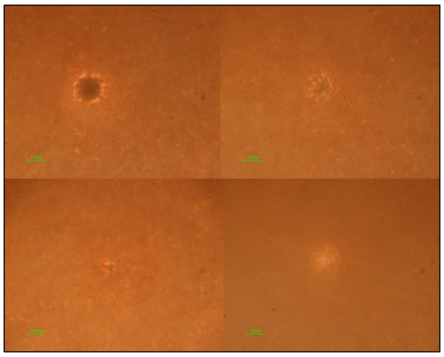


Figure 44: Pinch-off process for 10μm TSVs.

After seed layer pinch-off, the wafer is inverted and bottom up electroplating is performed to fill the vias completely with Cu (Figure 40(i)). The results of the bottom up plating are shown in Figure 45. After plating, the excess Cu on the top is removed by CMP and the seed layer is etched using wet etching(Figure 40(j)).

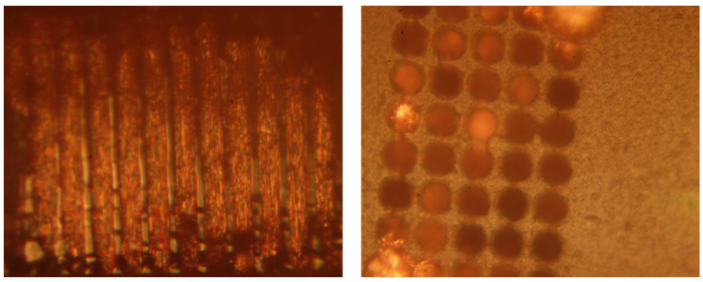


Figure 45: Cross section and top view of high density, high aspect ratio TSVs

Thus, we have successfully demonstrated void free fabrication of high aspect ratio (20:1) and high density (200K/cm^2) TSVs. This fabrication process is scalable to TSV diameters of 5μm and aspect ratios in range of >40:1 and can be integrated with microchannels using the processes shown in the previous section.

CHAPTER V

3D THERMAL TEST BENCH DEVELOPMENT

The last component of this thesis discusses the design and fabrication of a 3D thermal test bench in order to evaluate the cooling performance of microchannels in different stacking architectures such as memory on processor, processor on memory, and processor on processor.

5.1 Motivation

Three-dimensional chip stacking technology provides a new approach to address the so-called *memory wall* problem. Memory processor chip stacking reduces this memory wall problem, permitting faster clock rates (with suitable processor logic) or permitting multicore access to shared memory using a large number of vertical vias between tiers in the stack, for ultra wide bit path transfer of data and address information to and from various levels of cache. Performance enhancements of processor-memory configuration have been evaluated in [86]. Another advantage of 3D chip stacking is the possibility of stacking processors. One of the main applications of such stacking is high performance computing systems.Most supercomputers today are limited by network latency delays. Supercomputers implement the message passing interface (MPI) to communicate between the processor nodes. Huge applications that run on many processor nodes spend significant processing time in forming and processing packets that have to be sent across the optical networks to other processor nodes in the room. Currently the network latencies seen in handling the message packets are on the order of several hundreds of clock cycles. If processors are stacked, then the latency delays would decrease significantly and improve the overall system performance [35].

Clearly there is a need for novel architectures which involve processor-memory and

processor-processor stacking.However, there are certain thermal constraints which must be explored.

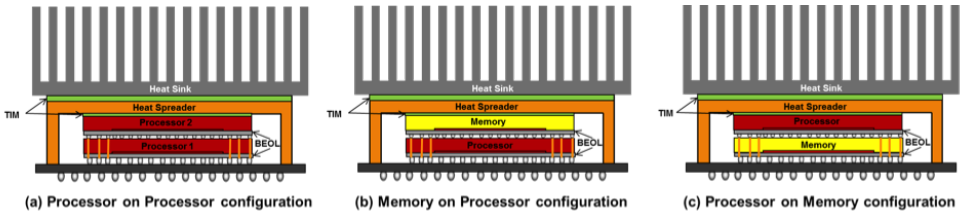


Figure 46: Different stacking configurations.

Processor on processor configuration: In processor on processor applications, there are two heat dissipating ICs directly on top of each other effectively increasing the heat dissipation per area. For example, if both processors dissipate 100 W/cm^2 of heat then when stacked the effective heat dissipation would be about 200 W/cm^2 (Figure 47). The situation is further aggravated in the presence of hotspots. Shown in Figure 46(a), is a graphical representation of how processor on processor configuration can be applied using conventional air cooling techniques. From the standpoint of processor 1, the path for heat dissipation is longer due to the presence of processor 2 in the path to the heat sink. Hence a temperature rise is seen in processor 1, and would be higher as compared to a standalone 2D processor. For processor 2, power delivery and signaling is a challenge as high density of TSVs will be needed to supply power and signaling to processor 2 from the board. These large numbers of TSVs will be routed through processor 1, thereby reducing the available area for active silicon.

Memory on Processor configuration: Shown in Figure 46(b) is a graphical representation of a memory on processor type configuration implemented using conventional air-cooled heat sink. Having the processor closer to the board is advantageous from the point of view of power delivery and signaling. However as stated above, the presence of the memory chip between the processor and heat sink results in a degraded thermal path, thus posing thermal challenges in cooling the processor chip

efficiently.

Processor on Memory configuration: Shown in Figure 46(c) is a graphical representation of a processor on memory type configuration implemented using conventional air-cooled heat sink. Having the processor closer to the heat sink helps dissipate the heat produced in the processor. However power supply and signaling must be routed through the memory chip from the board using a large number of TSVs which consumes area on the memory chip.

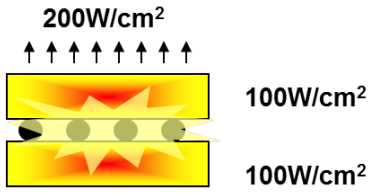


Figure 47: Power dissipation in stacked processors.

As seen above, there are trade-offs involved in stacking processors and memory and processor. One of the major challenges in implementing processor-processor and memory-processor stacking is that the heat dissipating devices are stacked directly on top of each other leading to a higher heat density than in a comparable 2D chip and a degraded thermal path which makes it challenging to remove heat from the active devices. Another issue is the thermal effects of one IC on other stacked components above and below it. This *thermal crosstalk* can affect the performance of other components in the stack, further degrading the system performance. We have already discussed the limitations of air cooled heat sinks and the motivation behind liquid cooling in Chapter II. To this end, we believe that back side microchannel cooling at each stratum will be necessary for effective cooling.

Shown in Figure 48 above is the 3D thermal test bed which focuses on the cooling needs of stacked architectures. Having shown the integration of TSVs and microchannels in Chapter IV, we did not include TSVs in this analysis to simplify fabrication complexity. The system includes stacking of 2 dies each having microchannel liquid

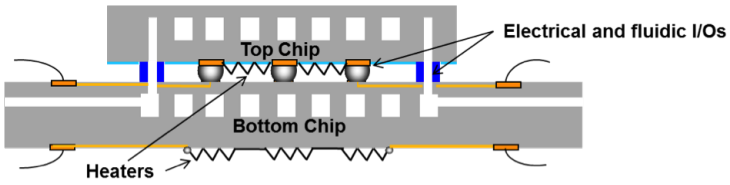


Figure 48: Schematic of proposed 3D thermal testbed.

cooling on the back side, a heat source to simulate active circuits and electrical and fluidic I/Os for bonding and routing liquid. It consists of microchannel cooling in each layer with the bottom chip also acting as the substrate to feed the liquid from the pump. The two chips are bonded using conventional flip chip bonding. We use electrical solder bumps to make electrical interconnections between the 2 layers and solder based fluidic I/O for fluidic sealing and routing between the layers. A detailed study about the electro-fluidic I/Os have been reported in [43].

The design goals for this system include:

- Power dissipation for Top and Bottom Chip: 100W/cm^2 (Can be varied depending on which configuration is being simulated)
- Target thermal resistance based on ITRS Projections: 0.2 °C/W
- Power supply constraint: 60V, 3A
- Max Flow rate due to pump restrictions: 100ml/min

A heating area of 0.7cm X 0.7cm is chosen which gives the area of chip (A_{chip}) = .49cm^2. Hence required power dissipation = 50W (in order to achieve target power dissipation of 100W/cm^2. Heaters and microchannels are designed with this as the starting point.

5.1.1 Heater Design

Multi-function thin-film heaters/thermometers were designed and fabricated on the test chips. In order to simulate active circuits, a platinum thin film heater was

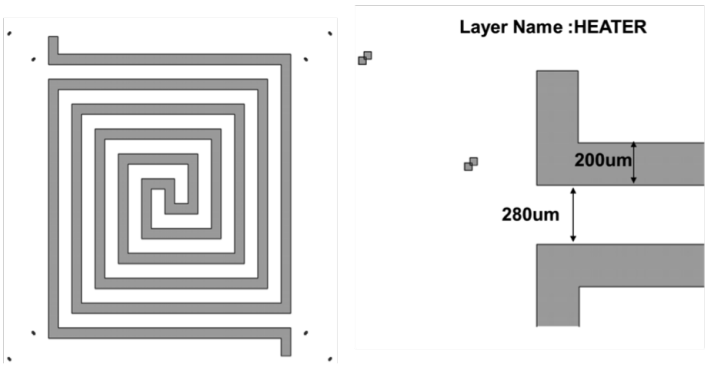


Figure 49: Mask design for platinum heaters.

designed to dissipate 50W of power. The reason that Pt was selected for the thin-film heater/thermometer is that it is a thermally stable noble metal and its resistance changes as a linear function of temperature. The temperature coefficient of the Ti/Pt film is 0.0033-0.0039 $K^{-}1$ [93]. Therefore, the heaters can also serve as thermometers for the purpose of temperature sensing.

A target resistance of 36Ω was chosen since due to the power supply constraints. A 36Ω resistance would require a voltage of 36V and current of 1.4A to dissipate 50W of power over an area of 0.7cm X 0.7cm. The design shown in the figure above has a length of the platinum heater of 73mm. With thickness of 200μm, and knowing the resistivity of platinum as 105nΩ-m, we can calculate the thickness of the heater using the following equation:

$$R = (\rho L)/(WH) \tag{5}$$

The thickness of the platinum heater is calculated to be 1μm.

5.1.2 Microchannel Design

From ITRS projections, the target thermal resistance of heat sinks for high performance ICs is less than 0.2 °C/W [4]. The microchannels in the top and bottom chip are designed using the equations shown in Figure 19. Figure 50 shows the microchannel design and Table 7 lists the design parameters.

The complete set of masks for the top chip superimposed on each other is as

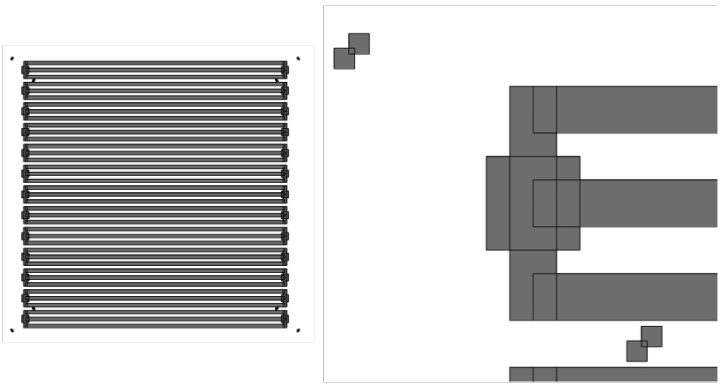


Figure 50: Mask design for microchannel heat sink.

Table 7: Design parameters for microchannel heat sink.

Parameter	**Value**
Width of channels, W_c *(μm)*	80
Height of channels, H_c *(μm)*	350
Length of channels *(cm)*	0.7
Number of channels	39
Thermal Resistance *(°C/W)*	0.2291

shown in the Figure 51. Fluidic vias (100μm diameter) are used to route the fluid from the bottom chip to the top chip into the microchannels. A single rectangular solder based fluidic I/O is chosen from the previous solder pipe designs to minimize the possibility of solder flowing into the fluidic vias during assembly. There are 621 solder bumps each having a diameter of 120μm. This gives a solder bump density of 1242/cm^2. The solder bumps provide the electrical connection from the heater to the copper pads fabricated on top of the bottom chip. The solder bumps also provide mechanical integrity to the bonding of the top chip to the bottom chip which is a solder-Cu bond.

The complete set of masks for the bottom chip superimposed on each other is as shown in Figure 52. It consists of a large feeding channel connected to inlet/outlet ports for fluidic delivery from the pumping system. The feeding channel supplies fluid to a set of microchannels on the substrate level. Part of the fluid is also routed to

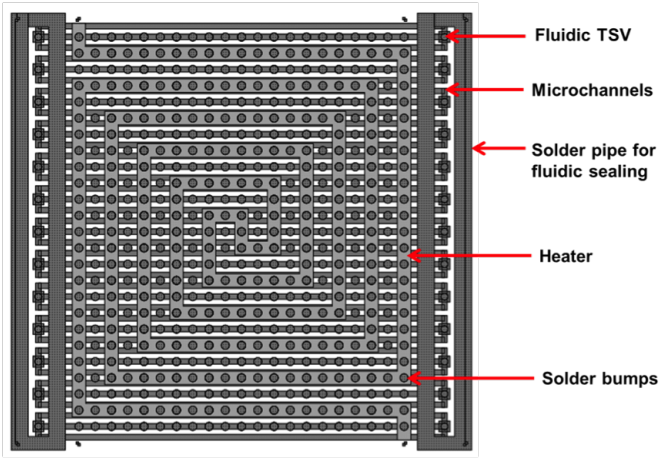


Figure 51: Mask design for top chip.

the top chip through a set of 26 fluidic vias. Copper pads are fabricated on top of the bottom chip to which solder bumps and the solder pipe are bonded using flip chip bonding. These copper pads are used to supply current to the heater located on the top chip. Another set of Cu pads are also present on the bottom side in order to make electrical connections with the heater fabricated on the bottom side of the bottom chip. This heater simulates an active layer in the bottom chip as well.

5.1.3 Top Chip Fabrication

The schematic in Figure 53 shows the fabrication process for the top chip. We begin with a 500μm thick double side polished blank silicon wafer and deposit 2μm SiO_2 on the backside of the wafer (Figure 53(a)). We then pattern and etch FTSVs and microchannels as discussed in chapter IV as a 2 step etching process (Figure 53(b)). The target depth of the microchannels is 350μm. Results of microchannel etching are as shown in Figure 54. Following etching, the wafers are cleaned using resist remover (RR4) and platinum heaters are deposited on the bottom of the top chip using a lift off process as follows (Figure 53(c)): a 18μm thick negative photoresist (NR5-8000, 1200rpm/500rps/50s) was first spun and patterned on the bottom side. After the development and a short RIE descum, Ti/Pt (10000$\mathring{A}$/300$\mathring{A}$) film was deposited

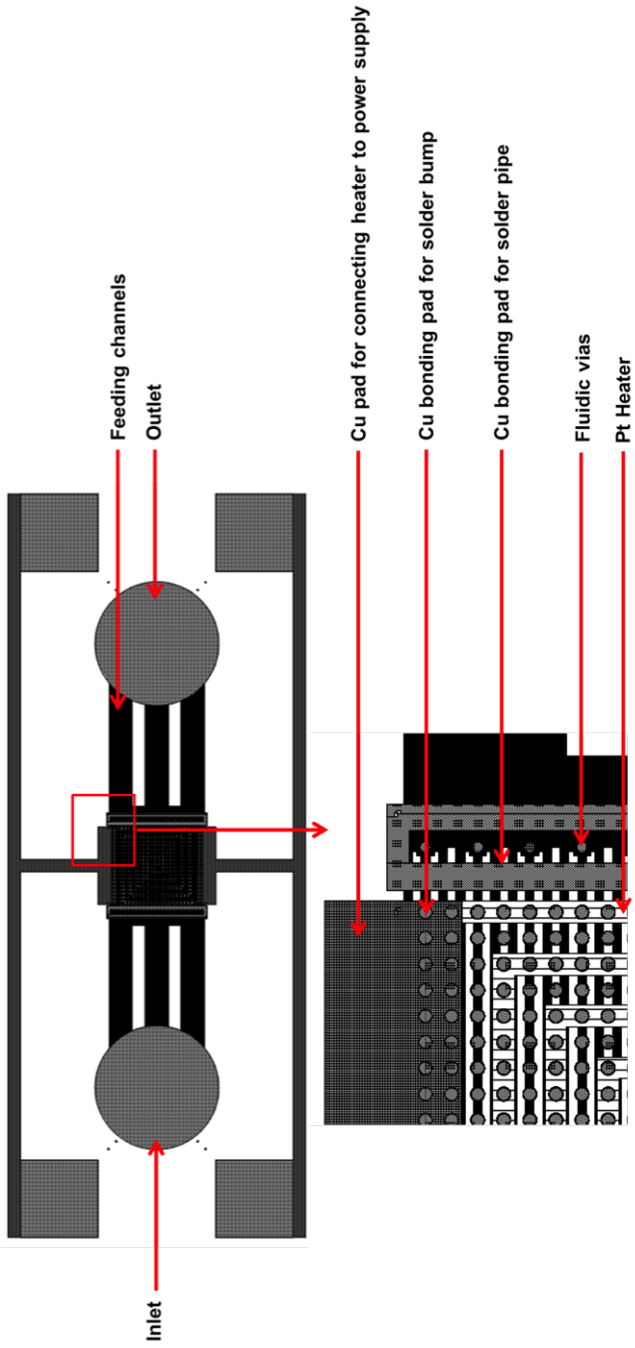


Figure 52: Mask design for bottom chip.

using the Uniflim sputter. The photoresist was then removed by soaking and agitation in acetone and the heaters were left as shown in Figure 55. The microchannels are capped with a 300μm thick blank silicon wafer using plasma enhanced direct silicon bonding also discussed in chapter IV (Figure 53(d)).

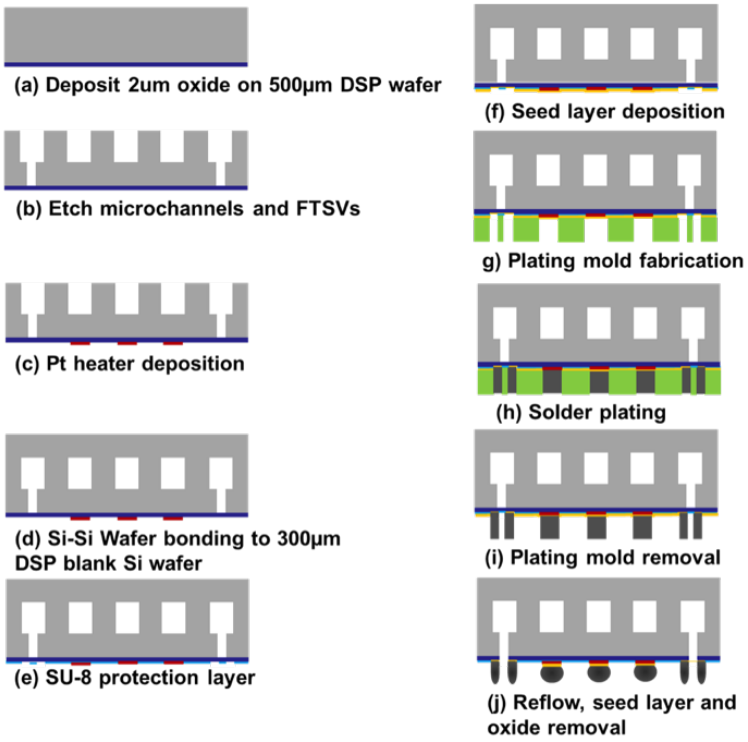


Figure 53: Process steps for top chip fabrication.

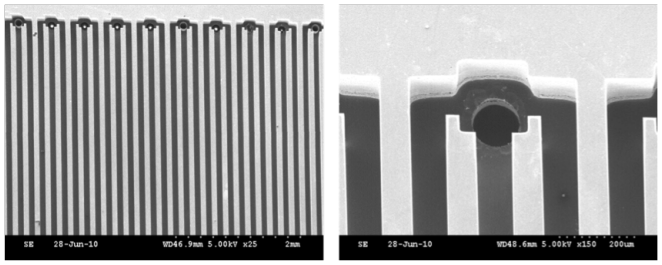


Figure 54: SEM image microchannels.

Following the capping process, a 2μm layer of SU-8 is deposited on the back side to protect the heaters from any further processing steps. The SU-8 is patterned such that there are openings in the resist which allows solder bumps to be plated on the heater

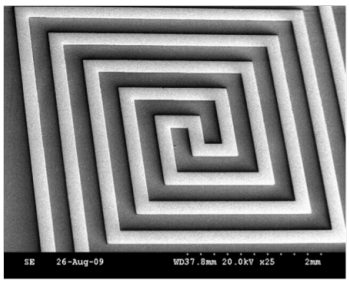


Figure 55: SEM image of Pt heaters.

surface. The SU-8 also acts as a solder dam which restricts the solder within the pad during the reflow process (Figure 53(e)). A seed layer of Ti/Cu/Ti is deposited on the bottom side which provides electrical continuity across the wafer (Figure 53(f)). This is followed by the fabrication of a plating mold (using NR5-8000) for the solder bumps and fluidic I/Os. At a spin speed of 600 rpm, a 30μm thick NR5-8000P photoresist is coated across the bottom surface (Figure 53(g)). After development, a descum process was performed in a reactive-ion-etcher (RIE) to remove photoresist residue. A thin layer (2-4μm) of Ni is plated which acts as the under bump metallurgy (UBM), and solder is then plated over the nickel to fill the mold completely. Solder must be plated immediately following nickel plating to avoid the growth of any oxide and a clean interface between the UBM and the solder alloy is ensured. This is critical for excellent wetting during reflow. Plating is carried out in steps to ensure uniformity across the wafer. The plating steps for Nickel were done in increments from 2mA to 9mA. Solder plating was also carried out in increments from 2mA to 10 mA.

After the plating was completed, the photoresist mold was stripped using acetone (Figure 53(i)). The seed layer was removed using a BOE and aluminum etchant dip. This was followed by a coating the surface with flux (RMA5, Indium Corp.) for the reflow process. Reflow was performed on a hot plate, in three steps: 160 °C for 30s, then 250 °C for 30s, and finally, 160 °C for 30s (Figure 53(j)).

The final step of the process is the removal of the oxide using dry etching and opening of the fluidic TSVs. The top chip after fabrication was examined under the

SEM and is shown in Figure 56.

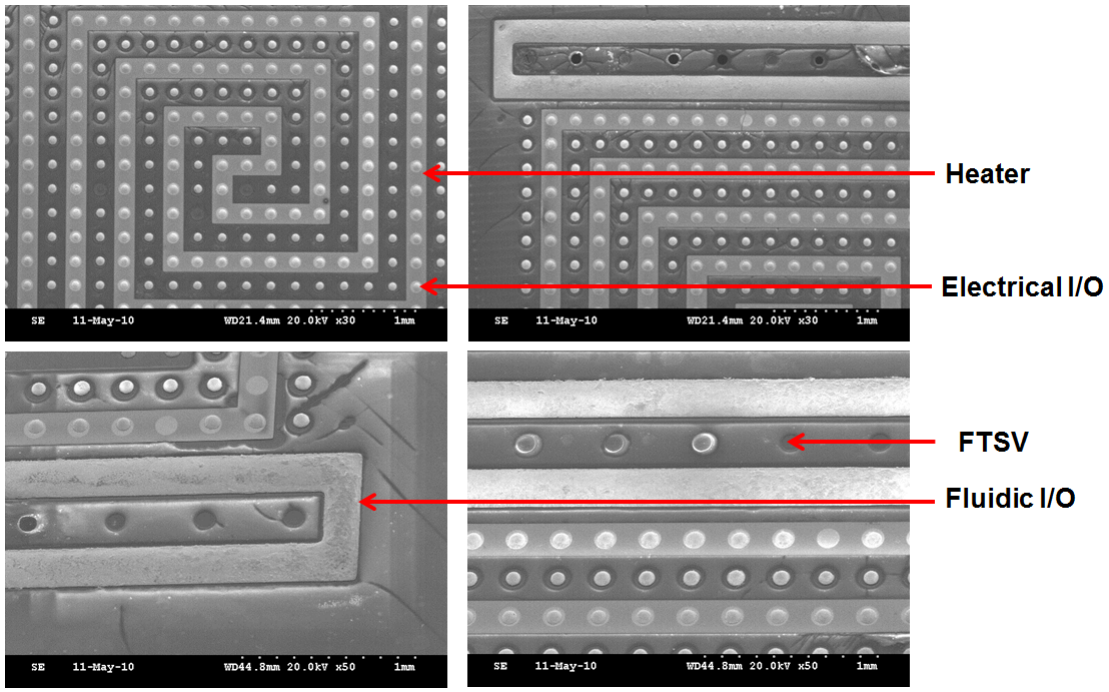


Figure 56: SEM image of top chip after fabrication.

5.1.4 Bottom Chip Fabrication

The schematic in Figure 57 shows the fabrication process for the bottom chip. We begin with a 500μm thick double side polished blank silicon wafer and deposit 2μm SiO_2 on the backside of the wafer (Figure 57(a)). Channels are patterned using NR5-8000 and etched in STS ICP to a depth of 350μm (Figure 57(b)). A SEM of the microchannels after etching is as shown in Figure 58. After resist removal platinum heaters are fabricated on the backside of the wafer using the process described above (Figure 57(c)). The channels are capped using wafer to wafer bonding discussed in Chapter IV (Figure 57(d)). After annealing, a 2μm layer of oxide is deposited on top of the capping wafer. This oxide layer insulates the top surface of the capping layer as copper pads will be fabricated on it eventually.

Cu bonding pads are then fabricated on the top side using the following process: A Ti/Cu/Ti (300$\mathring{A}$/3000$\mathring{A}$/300$\mathring{A}$) seed layer is sputtered using Unifilm sputterer. We

pattern the seed layer using NR5-8000 (1200rpm, 500rps, 50s) and after exposure and development we perform a 30s descum to remove any residual resist. Copper pads are electroplated in the openings to a thickness of 6-8μm. Resist is then removed using resist remover and an acetone dip. The process is repeated on the bottom side of the wafer to form Cu connection pads to the heater on the bottom side. During bottom side electroplating the top side is protected by spinning a thick positive resist on top of the already plated copper pads to prevent any further electroplating. Once the bottom side copper pads are plated to a thickness of 6-8μm, the plating mold and protective topside resist are removed. The last step is the removal of seed layer on top and bottom simultaneously (Figure 57(e)). An optical image of the Cu pads on the top surface is shown in Figure 59.

Oxide is then deposited on the bottom side of the wafer to protect the heaters from any damage. A layer of SU-8 is also deposited on the top side to form an insulating dam around the Cu pads to contain the solder during the assembly process (Figure 57(f)). The last and final step of the process is the etching of the fluidic vias and inlet/ outlet openings on the top side. The fluidic vias(100μm diameter) form a fluidic path from the feeding channels to the top chip and inlet/outlet (3mm μm) is where fluidic manifolds will be attached for fluid delivery from the pump (Figure 57(g)).

Following wafer level fabrication, the top and bottom chips were diced. The top chip was diced in chip sizes of 7mm X 7mm and bottom chip was diced to a dimension of 2.5cm X 6cm.

5.2 Assembly

The basic concept of the thermal-fluidic assembly is illustrated in Figure 60. With a precision flip-chip bonder, a compression force is applied after the top and bottom chip are aligned. The temperature is also increased to enable reflow of the solder

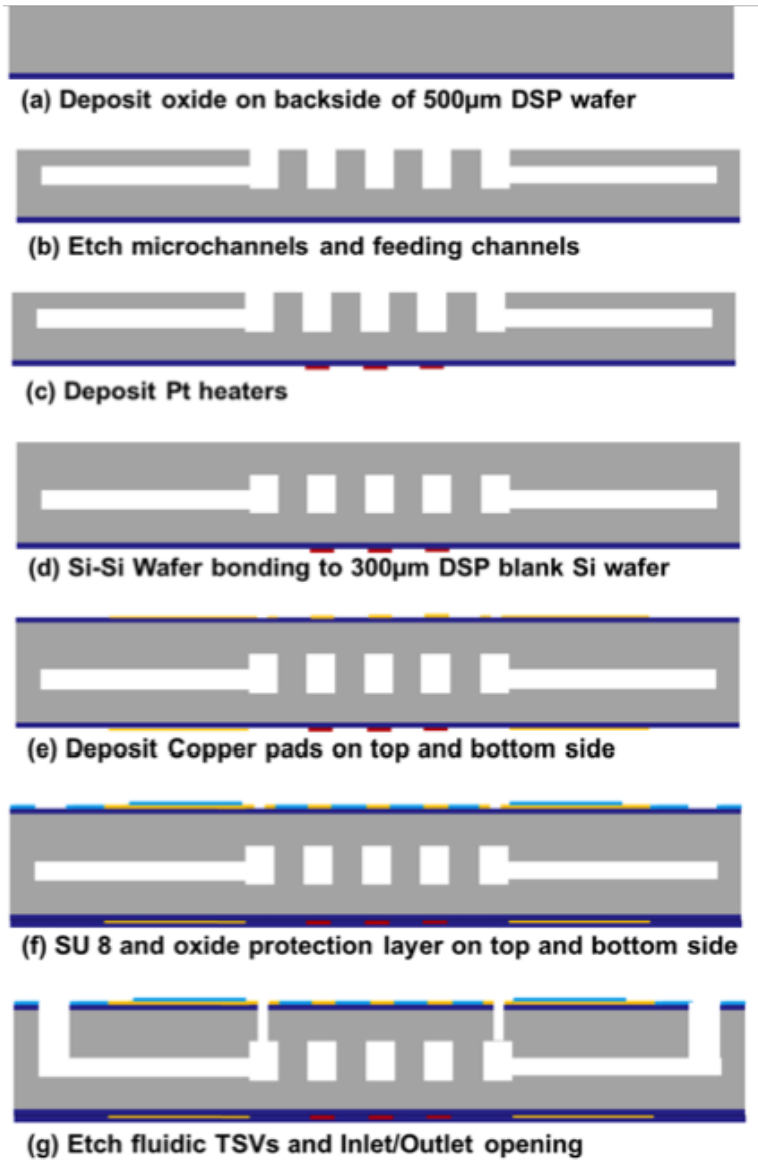


Figure 57: Process steps for bottom chip fabrication.

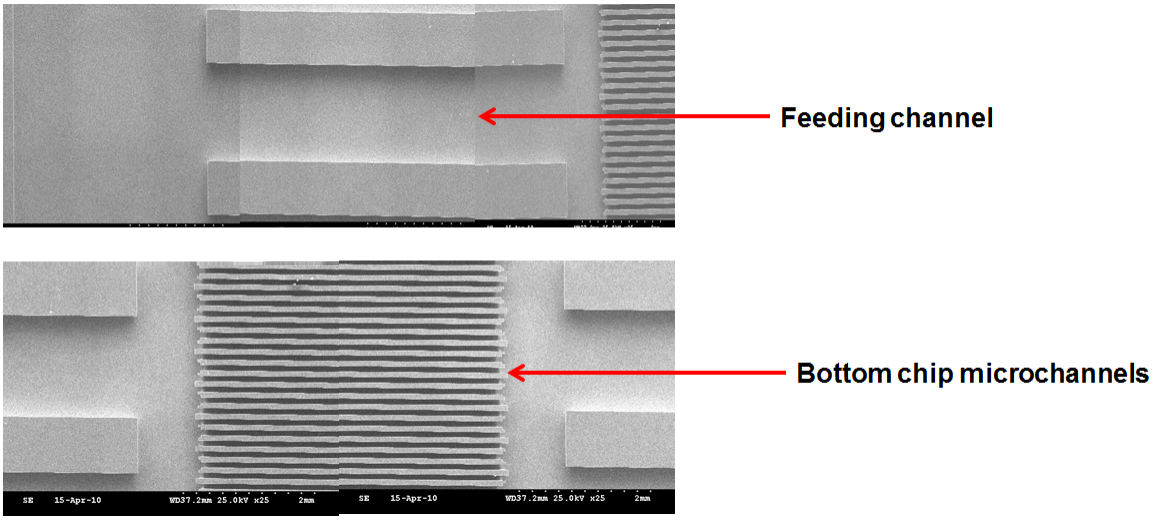


Figure 58: SEM image of microchannels and feeding channels in the bottom chip.

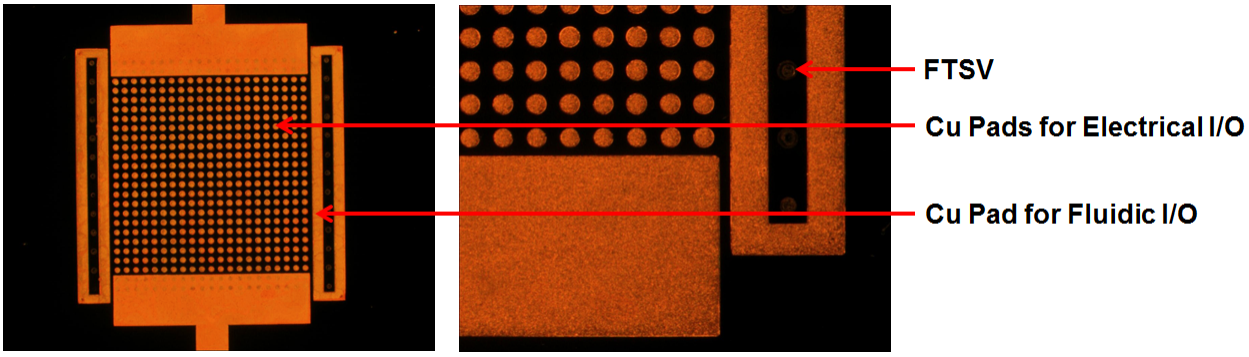


Figure 59: Optical image of Cu pads on the bottom chip.

bumps and solder pipe. A Finetech Lambda flip-chip bonder with high alignment accuracy (+/- 0.5μm) was used. A photograph of the flip chip bonder is shown in Figure 61. With the thermal-compression capability, chips can be bonded with controlled temperature-force profiles using the bonder. Prior to contact, the bottom chip was heated to 40°C and the top chip was heated to 60°C. After alignment a compression force (100g) was then applied to bring them into contact. At the same time, temperature of the substrate was increased to 140°C and the top chip was heated to the reflow temperature (235°C). The temperature profile is shown in Figure 62. Table 8 summarizes the bonding parameters used.

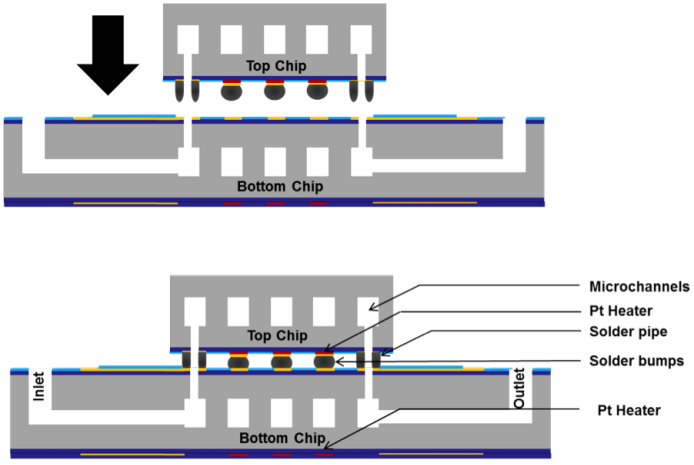


Figure 60: Schematic of assembly process.

Figure 61: Finetech Lambda flip chip bonder.

Table 8: Flip chip bonding parameters.

Parameter	Value
Pre-heating temperature of bottom chip	40°C
Pre-heating temperature of top chip	60°C
Compression force	100g
Bonding temperature of bottom chip	140°C
Bonding temperature of top chip	235°C

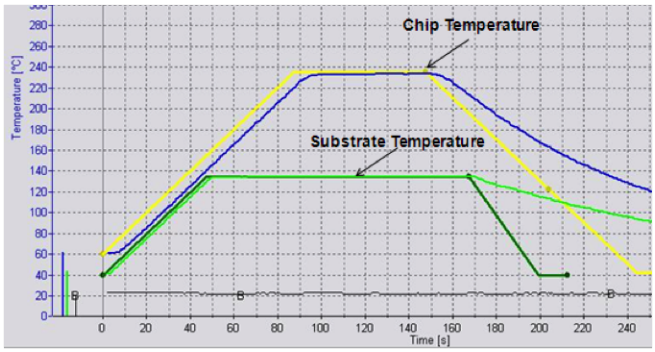


Figure 62: Flip chip bonding recipe showing temperature profiles for top and bottom layer.

Following bonding, we inspected the sample in an X-Ray machine. Figure 63 is the result of the inspection.

5.3 Testing and Measurements

After assembly fluidic manifolds were attached to the inlet/outlet ports as shown in Figure 65. Upchurch nanoports were used for fluidic routing as shown in Figure 64. Nanoport assemblies are commercially available products which are used to provide consistent fluid connections for chip-based analysis.

Hydraulic measurements were made in order to evaluate the sealing of the solder I/Os and the mechanical support provided by the solder bumps after flip chip assembly. The setup used for hydraulic testing is as shown in Figure 66 and Figure 67.

A pump made by FMI (Q Pump drive module, V300) was used. The output

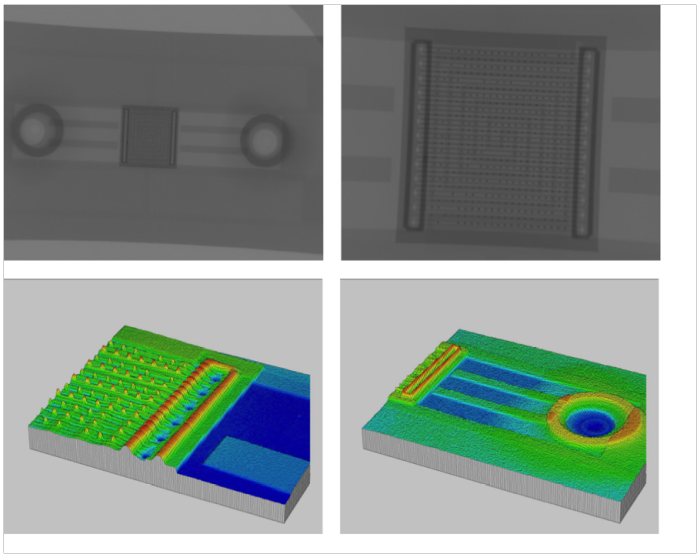


Figure 63: X-Ray images post-assembly.

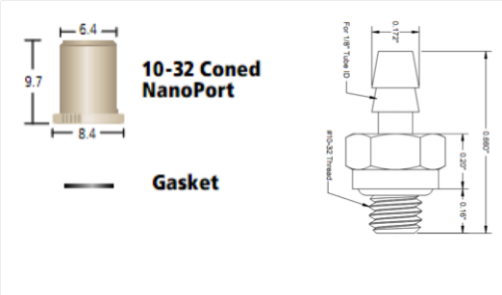


Figure 64: Nanoports for microfluidic assembly.

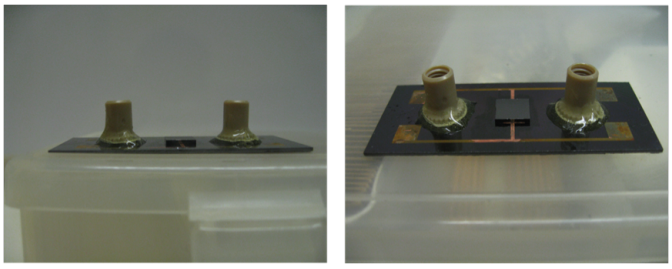


Figure 65: Assembled system with nanoports for fluidic testing.

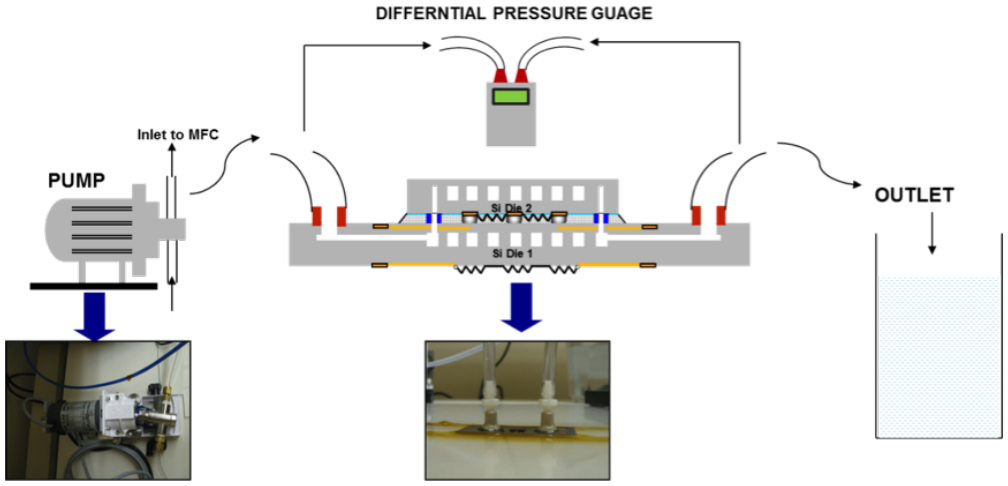


Figure 66: Experimental setup for reliability and pressure drop measurements.

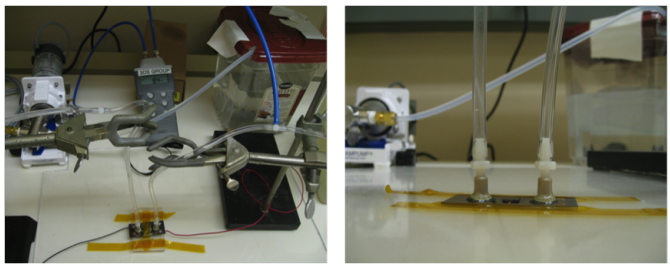


Figure 67: Pictures of experimental setup.

flow rate can be controlled precisely using a built in controller from 10ml/min to 300ml/min. To make pressure drop measurements, a handheld differential pressure guage EW-68600-14 from Cole Palmer was used.

The differential pressure drop was measured for different flow rates. The result of this measurement is shown in Figure 68. Flow rates up to 100ml/min were tested without any leakages in the fluidic sealing of the stack.

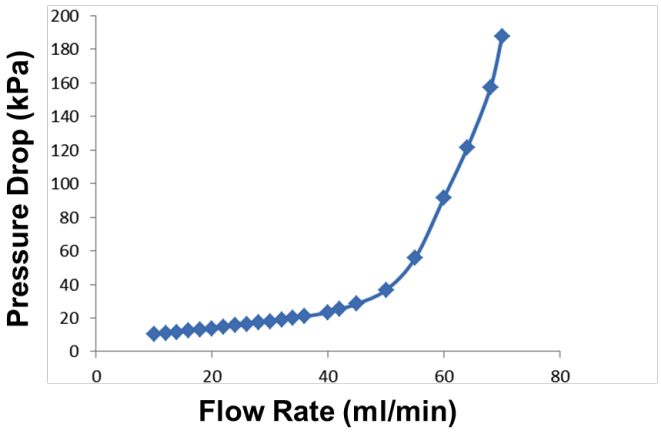


Figure 68: Hydraulic pressure drop measurements for 2 chip stack.

We have thus shown the fabrication, assembly and preliminary testing of a 2 chip stack each having microchannel cooling and a heating layer to simulate active circuits. This test bench can be used to simulate different stacking configurations which were discussed in the first section of this chapter and the effects of liquid cooling on overall system performance.

CHAPTER VI

CONCLUSION AND FUTURE WORK

We have discussed the bottlenecks of current scaling of devices and interconnects, and the lag in silicon ancillary technologies leading to the slowing down of system improvements. Present day market demand for high-performance computing has shifted the focus from 2-D planar system-on-a-chip-type single-chip solutions to alternatives such as 3D die stacks. 3D system integration is a disruptive technology that bridges the wafer and packaging worlds. It represents not only an enabling technology for further improvement of transistor integration densities and increased computing power ("More Moore"), but in addition will be a useful for so-called "More than Moore" applications such as heterogeneous integration of diverse technologies. Several challenges have been identified in implementing high performance 3D systems such as cooling, power delivery, and signaling. This thesis aimed at addressing some of these challenges by proposing a liquid cooled 3D stack of ICs consisting of microchannels, TSVs and interstrata electro-fluidic I/Os. Different integration schemes for fluidic and electrical interconnects were introduced. We also reported fabrication and testing of microchannels and TSVs and demonstrated fluidic reliability of such integration for the first time. Finally we discussed the design and implementation of a 3D thermal test bed in order to simulate different stacking architectures cooled by microchannels at each stratum.

As reported, there are conflicting requirements between the cooling and electrical requirements of 3D ICs. A major limiting factor is the TSV aspect ratio which affects via etching, dielectric deposition and via filling. In order for microchannels to be able to meet the ITRS requirements of 0.2°C/W, an optimized heat sink would require a

Table 9: Projected TSV dimensions for global interconnects [4].

TSV Dimensions	**2009-2012**	**2013-2015**
Minimum TSV diameter *(μm)*	4-8	2-4
Minimum TSV pitch *(μm)*	8-16	4-8
Minimum TSV aspect ratio	5:1-10:1	10:1-20:1

Table 10: Comparison of pin-fin and microchannel heat sink [94].

	R_{tot} (K/W)	**ΔP** (kPa)	**Flow rate** (ml/min)	**Geometry** (μm)
Micro Pin-fin	0.19	28.23	100.05	D=150μm Pitch = 225μm H_{fin} = 200μm
Microchannel	0.19	25	120	W_w= W_c = 70μm H_{ch}=386μm

depth of about 300-400μm [54]. The TSV dimensions for global interconnect level as mentioned in the ITRS roadmap is listed in Table 9.

In order to integrate these TSVs with microchannels, TSV aspect ratios >50:1 is required to simultaneously meet the cooling, power delivery, and signaling needs. These aspect ratios have been extremely difficult to fabricate if not impossible using the current TSV fabrication technologies. A potential solution to this issue can be the use of alternate microchannel heat sink architecture. One example is using pin-fin heat sinks instead of plain microchannel heat sinks. A comparison of pin fin heat sink and microchannels is reported in [94]. As seen from the table, to obtain same thermal resistance value, the height of the pin-fin geometry is half that of the microchannel heat sink with modest pressure drop increase. We believe that this architecture has potential to be used in a liquid cooled 3D stack due to reduction in thickness of each stratum and hence lower aspect ratio requirements for TSVs.

With regards to TSV technology, electrical characteristics and electrical and mechanical reliability need to be explored further. These properties change with thermal

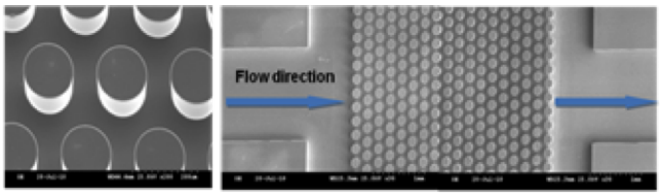


Figure 69: SEM image of staggered pin fin heat sink design [94]

performance of the stack and impact of cooling on TSV performance must be studied to fully exploit 3D system advantages.

A potential extension of the 3D test bench is the inclusion of electrical TSVs in the analysis to analyze the cooling effects of microchannels on electrical performance of the system. The thermal impact of hotspots and thermal crosstalk between different active layers must also be studied in the future.

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