THERMAL MANAGEMENT OF THREE-DIMENSIONAL INTEGRATED CIRCUITS USING INTER-LAYER LIQUID COOLING

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Dedicated to my wife, Mya,
my two sons, Calvin III and Jackson,
my parents, Calvin Sr. and Sarah,
and my sister and brother, Kimberly and Kyle
for their encouragement, love, and support.

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"What we are is God's gift to us. What we become is our gift to God." I would like to thank God for giving me the ability and endurance to complete three graduate degrees at Georgia Institute of Technology. I intend to use the education that I been blessed to receive as a tool to enable me to fulfill the purpose that God has for my life and to make a positive contribution to society.

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SUMMARY

Heat removal technologies are among the most critical needs for three-dimensional (3D) stacking of high-performance chips. This research reports a 3D integration platform that can support the heat removal requirements for 3D integrated circuits containing high-performance microprocessors.

This work shows the use of wafer-level batch fabrication to develop advanced electrical and fluidic three-dimensional interconnect networks in a 3D stack. Fabrication results are shown for the integration of microchannels and electrical through-silicon vias (TSVs). A compact physical model is developed to determine the design trade-offs for microchannel heat sink and electrical TSV integration. An experimental thermal test-bed for evaluating a 3D inter-layer liquid cooling platform is developed. Experimental thermal testing results for an air-cooled chip and a liquid-cooled chip are compared. Microchannel heat sink cooling shows a significant junction temperature and heat sink thermal resistance reduction compared to air-cooling. The on-chip integrated microchannel heat sink, which has a thermal resistance of 0.229 °C/W, enables cooling of >100W/cm^2 per tier, while maintaining an average junction temperature of less than 50°C. Cooling liquid is circulated through the 3D stack (two layers) at flow rates of up to 100 ml/min.

The ability to assemble chips with integrated electrical I/Os (density of ~1600/cm^2) and fluidic I/Os at each strata interface is demonstrated using various assembly and fluidic sealing techniques.

CHAPTER 1

INTRODUCTION AND BACKGROUND

The silicon integrated circuit (IC) has served as the foundation of high performance computing, been the main driver of the information revolution, revolutionized the electronics industry, and has had a monumental impact on our society. Following the invention of the transistor in 1947 [1.1] and the subsequent invention of the integrated circuit in 1958 (Figure 1.1a) [1.2-1.4], Gordon Moore predicted that the number of transistors that can be integrated onto a microchip would double approximately every two years (Figure 1.2) [1.5-1.6].

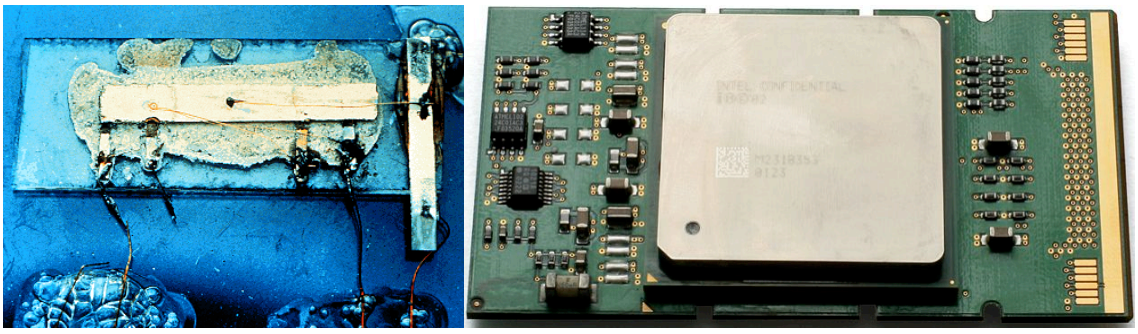


Figure 1.1: (a.) The first integrated circuit. (b.) Intel's Itanium Poulson microprocessor containing over 3.1 billion transistors.

From manufacturing a chip with hundreds of transistors in the 1960s to manufacturing chips with over a billion transistors in the 2000s (Figure 1.1b), the semiconductor industry has kept pace with Moore's Law for over 50 years.

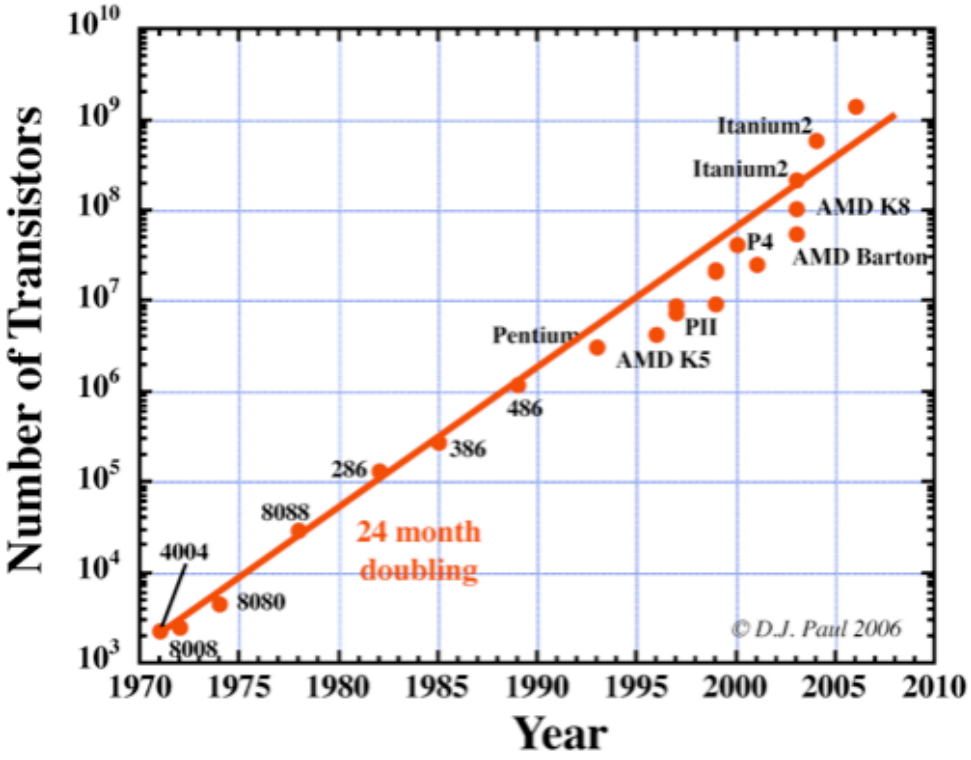


Figure 1.2: Moore's Law Data [1.6].

1.1. Thermal Management Challenges in High-performance ICs

1.1.1. Increasing Power Density

While Moore's Law and device scaling has provided higher functionality and performance, increased device density has also historically resulted in increased power dissipation and increased operating temperature. Chip operating temperature is a major determinate of semiconductor device reliability, and data shows that more than 50% of integrated circuit failures are related to thermal issues [1.7, 1.8]. Figure 1.3 shows historical data of how increasing power densities have accompanied successive microprocessor technology generations [1.9]. With respect to implications for on-chip interconnects, as temperature increases, the resistivity of interconnects increases, causing

decreased bandwidth and higher resistive losses as well as lower reliability due to electromigration.

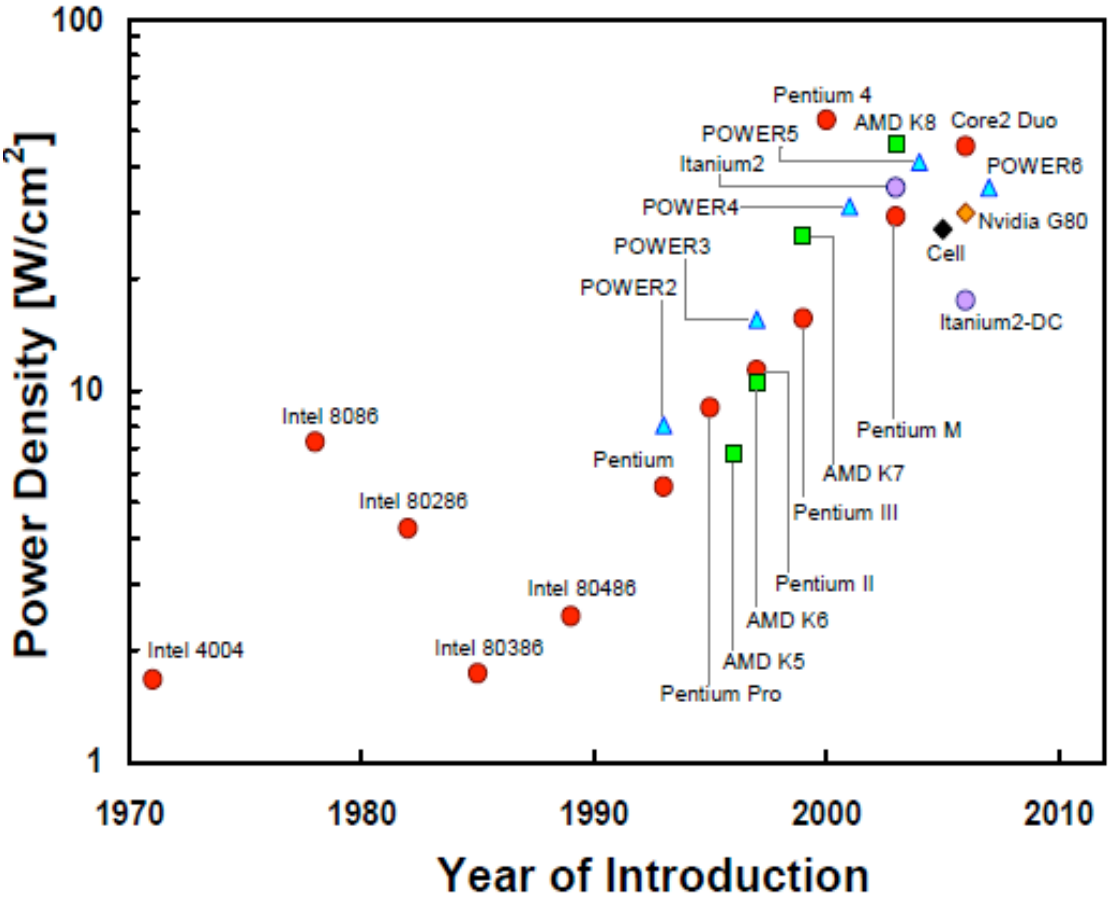


Figure 1.3: Historical power density of various commercial microprocessors [1.9].

1.1.2. Static Power

Elevated temperatures can cause circuit timing related issues, on-chip temperature gradients, and increased leakage power consumption. Figure 1.4 depicts how leakage power substantially increases as chip temperature increases. At elevated temperatures, leakage power can account for over 50% of the power dissipation in an integrated circuit [1.7]. Thus, there is clear motivation to operate at lower temperature for highly scaled CMOS circuits.

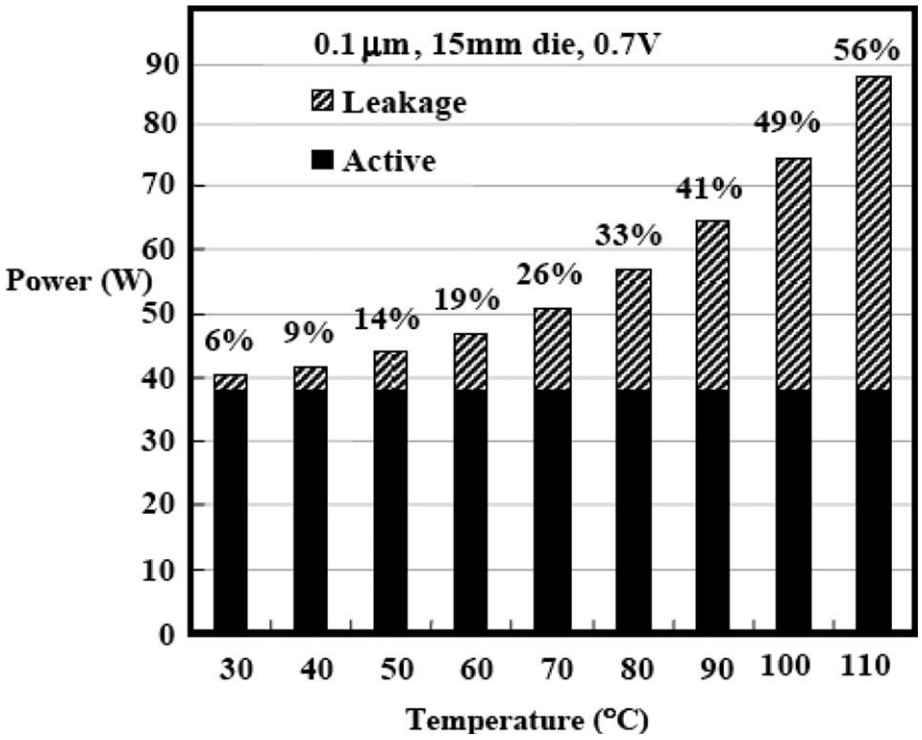


Figure 1.4: Chip power consumption as a function of temperature; leakage power dependence on chip temperature [1.7].

1.1.3. Increasing Heat Sink Size

Although transistors have continued to scale smaller, thermal interconnects (interconnects responsible for rejecting heat to the ambient) have scaled inversely with CMOS technology. In order to achieve smaller junction-to-ambient thermal resistance and to maintain constant junction temperature with increasing power, the mass and volume of conventional air-cooling heat sinks have progressively increased with each new microprocessor generation [1.10]. As thermal interconnects have scaled larger, thermal interconnects impose limits on system size, chip packing efficiency, and interconnect length between chips. Figure 1.5 outlines how the heat sink volume of various Intel microprocessors has increased over time. The figure also illustrates how, in order to maintain junction temperature with increasing processor power dissipation, heat

sink size and fan power have increased [1.10]. Figure 1.6 illustrates an example of the size difference in heat sinks for two Intel Pentium processors from different technology generations.

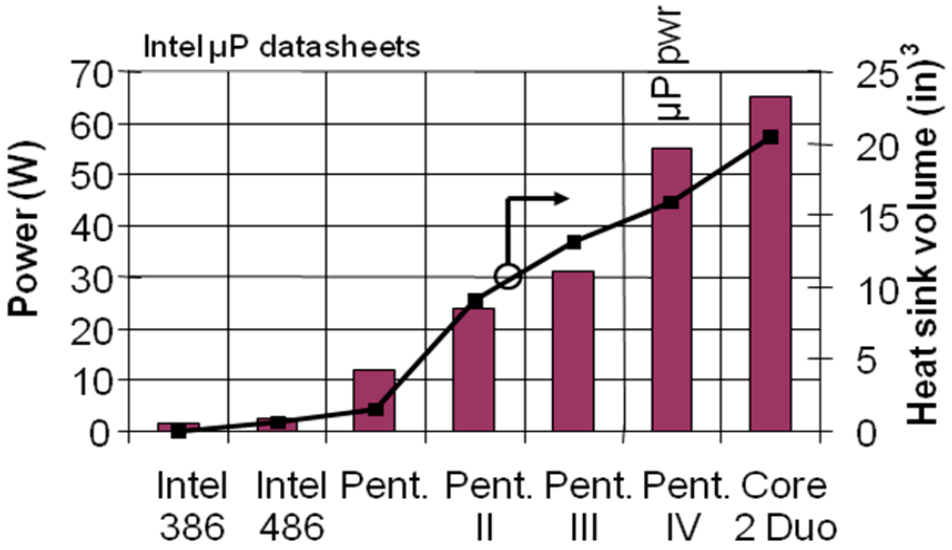


Figure 1.5: Graph of increasing heat sink volume and heat sink fan power for various Intel microprocessors [1.10].

Figure 1.6: Pentium Overdrive "chip and heat sink" from 1993 (bottom left); standard Pentium 4 "heat sink only" from 2005 (top right).

1.1.4. Heat Sink Thermal Resistance

Figure 1.7 shows a schematic of a conventional air-cooling heat sink for a flip chip package. According to the International Technology Roadmap for Semiconductors (ITRS), the projected junction-to-ambient (ja) thermal resistance of an adequate heat sink for cooling high-performance microprocessors at the 14nm technology node should be approximately 0.2˚C/W [1.11]. The overall thermal resistance (ºC/W), R_{th} , of the heat sink and silicon chip shown in Figure 1.7 can be estimated as follows:

$$R_{th-ja} \approx R_{Si} + R_{TIM} + R_{sp} + R_{heat\,sink}$$

where R_{Si}, R_{TIM}, R_{sp}, and $R_{heatsink}$ are the thermal resistances of the silicon chip, the thermal interface materials (TIMs), the heat spreader, and the heat sink [1.12].

Yet, even when using the best available materials for the various thermal interconnects between the silicon die and the ambient (the heat sink, heat spreader, and thermal interface materials (TIM)), the sum of the thermal resistances typically associated with these thermal interconnects has a lowest attainable thermal resistance of approximately 0.5˚C/W [1.13].

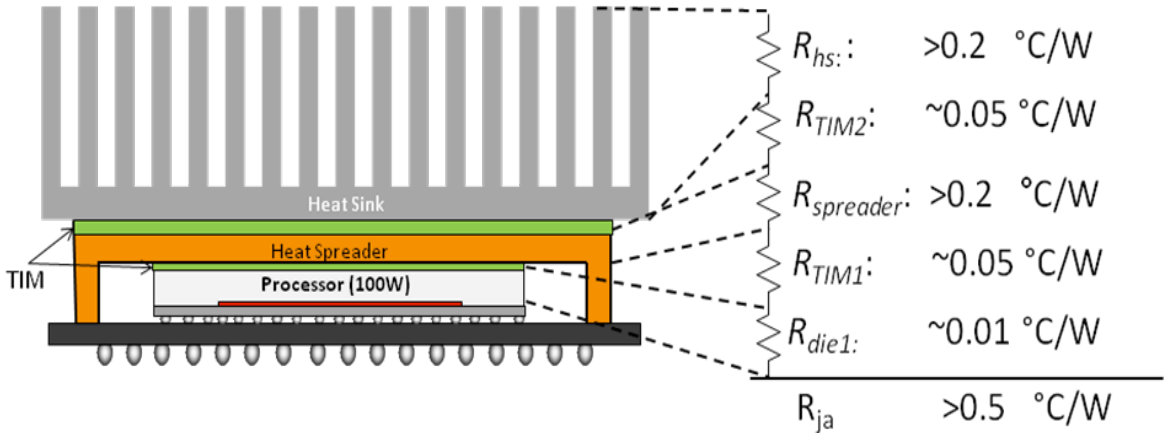


Figure 1.7: Schematic of thermal resistances associated with a conventional air-cooling heat sink.

1.1.5. Microprocessor Clock Frequency

Approximately during the past decade, state of the art microprocessors approached the heat flux air cooling limit of ~100 W/cm^2[1.14]. Because of this thermal management limit (as well as other constraints), historic clock frequency scaling slowed and has been relatively flat since 2004, as shown in Figure 1.8 [1.14].

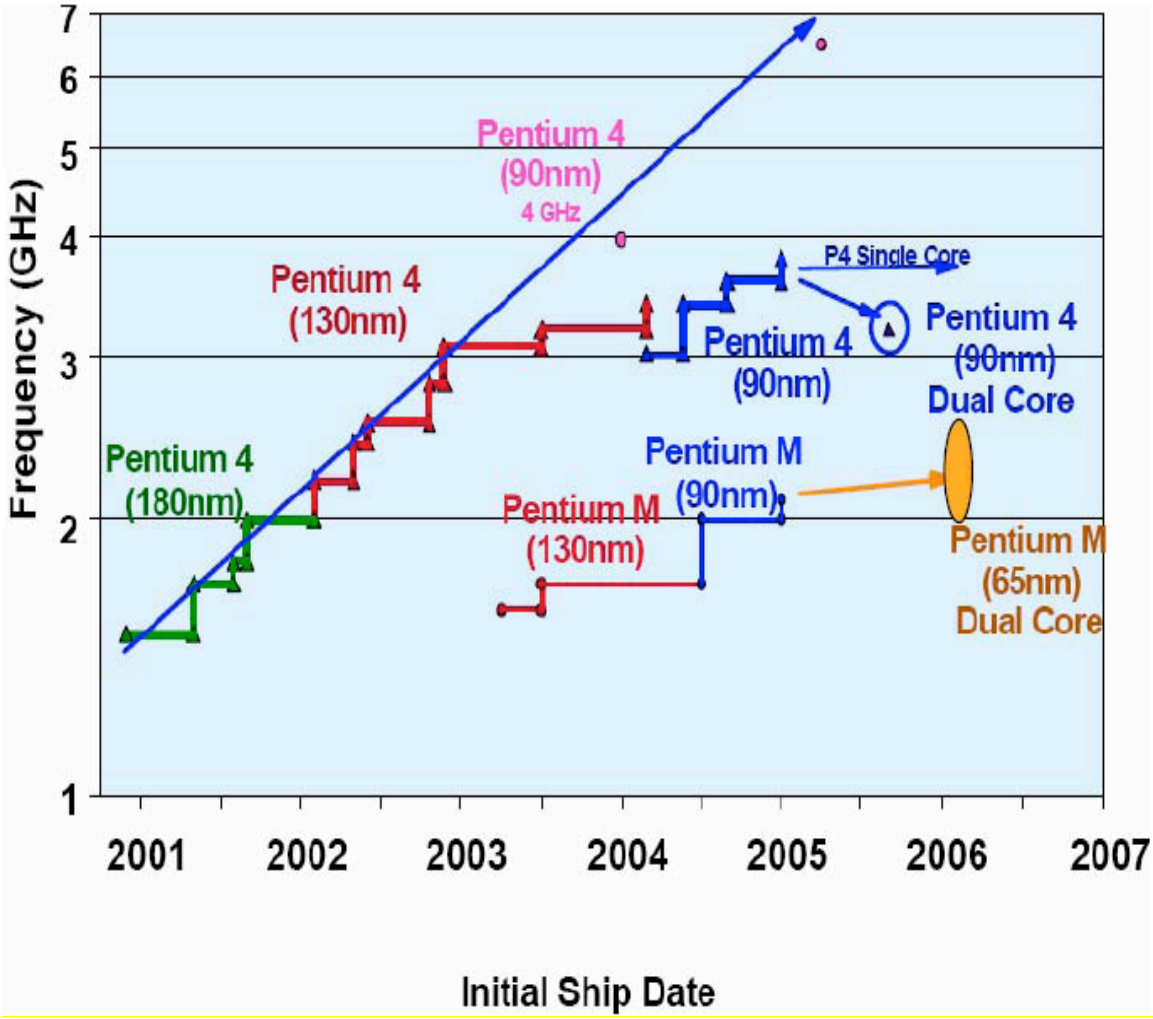


Figure 1.8: Frequency vs. Year for various Intel microprocessors [1.14].

To address power dissipation challenges, microprocessor design has shifted from single-core to multi-core processors [1.15]. Furthermore, having multiple strategically

placed cores on a single chip helps to mitigate thermal issues [1.16], as heat can be more evenly spread across the chip surface. Moreover, processor performance has continued to improve at a faster rate than memory access time, limiting overall system performance improvement. As the number of cores increases, issues of memory access time, bandwidth density, and off-chip interconnect latency become more challenging [1.15, 1.17].

1.2. Three-dimensional Integrated Circuits

The continuation of exponential improvement in productivity and performance by transistor scaling is becoming challenging. According to researchers, physical limits of atomic structures, power density limits, and thermal management requirements could cause Moore's Law and the accustomed rates of device scaling to substantially decrease and eventually come to an end [1.18-1.25].

3D integration is a promising technology that will extend Moore's Law in the "z-direction" by vertically integrating multiple layers of active electronic circuits into a single circuit. 3D integrated circuits offer many advantages including increased device density, shorter interconnect distances, system performance enhancements, decreased system form factor, and integration of heterogeneous technologies in the same chip stack.

Advances in through-silicon via (TSV) technology, wafer thinning, fine-pitch interconnections, and bonding have enabled stacking of multiple chips to achieve system performance enhancements [1.26-1.32]. Figure 1.9 shows examples of 3D integrated circuits implemented using electrical TSVs and wire-bonding.

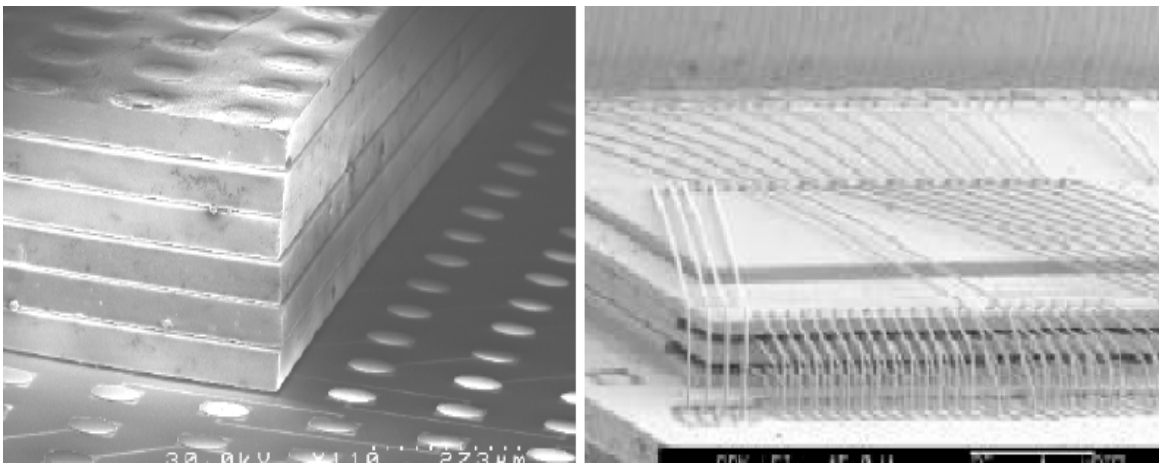


Figure 1.9: Examples of 3D integration using electrical TSVs (left) [1.27] and wire bonding (right) [1.26].

Furthermore, because 3D technology can enable the integration of memory layers onto the processor chip, slower off-chip electrical interconnects can be eliminated and replaced with high-bandwidth, low-latency vertical interconnections [1.17]. Consequently, processor-memory interconnections which once required tens of millimeters of wire can be connected vertically using electrical TSVs, which are only tens of microns in vertical length [1.17]. As a result, chip-to-chip interconnection performance and bandwidth are significantly improved.

1.3. Thermal Challenges in Three-dimensional Integrated Circuits

Although there are many advantages to 3D integration, one of the most significant challenges is heat removal. To date, only low-power commercial products have been able to exploit the advantages of the improved performance and increased device packing density realized by the three-dimensional (3D) stacking of chips. Just as increased power density causes thermal management challenges in 2D integrated circuits, heat removal is

even more challenging in 3D integrated circuits because 3D technology enables much denser device integration.

1.3.1. Challenges of Conventional Air-cooling Heat Sinks

While stacking low-power memory chips can be thermally managed by conventional cooling methods [1.33], 3D chip stacks which contain multiple high-performance processors have a power density which exceeds the heat removal capability of conventional cooling techniques [1.34]. Because high-performance chips are projected to dissipate more than 100W/cm^2 (Table 1.1, Figure 1.10) [1.11], when such chips are stacked, the challenges in power delivery and cooling become greatly exacerbated. For example, for a two-chip stack of high-performance processers that dissipate 100W/cm^2, the power dissipation doubles from that of a single high-performance chip and the heat flux increases to 200W/cm^2 (Figure 1.11), which exceeds the conventional air-cooling heat sink capability [1.14].

With the addition of each device layer, the total power density and maximum junction temperature in the 3D stack increase. According to the ITRS, the number of high-performance chips (for high-performance applications) in a 3D chip stack will increase to 7 chips per stack and 10 chips per package by the year 2022 [1.11], as shown in Table 1.2.

Table 1.1: ITRS projections for high-performance chip junction temperature and power dissipation [1.11].

ITRS Data (High Performance Chips)	2011	2013	2015	2017	2019	2021
Single Chip Junction Temperature (^{o}C)	**85**	**80**	**80**	**75**	**70**	**70**
Dissipated Power (W)	**161**	**149**	**143**	**130**	**130**	**130**

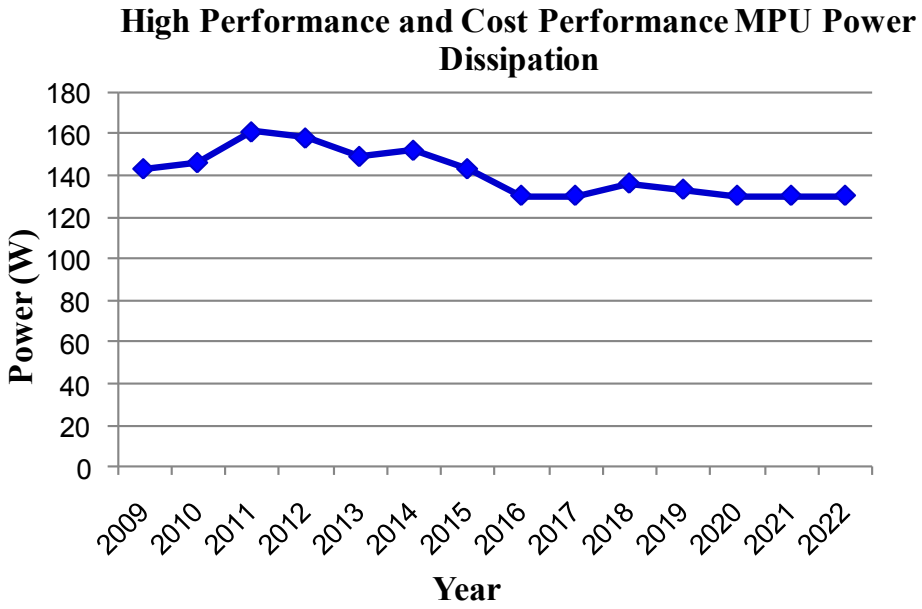


Figure 1.10: ITRS projected power dissipation for high performance and cost performance microprocessors [1.11].

Table 1.2: ITRS projections for the maximum number of high-performance dice in a 3D chip stack and in a 3D package [1.11].

ITRS Data (High Performance Chips)	2011	2012	2013	2014	2015	2016
Max Number of Stacked Die (TSV)	-	-	-	-	2	2
Number of Dice in Package	7	7	8	8	8	9
	2017	2018	2019	2020	2021	2022
Max Number of Stacked Die (TSV)	3	4	5	6	7	7
Number of Dice in Package	9	9	10	10	10	10

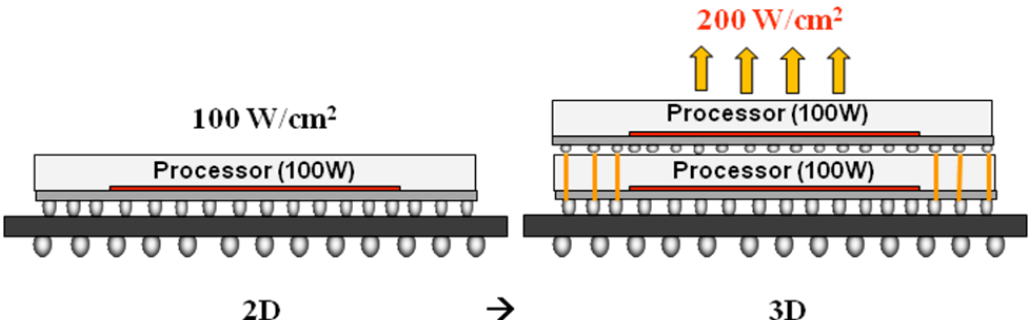


Figure 1.11: A schematic illustrating how heat flux increases from 2D to 3D circuits.

Furthermore, when using a conventional air-cooling approach, heat flux from chips in the 3D stack has to overcome a larger thermal resistance by traveling through a longer conductive path in order to be dissipated through the heat sink [1.35]. Moreover, because the heat generated in one stratum must travel through several other strata before dissipating into the heat sink, the temperature rise in one stratum influences temperature rise in other strata in the 3D stack [1.36].

If conventional air cooling techniques will not meet the power density, heat flux, and thermal resistance requirements for a single high-performance chip, as shown in Figure 1.7, conventional cooling will not be appropriate for a 3D stack of chips which has multiple high-performance processors (Figure 1.12) [1.34].

To further illustrate disadvantages of cooling a high-performance 3D chip stack with air-cooling, Figure 1.13 shows a 3D processor-memory stack where the processor chip is on top and the memory chip is on bottom. Stacking the processor chip, which dissipates more power, on the top layer is the best case thermally, as the processor is directly under the heat sink. However, using this approach makes it challenging to deliver the power required by a high-performance processor. Since the processor chip requires more I/O (input/output) connections than the memory chip, more electrical through-silicon vias (TSVs) will need to be routed through the memory chip consuming valuable memory chip area and making memory design and layout more difficult and less efficient.

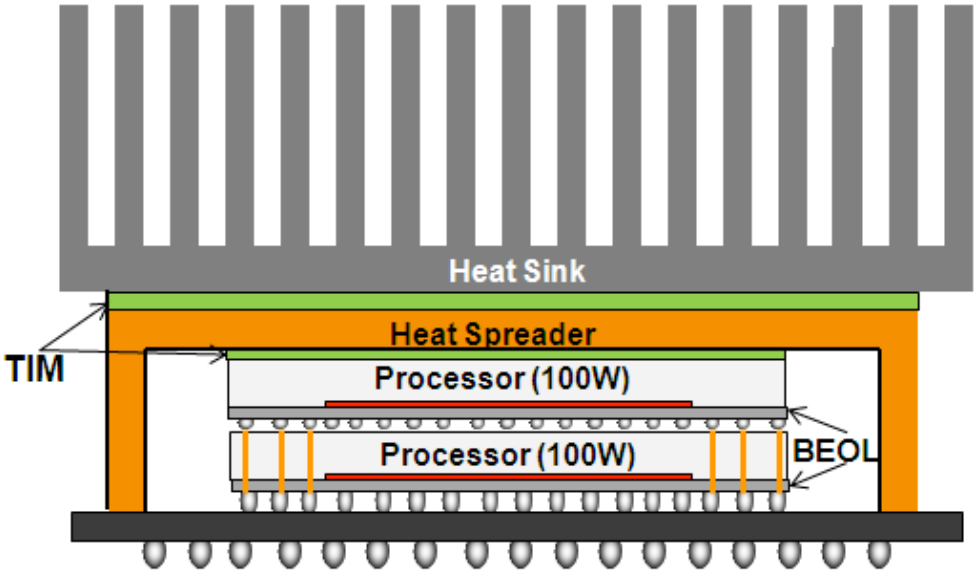


Figure 1.12: Schematic of thermal resistances associated with a conventional air-cooling heat sink.

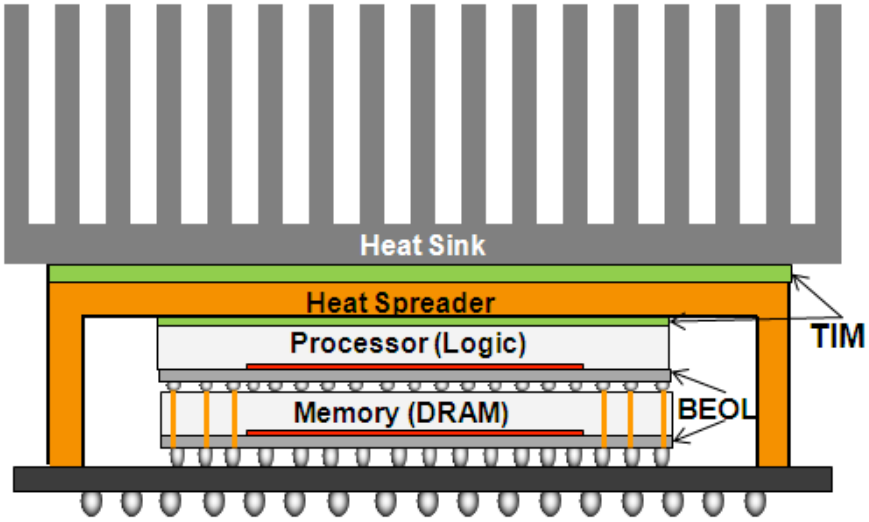


Figure 1.13: 3D thermal management using conventional air cooling.

In an alternative approach, the processor can be placed on the bottom of the 3D stack and the memory chip(s) on top. Because the memory chip has fewer I/Os, fewer TSVs are needed than in the previous case. Yet, placing the processor on the bottom of the stack is thermally disadvantageous, as the processor dissipates much more power than

the memory chip(s). With the addition of each memory chip, the thermal resistance is increased between the bottom device layer and the heat sink, limiting the number of chips that can be stacked.

1.3.2. Advanced Cooling of High-performance 3D Integrated Circuits

Thermal issues are increasingly becoming a device and system design concern, as researchers suggest that thermal management of high performance microprocessors is pushing the limits of air cooling, especially for applications such as servers used in data centers which contain high-performance processors that have high power dissipation and high density packaging [1.10, 1.14, 1.37]. Because the heat generated from multiple layers increases the potential of electrical failure [1.17, 1.38] and because the maximum allowable average power density is constrained by the limitation of heat removal capability of the heat sink [1.8], the increased device density as a result of 3D chip stacking requires innovative thermal management strategies. Thus, a significant amount of research is being focused on creating advanced cooling technologies.

Liquid cooling using microchannels has been identified as a promising cooling solution to meet the thermal management requirements of future high-performance microprocessors due to the superior thermal properties of liquid compared to air. Figure 1.14 shows a comparison of heat transfer coefficients of various thermal buses, which shows that the heat transfer coefficient of removing heat through microchannel cooling is a higher capacity heat removal solution compared to forced air cooling [1.12].

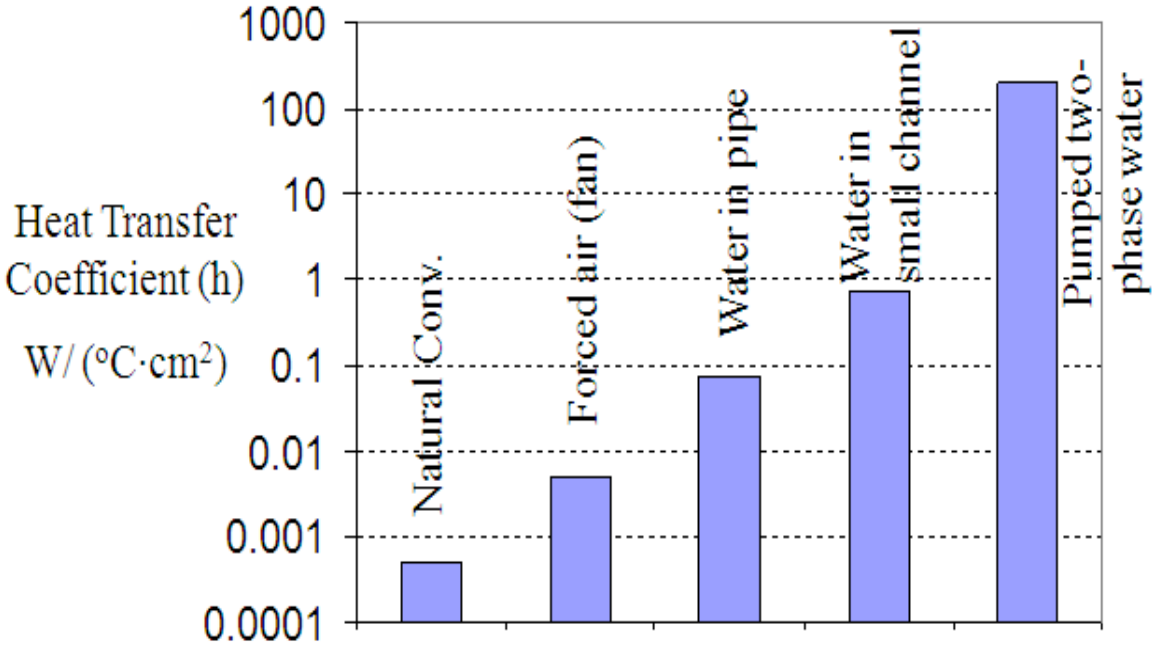


Figure 1.14: Heat transfer coefficient of various thermal buses [1.12].

Tuckerman and Pease were the first to demonstrate an on-chip, integrated microchannel heat sink which showed the ability to remove a heat flux of 790 W/cm^2 with a maximum chip temperature rise of 71°C [1.39]. Although a number of researchers have explored the advantages of using liquid cooling to solve thermal management challenges [1.12, 1.40-1.43], there are many unknowns for its implementation for 3D integrated systems. Some of the unknowns for liquid cooling using microchannels include fabrication of an on-chip microfluidic heat sink and integration of electrical through-silicon vias (TSVs), where to place fluidic I/O interconnects for 3D chips, how to supply fluid to and extract fluid from microchannels embedded in a 3D stack, how to seal fluidic I/O interconnections at the interface of each strata, and how to assemble 3D ICs with microfluidic functionality.

1.4. Summary of Research Objectives

The objective of this research is to investigate and report the configuration, fabrication, assembly, and experimental results of a 3D integration platform that can support the heat removal requirements for high-performance chips. A novel microchannel heat sink liquid cooling scheme for 3D integrated circuits (ICs) and the fabrication processes necessary for integrating microchannels and electrical TSVs will be outlined. The on-chip integrated microchannel heat sinks, which have a thermal resistance of 0.229 °C/W, enable cooling of >100W/cm^2 per tier at an average junction temperature of less than 50°C. Compact physical modeling is used to determine the design trade-offs for microchannel heat sink and electrical TSV integration.

Fluidic input/output (I/O) interconnect technologies that enable fluidic connectivity of the 3D microfluidic network are demonstrated. Three distinct fluidic I/O technologies and assembly methods used for 3D chip stacking and fluidic sealing are demonstrated. Simultaneous fabrication of electrical and fluidic I/Os is demonstrated, and an electrical I/O density of ~1600/cm^2 is achieved.

An experimental thermal measurement test-bed for evaluating a 3D inter-layer liquid cooling platform is developed. The experimental thermal measurements demonstrate the cooling of chips which dissipate a heat flux of 100W/cm^2; electrical and fluidic interconnection between layers is also demonstrated. Cooling liquid is circulated through the 3D stack at flow rates of up to 100 ml/min.

1.5. Dissertation Outline

The organization of the research in this dissertation is described as follows:

- Chapter 2 describes the wafer-level batch fabrication and micromachining technologies used to fabricate the necessary electrical and microfluidic interconnects for the proposed 3D inter-layer cooling platform. Each silicon die of the 3D stack contains the following features: 1) a monolithically integrated microchannel heat sink, 2) through-silicon fluidic vias (TSFV) used for fluidic routing in the 3D stack, and 3) solder bumps (electrical I/Os) and microscale controlled collapse chip connection (C4) pipes (fluidic I/Os) on the side of the chip opposite to the microchannel heat sink.

  Additionally, compact physical modeling is used to analyze the impact of microchannel geometry and fluid flow rates on thermal resistance and pressure drop of the 3D systems. Additionally, compact physical modeling is also used to explore the electrical TSV performance and microchannel heat sink cooling trade-offs when integrating microchannel heat sinks and electrical TSVs in a 3D chip stack.
- Chapter 3 describes fabrication and process integration techniques for three distinct fluidic I/O technologies including a C4 pipe fluidic I/O, an air-gap C4 fluidic I/O, and a polymer pipe fluidic I/O interconnect technology. Fluidic testing is performed to verify the reliability of the fluidic I/O interconnect structures. The advantages and disadvantages of the three fluidic I/O technologies are discussed.
- Chapter 4 discusses the flip-chip die-to-substrate and die-to-die bonding processes that enable the integration of electrical and fluidic components in a 3D chip stack.

- Chapter 5 outlines the thermal and fluidic analysis and testing results of the on-chip microhannel heat sink. Experimental results for an air-cooled chip and a liquid-cooled chip are compared. Preliminary fabrication results for an alternative pin-fin heat sink technology are demonstrated, and the advantages of the pin-fin heat sink compared to the microchannel heat sink technology are discussed.
- Chapter 6 presents the conclusion and opportunities for future work.

CHAPTER 2

DEVELOPMENT OF AN INTER-LAYER LIQUID COOLING PLATFORM FOR THERMAL MANAGEMENT OF 3D INTEGRATED CIRCUITS

2.1. Development of an Inter-layer Liquid Cooling Platform for Thermal Management of 3D Integrated Circuits

Cooling multiple stacked high-power chips presents significant thermal challenges. Thus, revolutionary advanced cooling technologies are necessary to provide adequate cooling and enable circuit designers to have full flexibility when designing processor-memory and processor-processor 3D chip stacks. Using integrated microchannel heat sinks to cool high-performance 3D chip stacks is discussed in [2.1], where experimental results show that single chips cooled by microchannel heat sinks exhibit a junction-to-ambient thermal resistance of 0.24^{o}C/W. Thus, using inter-layer microchannel heat sinks to cool chips at any tier in the 3D stack allows higher chip stacks, enabling more functionality in a given system foot print.

Figure 2.1a outlines a 3D stack configuration where the processor is on the bottom of the 3D stack. Although this approach would be thermally challenging using air cooling, the integrated microchannel heat sink on the back side of the processor enables sufficient cooling of the processor layer, while enabling most efficient power delivery to the processor. When stacking multiple high performance processors (Figure 2.1b), each die in the stack can be thermally isolated. One of the most significant aspects of this

technology is that multiple processor and memory chips can be stacked without having to place the high power chips on the top of the stack, which would be the best thermal solution when using conventional air cooling but not the most effective configuration for power delivery to the processor chip [2.2].

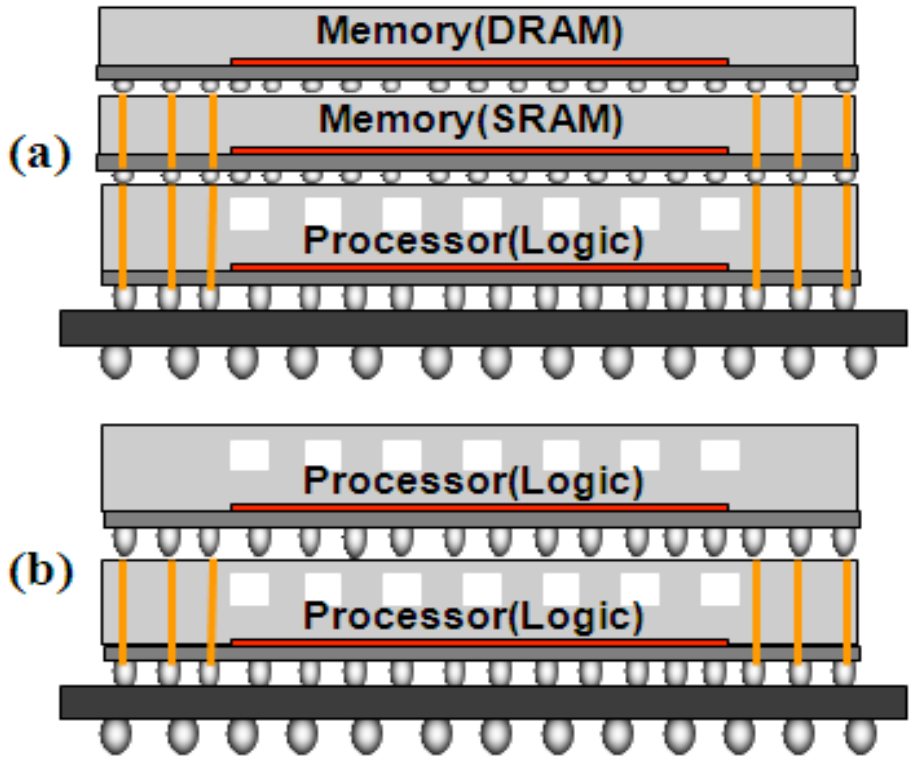


Figure 2.1: 3D IC (a) processor-memory and (b) processor-processor thermal management approaches using a microchannel heat sink inter-layer liquid cooling.

The microchannel liquid cooling scheme shown in Figure 2.2 can be used for cooling 3D chip stacks that contain high-performance processors. The cooling scheme reduces the overall thermal resistance of the cooling system, removes thermal resistances associated with TIMs, reduces chip cooling hardware size from inches to microns, and enables cooling of >100W/cm^2 of each high-power density chip [2.3-2.4].

2.2. 3D Inter-layer Liquid Cooling Platform Process Development and Integration of Microchannel Heat Sink, Electrical TSVs, Fluidic TSVs, Electrical I/Os, and Fluidic I/Os

Figure 2.3 outlines the processing steps necessary for fabrication of the features that enable the electrical and fluidic networks shown in Figure 2.2. Following back-end-of-the-line (BEOL) processing, microchannels and fluidic TSVs are formed into the back side of the wafer by inductively coupled plasma (ICP) etching (Figure 2.3a, 2.3b). The microchannels can be capped using the sacrificial polymer process described in [2.1] or by the silicon-to-silicon bonding process described in [2.5] (Figure 2.3c). Next, TSVs are etched in the wafer using ICP etching, and copper is electroplated in the TSVs as shown in [2.6] (Figure 2.3d, 2.3e). Figure 2.4 shows 200μm deep, 100μm wide polymer-capped microchannels with integrated 50μm diameter copper electrical TSVs. Figure 2.5 shows 170μm tall, 100μm wide silicon-capped microchannels with integrated 50μm diameter copper electrical TSVs. This work is the first 3D cooling research to demonstrate the integration of microchannel heat sinks and electrical TSVs (Figures 2.4-2.5), as shown in [2.3, 2.7].

Subsequently, polymer sockets, which enable assembly of the electrical and fluidic I/Os are fabricated by spinning on and patterning a photo-definable polymer as described in [2.3] (Figure 2.3f). Electrical I/O interconnects (solder bumps) are fabricated by electroplating, and fluidic I/O interconnects (polymer or solder pipes) are fabricated patterning a photo-definable polymer [2.8] or electroplating solder [2.9]. Figure 2.6 shows an SEM image of integrated electrical and fluidic I/O interconnects

[2.9]. Fabrication processes for electrical and fluidic I/Os are described in more detail in Chapter 3.

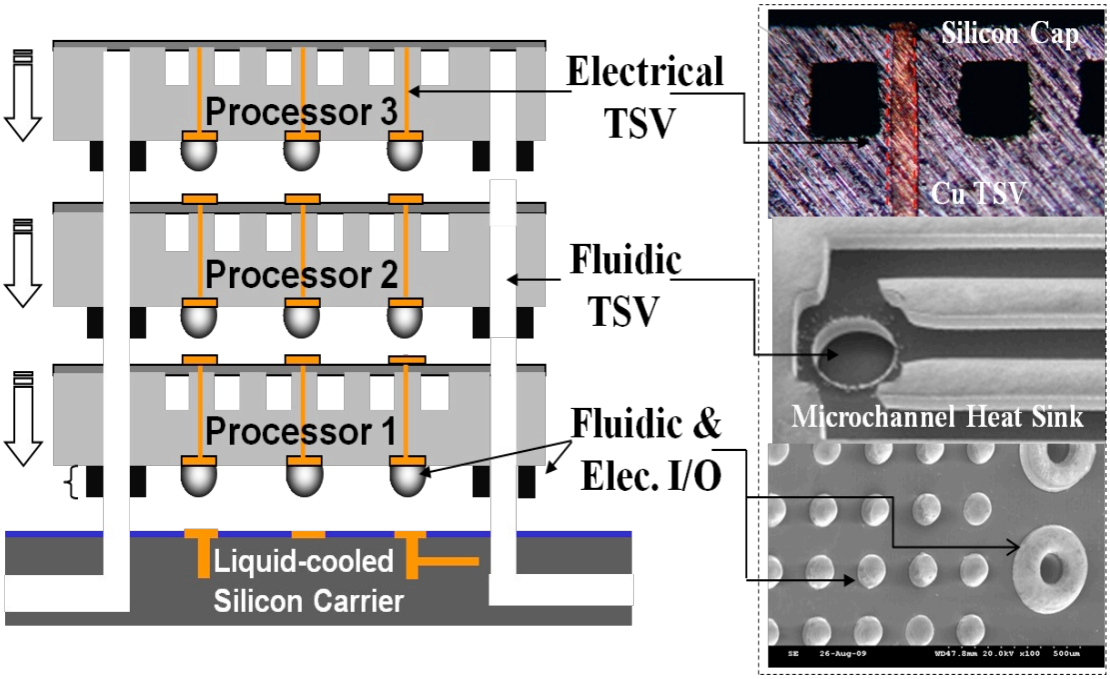


Figure 2.2: Schematic of chip-scale microchannel heat sink cooling scheme for 3D integrated circuits.

Microscale fluidic interconnection between strata is enabled by through-wafer fluidic vias and fluidic I/O interconnects. Power delivery and signaling can be supported by the electrical interconnects (solder bumps and copper TSVs), and heat removal for each stratum can be supported by the fluidic I/Os and microchannel heat sinks. Chips can be aligned, stacked, and assembled; assembly processes are discussed in the Chapter 4.

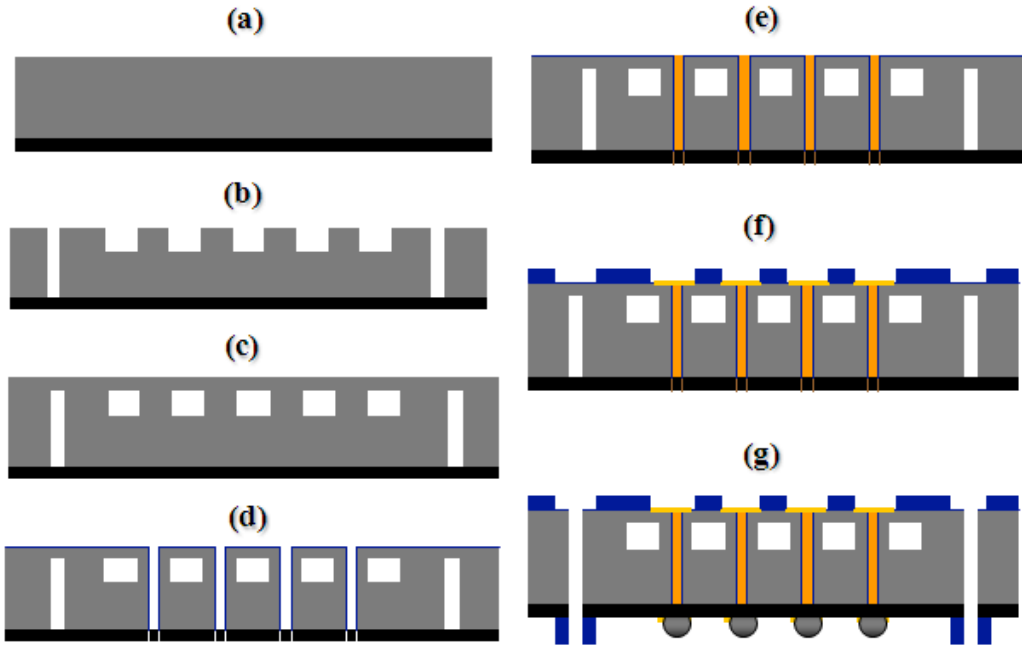


Figure 2.3: Schematic of wafer-level integration of microchannels, fluidic through-silicon vias, silicon dioxide insulated electrical through-silicon vias, and electrical and fluidic I/Os to enable liquid cooling of high-performance 3D integrated systems.

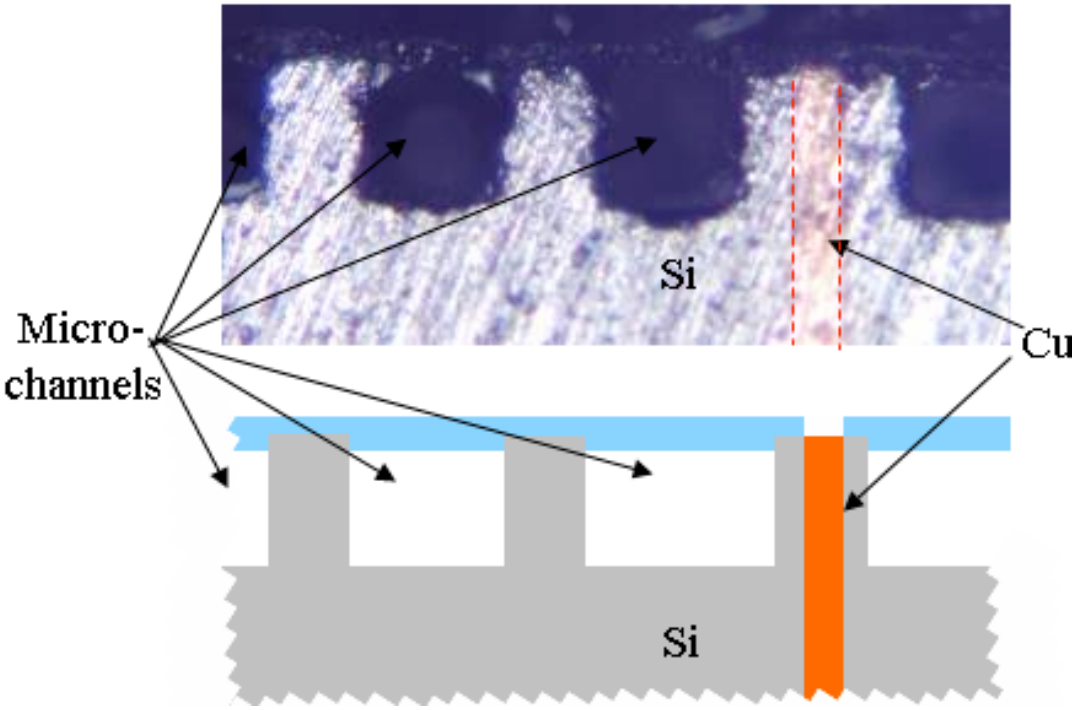


Figure 2.4: Cross-sectional optical image and schematic of a polymer-capped microchannel heat sink and integrated electrical through-silicon vias [2.3, 2.7].

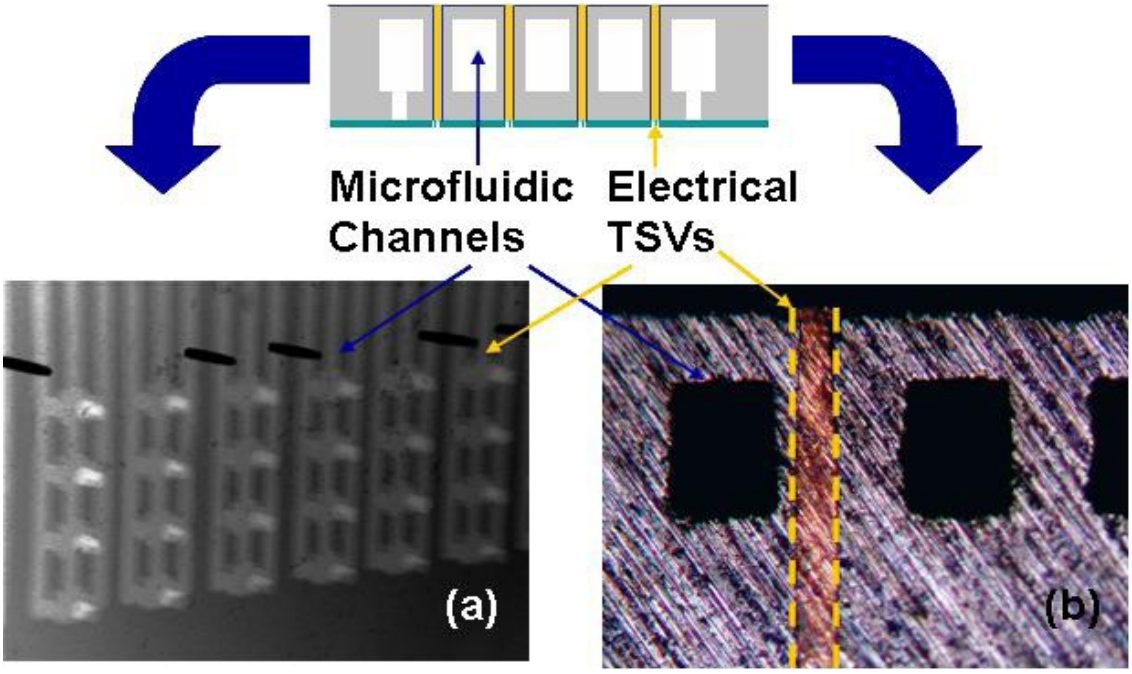


Figure 2.5: (a) X-ray image and (b) cross-sectional optical image of a silicon-capped microchannel heat sink and integrated electrical through-silicon vias [2.5].

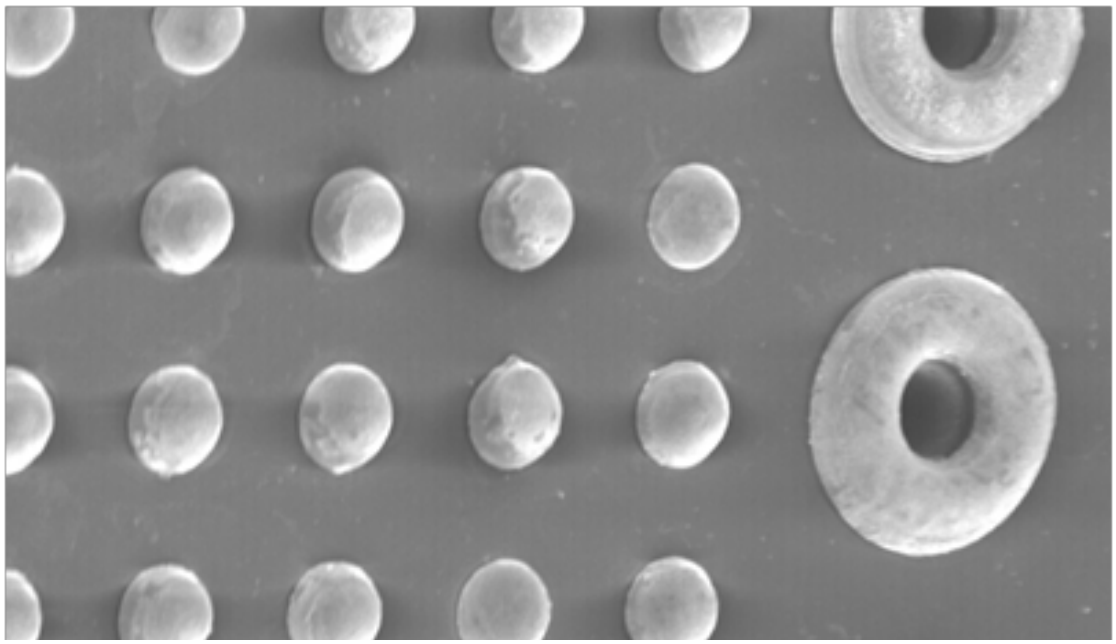


Figure 2.6: SEM image of integrated electrical and fluidic I/O interconnects [2.9].

A thin-film platinum resistor is fabricated on the bottom side of each chip of the 3D stack (Figure 2.7). When applying a current source to the resistors, the resistors serve as a heating source to simulate heat dissipated by transistors and interconnects on a microprocessor. The change in resistance of the resistor is measured and used to calculate the change in chip temperature.

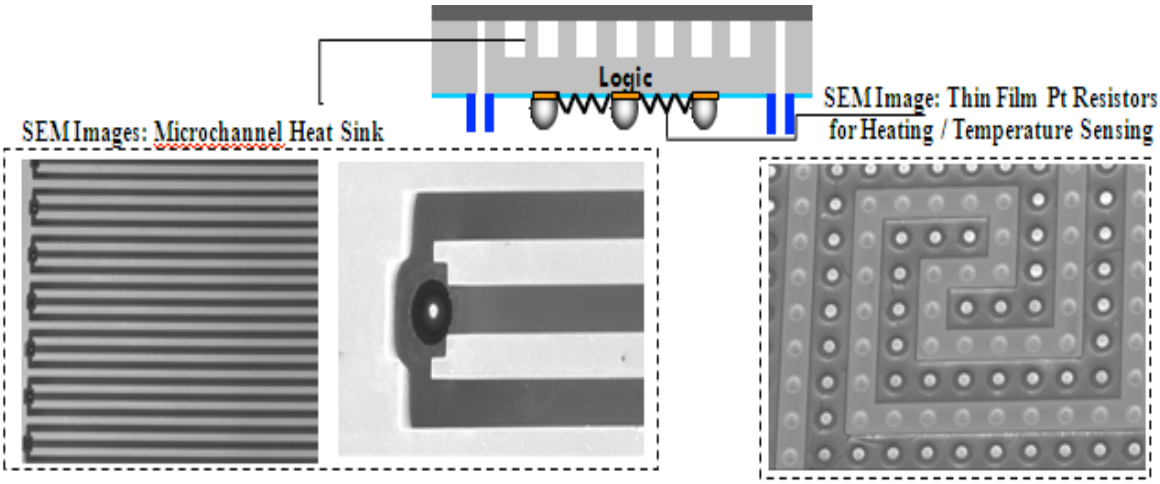


Figure 2.7: SEM images of (left) microchannel heat sink and (right) integrated thin-film platinum resistors and electrical I/Os.

2.3. Methods for Microchannel Heat Sink Capping

As shown in Figure 2.3, trenches can be etched into the back side of a silicon chip by inductively coupled plasma (ICP) etching (Figure 2.3a, 2.3b), thereby creating microchannels on the back side of the chip that can be used as an on-chip microchannel heat sink. Figure 2.8 shows SEM images of microchannels that have been etched onto the back side of a silicon chip. After trench etching, the microchannels must be capped to enable liquid to be circulated on the back side of the chip. Although various methods for microchannel heat sink fabrication have been explored, the three methods of

microchannel capping investigated during this research are using a polymer overcoat [2.1], using silicon-to-silicon bonding to create a silicon cap [2.5, 2.9], and using adhesive bonding [2.5]. The silicon-to-silicon bonding and polymer overcoat methods will be discussed in the following sections.

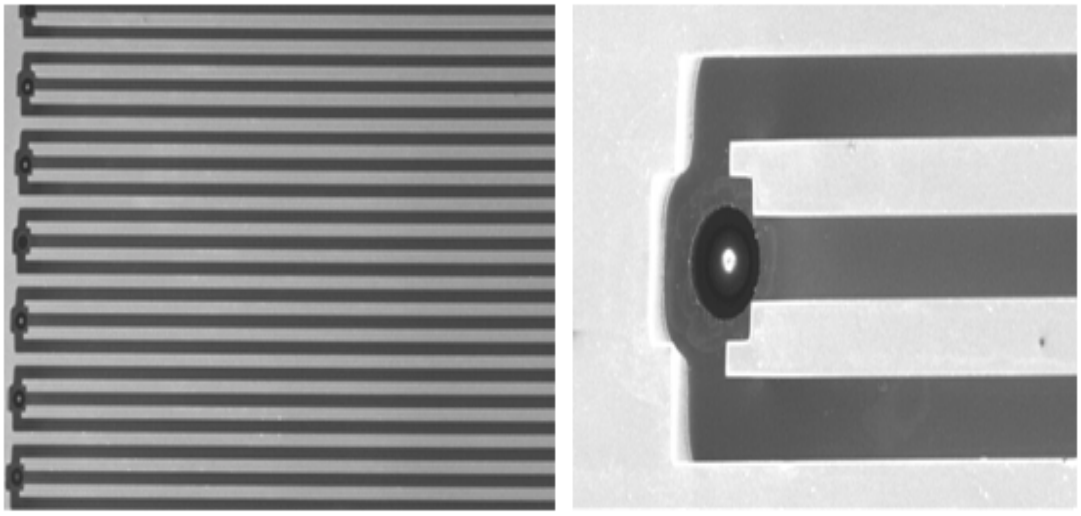


Figure 2.8: Top view of microchannel heat sink and fluidic TSVs after silicon etching.

2.3.1. Silicon-to-Silicon Bonding

Microchannel capping can be achieved by direct, silicon-to-silicon (Si-Si) wafer bonding. Semiconductor wafer bonding can be classified by a process where two polished wafers can be adhered or bonded together at room temperature under atmospheric conditions without the use of an adhesive layer or other outside force. Bonding is established by molecular bonds between molecules on the surfaces of the two substrates. The adhesion forces responsible for enabling this process include Van der Waals forces, electrostatic coulomb forces, capillary forces, or hydrogen bridge bonds [2.10].

Initial bonding is performed at room temperature, where a weak adhesion is established between the substrates and subsequently followed by a high temperature annealing step where the strength of the weak bonds is increased by a factor of 10 and converted to strong permanent bonds by transforming the hydrogen bridge bonds across the interface via the reactions (shown in Figure 2.9) [2.11].

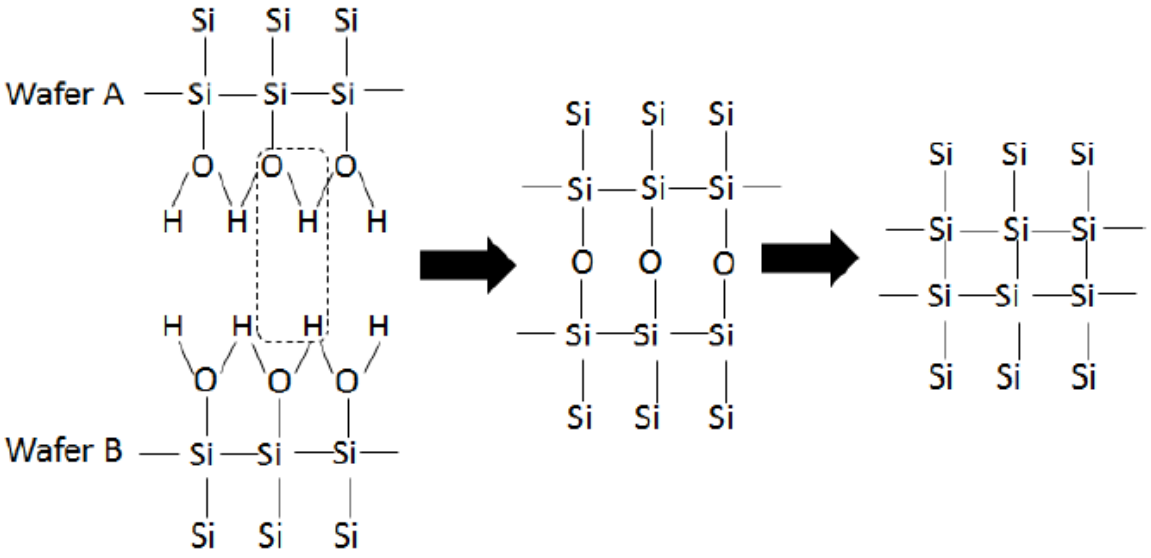


Figure 2.9: Chemical reactions during the hydrophilic bonding process.

Because direct bonding can require annealing temperatures >1000 ^{o}C to establish a permanent bond, for low-temperature processes, establishing appropriate surface conditions on the two substrates is necessary to achieve sufficient interface bonding forces during low-temperature annealing.

Activation of the two bonding surfaces by increasing the density of the silanol groups on the surface via plasma treatment helps to increase bonding strength, allowing strong hydrophilic bonding at annealing temperatures <400 ^{o}C [2.12-2.13].

For hydrophilic surfaces, the interface energy is equivalent to the number of silanol groups (Si-OH) at the initial surface. Therefore, activation of the surfaces by increasing the density of silanol groups would also increase the interface energy. This activation can be achieved using plasma treatment. It has been reported that strong hydrophilic bonding with Si can be achieved at a low annealing temperature <400^{o}C by exposing wafers to a low pressure plasma prior to the bonding [2.12-2.13].

To cap the microchannels, a low temperature plasma-activated Si-Si direct bonding approach was implemented for capping microchannels. Figure 2.10 outlines the fabrication processing steps necessary to achieve wafer-to-wafer bonding. First, the surface of a wafer containing microfluidic channels and a 400μm double-side polished silicon capping wafer are dipped in RCA-1 solution (H_2O, NH_4OH, H_2O_2, mixed with a ratio of 5:1:1 respectively). RCA-1 solution removes organic impurities that may be present on the surface of the wafers and changes the surface on the silicon wafers to hydrophilic surfaces.

Next, the wafer surface is treated with O_2 plasma in a reactive ion etching (RIE) system and bonded at room temperature and in atmosphere. During the plasma activation process, oxidation occurs on the surface, which helps to facilitate high bonding strength [SB4]. After plasma treatment, the wafers are rinsed with DI water, and bonding can be performed by aligning and bonding the two wafers by hand at room temperature. Additionally, for better control of applied force and force distribution across the wafers during bonding, a wafer-to-wafer bonding tool may be used.

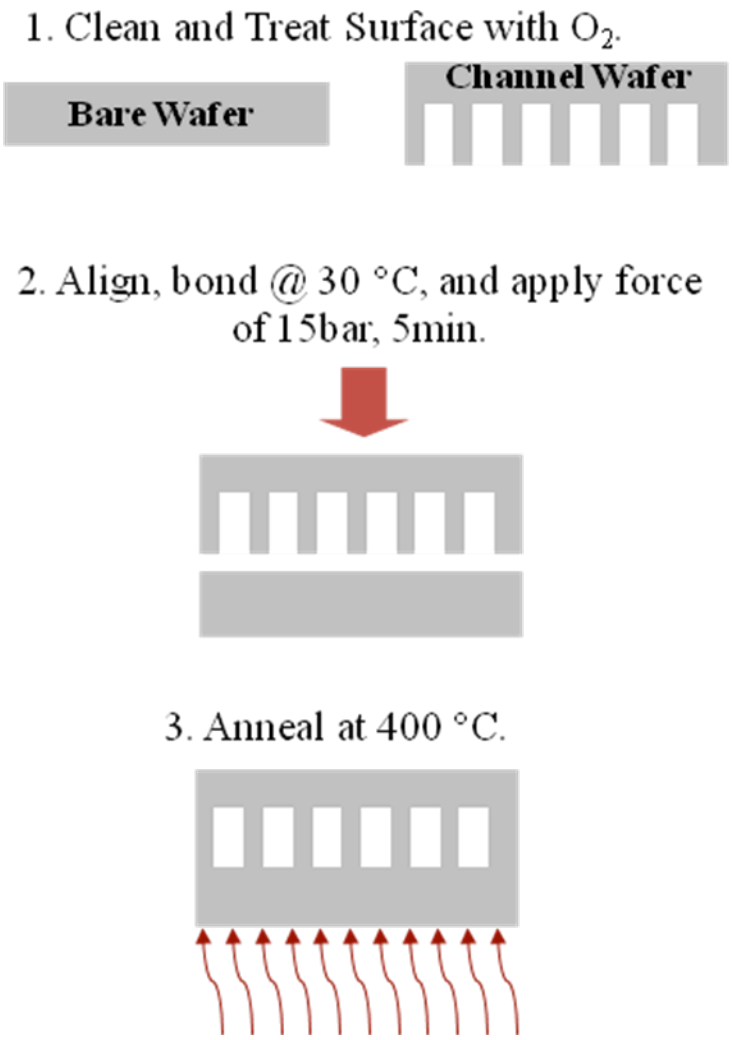


Figure 2.10: Schematic of process flow for capping microchannels via silicon-to-silicon bonding.

Finally, thermal annealing is performed at 400 ^{o}C for 12 hours, transforming the weak chemical bonds to strong chemical bonds. Silicon-capped microchannels were tested by examining the bonded wafer for voids and cracks using an infrared microscope, by destructive tests such as dicing, and by passing fluid through the microchannels at flow rates up to 100ml/min. Figure 2.11 shows a cross-sectional SEM image of a bonded silicon wafer containing microchannels and a silicon capping wafer. Wafers were consistently bonded with a yield of 70-80% using the Si-Si bonding technique [2.5].

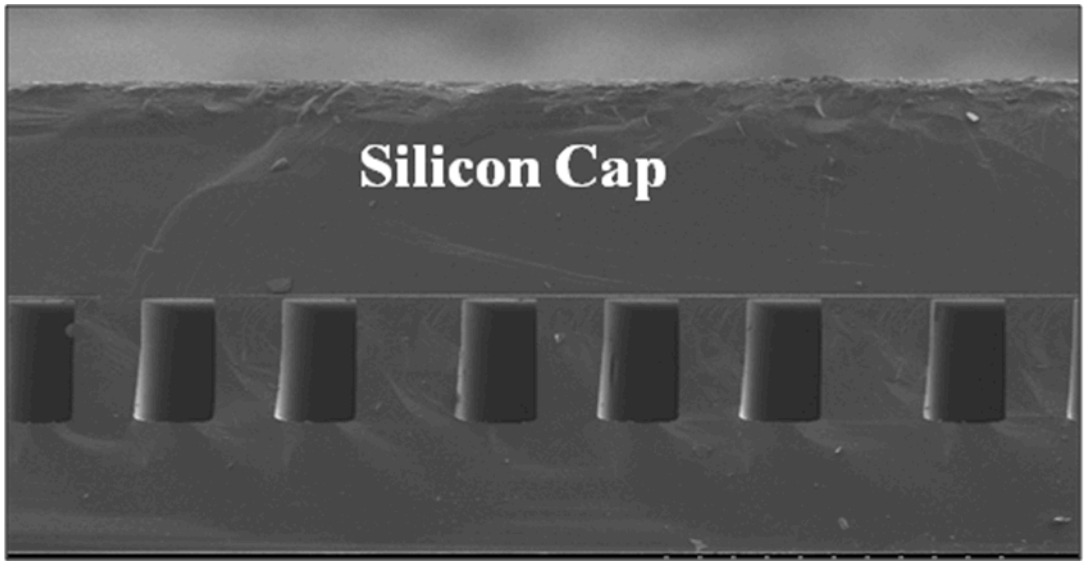


Figure 2.11: Schematic of process flow for capping microchannels via silicon-to-silicon bonding.

2.3.2. Polymer Overcoat

A second method for capping microchannels is by using the sacrificial polymer process described in [2.1, 2.7]. After etching microchannel trenches into the back side of the wafer (Figure 2.12a), Unity sacrificial polymer (Promerus, LLC) is spin-coated on the wafer, filling the microchannels. Afterwards, mechanical polishing is performed to planarize the surface (Figure 2.12b). Next, 15 μm of Avatrel 2090P polymer (Promerus, LLC) is spin-coated onto the wafer (Figure 2.12c). Finally, the Avatrel polymer is cured, and the Unity sacrificial polymer is thermally decomposed simultaneously in a nitrogen-purged furnace at low temperatures (≤200ºC) (Figure 2.12d) [2.8]. Figure 2.4 shows a cross-sectional optical image of a sample after the previously described processing steps

are completed. The non-optimized microchannels are 200µm tall and 100µm wide (Figure 2.4), and the copper TSVs have a 50µm diameter.

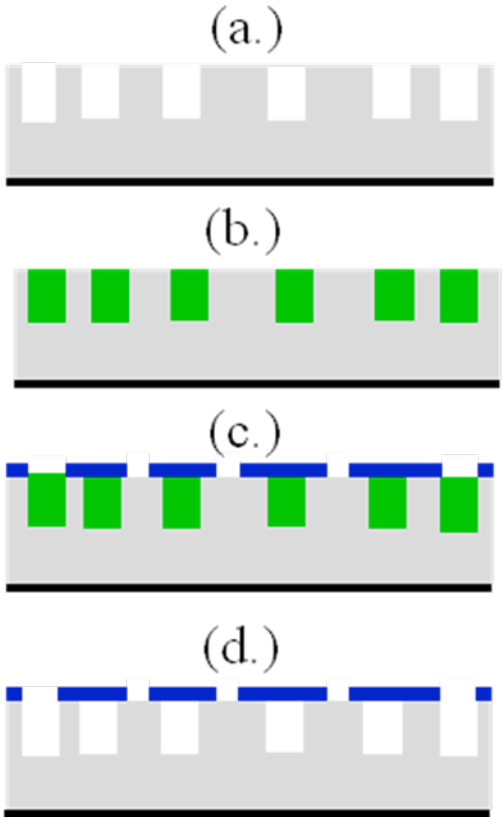


Figure 2.12. Schematic of capping microchannels using a polymer overcoat. (a)Microchannel trenches are etched into the back side of the wafer. (b)Spin coat and polish Unity sacrificial polymer. (c) Spin coat and pattern Avatrel polymer sockets as an overcoat layer. (d) Simultaneous curing of Avatrel polymer and thermal decomposition of sacrificial polymer.

2.4. Microchannel Heat Sink Design

2.4.1. Microchannel Heak Sink Theory

In [1.39], Tuckerman and Pease derived and experimentally verified the equations necessary to calculate the thermal resistance of a microchannel heat sink. A schematic of the microchannel heat sink concept demonstrated by Tuckerman and Pease is shown in Figure 2.13.

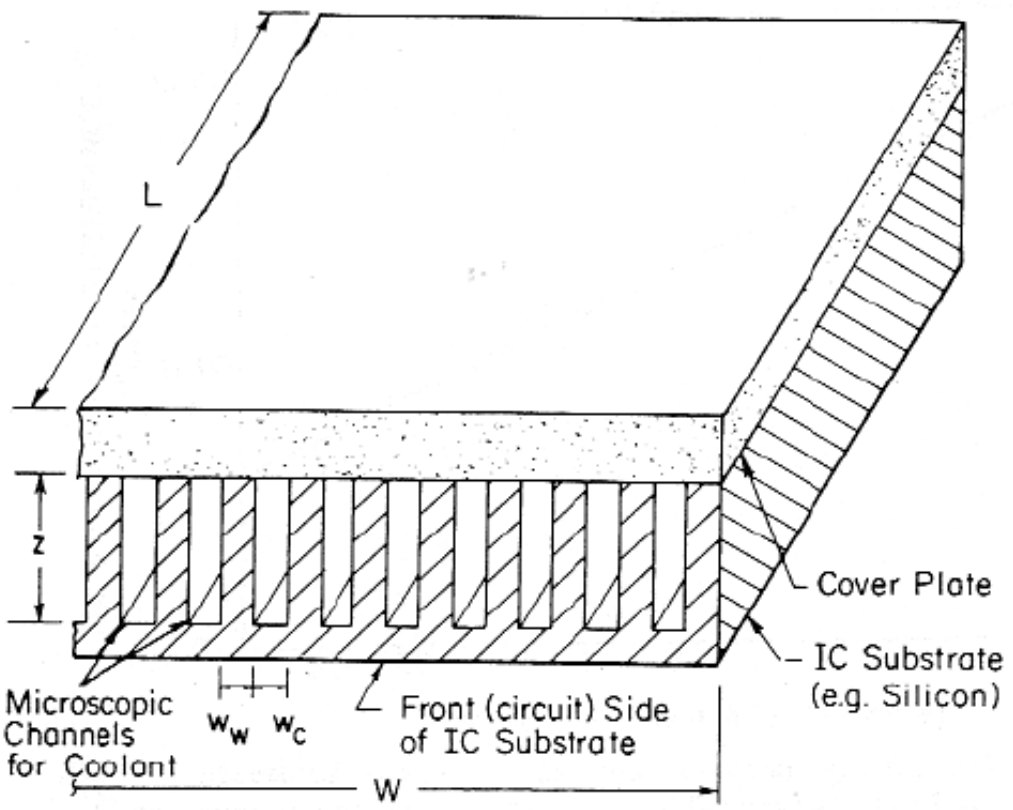


Figure 2.13: Schematic illustration of a microchannel heat sink concept demonstrated by Tuckerman and Pease [1.39].

The thermal resistance of a microchannel heat sink can be calculated using the sum of three resistances [1.39, 2.8]:

$$R_{th} = R_{cond} + R_{conv} + R_{heat},$$

where R_{cond}, the resistance due to conduction, is dependent on thermal conductivity of silicon, the distance between the bottom surface of a channel and the integrated circuits at the bottom side of the wafer, and the chip area. R_{conv}, the convective resistance, is dependent on the heat transfer coefficient of the cooling fluid and the area of the surfaces of the microchannels. The surface area of the channels is determined by the channel width, channel length, channel height, and the number of channels. R_{heat}, the resistance

due to heating of the cooling fluid, is determined by the temperature rise of the cooling fluid between the liquid inlet and outlet and the heat flux generated by the integrated circuit on the bottom side of the chip [1.39, 2.8, 2.14].

The conductive thermal resistance, R_{cond}, can be calculated by using the following equation:

$$R_{cond} = \frac{t}{k_{Si} A_{chip}},$$

where k_{Si} is determined by the thermal conductivity of silicon, A_{chip} is established by the area of the chip, and t is determined by the distance between the bottom surface of the microchannel and the integrated circuits at the front side on the chip.

The convective resistance, R_{conv}, is determined by the following equation:

$$R_{conv} = \frac{1}{hA_{channels}},$$

where the area of the microchannels is calculated as:

$$A_{channels} = n_c \cdot L_c \cdot (2H_c + W_c).$$

The surface area of the channels is determined by the channel width (W), channel length (L), channel height (H), and the number of channels (n). Consequently, the convective resistance is proportional to the channel height, channel width, and channel length.

For modeling and experimental purposes, deionized water is used as the cooling liquid. Assuming that DI water is at a laminar flow [2.15-2.16], the convective heat transfer coefficient h can be calculated by the following equation:

$$h = \frac{k_f Nu_{fd}}{D_h}.$$

where k_f is the fluid thermal conductivity, and D_h is the hydraulic diameter of a microchannel:

$$D_h = \frac{2W_c H_c}{H_c + W_c}.$$

Nu_{fd} is the Nusselt number of the fluid, a dimensionless heat transfer coefficient, which can be calculated by using the following equation:

$$Nu_{fd} = 8.235\left(1 - 1.883\alpha + 3.767\alpha^2 - 5.814\alpha^3 + 5.361\alpha^4 - 2\alpha^5\right),$$

where α is the ratio of channel width to the channel height (W_c/H_c) [2.8, 2.14].

The third component, R_{heat}, can be calculated by using the following equation:

$$R_{heat} = \frac{\Delta T_{inlet/outle}}{Q} = \frac{1}{V \cdot \rho \cdot C_p},$$

where V is the liquid flow rate, ρ is the density of the cooling liquid, and C_p is the specific heat capacity of the cooling liquid.

According to the ITRS, the required heat sink thermal resistance for high performance microprocessors will be 0.2 ^{o}C/W by the year 2018 [1.40], and the necessary chip junction temperature will continue to decrease (Table 2.1) [1.11].

Table 2.1: ITRS data for high-performance microprocessors.

ITRS Data (High Performance Chips)	2011	2012	2013	2014	2015	2016
Single Chip Junction Temperature (^{o}C)	85	85	80	80	80	75
Dissipated Power (W)	161	158	149	152	143	130
	2017	2018	2019	2020	2021	2022
Single Chip Junction Temperature (^{o}C)	75	75	70	70	70	70
Dissipated Power (W)	130	130	130	130	130	130

Figure 2.14 shows a summary of the equations necessary for microchannel heat sink analysis [1.39, 2.8, 2.14-2.16].

Equations	Symbol Legend
$R_{th} = R_{cond} + R_{conv} + R_{heat}$	R_{th} = Total thermal resistance
$R_{cond} = \frac{t}{k_{Si} A_{chip}}$	$A_{channels}$ = area of channel
$R_{conv} = \frac{1}{hA_{channels}}$	h = heat transfer coefficient
$R_{heat} = \frac{\Delta T_{inlet/outle}}{Q} = \frac{1}{V \cdot \rho \cdot C_p}$	H_c = channel height
$A_{channels} = n_c \cdot L_c \cdot (2H_c + W_c)$	L_c = channel length
$h = \frac{k_f Nu_{fd}}{D_h}$	D_h = channel hydraulic diameter
$D_h = \frac{2W_c H_c}{H_c + W_c}$	Nu_{fd} = Nusselt number
$Nu_{fd} = 8.235\left(1 - 1.883\alpha + 3.767\alpha^2 - 5.814\alpha^3 + 5.361\alpha^4 - 2\alpha^5\right)$	ΔP_{ch} = pressure drop in microchannels
$\Delta P_{ch} = \frac{1}{2} f \cdot \mathrm{Re} \cdot L_c \cdot \frac{\mu \cdot V (1 + W_c / H_c)^2}{n \cdot H_c \cdot W_c^3}$	f = friction coefficient
$f\,\mathrm{Re} = 64$	Re = Reynolds number
$v = \frac{flow\quad rate}{overall\quad cross-sectional\quad area} = \frac{V}{n_{via}\pi(\frac{D_{via}^2}{4})}$	V = flow rate
	C_p = specific heat
	ρ = fluid density
	μ = fluid kinematic viscosity
	k_{si} = Si thermal conductivity
	k_f = fluid thermal conductivity
	n_c = number of channels
	Q = Power

Figure 2.14: Hydro-dynamic equations for microchannel heat sink theory.

2.4.2. Microchannel Heak Sink Geometry and Thermal Resistance

The channel geometry of a microchannel heat sink is a major component of determining the thermal resistance of a microchannel heat sink. Figure 2.15 shows a schematic of a microchannel heat sink.

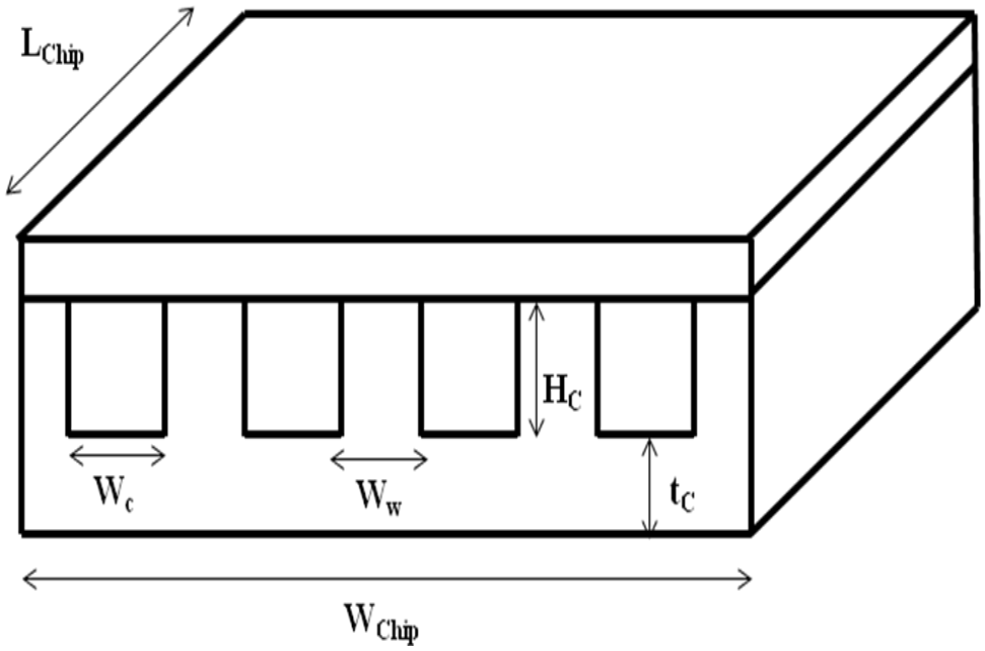


Figure 2.15: Schematic illustration of a microchannel heat sink [1.39].

Matlab was used to calculate the thermal resistance of various heat sink configurations in order to determine the appropriate microchannel geometry for the proposed microchannel heat sink. The chip size used for modeling purposed was chosen to be 1cm x 1cm in area. To analyze the impact of the channel height on the heat sink thermal resistance, a fixed number of channels, a fixed fluid flow rate, and a fixed channel fin width were chosen. Thermal resistance values were generated for varying

microchannel heights of 100µm to 400µm, as shown in Figure 2.16, Table 2.2, Table 2.3, and Table 2.4.

Simulation results show that microchannel heat sink thermal resistance decreases as the channel height increases. As the channel height increases, the surface area that is in contact with the cooling fluid increase, causing the thermal resistance to decrease. Figure 2.16 also illustrates that the thermal resistance decreases as the channel fin width (W_w) decreases. This reduction in thermal resistance occurs because as the channel fin width is decreased, the number of microchannels that can be integrated into a given area increases, which enables more microchannel cooling capability.

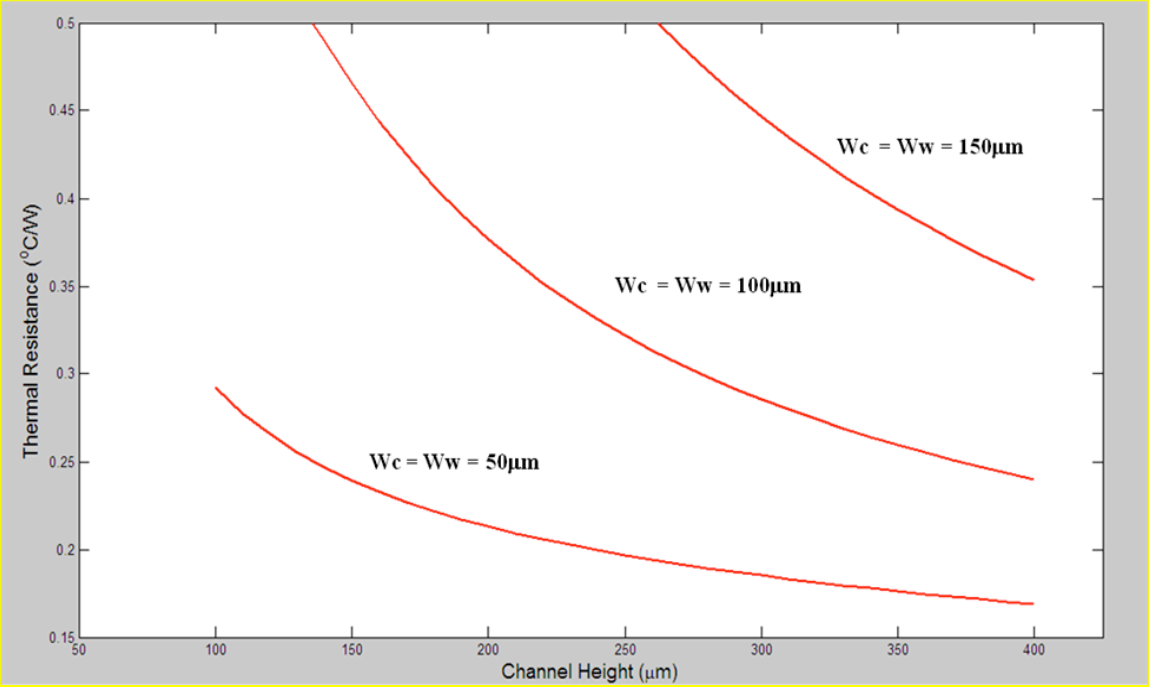


Figure 2.16: Simulation results for thermal resistance as a function of channel height for various fixed channel fin widths.

Table 2.2: Summary of simulation results for thermal resistance as a function of channel height (channel width = 100μm).

Channel Height (μm)	Thermal Resistance (C/W)	Flow Rate (ml/min)	Number of Channels	Channel Width (μm)
100	0.628	100	51	100
150	0.466	100	51	100
250	0.322	100	51	100
350	0.259	100	51	100
400	0.239	100	51	100

Table 2.3: Summary of simulation results for thermal resistance as a function of channel height (channel width = 50μm).

Channel Height (μm)	Thermal Resistance (C/W)	Flow Rate (ml/min)	Number of Channels	Channel Width (μm)
100	0.292	100	101	50
150	0.239	100	101	50
250	0.197	100	101	50
350	0.176	100	101	50
400	0.169	100	101	50

Table 2.4: Summary of simulation results for thermal resistance as a function of channel height (channel width = 150μm).

Channel Height (μm)	Thermal Resistance (C/W)	Flow Rate (ml/min)	Number of Channels	Channel Width (μm)
150	0.772	100	34	150
250	0.512	100	34	150
350	0.388	100	34	150
400	0.349	100	34	150

2.4.3. Microchannel Heak Sink Geometry and Pressure Drop

The channel geometry of a microchannel heat sink is also a determinant of the pressure drop in the heat sink. The pressure drop in the system can be calculated as a

function of the chip power (heat flux) to be removed based on the hydrodynamic equations found in Figure 2.14,

$$\Delta P_{ch} = \frac{1}{2} f \cdot \mathrm{Re} \cdot L_c \cdot \frac{\mu \cdot V (1 + W_c / H_c)^2}{n \cdot H_c \cdot W_c^3}.$$

For modeling purposes, it is assumed that DI water is used as the cooling fluid and a fully developed laminar flow is present in the microchannels, and a fixed chip area of 1cm x 1cm is chosen.

To analyze the impact of the channel height on the heat sink pressure drop, a fixed number of channels, a fixed fluid flow rate, and a fixed channel fin width were chosen. Pressure drop values were generated for varying microchannel heights of 100µm to 400µm, as shown in Figure 2.17 and Table 2.5.

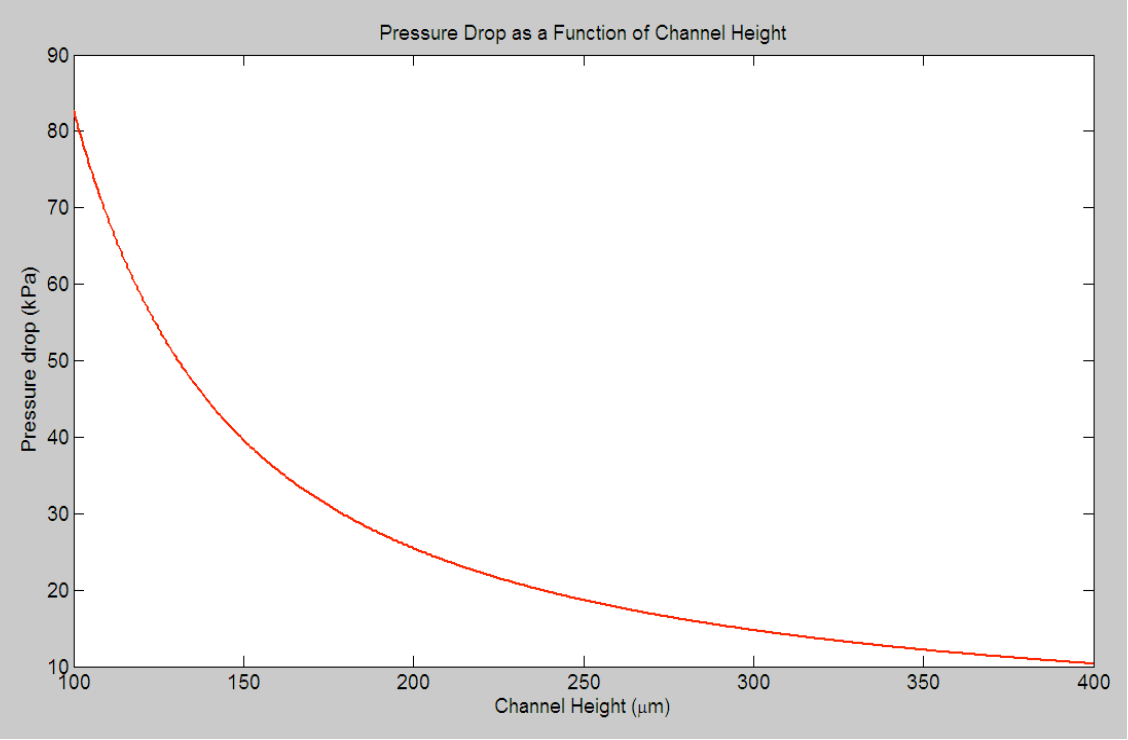


Figure 2.17: Simulation results for thermal resistance as a function of channel height (channel width = 100µm).

Table 2.5: Summary of simulation results for pressure drop as a function of channel height (channel width = 100µm).

Channel Height (µm)	Pressure Drop (kPa)	Flow Rate (ml/min)	Number of Channels	Channel Width (µm)
100	82.8	100	49	100
150	39.6	100	49	100
200	25.5	100	49	100
300	14.7	100	49	100
400	10.4	100	49	100

To analyze the impact of channel width on the heat sink pressure drop, a fixed channel height and a fixed fluid flow rate were chosen. Pressure drop values were generated for varying microchannel widths of 50µm to 150µm, as shown in Figure 2.18, and Table 2.6.

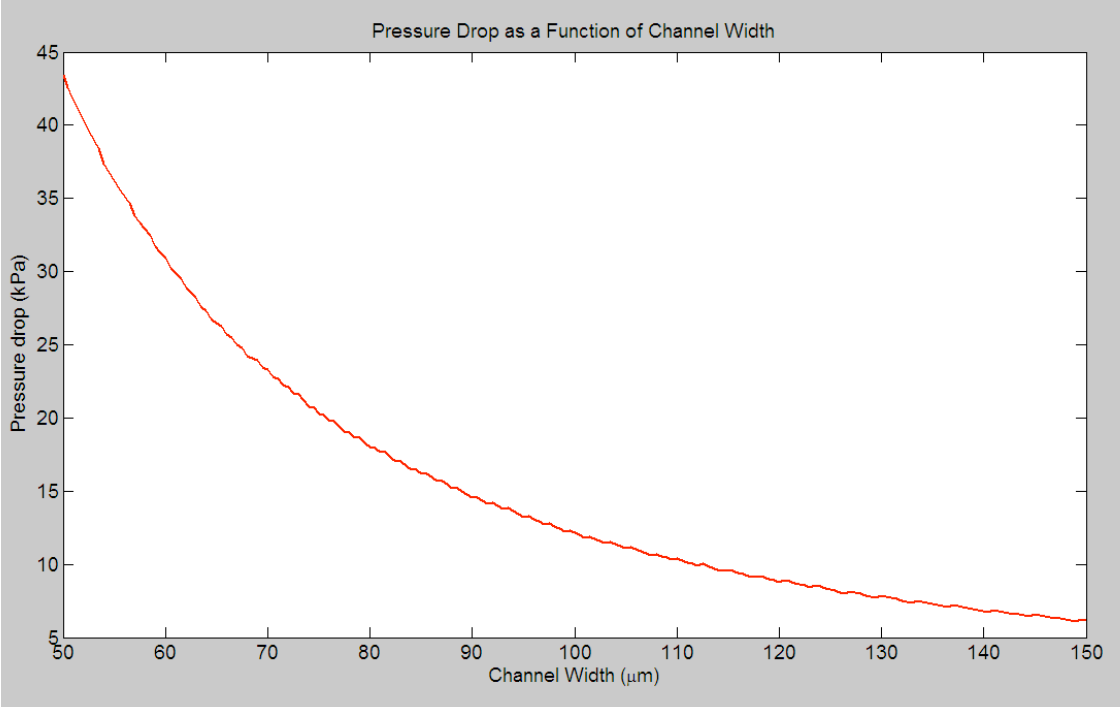


Figure 2.18: Simulation results for pressure drop as a function of channel width (channel height = 350µm).

Table 2.6: Summary of simulation results for pressure drop as a function of channel width (channel height = 350μm).

Channel Height (μm)	Pressure Drop (kPa)	Flow Rate (ml/min)	Number of Channels	Channel Width (μm)
350	**43.4**	**100**	**99**	**50**
350	**23.3**	**100**	**62**	**80**
350	**12.2**	**100**	**49**	**100**
350	**7.9**	**100**	**37**	**130**
350	**6.2**	**100**	**32**	**150**

Results of the Matlab simulation show that pressure drop can be decreased by increasing the channel width or by increasing the channel height, as shown in Table 2.5 and Table 2.6. However, it is important to note that if the channel width is increased, the number of channels that can be fabricated in a given area decreases. Consequently, the overall thermal resistance of the microchannel heat sink increases.

It is also important to note that, when increasing the channel height while having a fixed channel width, as pressure drop decreases, thermal resistance decreases, as shown in Figure 2.17 and Table 2.5.

Figure 2.19 shows a graph of microchannel heat sink thermal resistance as a function pressure drop. For this simulation, the channel width is fixed, and the microchannel height varies from 100μm to 400μm. The graph shows that as pressure drop decreases, the microchannel heat sink thermal resistance decreases. This result is expected, as channel height (H_c) is inversely proportional to ΔP_{ch}, R_{cond} and R_{conv}.

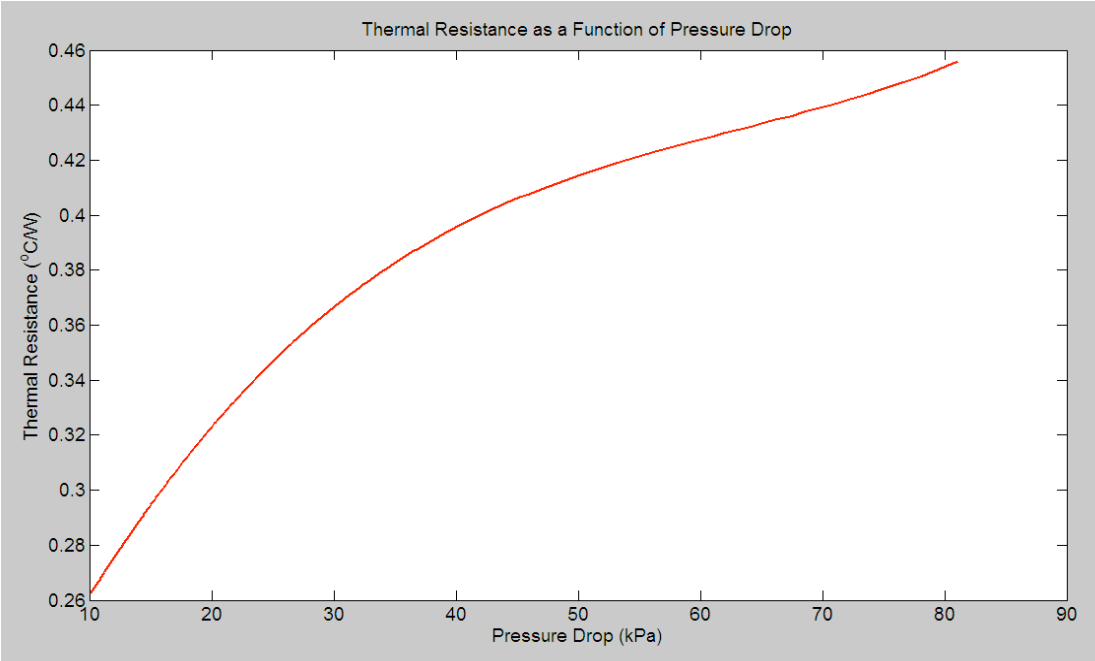


Figure 2.19: Simulation results for thermal resistance as a function of pressure drop.

Table 2.7: Summary of simulation results for thermal resistance as a function of pressure drop.

Channel Height (µm)	Pressure Drop (kPa)	Flow Rate (ml/min)	Number of Channels	Channel Width (µm)	Thermal Resistance (C/W)
100	**82.8**	**100**	**49**	**100**	**0.456**
150	**39.6**	**100**	**49**	**100**	**0.393**
200	**25.5**	**100**	**49**	**100**	**0.347**
300	**14.7**	**100**	**49**	**100**	**0.291**
400	**10.4**	**100**	**49**	**100**	**0.263**

Using the equations in Figure 2.14 to determine the thermal resistance and pressure drop for various microchannel heat sink configurations and by using the ITRS projected heat sink thermal resistance required for high-performance chips, the dimensions of proposed microchannel heat sink design were calculated, as shown in Table 2.8. Each chip in the 3D stack has 39, 80µm wide, 350µm tall microchannels.

SEM images of the fabricated microchannel heat sink are shown in Figure 2.8, and a schematic of the mask layout of the microchannels is shown in Figure 2.20. A more detailed discussion of the heat sink thermal resistance and pressure drop values that were measured during thermal and fluidic testing will be discussed in more detail in Chapter 5.

Table 2.8: Microchannel heat sink dimensions for proposed 3D cooling scheme (fluid flow rate = 100ml/min).

Microchannel Heat Sink Dimensions	
Channel Width	80 um
Channel Height	350 um
Fin Width	80 um
Thermal Resistance	0.229 °C/W

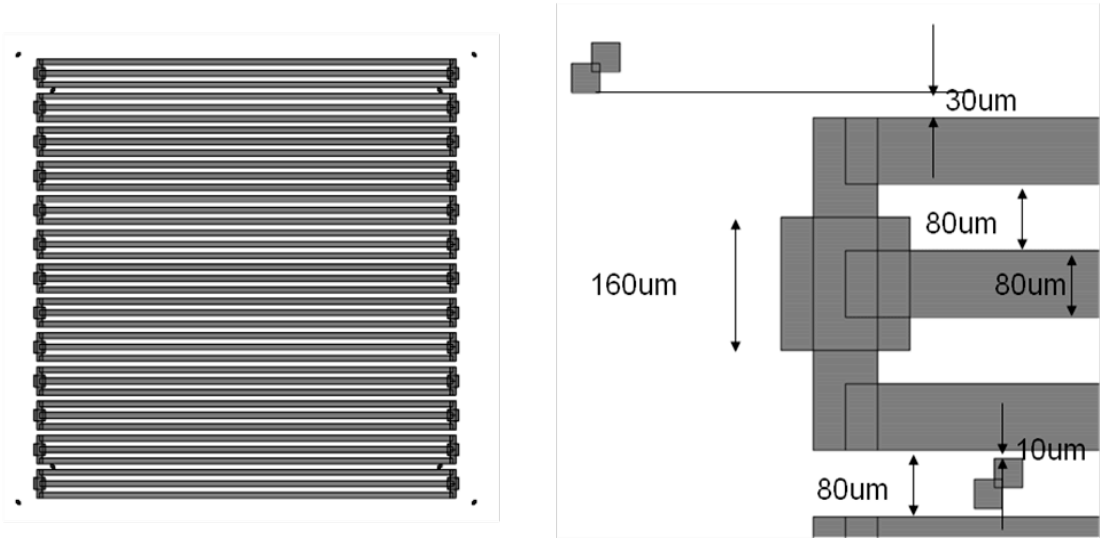


Figure 2.20: Schematic illustration of proposed microchannel heat sink design.

2.5. Microchannel Heat Sink and Electrical TSV Co-design

In the proposed 3D inter-layer liquid cooling technology, while microchannels are needed for cooling, electrical TSVs are needed for signaling and power delivery in the

3D system. For 3D technology, usually wafers are thinned down in order to make electrical TSV fabrication easier. However, as previously discussed, microchannel heat sink cooling capability is a function of channel geometry. Cooling capability increases with increasing channel surface area in contact with the cooling liquid. Consequently, there are tradeoffs when co-designing electrical TSVs and microchannel heat sinks for integration in 3D chip stacks.

2.5.1. Microchannel Heak Sink Geometry and Electrical TSV Density

According to the ITRS, the minimum TSV pitch will continue to decrease, the minimum die thickness will continue to decrease, and the number of electrical TSVs in a high-performance processor will continue to increase through the year 2022 [1.11], as shown in Table 2.9. Consequently, when using a microchannel heat sink as the chip cooling solution, it is important to use a channel geometry that allows a sufficient number of electrical TSVs to be fabricated in the chip.

Table 2.9: ITRS projections for high-performance chips: number of electrical TSVs, minimum TSV pitch, maximum TSV aspect ratio, and minimum die thickness [1.11].

ITRS Data (High Performance Chips)	2011	2012	2013	2014	2015	2016
TSVs (x1000)	-	-	-	-	5	5
Minimum TSV Pitch (µm) (die to die)	4	3.8	3.6	3.4	3.3	3.1
TSV Maximum Aspect Ratio	10	10	10	10	10	10
Minimum Die Thickness (µm) (TSV)	-	-	-	-	25	20
Minimum Die Thickness (µm) (Side by Side)	100	100	100	100	100	100
	2017	2018	2019	2020	2021	2022
TSVs (x1000)	6	6	7	7	8	8
Minimum TSV Pitch (µm) (die to die)	2.9	2.8	2.7	2.5	2.4	2.3
TSV Maximum Aspect Ratio	10	10	10	10	10	10
Minimum Die Thickness (µm) (TSV)	20	18	18	15	15	10
Minimum Die Thickness (µm) (Side by Side)	100	100	100	100	100	100

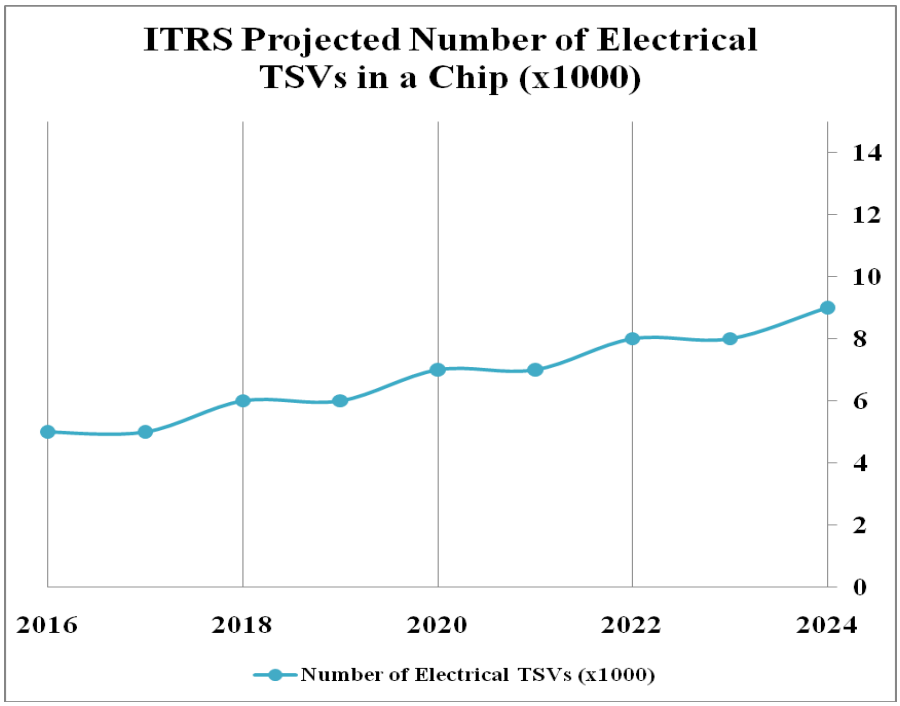


Figure 2.21: ITRS projections for number of electrical TSVs per high-performance chip [1.11].

As the channel fin width increases, more electrical TSVs can be fabricated in the channel fin (also known as the microchannel wall, W_w), as shown in Figure 2.2. However, as the width of the microchannel fins increase, the number of microchannels that can be fabricated in a given area decreases, which results in less cooling capability.

Based on channel geometrical considerations, Matlab code was used to calculate the number of electrical TSVs that can be fabricated in silicon channel walls of a microchannel heat sink, as a function of electrical TSV diameter. The height of the microchannel channels and thickness of the wafer range from 200μm to 400um. The chip width (W) is assumed to be 1cm, and the chip length (L) is assumed to be 1cm.

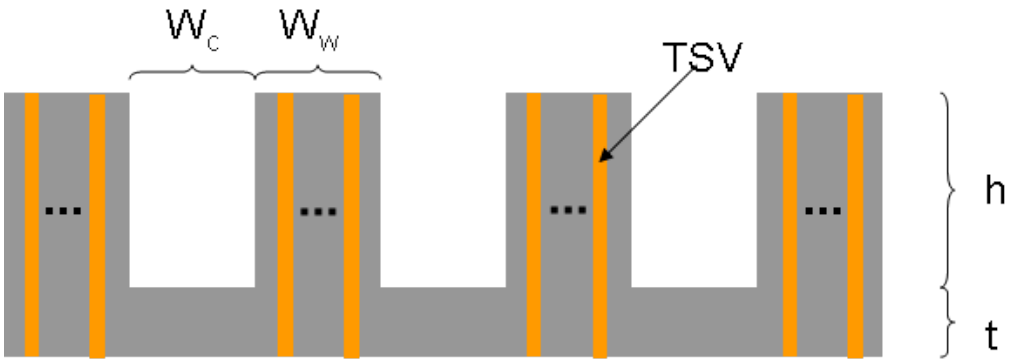


Figure 2.22: Schematic illustration of a wafer with integrated electrical TSVs and a microchannel heat sink [2.17].

The width of the microchannel wall (W_W) can be expressed as a function of TSV parameters as,

$$W_W = 50 + P_{TSV} \cdot (N_{TSVColumns} - 1) + D_{TSV},$$

where P_{TSV} is the TSV pitch, D_{TSV} is the TSV diameter, and $N_{TSVcolumns}$ represents the number of TSV columns in the microchannel wall. ($N_{TSVcolumns} \geq 1$) [2.17]. The first term in the above equation, 50μm, is an assumed constant value that is used to establish the clearance between the edge of the outermost column of TSVs and the edge of the microchannel wall, as shown in see Figure 2.23. P_{TSV} is assumed to be 1.5(D_{TSV}).

The total number of TSVs, N_{TSVs}, that can be fabricated on a 1cm^2 chip in the microchannel heat sink fins can be estimated as

$$N_{TSVs} = N_{TSVColumns} \cdot (n+1)\frac{L}{P_{TSV}},$$

where n is the total number of microchannels. , which can be calculated using the expression

$$n = \frac{W - W_W}{W_W + W_C}.$$

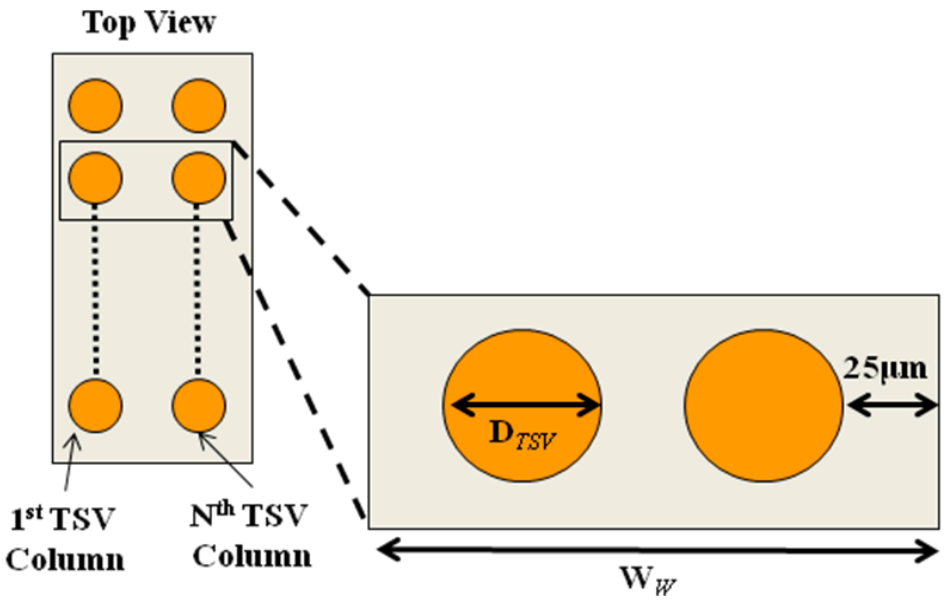


Figure 2.23: Schematic of microchannel fin with integrated electrical TSVs.

Figures 2.24 and 2.25 show simulation results for microchannel heat sink thermal resistance and pressure drop as a function of TSV diameter (20µm diameter and 5µm diameter), number of TSVs columns per microchannel fin, and varying microchannel heights (wafer thickness) that vary from 200µm to 400um.

The simulation results are summarized in Table 2.10. The simulation results show that as the width of microchannel fin increases, the number of columns of electrical TSVs can also be increased, which causes the microchannel heat sink thermal resistance and pressure drop to increase. This increase occurs because, as the number of TSV columns increases, the width of the channel fin increases. For a fixed microchannel width, this results in a decreased number of microchannels available for cooling. A decreased number of microchannels leads to a decrease in the surface area in contact with the cooling fluid. Furthermore, a decrease in the number of microchannels also increases

the pressure drop, as the number of channels in inversely proportional to the pressure drop in the microchannel heat sink.

Additionally, an increase in the diameter of the electrical TSVs also causes an increase in microchannel fin width. Consequently, the thermal resistance and pressure drop increase, as the number of microchannels available for cooling decreases. An increase in thermal resistance and pressure drop are also observed when the microchannel height and wafer thickness increase due to the impact of channel geometry on thermal resistance and pressure drop, as previously discussed.

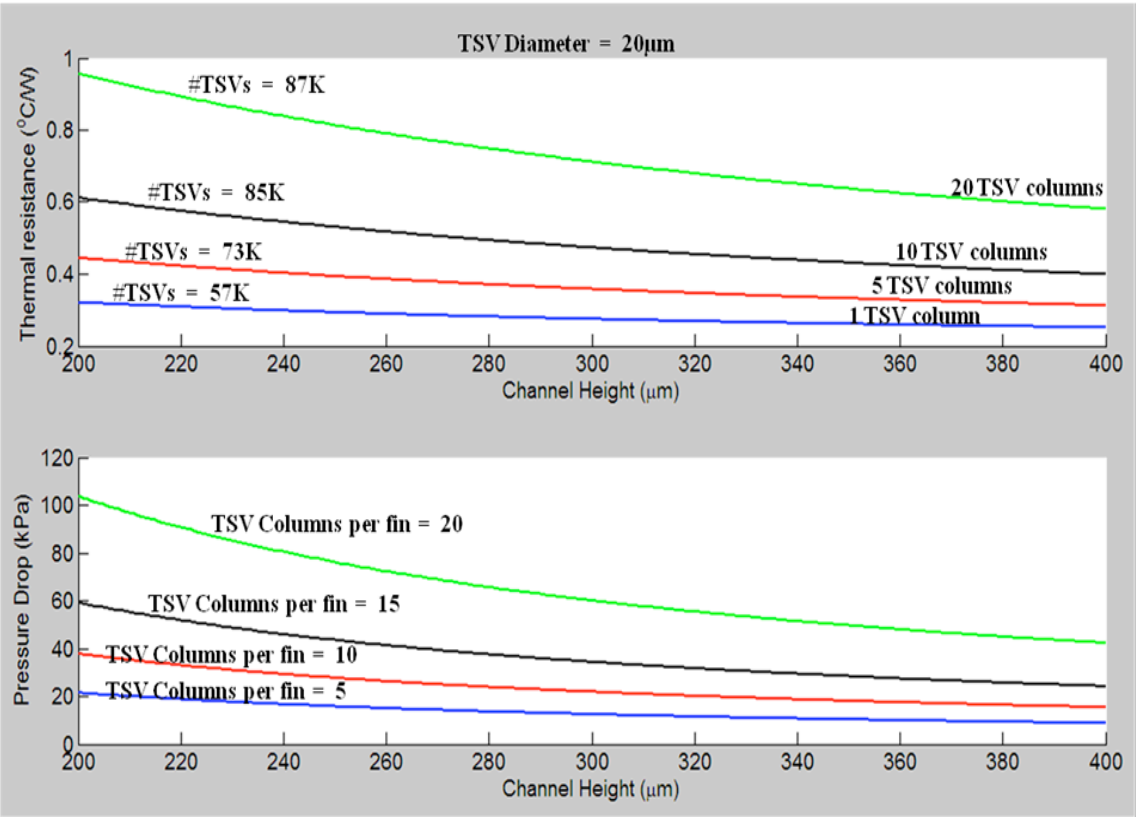


Figure 2.24: Electrical TSV density as a function of channel fin width and electrical TSV diameter (20um).

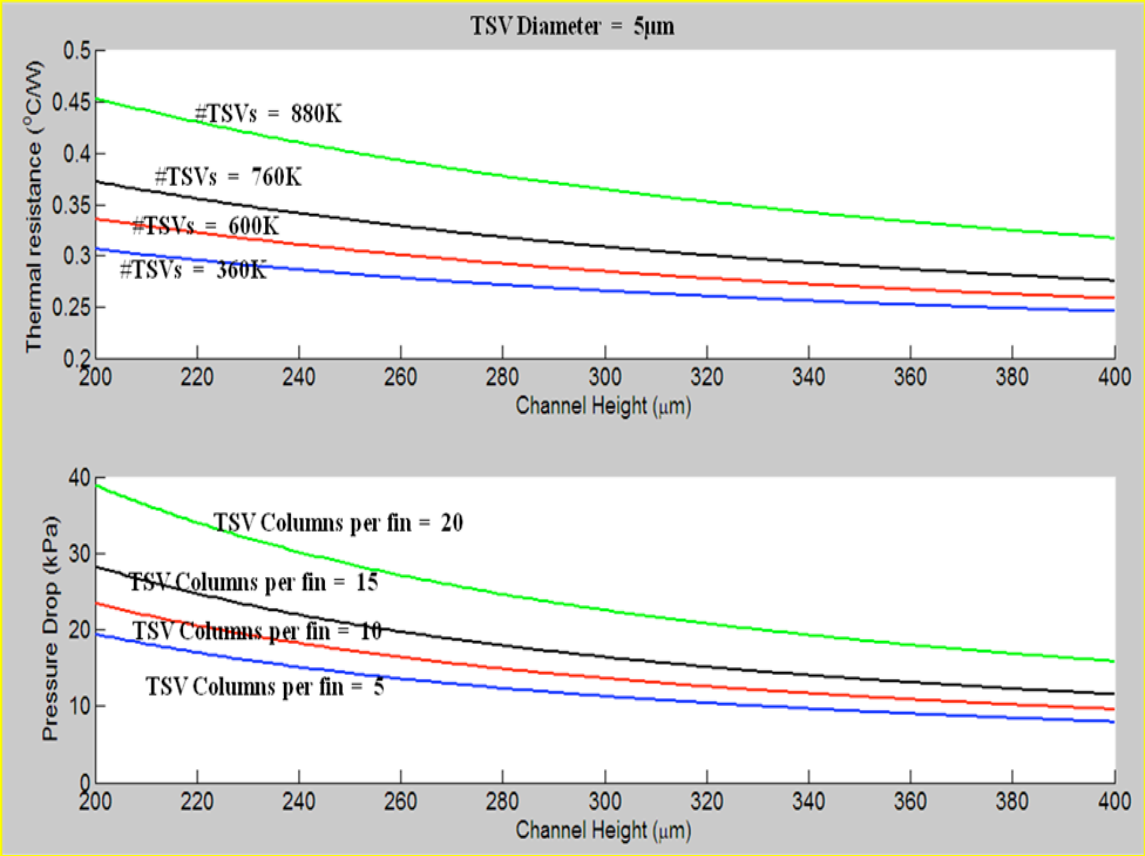


Figure 2.25: Electrical TSV density as a function of channel fin width and electrical TSV diameter (5um).

The results from the analysis shown in Table 2.10 illustrate that the electrical TSV density required for future high-performance chips, based on ITRS projections, can be achieved when using a microchannel heat sink cooling solution. Consequently, the limiting factors for integrating microchannel heat sinks and electrical TSVs will be electrical TSV aspect ratio and the amount of chip area that will be dedicated to electrical TSVs.

Table 2.10: Electrical TSV density as a function of channel fin width and electrical TSV diameter.

Number of TSVs	TSV Diameter (µm)	Number of TSV Columns	Number of Channels	Channel Fin Width (µm)	Channel Width (µm)
360,000	5	5	53	85	100
600,000	5	10	44	122.5	100
760,000	5	15	37	160	100
880,000	5	20	32	197.5	100
150,000	10	5	44	120	100
226,670	10	10	33	195	100
270,000	10	15	26	270	100
293,330	10	20	21	345	100
86,667	15	5	38	155	100
120,000	15	10	26	267.5	100
140,000	15	15	20	380	100
151,110	15	20	16	492.5	100
56,667	20	5	33	190	100
73,333	20	10	21	340	100
85,000	20	15	16	490	100
86,667	20	20	12	640	100

Regarding aspect ratio, the minimum aspect ratio of 10:1 is projected for electrical TSVs integrated in high-performance chips, as shown in Table 2.9 [1.11]. In the literature, a copper filled TSV with an aspect ratio of 49:1 has been demonstrated in a thinned silicon wafer [2.17]. The analysis that was done in this research shows electrical TSV density results for electrical TSVs with diameters of 5µm, 10µm, 15µm, and 20µm and for microchannel channel heights and wafer thickness ranging from 200µm to 400µm. For the smallest diameter electrical TSV used in this analysis, 5µm diameter TSVs, the aspect ratio would be 40:1 when using a 200µm thick silicon wafer and 80:1 when using a 400µm thick wafer. Consequently, for cooling solutions that require thicker chips, electrical TSVs with larger diameters will be necessary when using current

electrical TSV fabrication technologies. However, it is important to note that smaller diameter TSVs allow the most TSV density to be achieved, which is important for chip designs where the silicon area allowed for electrical TSV fabrication is limited.

2.5.2. Microchannel Heak Sink Geometry and Electrical TSV Performance

When integrating microchannel heat sink technology in a 3D chip stack, cooling capability of the heat sink increases with microchannel height and wafer thickness, as shown from modeling results in the previous sections. However, thinner wafers help to facilitate easier electrical TSV fabrication. Furthermore, wafer thickness has an impact on the electrical impedances and performance of electrical TSVs.

In the following analysis, electrical properties including resistance and capacitance are modeled for electrical TSVs of various diameters (5μm, 10μm, 15μm, and 20μm). Simulation results examine the impact of electrical TSV diameter and electrical TSV length (based on wafer thickness) on TSV resistance and capacitance.

The resistance of an electrical TSV can be determined using the following equation:

$$R_{TSV} = \frac{\rho \cdot l_{TSV}}{\pi \cdot r_{TSV}^2},$$

where ρ is the resistivity of the conducting material, l_{TSV} is the length of the TSV, and . r_{TSV} is the TSV radius. In this analysis, copper is used as the electrical TSV metal.

The modeled results in Figure 2.26 and Table 2.11 show electrical TSV resistance as a function of wafer thickness and TSV diameter.

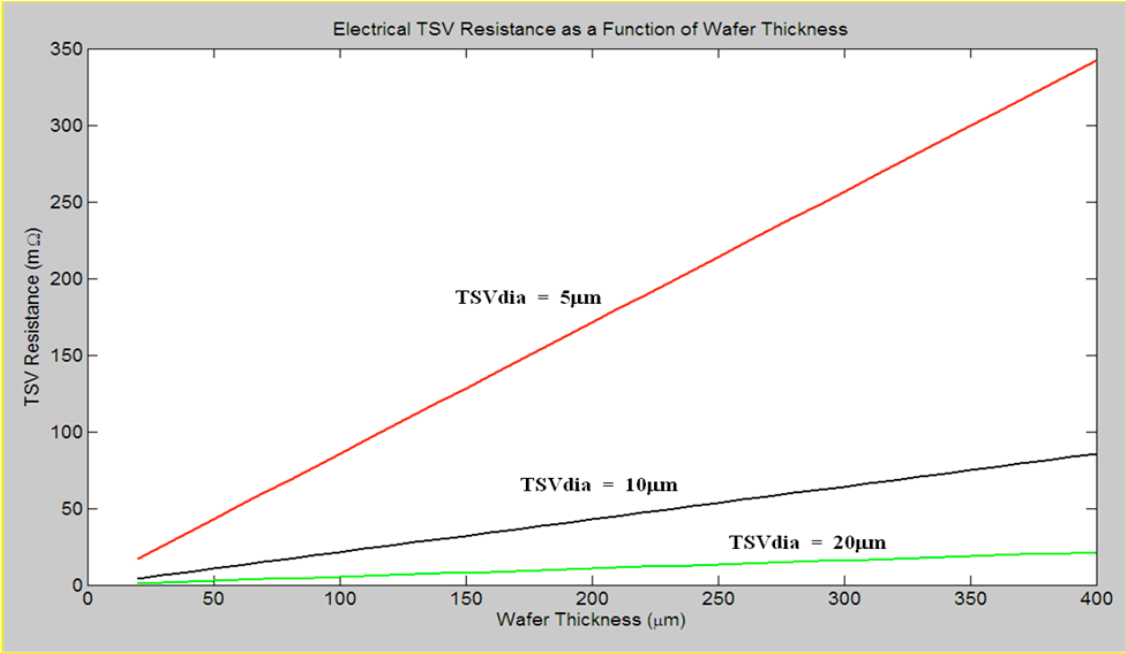


Figure 2.26: Electrical TSV resistance as a function of wafer thickness and TSV diameter.

Table 2.11: Electrical TSV resistance as a function of wafer thickness and TSV diameter.

TSV Diameter (μm)	TSV Length (μm)	TSV Resistance (mΩ)
5	20	17.11
5	50	42.78
5	100	85.56
5	200	171.12
5	400	342.25
10	20	4.28
10	50	10.7
10	100	21.31
10	200	42.78
10	400	85.56
20	20	1.07
20	50	2.67
20	100	5.35
20	200	10.7
20	400	21.39

As expected, the data shows that electrical resistance is decreased for shorter TSVs and for TSVs having larger diameters.

Electrical TSVs are typically fabricated by etching holes in a silicon wafer and filling the holes with a thin layer of oxide and a metal, as shown in Figure 2.27.

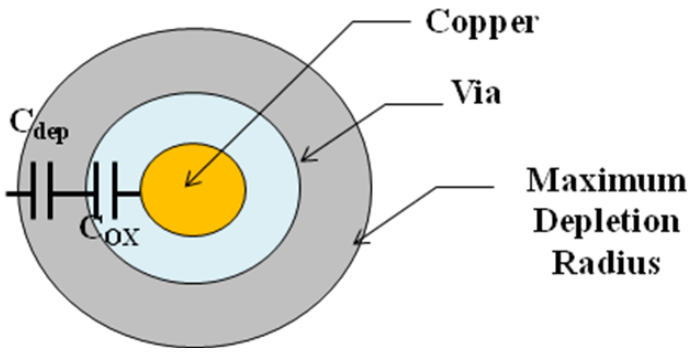


Figure 2.27: Top view of an electrical TSV in silicon and the capacitances associated with the TSV structure.

The self-capacitance can be calculated by the using the following expression:

$$C_{TSV\,\min} = \frac{C_{OX} C_{dep\,\min}}{C_{OX} + C_{dep\,\min}},$$

where C_{OX} is the oxide capacitance and $C_{dep\,\min}$ is the depletion capacitance [2.18].

When the voltage applied to TSVs is higher than the flat-band voltage ($V_{TSV} \geq V_{FB}$), the substrate is depleted so that the total capacitance is the series of the oxide capacitance and the depletion capacitance (C_{dep}) [2.19].

$$C_{TSV} = \frac{1}{C_{OX}} + \frac{1}{C_{dep\,\min}} = \frac{C_{OX} C_{dep\,\min}}{C_{OX} + C_{dep\,\min}}$$

When capacitors are in series, the smaller capacitance dominates the value of the overall capacitance. In this case, C_{OX} results in a much smaller capacitance for most cases

considered in this work. For this analysis, the overall capacitance is estimated as being the value of C_{OX}. The TSV oxide capacitance is determined by:

$$C_{OX} = \frac{2\pi\varepsilon_{OX} L_{TSV}}{\ln\left(\frac{R_{via}}{R_{metal}}\right)},$$

where ε_{ox} is the oxide permittivity, L_{TSV} is the TSV length, R_{via} and R_{metal} are the radii of the via and copper (Figure 2.27) [2.18].

The C_{ox} is modeled and plotted for different heat sink heights and different TSV aspect ratios, assuming the thickness of the dielectric (oxide) to be 1μm. The simulation results in Figure 2.28 show that the TSV capacitance increases linearly as the thickness of the die increases.

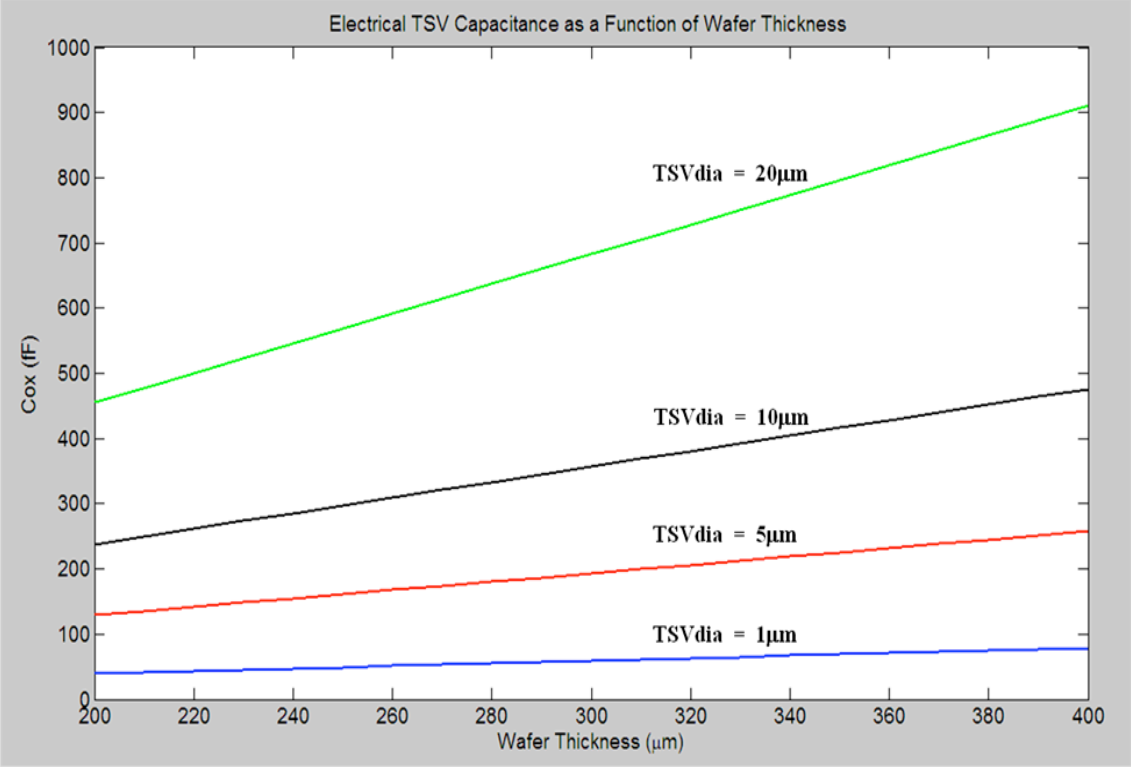


Figure 2.28: Electrical TSV oxide capacitance as a function of wafer thickness and TSV diameter.

Table 2.12 shows a summary of the simulation results. For 10μm diameter electrical TSVs, C_{TSV} for a 200μm thick wafer is 237.9fF, while the TSV capacitance for a 400μm thick wafer is 475.8fF. Table 2.12 also shows that TSV capacitance increases with increasing TSV diameter and increasing wafer thickness. Furthermore, as the TSV aspect ratio increases, the TSV capacitance decreases. The capacitance reduction improves the interconnect latency and power consumption.

Table 2.12: Electrical TSV capacitance as a function of wafer thickness and TSV diameter.

TSV Diameter (μm)	TSV Length (μm)	TSV Capacitance (fF)
1	200	39.5
1	300	59.2
1	400	79
5	200	128.9
5	300	193.4
5	400	257.8
10	200	237.9
10	300	356.8
10	400	475.8
20	200	455.1
20	300	682.6
20	400	910.1

2.6. Summary

This chapter describes the wafer-level batch fabrication and micromachining technologies that are used to fabricate the necessary electrical and microfluidic interconnects for the proposed 3D inter-layer cooling platform.

Each silicon die of the 3D stack contains the following features: 1) a monolithically integrated microchannel heat sink, 2) through-silicon fluidic vias (TSFV)

used for fluidic routing in the 3D stack, and 3) solder bumps (electrical I/Os) and microscale C4 pipes (fluidic I/Os) on the side of the chip opposite to the microchannel heat sink. Fabrication results of the individual components and their integration is demonstrated.

Additionally, compact physical modeling is used to analyze the impact of microchannel geometry and fluid flow rates on thermal resistance and pressure drop of the 3D systems. Compact physical modeling is also used to explore the electrical TSV performance and microchannel heat sink cooling trade-offs when integrating microchannel heat sinks and electrical TSVs in a 3D chip stack.

CHAPTER 3

DESIGN AND FABRICATION OF ELECTRICAL AND FLUIDIC I/O INTERCONNECTS

3.1. Integrated Electrical and Fluidic I/O Technologies for 3D Inter-layer Liquid Cooling

In the 3D cooling scheme outlined in Figure 2.2, microscale fluidic interconnection between strata is enabled by through-wafer fluidic vias and fluidic I/O interconnects. Three distinct fluidic I/O technologies have been developed, including a controlled collapse chip connection (C4) pipe fluidic I/O (Figure 3.1a) [2.9], an air-gap C4 fluidic I/O (Figure 3.1b) [2.9], and a polymer pipe fluidic I/O (Figure 3.1c) [2.3-2.4].

Solder ring based fluidic sealing approaches have been previously studied to form compact 3D packages by stacking multi-layer FR-4 substrates in [3.1]. Development of a micro-scale solder-based fluidic interconnect technology allows simultaneous batch fabrication of electrical and fluidic I/Os, making electrical and fluidic I/O integration seamless. The following sections outline process integration and assembly technologies for fluidic I/O interconnect technologies which can be used to hermetically seal fluidic interfaces in 3D chip stacks.

The solder-based fluidic I/Os have multiple advantages over the polymer-based fluidic I/Os. The solder fluidic I/Os do not require polymer sockets to aid in sealing. Thus, because of the ability to fabricate shorter fluidic I/Os, there is less space between chips in the 3D stack, making the 3D stack more compact. Additionally, it is not

necessary that an epoxy-based sealant be applied at the edges of the I/Os, as the assembly of the solder fluidic I/Os to copper rings on the substrate creates a hermetic seal. Because sealant/underfill is not required for the solder-based fluidic I/Os, reworkability is possible. Also, the metal C4 I/Os have a much lower moisture absorption rate than polymer-based fluidic I/Os. Another important feature is that the fabrication of electrical and solder fluidic I/Os can be done simultaneously, and this process is compatible with existing C4 solder bumping technologies.

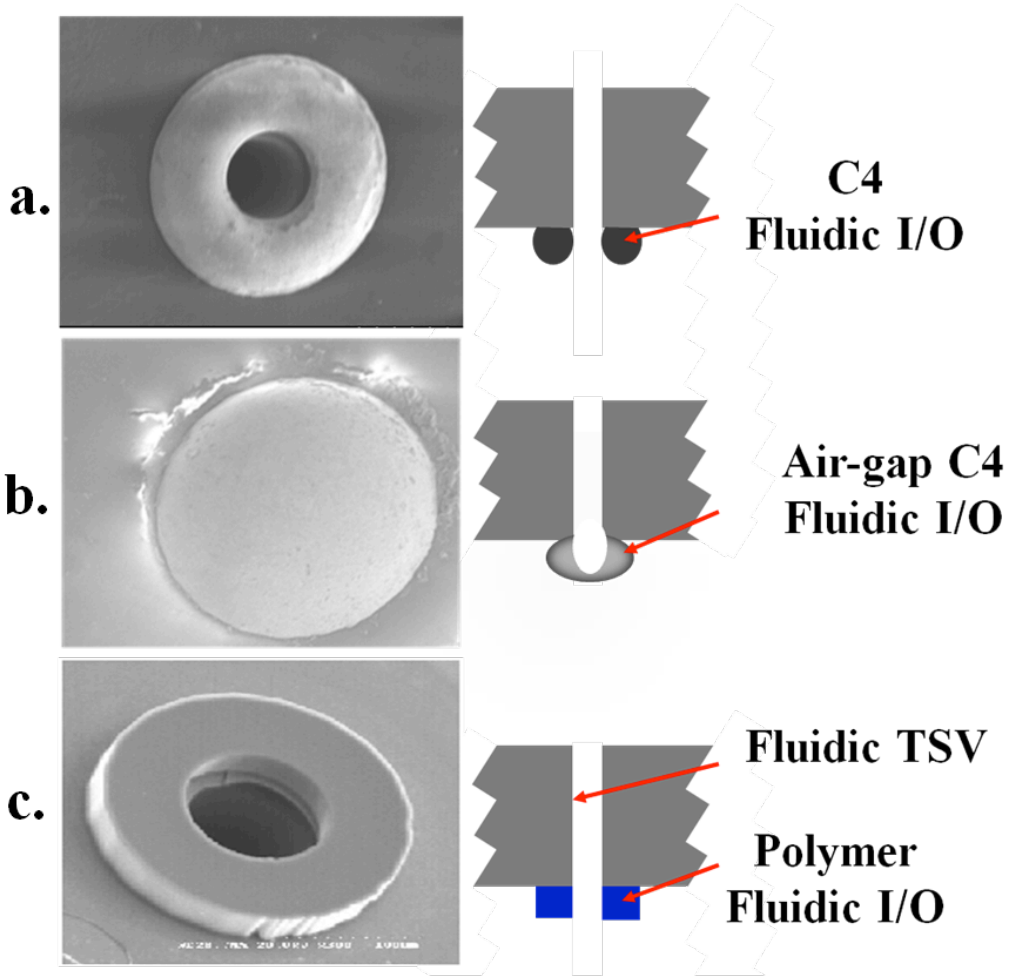
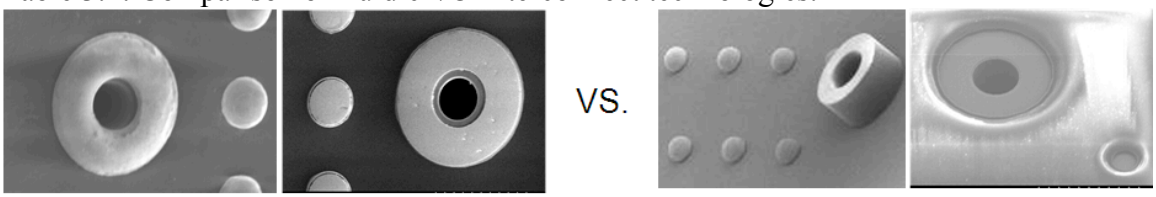


Figure 3.1: (a) C4 fluidic I/O, (b) air-gap C4 fluidic I/O, and (c) polymer pipe fluidic I/O.

An advantage of the polymer fluidic I/Os is the flexibility in height in which these I/Os can be fabricated. Polymer fluidic I/Os can be fabricated up to hundreds of microns in height. This I/O interconnect height flexibility could be useful when designing various 3D chip stack configurations. Table 3.1 summarizes the advantages and disadvantages of each I/O technology.

Table 3.1: Comparison of fluidic I/O Interconnect technologies.



Solder Pipe Cu Bonding Pad Polymer Pipe Polymer Socket

Solder Pipe		Polymer Pipe
No	Need for additional level of sealing (polymer socket)	Yes
No	Underfill needed	Yes
Yes	Reworkable	No
Yes	Simultaneous fabrication with electrical I/Os (fewer processing steps)	No
+ + +	Thermal conductivity; Thermal resistance	+
+ + +	Low Moisture Absorption	+
+	Flexibility of I/O height	+++

3.2. C4 Fluidic I/O Interconnects

Figure 3.2 outlines the steps necessary for fabrication of solder-based fluidic I/O interconnects. After sputtering a Ti/Cu/Ti seed layer (Figure 3.2a), photoresist is used to pattern an electroplating mold (Figure 3.2b). After electroplating a Ni under-bump metallization layer, solder is electroplated in the mold. After electroplating, the

photoresist is etched by solvent removal, the seed layer is removed by wet etching, and the solder is reflowed (Figure 3.2c).

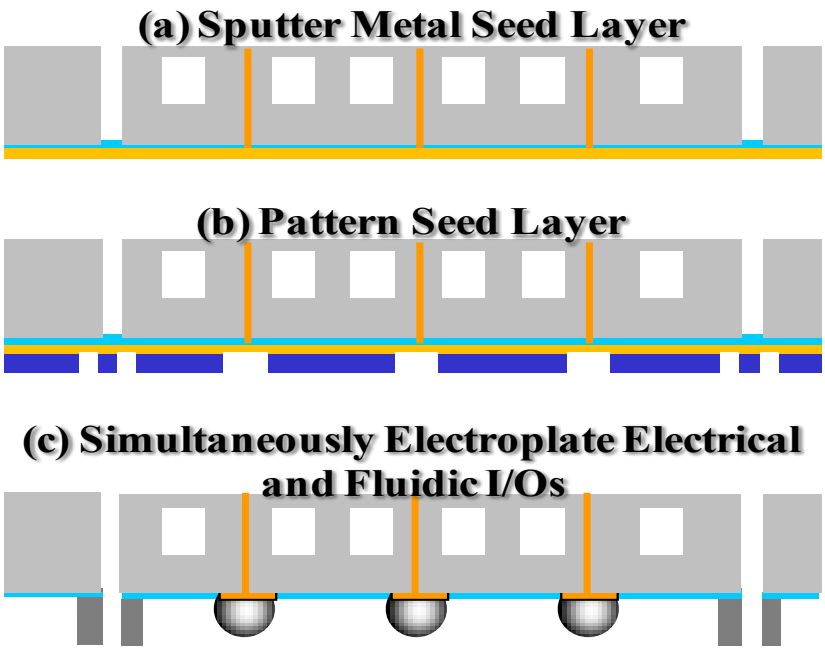


Figure 3.2: Schematic of C4 electrical and fluidic I/O fabrication.

Figures 3.3a and 3.3b show SEM images of 30µm solder fluidic I/Os before and after reflow. The inner-diameter of the I/Os is 120µm, and the outer-diameter is 340µm. Figure 3.4 shows optical images of the solder-based fluidic I/Os.

To measure feature uniformity, the height and inner diameter of fifteen random (~25µm tall before and ~35µm tall after reflow) I/Os were measured before and after reflow. The data measured for one sample reveals that the features are verified to have good uniformity. When measuring the C4 fluidic I/Os, it was observed that the standard deviation of the height and inner diameter of the features improves after reflow. The standard deviation of the height and inner diameter of the fluidic I/Os after reflow are found to be ~0.74µm and ~4.16µm respectively (Figures 3.5a and 3.5b). Furthermore, it

is also important to note that the average height of the C4 fluidic I/Os increased ~26% after reflow, and the inner diameter of the C4 fluidic I/Os increased ~33% after reflow.

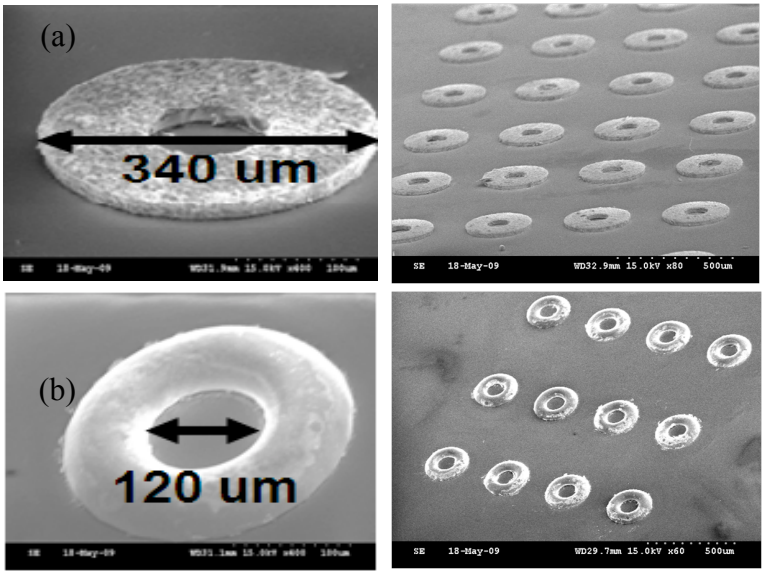


Figure 3.3: SEM images 30μm tall C4 fluidic I/Os (a.) before and (b) after reflow.

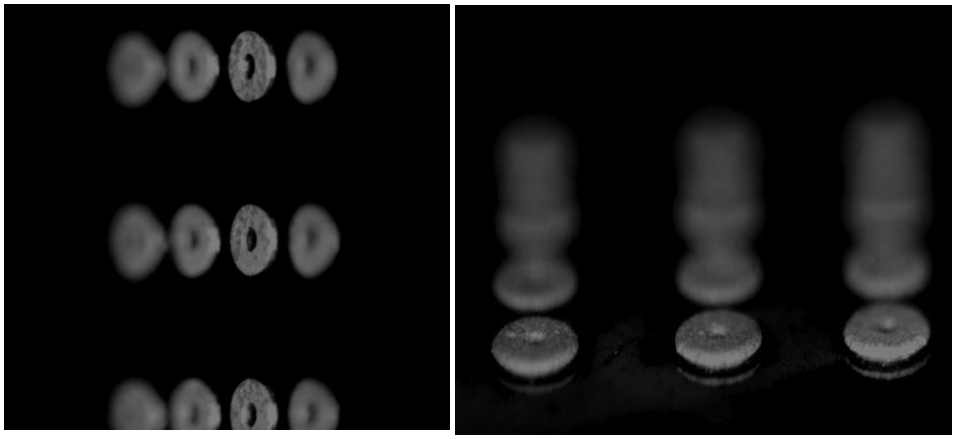


Figure 3.4: Optical images of C4 fluidic I/Os.

During the initial design of the fluidic I/Os, two shapes were considered – a circular shape (Figure 3.6a) and a square-like shape (Figure 3.6b). During electroplating, both of these feature shapes can be plated uniformly. However, the uniformity of the

features is best characterized after solder reflow. In the square-like I/O structure, the sides and the edge of the feature reflow to different heights (Table 3.2). Yet, the circular pipe-like structure has uniform height after reflow (Table 3.3).

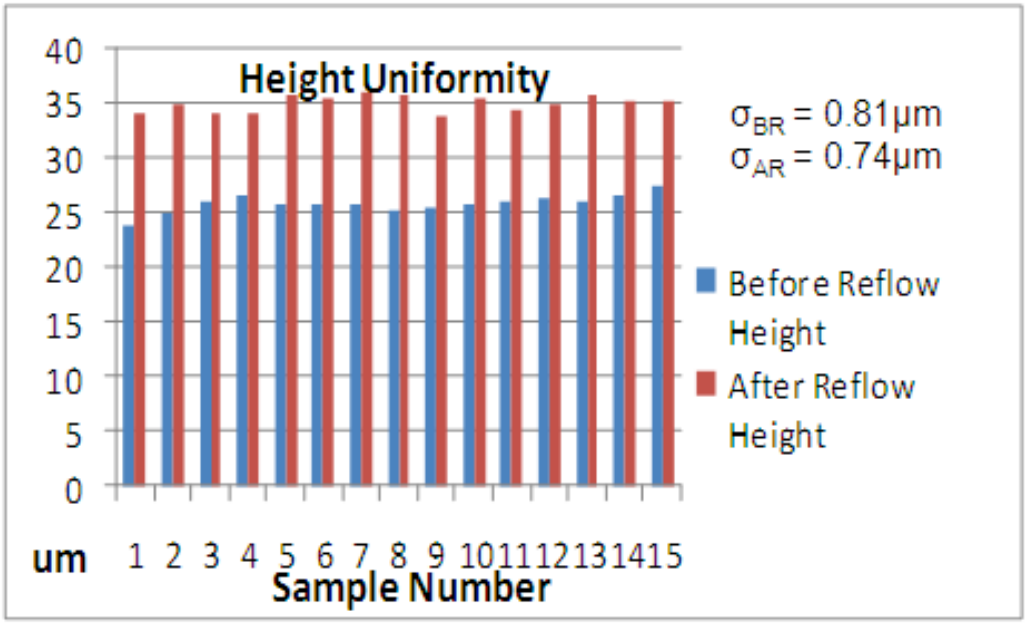


Figure 3.5a: C4 Fluidic I/O height uniformity before and after reflow.

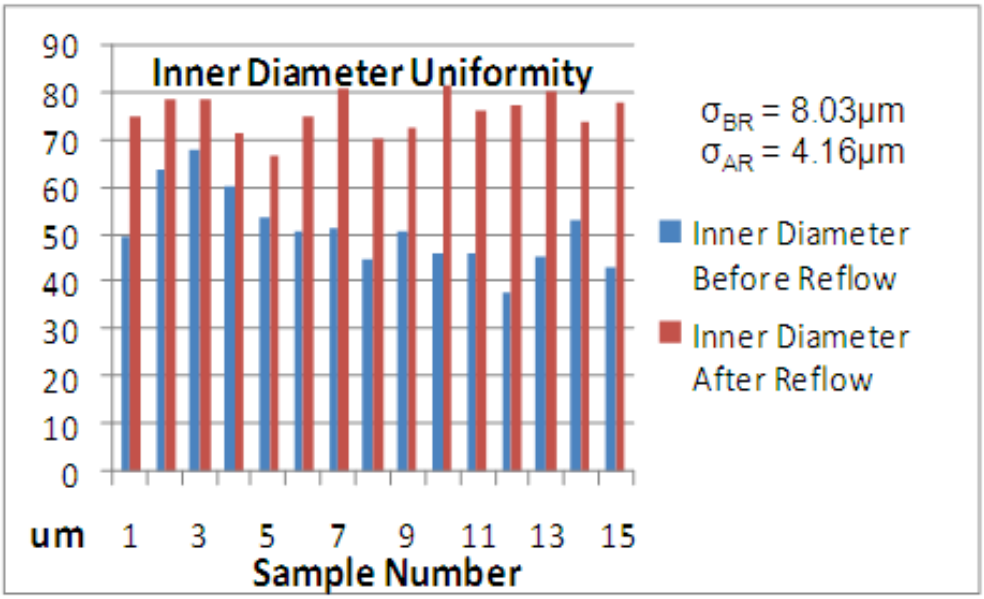


Figure 3.5b: C4 Fluidic I/O inner diameter uniformity before and after reflow.

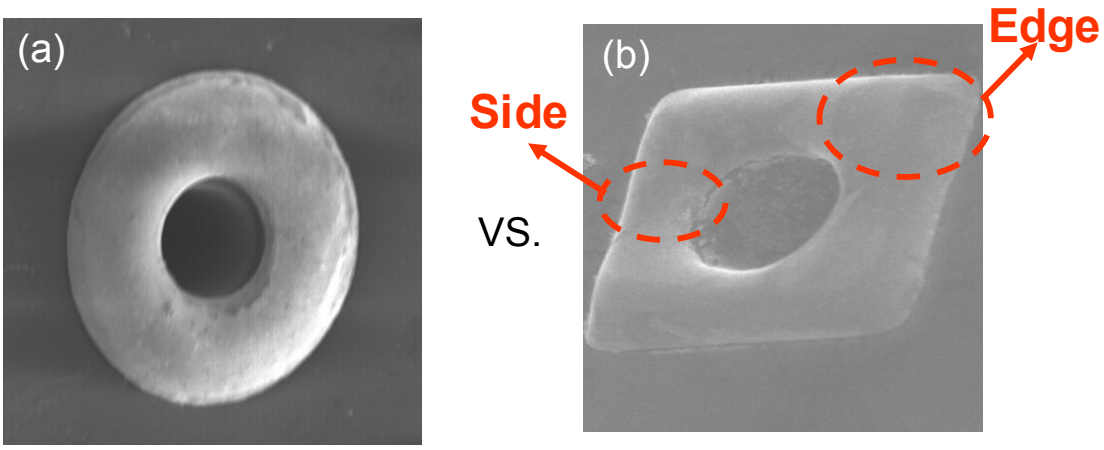


Figure 3.6 Feature Height Uniformity Shape Dependence – (a) circular solder fluidic I/O and (b) square-like solder fluidic I/O.

Table 3.2: Characterization of feature height of square-like fluidic I/O.

Height	Before Reflow	After Reflow
Side	33µm	37µm
Edge	34µm	46µm

Table 3.3: Characterization of feature height of circular fluidic I/O.

Height	Before	After
	33.5µm	45µm

3.3. Integrated C4 Electrical and Fluidic I/O Interconnects

When using the solder-based fluidic I/O technologies, electrical and fluidic I/Os can be fabricated using a single masking step. The fabrication process yields high density electrical I/Os (~1600/cm^2) which have a pitch of 240µm, although smaller pitches are possible. The adjacent fluidic I/Os have a pitch of 480µm (Figure 3.7). The fabrication of electrical and fluidic I/Os yields features with good uniformity and a

standard deviation in feature size of <1μm. Figures 3.8a and 3.8b show SEM images of integrated electrical and fluidic I/O interconnects before reflow and after reflow.

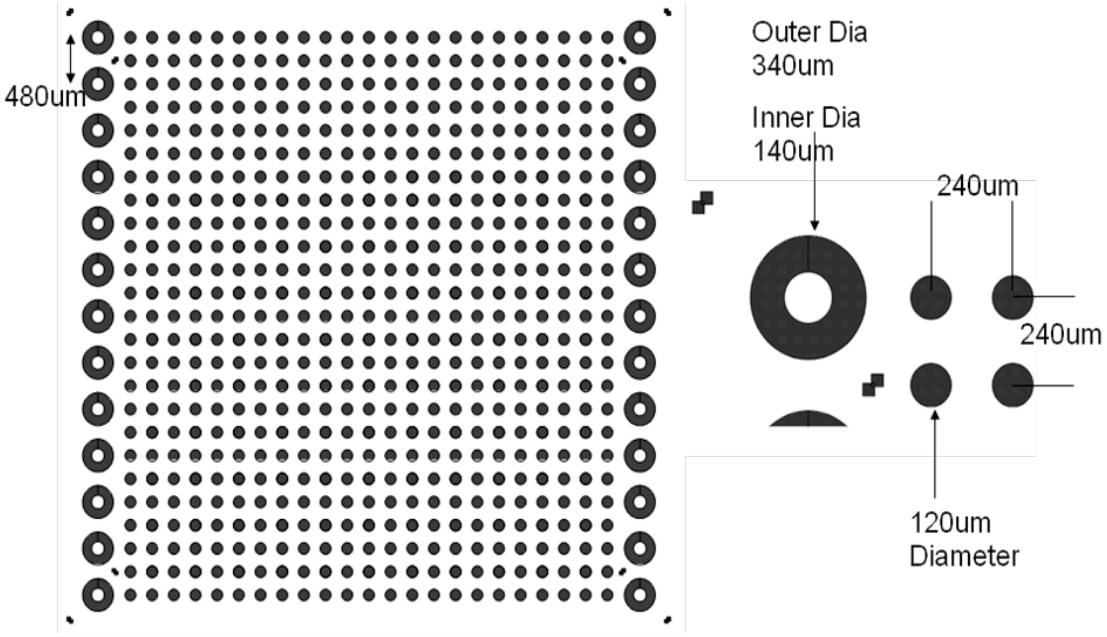


Figure 3.7: Schematic of the chip layout design for C4 electrical and fluidic I/Os.

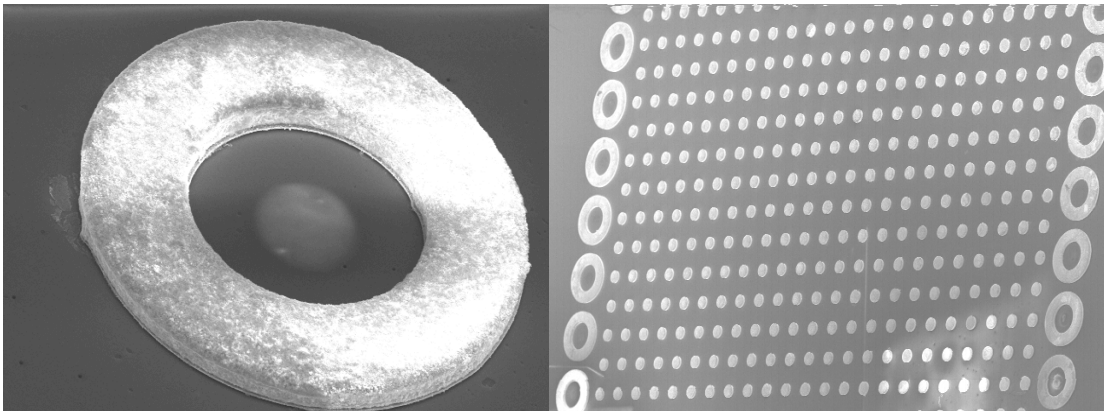


Figure 3.8a: SEM image of integrated C4 electrical and fluidic I/Os before reflow.

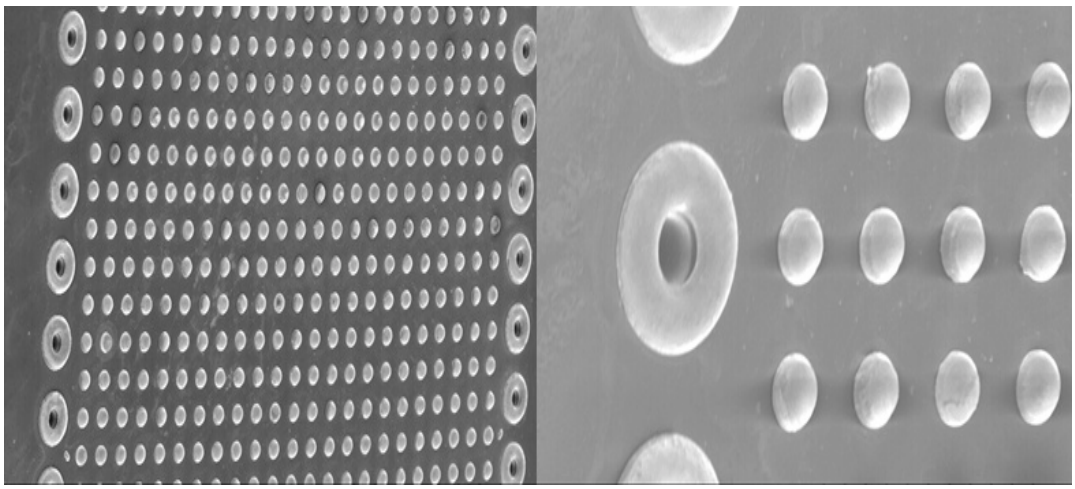


Figure 3.8b: SEM image of integrated C4 electrical and fluidic I/Os after reflow.

For ideal assembly conditions, it is preferred that the height of the solder bumps be slightly taller than the height of the solder pipes in order to ensure electrical connectivity during flip-chip assembly. Thus, ten different C4 bump-pipe feature size combinations were fabricated in order to achieve a feature size combine that resulted in a 2μm height difference between the solder bumps and the solder pipes.

Experimental results revealed that as the surface area of the solder bump and fluidic I/O become closer in value, the post-reflow feature height becomes almost equal in height. Furthermore, it is also important to note that the "solder pipe thickness" (ring thickness) is similar to the diameter of the solder bump for feature combinations that that have a similar post-reflow feature height. For example, for a 340μm outer diameter (140μm inner diameter) pipe, the pipe/ring thickness is 100μm. Similarly, the bump diameter is also 100μm. Table 3.4 outlines the bump-pipe feature sizes that yielded the best results for obtaining the desired C4 electrical and fluidic I/O post-reflow height.

Table 3.4: Feature sizes of various bump-pipe combinations before and after solder reflow.

Wafer 1	Before Reflow	After Reflow	σ
Bump	30μm	38.5μm	<1μm
Pipe	31.5μm	40.5μm	<1μm

Bump Dia	80μm
Pipe Dia	300μm
Fluidic TSV Dia	100μm

Wafer 2	Before Reflow	After Reflow	σ
Bump	32μm	43μm	<1μm
Pipe	33.5μm	45μm	<1μm

Bump Dia	100μm
Pipe Dia	340μm
Fluidic TSV Dia	100μm

Wafer 3	Before Reflow	After Reflow	σ
Bump	34μm	47.5μm	<1μm
Pipe	36μm	45.5μm	<1μm

Bump Dia	120μm
Pipe Dia	340μm
Fluidic TSV Dia	100μm

3.3.1. Integrated C4 Electrical and Rectangular Fluidic I/O Interconnects

A rectangular fluidic I/O design was also considered. This fluidic I/O design requires the fabrication of a single square-like fluidic via and fluidic I/O on each side of the chip. Figure 3.9 shows SEM images of integrated C4 electrical and rectangular fluidic I/Os.

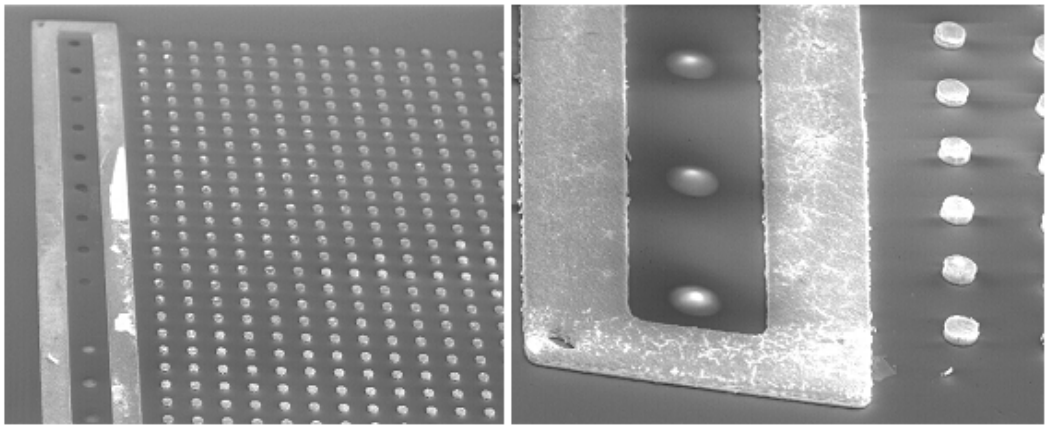


Figure 3.9: SEM images of integrated C4 electrical and rectangular C4 fluidic I/Os.

An advantage of using the rectangular fluidic I/O design is that the pressure drop across the microfluidic system is decreased, as the cross sectional area of the opening for a singular rectangular fluidic I/O is much larger than the area of the smaller individual circular fluidic I/Os. However, a very important advantage of using the circular C4 fluidic I/O is that the circular fluidic I/Os require less silicon area. Additionally, using individual circular I/Os instead of a single fluidic I/O that spans almost the entire length of the chip uses less silicon area near the edges of the chip that may be required for the fan out of signal interconnects from the electrical I/Os.

Table 3.5 outlines a summary of the equations that can be used to calculate the pressure drop and silicon area occupied for each fluidic I/O design [2.8,3.3]. A comparison of the pressure drop of each fluidic I/O design is summarized in Table 3.6, and the silicon area occupied by each fluidic I/O design is summarized in Table 3.7.

The pressure drop and silicon area calculations for the circular fluidic I/Os include the following assumptions: chip area is 1cm x 1cm, number of fluidic I/Os and fluidic vias = 17, fluidic via and fluidic I/O diameter = 100um, height of fluidic via = 400um, height of fluidic I/O = 50um. The pressure drop of a rectangular fluidic I/O can be calculated by using the equation in Table 3.5 Figure 2.14. The pressure drop and silicon area calculations for the rectangular fluidic I/Os include the following assumptions: chip area is 1cm x 1cm, number of fluidic I/Os and fluidic vias = 2, fluidic via and fluidic I/O width = 100um, height of fluidic via = 400um, height of fluidic I/O = 50um.

Analysis shows that, for a $1cm^2$ chip, the pressure drop when using 26 circular fluidc I/Os is ~3.4kPa compared to a pressure drop of only 0.42kPa when using the 2 rectangular fluidic I/Os. However, although the rectangular fluidic I/Os result in a lower

pressure drop, the rectangular fluidic I/Os occupy 70% more silicon area than the circular fluidic I/Os. Consequently, the tradeoff of pressure drop and silicon area must be considered when deciding which fluidic I/O design to implement.

Table 3.5: Hydro-dynamic equations for calculating pressure drop in fluidic I/Os [2.8, 3.2].

Equations	Symbol Legend
$\Delta P_{via+micropipe} = 512 \cdot \frac{\mu \cdot V \cdot (2H_{via} + 2H_{pipe})}{n_{via} \cdot \pi \cdot D_{via}^4}$	D_{via} = fluidic via diameter
$\Delta P_{via+squareIO} = \frac{1}{2} f \cdot \mathrm{Re} \cdot L_{SqIO} \cdot \frac{\mu \cdot V (1 + W_{SqIO} / H_{SqIO})^2}{n_{via} \cdot H_{SqIO} \cdot W_{SqIO}^3}$	$\Delta P_{via+squareIO}$ = pressure drop in circular fluidic I/Os and fluidic vias
$H_{SqIO} = H_{via} + H_{SqIO}$	$\Delta P_{via+micropipe}$ = pressure drop in rectangular fluidic I/Os and fluidic vias
$\frac{Silicon \quad area \quad for \quad fluidic \quad IOs}{Chip \quad area} = \%$ *area occupied by fluidic IOs*	f = friction coefficient
	Re = Reynolds number
	V = flow rate
	n_{vias} = number of fluidic vias
	μ = fluid kinematic viscosity
	H = height
	L = length
	W = width

Table 3.6: Summary of pressure drop calculations for fluidic I/O designs.

Fluidic I/O Design	Number of Fludic Vias per Chip	Number of Fludic I/Os Per Chip	Fluidic I/O Height (µm)	Fluidic I/O Width (inner) (µm)	Fluidic I/O Length (cm)	Fluidic I/O Diameter (µm)	Wafer Thickness (µm)	Pressure Drop (kPa)
Circular	34	34	50	n/a	n/a	100	400	3.4
Rectangular	2	2	50	100	1	n/a	400	0.42

Table 3.7: Summary of chip area occupied by fluidic I/Os.

Fluidic I/O Design	Number of Fludic Vias per Chip	Number of Fludic I/Os Per Chip	Fluidic I/O Width (outer) (µm)	Fluidic I/O Length (cm)	Fluidic I/O Outer Diameter (µm)	Area (cm^2)	% Chip Area Occupied
Circular	34	34	n/a	n/a	340	0.03	~ 3%
Rectangular	2	2	500	1	n/a	0.1	~ 10%

3.4 Air-gap C4 Fluidic I/O Interconnects

Air-gap C4 I/Os can be fabricated in a similar manner as the circular C4 fluidic I/Os in the previous section. The air-gap fluidic I/Os were made by electroplating solder in the fluidic I/O mold to be ~twice the height of the mold. So, for a 25µm tall mold, it would be necessary to electroplate ~50µm of solder to achieve an air-gap in the structure.

To fabricate a taller structure, 50µm of solder was electroplated in a 25µm photoresist electroplating mold. As the height of the electroplating mold was 25µm, the solder was over-plated by a height of 25µm to form a 50µm tall solder pipe I/O structure. Additionally, when over-plating solder (i.e., height of plated solder is greater than the height of the resist mold), the inner diameter of the electroplated structures decreases to ~25µm (Figure 3.10a). After reflow, because of the decreased inner-diameter of the structure, the solder at the top of the structure merges (Figure 3.10b). Although, these

reflowed fluidic I/Os appear to look like solder bumps, the domed structures actually have an air-filled depression in the middle of the structure.

This air-filled depression occurs because when solder begins to electroplate over the height of the photoresist electroplating mold, the over-plated solder decreases the C4 fluidic I/O inner diameter only at the top of the electroplated fluidic I/O. The inner diameter on the bottom half of the air-gap C4 fluidic I/O cannot become smaller prior to reflow because the solder at the bottom half of the fluidic I/O is still separated by photoresist mold. After the photoresist is removed and when reflow occurs, the solder merges only at the top of the fluidic I/O, where the inner diameter of the pipe structure has become smaller.

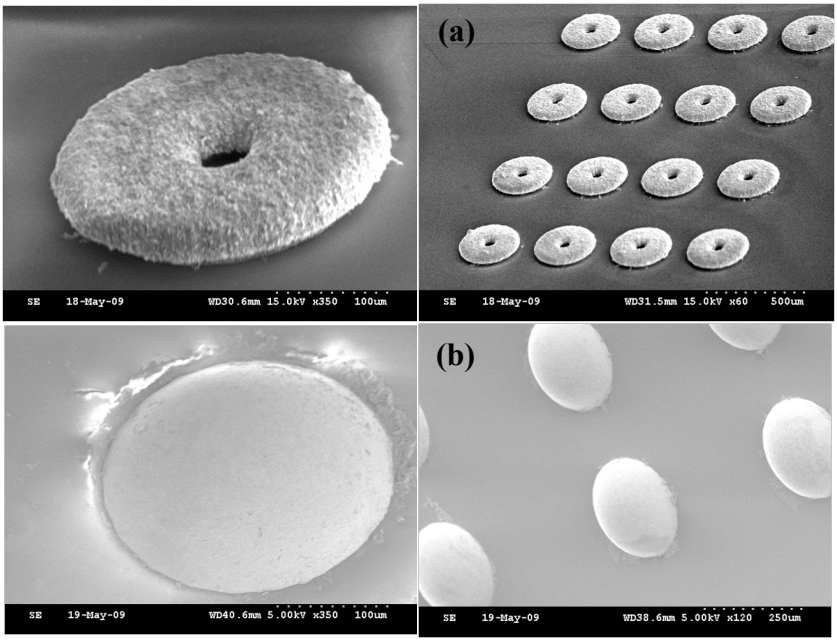


Figure 3.10: 50μm tall, over-plated air-gap C4 fluidic I/Os (a) before and (b) after reflow.

The air void is verified by the x-ray image of the structure taken after reflow (Figure 3.11). All visually inspected bumps contained the air-gap. One key advantage to

the air-gap fluidic I/O technology is that it is transparent to the flip-chip assembly process. Furthermore, the air-gap C4 technology enables the ability to use no-flow underfill in applications for which it is required.

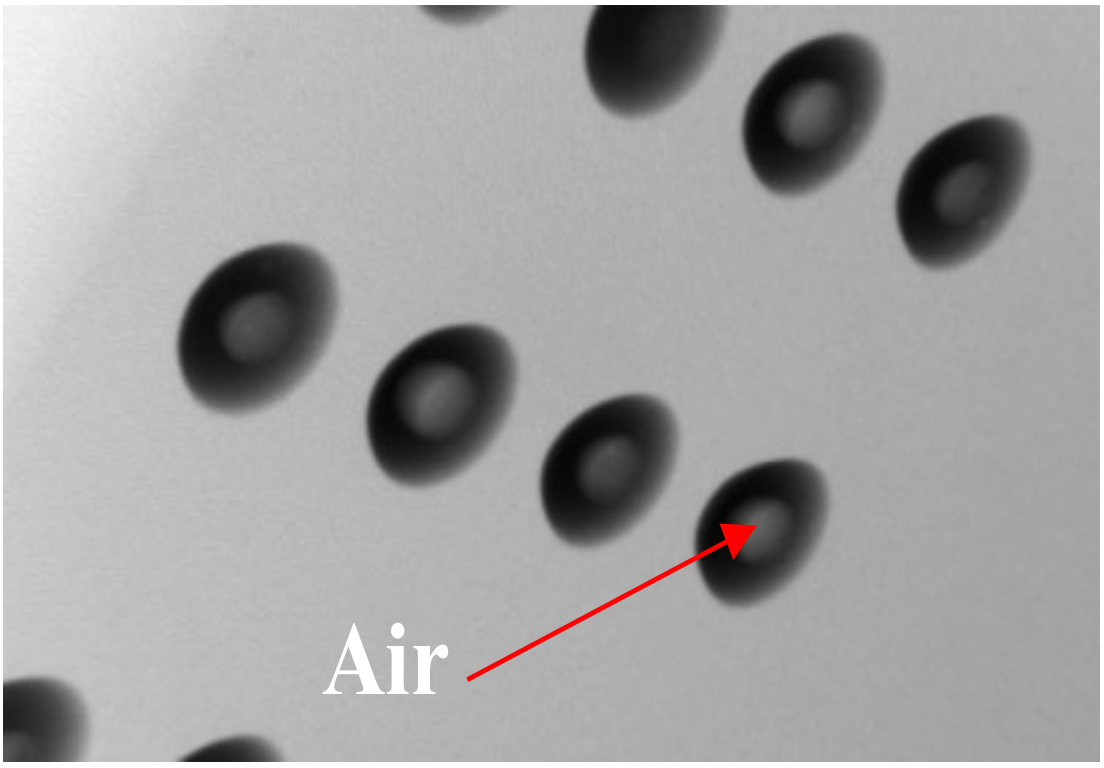


Figure 3.11: X-ray image of air-gap C4 fluidic I/Os after solder reflow.

3.5. Integrated Polymer Sockets, Fluidic TSVs, Electrical I/Os , and Polymer Pipe Fluidic I/Os

An alternative fluidic sealing approach can be implemented using polymer fluidic I/Os. Figure 3.12 shows a schematic of the fabrication process flow for a silicon die with integrated polymer sockets, through-wafer fluidic interconnects, thermofluidic I/O interconnects, and electrical I/O interconnects. The process begins by sputtering a

300/10000/300Å titanium/ copper/titanium (Ti/Cu/Ti) metal layer, where Ti serves as an adhesion promoter between Cu and silicon (Figure 3.12a). The metal is patterned using a wet etch process (Figure 3.12b). Next, 1μm of oxide is deposited on the back side of the wafer as a polymer adhesion layer (Figure 3.12c), and 3μm of oxide is deposited on the front side as a through-silicon via etch-stop layer (Figure 3.12d). Next, 15μm of Avatrel 2090P polymer is spin coated onto the wafer (Figure 3.12e). Afterwards, polymer sockets are patterned on top of the metal (Figure 3.12f, Figure 3.13). The first layer of Ti is removed using a wet-etching process. Through-wafer fluidic vias are patterned and anisotropically etched into the back side of the silicon wafer in an ICP etching tool (Figure 3.12g, Figure 3.14); the etching stops at the etch-stop layer on the front side of the wafer. Next, a 12μm layer of Avatrel polymer is spin coated and patterned on the front side of the wafer and used as a passivation layer (Figure 3.12h). After sputtering a 300/2000/300Å Ti/Cu/Ti seed layer and electroplating a 2μm nickel under-bump metallurgy layer, 50μm C4 solder bumps are electroplated for area-array electrical interconnects (Figure 3.12i, Figure 3.15). Afterwards, a 60μm layer of Avatrel polymer is spin coated onto the front side of the wafer and used to pattern polymer pipes, which serve as thermofluidic I/O interconnects (Figure 3.12j, Figure 3.16). Finally, the oxide layer covering the through-wafer fluidic vias on the front side of the wafer is removed using a wet etch process to allow fluidic circulation.

As outlined in Table 3.3, an advantage of the polymer based fluidic I/Os is the flexibility in height in which these I/Os can be fabricated. Polymer-based I/Os can be fabricated up to hundreds of microns in height. This I/O interconnect height flexibility could be useful if one were to design a processor memory chip stack in which fluidic I/Os

were needed to route liquid to high-performance processor chips separated by memory chips in the 3D chip stack. The ability to fabricate longer I/Os would enable routing of liquid over longer distances in a multi-chip 3D stack, as shown in Figure 3.17.

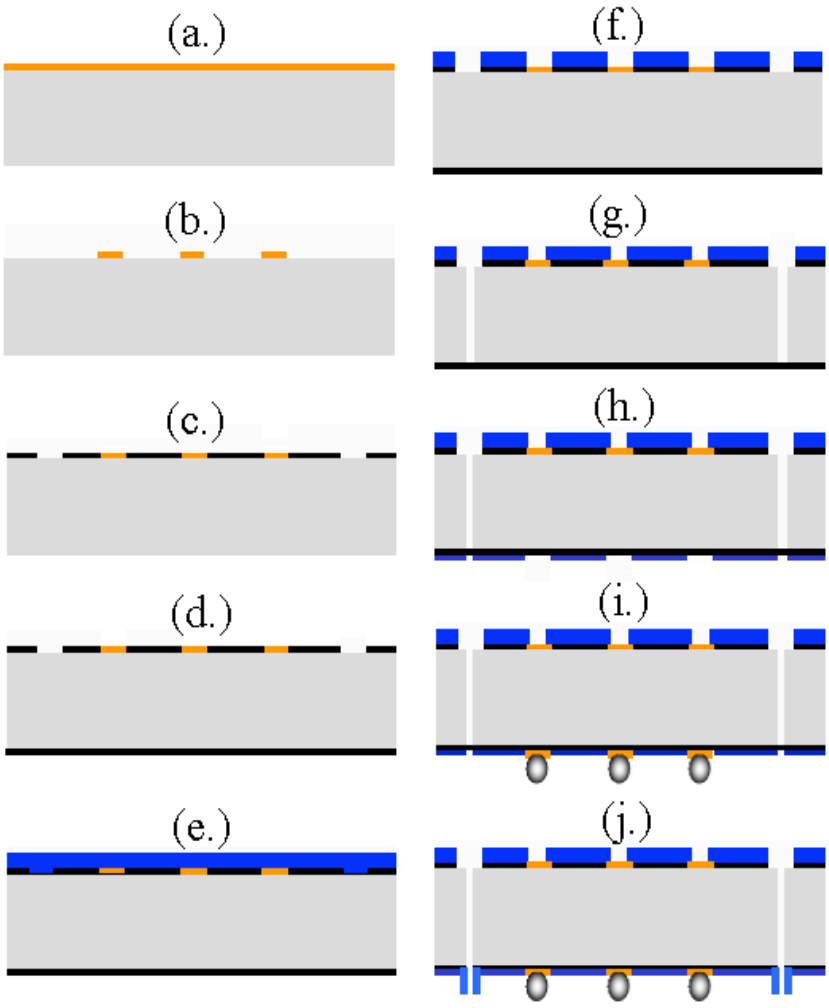


Figure 3.12: Schematic of wafer-level integration of polymer sockets, electrical I/O and fluidic I/O interconnects for a 3D flip-chip package.

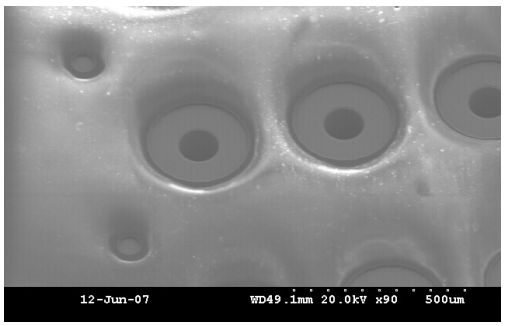


Figure 3.13: SEM image of 15µm tall, 270µm and 60µm diameter polymer sockets.

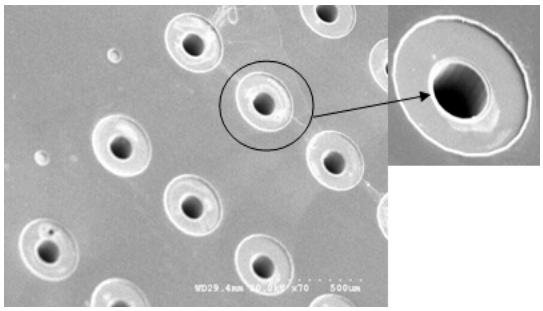


Figure 3.14: SEM image of 100µm diameter through-wafer fluidic interconnects.

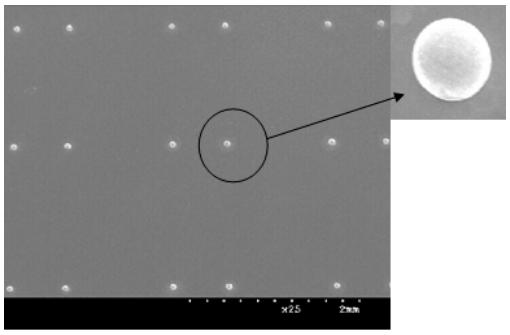


Figure 3.15: SEM image of 50µm tall solder bumps used as electrical I/O interconnects.

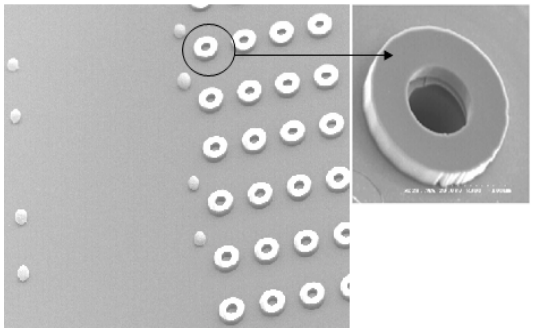


Figure 3.16: SEM image of 60µm tall polymer pipes used as I/O fluidic interconnects.

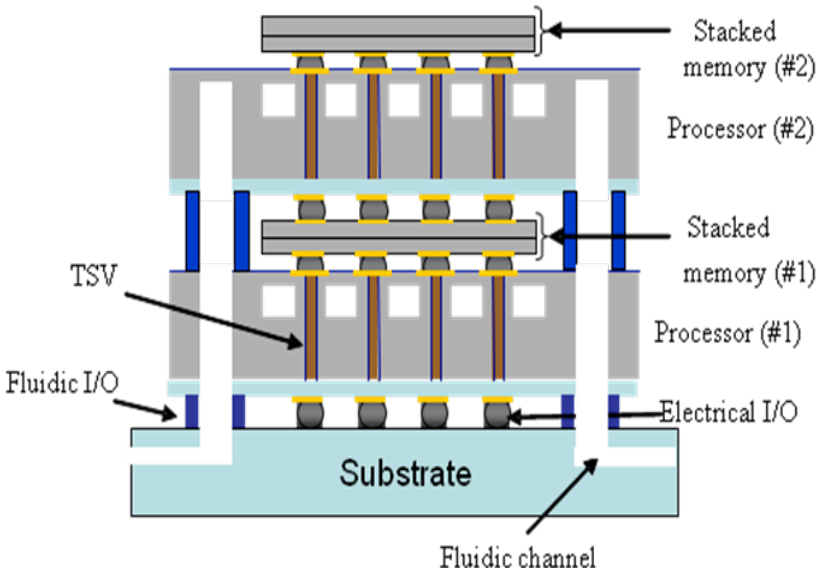


Figure 3.17: Schematic illustrating how polymer fluidic I/Os can be used to route liquid over longer distances in the 3D chip stack [3.3].

3.6. Summary

Chapter 3 describes the fabrication and process integration techniques for three distinct fluidic I/O technologies including a C4 pipe fluidic I/O, an air-gap C4 fluidic I/O, and a polymer pipe fluidic I/O interconnect technology. An electrical I/O density of ~1600/cm^2 is demonstrated. The advantages and disadvantages of the three fluidic I/O technologies are discussed.

CHAPTER 4

3D CHIP ASSEMBLY USING ELECTRICAL AND FLUIDIC I/O INTERCONNECTS

4.1 3D Chip Stacking Using Electrical and Fluidic I/O Interconnects

A challenge in such a 3D configuration, as shown in Figure 2.2, is the flip-chip bonding process, especially since one must be able to provide fluidic sealing to prevent leakage in the 3D chip stack. Because there are three distinct fluidic I/O technologies, different 3D stacking and assembly methods are required for the assembling microfluidic chips in the 3D chip stack, depending on which fluidic I/O technology is implemented. This section discusses the flip-chip bonding processes that enable assembly of the microfluidic chips in the liquid-cooled 3D chip stack.

4.2 Assembly of C4 Electrical and C4 Fluidic I/Os

After fabrication of the electrical and fluidic I/O interconnections, as shown in Figure 2.3, the solder-based electrical and fluidic I/Os can be simultaneously aligned and assembled to a substrate which has patterned copper pads and copper rings. The solder bumps (electrical I/Os) are assembled to the copper pads, and the solder pipes (fluidic I/Os) are assembled to the copper rings, as shown in Figure 4.1.

The copper pads and copper rings on the substrate have slightly larger features sizes than the C4 electrical and fluidic I/Os on the chip (Figure 4.1). After copper is deposited on the substrate, the copper pads and rings can be patterned by silicon dioxide

or polymer, which is needed to contain the solder during assembly, as shown in Figure 4.2. Patterning the copper rings with a polymer layer of an appropriate thickness can provide an additional level of fluidic sealing. SEM images of the copper pads and copper rings on the substrate are shown in Figure 4.3.

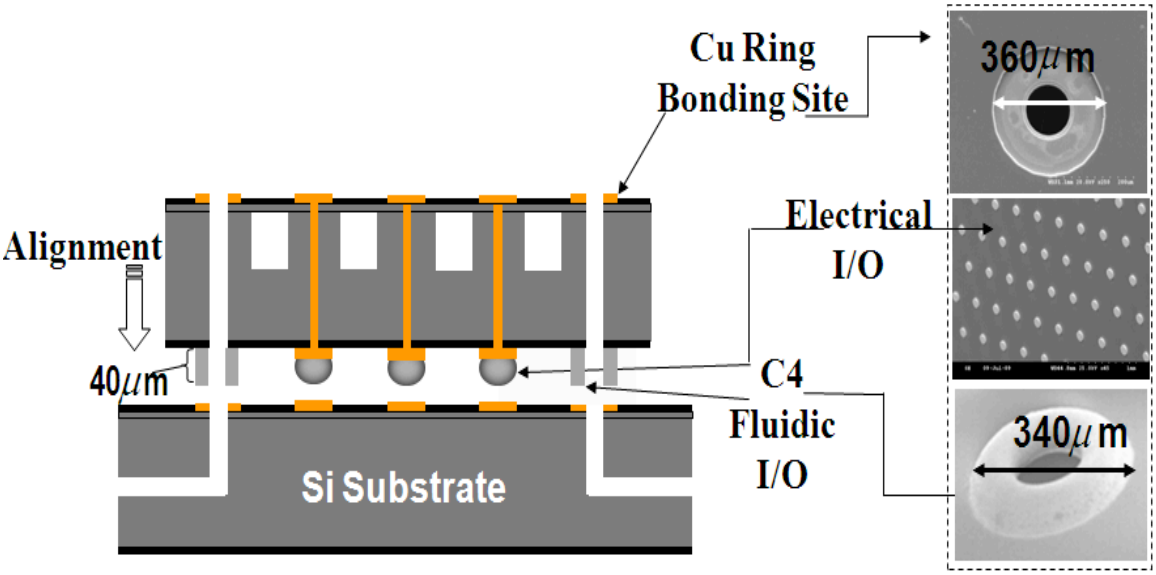


Figure 4.1: Characterization and assembly of C4 fluidic I/Os.

When the C4 fluidic I/Os are assembled to the substrate, the solder only wets the patterned copper on the substrate. The C4 electrical and fluidic I/Os and the copper pads and rings on the substrate are simultaneously aligned and brought in to contact with an appropriate force and temperature. Subsequently, an electrical and mechanical connection is formed between the solder bumps and copper pads, and a hermetically sealed fluidic pathway is created when the solder pipes are bonded to the corresponding copper pads on the substrate (Figure 4.2).

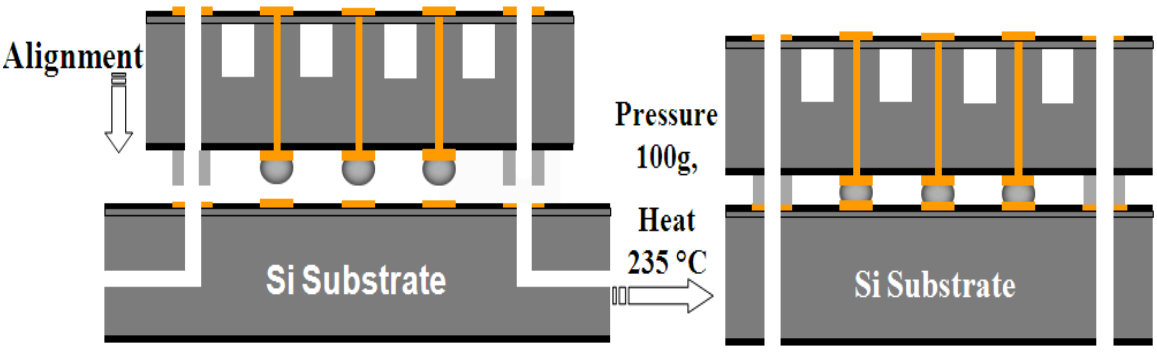


Figure 4.2: Schematic of assembly of C4 electrical and fluidic I/Os.

For ideal assembly conditions, it is preferred that the height of the electrical I/Os be slightly taller than the height of the fluidic I/Os in order to ensure electrical connectivity. Thus, various solder bump diameters were fabricated in order to achieve a 2μm height difference between the solder bumps and the solder pipes. Table 4.1 outlines the feature heights that were fabricated when producing the subsequent assembly results.

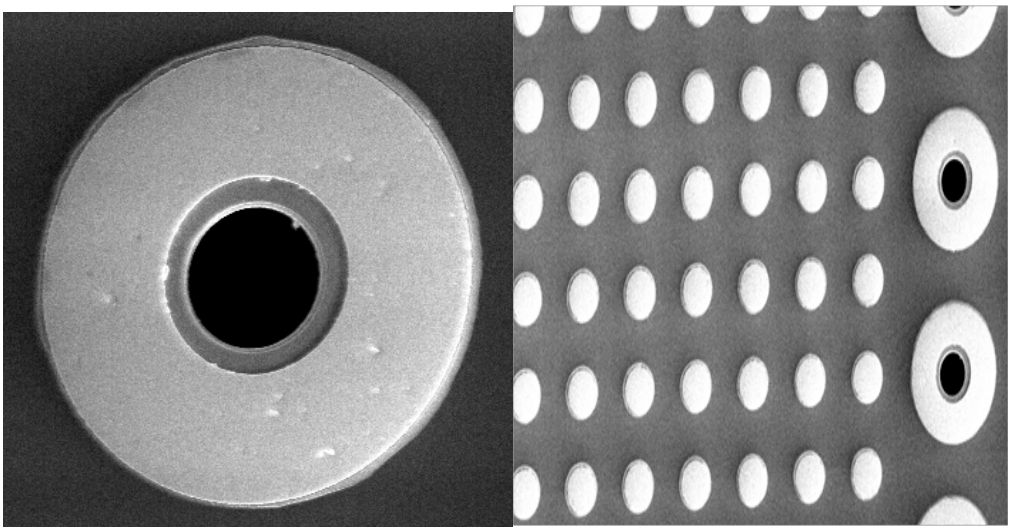


Figure 4.3: SEM image of substrate with patterned copper rings (360μm outer diameter) and integrated fluidic TSVs (left) and an SEM image integrated copper pads and copper rings.

Height	Before	After
Bump	34µm	47.5µm
Pipe	36µm	45.5µm

Table 4.1: Before and after reflow feature height parameters for assembly.

A Finetech Fineplacer Lambda flip-chip bonder was used to perform assembly of the 3D chip stack. Figure 4.4 shows a photograph of the Finetech Fineplacer Lambda flip-chip bonder, which has an alignment accuracy of 0.5µm.

Figure 4.4: Photograph of Finetech Fineplacer Lambda flip-chip bonder.

The process used for assembly is summarized in Table 4.2, and the bonding temperature profile used for assembly is shown by the reflow profile image that is generated by the Finetech bonding during assembly (Figure 4.5). After pre-heating the die and the substrate to temperatures of 60°C and 40°C, respectively, the two are brought into contact with a compression force of 100g. Subsequently, the temperature of the chip

and the substrate are elevated to 235°C and 140°C, respectively. The 340μm diameter air-gap C4 fluidic I/Os are aligned to the 360μm diameter copper rings on the substrate (Figure 4.3).

Table 4.2 Bonding process parameters.

Assembly Parameters and Sequence of Steps	Value
Pre-heating Temperature of Substrate	40°C
Pre-heating Temperature of Die 1	60°C
Compression Force	100g
Bonding Temperature of Substrate	140°C
Bonding Temperature of Die 1	235°C

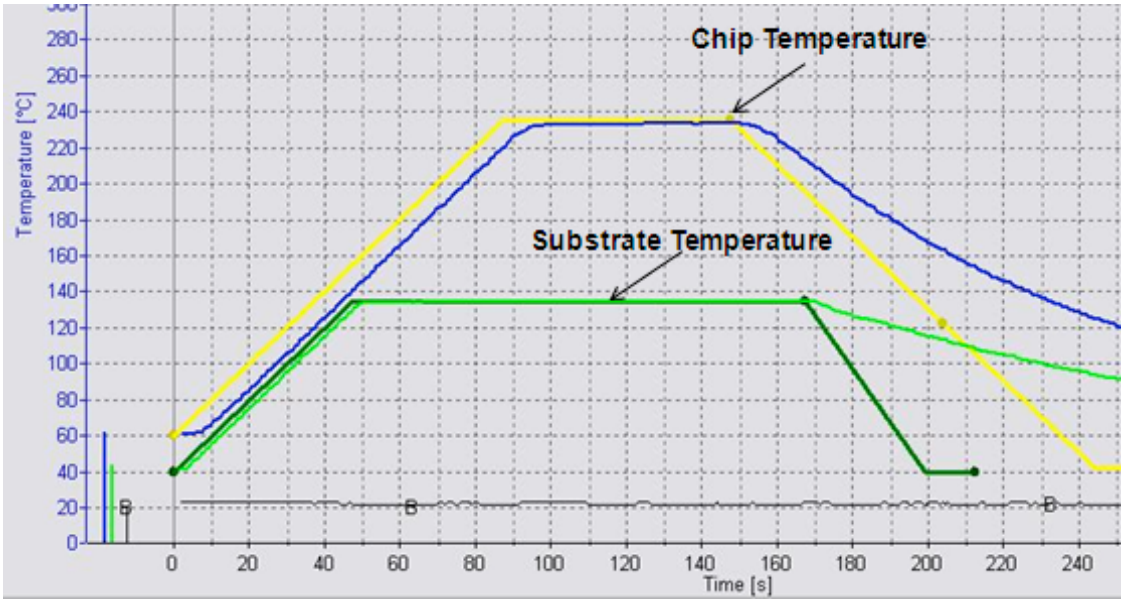


Figure 4.5: Bonding process parameters.

4.3 Assembly of C4 Electrical I/Os and Air-gap C4 Fluidic I/Os

The assembly process for C4 electrical I/Os and air-gap C4 fluidic I/Os is similar to flip-chip bonding process shown in the previous section. When the air-gap C4 fluidic

I/Os are assembled to the substrate, the solder only wets the patterned copper on the substrate. Thus, the assembly of the air-gap C4 fluidic I/Os to the copper rings on the substrate enables the air-filled solder bump-like structures to be shaped into solder pipe-like fluidic I/O interconnects. The assembly process is similar for the C4 fluidic I/Os. However, since the fluidic pipe structures are already formed, the hermetically sealed fluidic pathway is created when the solder pipe is bonded to the copper pads, as shown in Figure 4.6 and Figure 4.7.

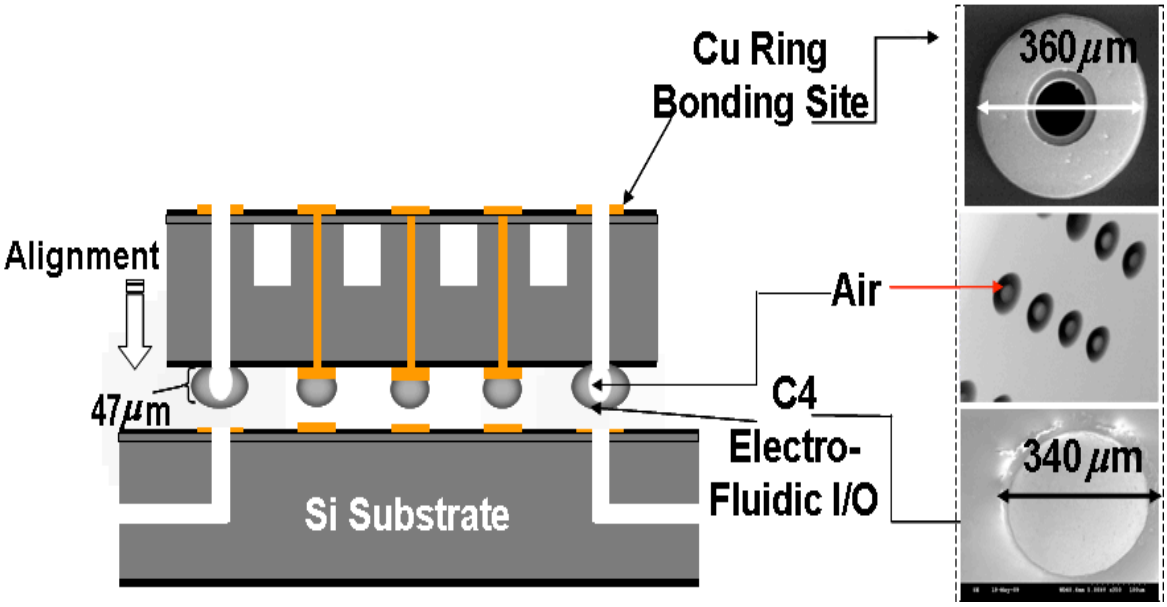


Figure 4.6: Characterization and assembly of air-gap C4 fluidic I/Os.

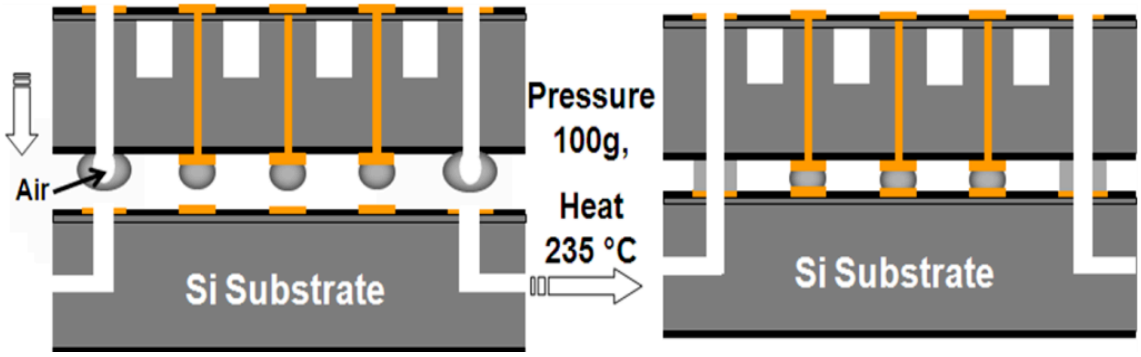


Figure 4.7: 3D assembly using air-gap C4 fluidic I/Os and electrical I/Os.

For the air-gap C4 fluidic I/O, the formation of the C4 fluidic pipe structure is verified by x-ray images taken of the I/Os after assembly (Figure 4.8, Figure 4.9). Figure 4.10 shows a SEM image of a 2-chip stack of microfluidic chips with C4 electrical and fluidic I/Os after assembly.

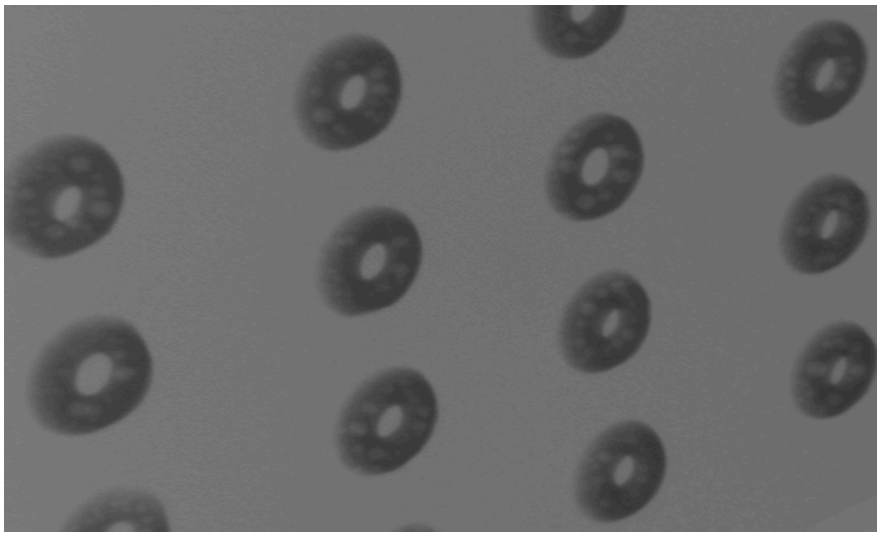


Figure 4.8: X-ray image of air-gap C4 fluidic I/Os after assembly.

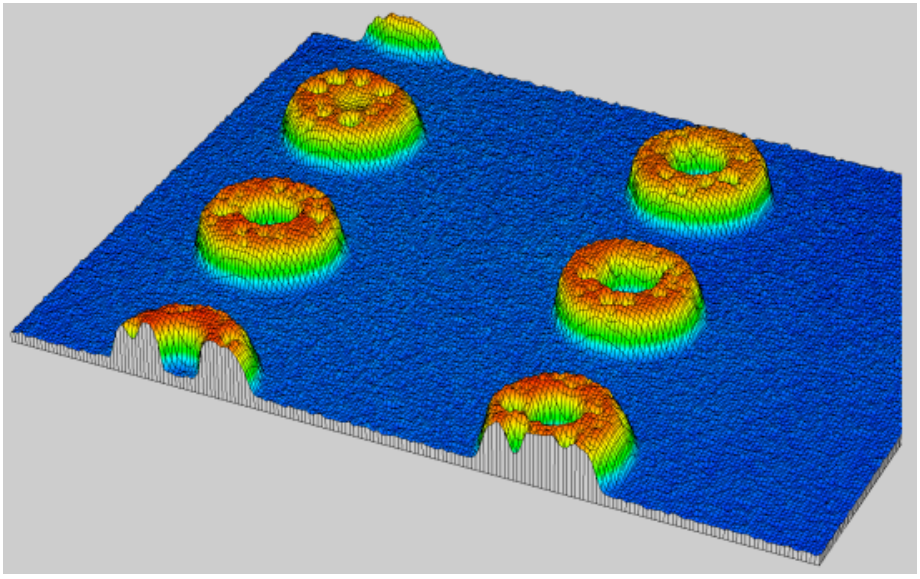


Figure 4.9: X-ray image of air-gap C4 fluidic I/Os after assembly.

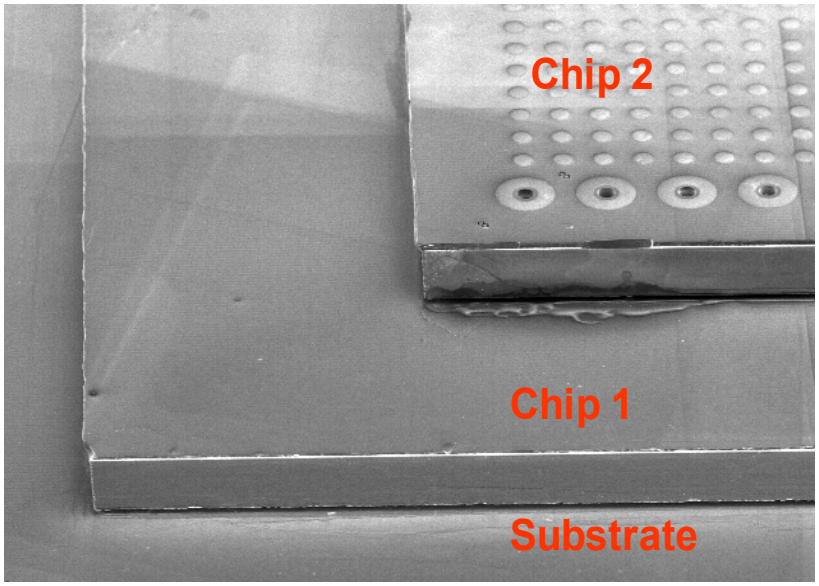


Figure 4.10: SEM image of a 3D chip stack assembled using C4 fluidic and electrical I/Os.

It is important to note the significance of optimizing the appropriate bonding force and having a sufficiently large C4 fluidic I/O inner diameter, which must be larger than the diameter of the fluidic TSV. Experimental results revealed that, for chips that contained 100µm diameter fluidic TSVs, fluidic TSV clogging was observed when the inner diameter of the C4 fluidic I/Os were fabricated to be less than 130µm. Furthermore, for a chip with an area of 0.7cm x 0.7cm, some fluidic I/O bonding sites across the chip were observed to have fluidic TSV clogging when flip-chip assembly was performed at a bonding force over 100g. Figure 4.11 shows a cross-sectional optical image of an assembled 3D chip stack where solder from the fluidic I/Os is clogging fluidic vias in the chip stack. Figure 4.12 shows a cross-sectional optical image of a 3D chip stack assembled using C4 fluidic and electrical I/Os. An optimal amount of bonding force and an appropriate amount of fluidic TSV clearance were used to prevent fluidic

TSV clogging, and a clear fluidic pathway is created for facilitating fluid flow to each layer in the 3D chip stack.

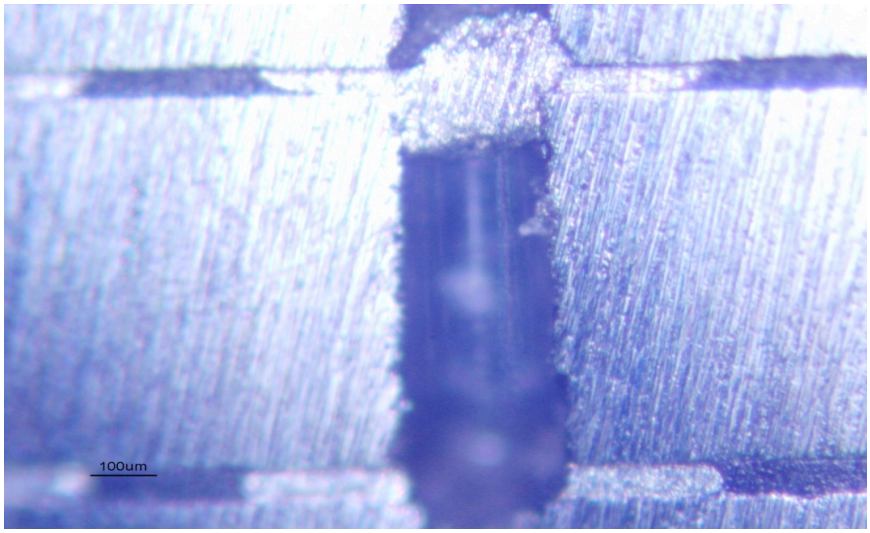


Figure 4.11: Optical image showing fluidic TSV clogged with solder.

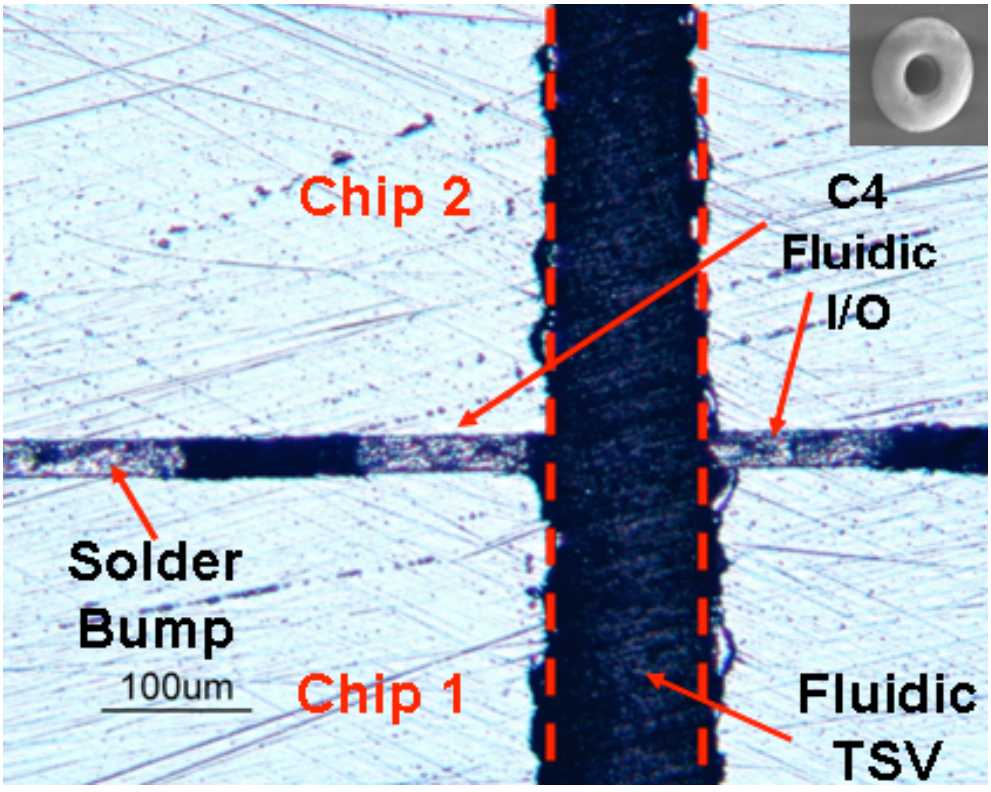


Figure 4.12: Cross-sectional optical image of a 3D chip stack assembled using C4 fluidic and electrical I/Os.

As discussed in Chapter 3, a rectangular fluidic I/O configuration can be used to reduce the pressure drop associated with the chip fluidic I/Os. The same flip-chip assembly recipes and principles used for assembly of the C4 electrical and fluidic I/Os can be applied to performing assembly of C4 electrical I/Os and C4 rectangular fluidic I/Os. Figure 4.13a presents a SEM image of integrated C4 electrical and rectangular fluidic I/Os, and Figure 4.13b shows an optical image of the corresponding copper pads that are fabricated on the substrate to facilitate assembly. Figure 4.14 shows x-ray images of successful 3D chip stacking using C4 electrical and rectangular fluidic I/Os.

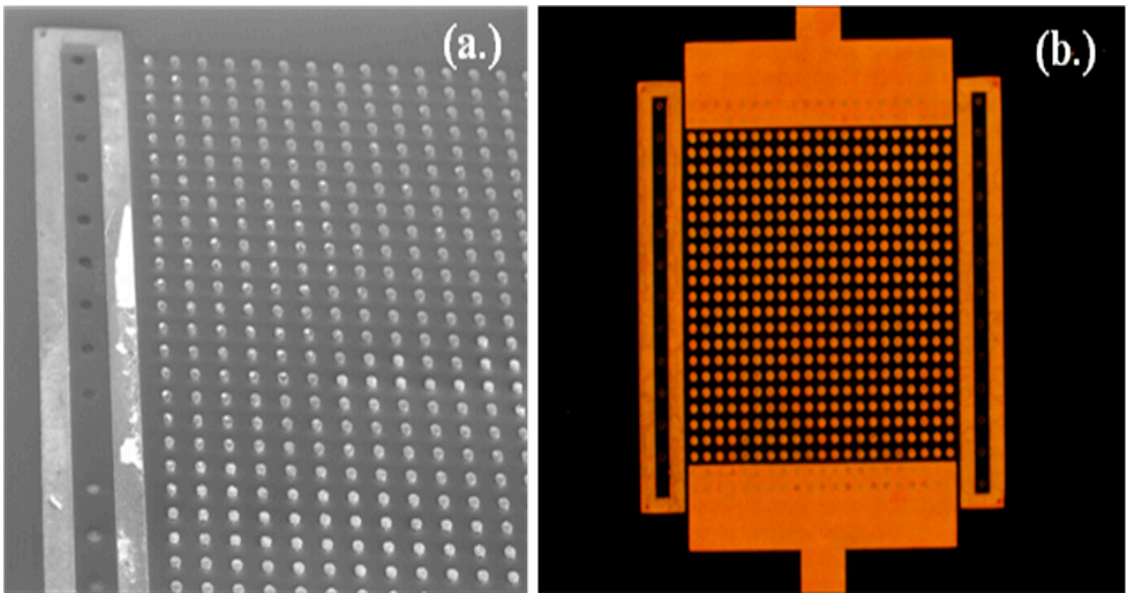


Figure 4.13: (a.) Integrated C4 electrical and rectangular C4 fluidic I/Os. (b.) Copper pads fabricated on the substrate to facilitate assembly.

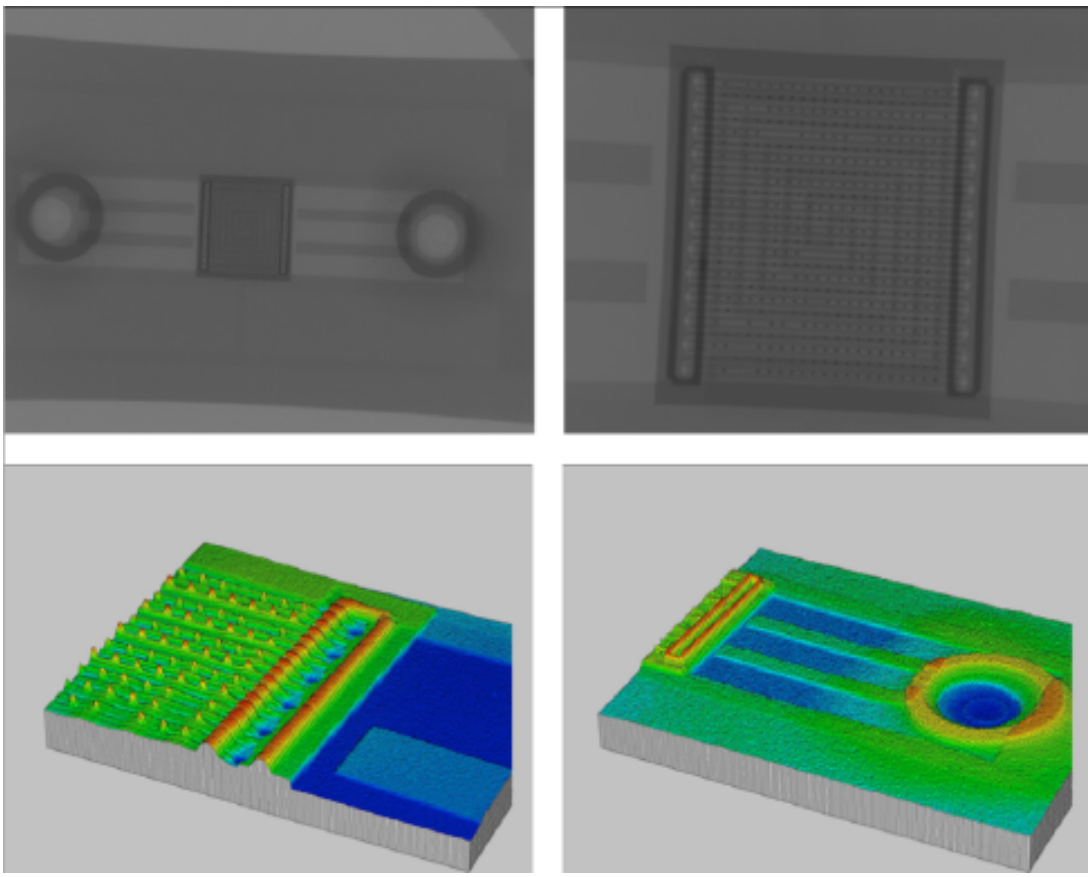


Figure 4.14: X-ray images of successfully bonded 3D stack of chips with C4 electrical and rectangular fluidic I/Os.

4.4 Fluidic Testing of C4 Fluidic I/O Interconnects

To test the C4 fluidic I/Os, two chips were assembled to a silicon substrate. A mechanical pump and fluid inlet pipe were attached to the bottom side of the silicon substrate in the 3D stack and used to pass fluid through the chip stack (Figure 4.15). It was observed that fluid can be delivered from the bottom of the stack, through the 3D stack, and out of the fluidic vias of the top-most chip. Fluid was circulated through the fluidic I/Os at flow rates up to 100ml/min, and no leakage was observed. As previously discussed in Chapter 2, for the microchannel heat sink configuration used in the

experimental component of this work, a fluid flow rate of 100ml/min would be sufficient for achieving a desired thermal resistance of >0.28 °C/W.

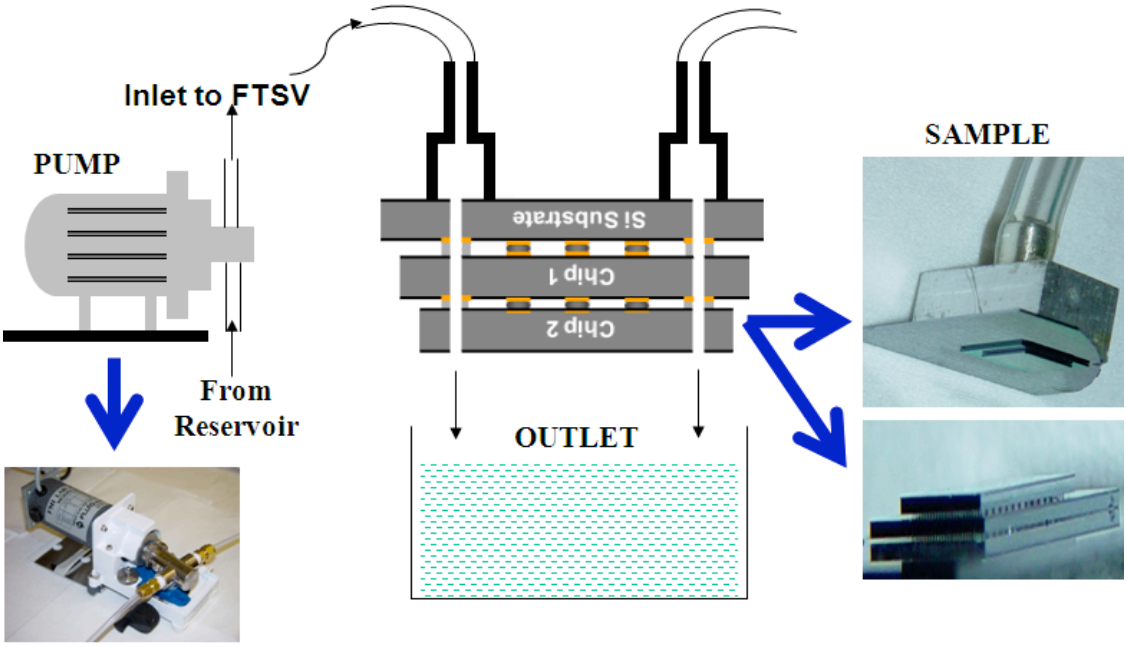


Figure 4.15: Experimental setup for fluidic testing of C4 fluidic I/Os.

4.5 Assembly Using Polymer Sockets, Polymer Pipe Fluidic I/Os, and Electrical I/Os

Microfluidic chips can also be stacked when using polymer pipe fluidic I/Os and solder electrical I/Os. To develop the necessary assembly processes, a silicon chip was fabricated which contained the following features: fluidic TSVs, polymer pipe I/O interconnects, high density solder bump electrical I/O interconnects on the front side of the dice, and polymer sockets on the back side of the dice, as shown in Figure 4.16. The silicon substrate contains copper pads, polymer sockets, and integrated fluidic TSVs.

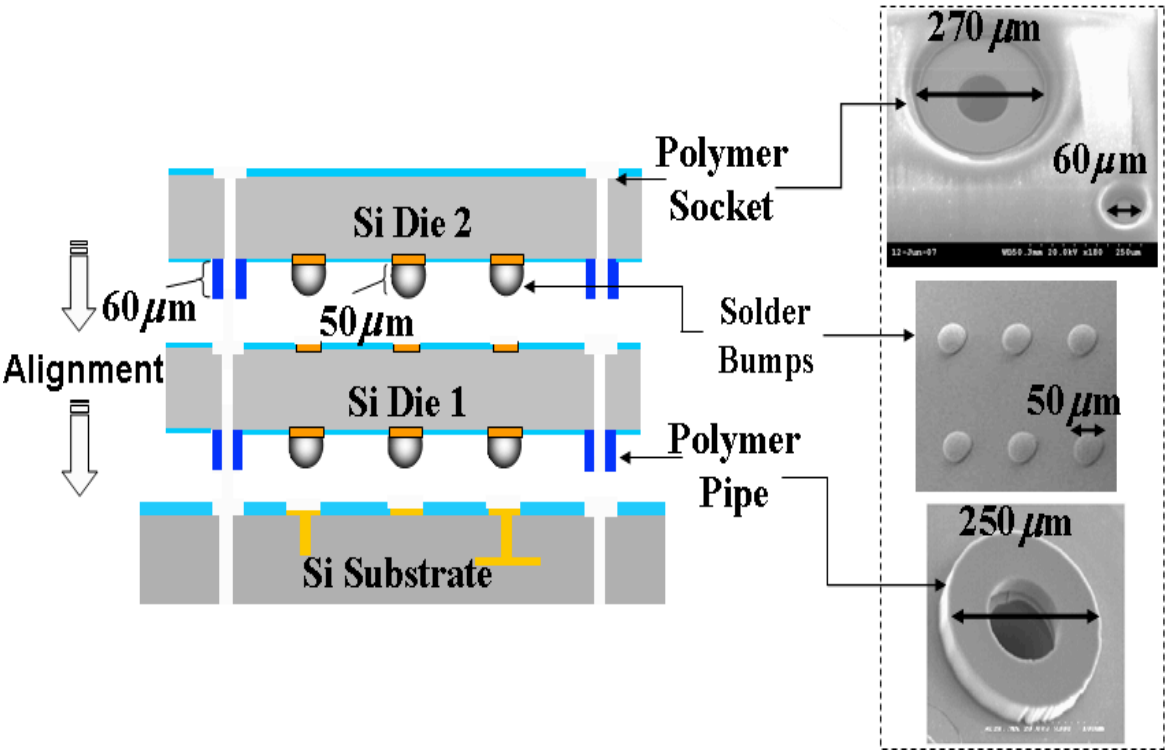


Figure 4.16: 3D assembly using polymer fluidic I/Os and solder electrical I/Os.

Using this configuration, dice were aligned, stacked, and assembled on a silicon substrate using a RD Automation flip-chip bonder that has an alignment accuracy of <2μm. The process used for assembly involves pre-heating the die and the substrate to temperatures of 180°C and 140°C, respectively, bringing the two into contact with a compression force of 200g, and elevating the temperature of the chip and the substrate to 230°C and 150°C, respectively. The bonding process parameters are listed in Table 4.3.

The fluidic I/Os and electrical I/Os are assembled simultaneously. The 250μm diameter polymer pipes are aligned to the 270μm diameter polymer sockets on the substrate, and the 50μm diameter solder bumps are aligned to the copper traces and 60μm polymer sockets on the substrate (Figure 4.16). In addition to serving as electrical and

fluidic I/Os, the solder bumps and polymer pipes provide mechanical interconnection between the bottom die and the substrate and between the dice in the 3D stack.

Because copper pads and polymer sockets are fabricated onto the back side of the first die, the second die can assembled onto the back side of the first die using the same bonding recipe. The self-alignment property of solder increases the alignment accuracy of the die to the substrate. Patterned silicon dioxide on the substrate contains the solder during reflow. The process used for assembly of the 3D prototype is thus compatible with conventional flip-chip bonding. Figure 4.17 shows an SEM cross-sectional image of a 3D stack of two microfluidic chips. Figures 4.18a and 4.18b show infrared microscope images of through-silicon fluidic via alignment of the two chips. Figure 4.19 shows a 3D stack of two chips assembled to a silicon substrate and a 3D stack of four chips assembled to a silicon substrate.

Table 4.3: Bonding Process Parameters.

Assembly Parameters and Sequence of Steps	Value
Pre-heating Temperature of Substrate	140°C
Pre-heating Temperature of Die 1	180°C
Compression Force	200g
Bonding Temperature of Substrate	150°C
Bonding Temperature of Die 1	230°C
Pre-heating Temperature of Substrate and Die 1	140°C
Pre-heating Temperature of Die 2	180°C
Compression Force	200g
Bonding Temperature of Substrate and Die 1	180°C
Bonding Temperature of Die 2	230°C

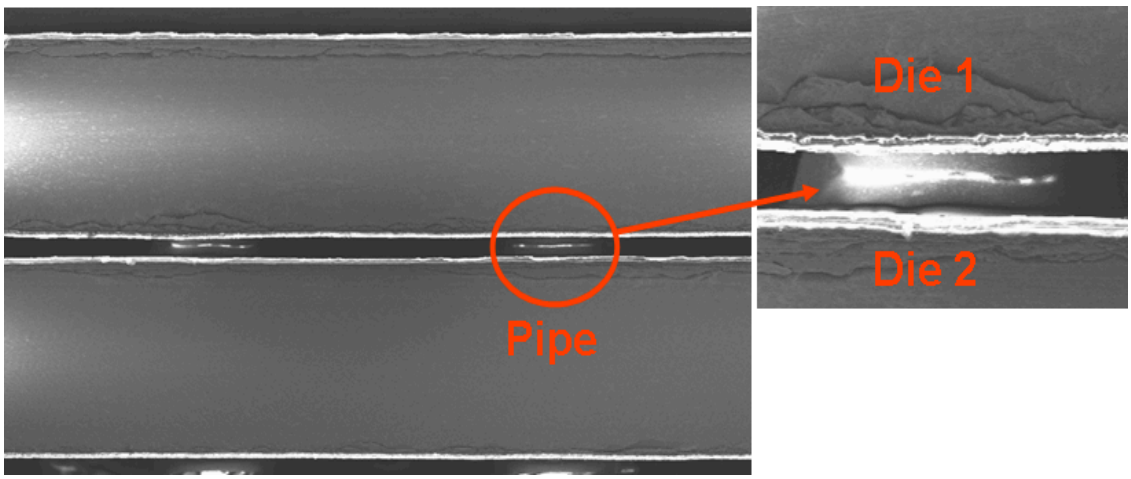


Figure 4.17: Cross-sectional SEM image of 3D microfludic chip-to-chip bonding.

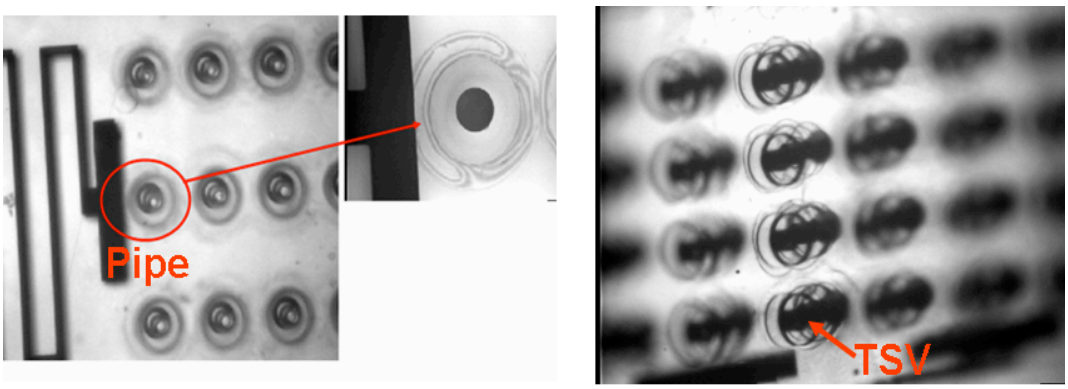


Figure 4.18a: Top-view IR-microscope image of 3D stack. Figure 4.18b: Tilted IR-microscope image of 3D stack.

After assembly, to seal the fluidic I/Os on the front side of each chip, an epoxy-based underfill is applied at the edges of chip (Figure 4.20). The underfill provides a stronger mechanical connection between each interface. For this application, most importantly, underfill is used for the purpose of sealing the fluidic interconnect interfaces between the die and the substrate and between the dice in the 3D stack.

To test the reliability of the fluidic sealant, a syringe pump and fluid inlet pipe were attached to the back side of the top-most die in the 3D stack and used to pass fluid through the chip stack (Figure 4.21). Fluid can be delivered from the top chip, through

the 3D stack, and out of the bottom of the substrate with no leakage at the chip-to-chip and chip-to-substrate interfaces. Consequently, based on this preliminary test, this fluidic I/O technology can be used to route fluid to each layer of microchannels in a 3D chip stack.

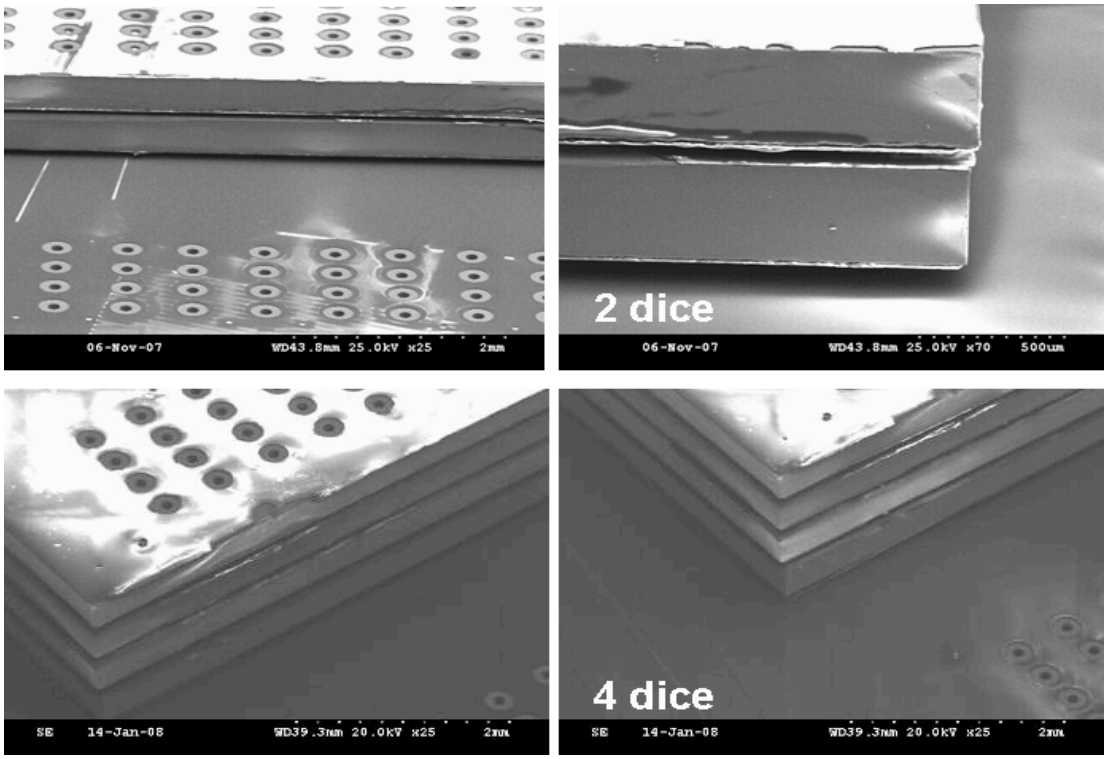


Figure 4.19: SEM images of 2-chip and 4-chip 3D stacks.

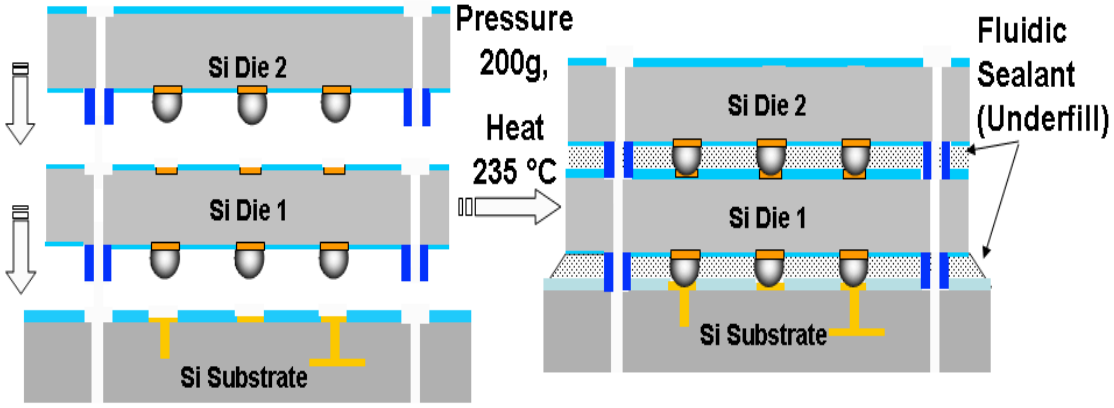


Figure 4.20: 3D assembly and fluidic sealing.

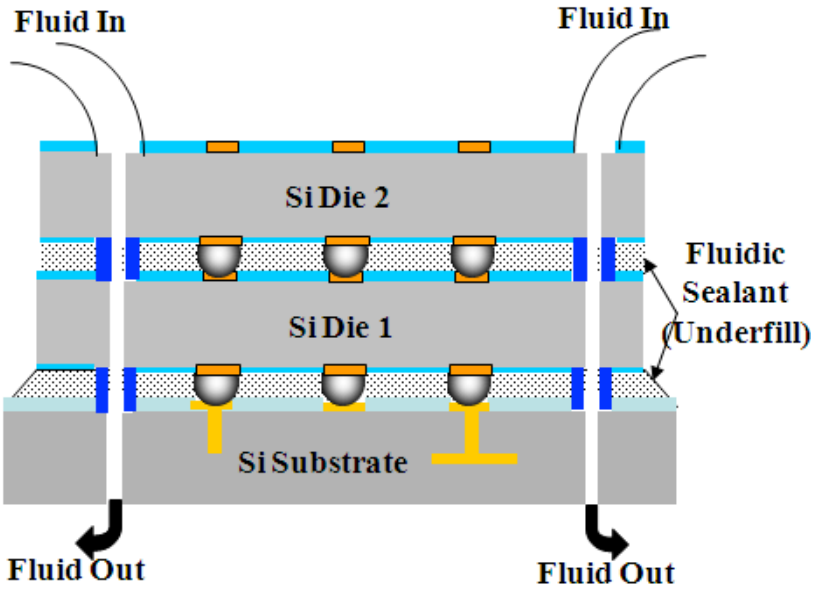


Figure 4.21: Experimental setup for fluidic testing of polymer pipe fluidic I/Os.

4.6. Summary

Chapter 4 discusses the flip-chip bonding processes that enable assembly of the microfluidic chips in the liquid-cooled 3D chip stack. Bonding process parameters are outlined for the flip-chip die-to-substrate and die-to-die bonding processes for three fluidic I/O sealing technologies.

The ability to assemble chips with integrated electrical and fluidic I/Os and seal fluidic interconnections at each strata interface is demonstrated using three assembly and fluidic sealing techniques. Assembly results show the stacking of up to four chips that contain integrated electrical and fluidic I/O interconnects, with an electrical I/O density of ~1600/cm^2. Fluidic testing is performed by circulating fluid through the 3D stack at flow rates up to 100ml/min, with no fluid leakage observed.

CHAPTER 5

THERMAL AND FLUIDIC TESTING OF THE 3D INTER-LAYER LIQUID COOLING PLATFORM

5.1 Experimental Thermal Test-bed for 3D Liquid Cooling

An experimental thermal test-bed for evaluating the cooling needs for 3D chip stacks which contain high-performance microprocessors has been developed. This test-bed enables the thermal simulation and experimental thermal measurements of liquid-cooled processor-on-processor (Figure 5.1) and memory-on-processor (Figure 5.2) 3D chip stacks.

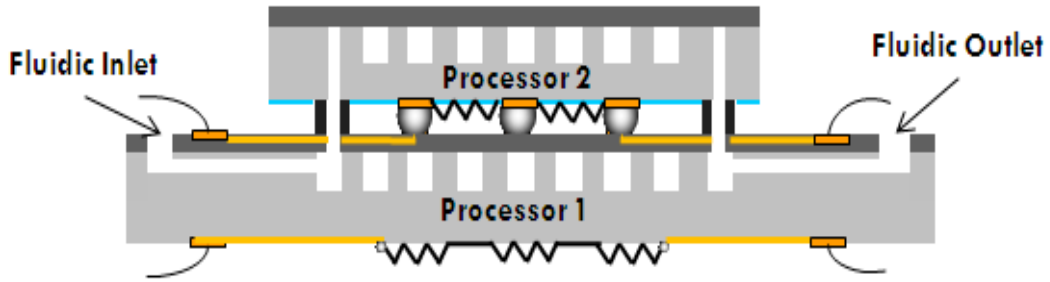


Figure 5.1: Schematic of processor-on-processor 3D chip stack.

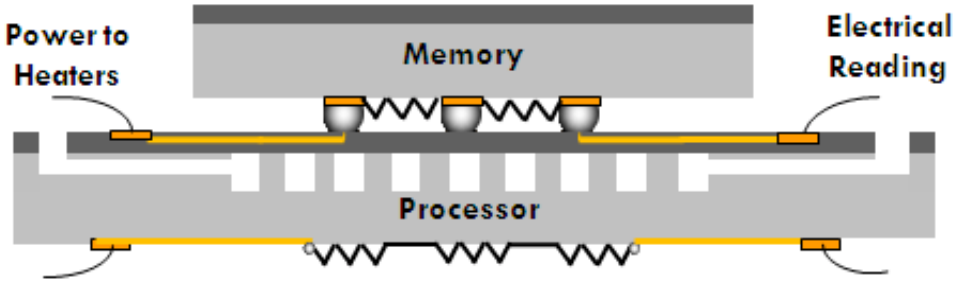


Figure 5.2: Schematic of memory-on-processor 3D chip stack.

The controllable parameters of the experimental setup include power dissipation and heat flux of each chip in the 3D stack, fluid flow rate, the number of I/Os on a chip, and selective layer heating and cooling. The measurable parameters of the chips in the 3D stack include thermal resistance of each chip in the stack, average pressure drop of the 3D stack, and temperature rise of each chip.

5.2 Fabrication of Top Layer in 3D Chip Stack

Fabrication of the top layer of the 3D stack, chips which contain a microchannel heat sink, fluidic through silicon vias, fluidic I/Os, electrical I/Os, and integrated platinum heaters/resistors (used for heating and temperature sensing), has been demonstrated. Figure 5.3 shows the design layout schematic of the top layer in the 3D stack, and Figure 5.4 outlines the fabrication process flow for fabrication of the top layer of the 3D chip stack.

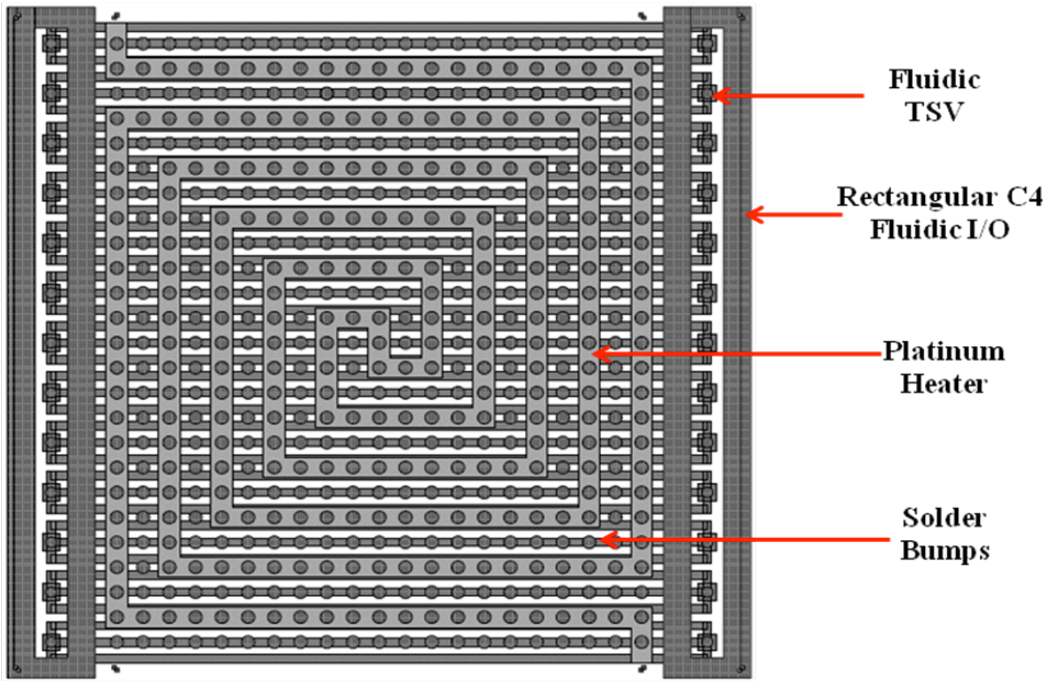


Figure 5.3: Schematic of the top view of mask design with integrated (top layer).

A summary of the fabrication process for the chip on the top layer includes fabrication of the platinum resistor network (Figure 5.4a), etching of microchannels and fluidic TSVs in the wafer (Figure 5.4b), capping the microchannels with a silicon capping wafer (Figure 5.4c), and fabrication of copper pads, electrical I/Os, and fluidic I/Os (Figure 5.4d). To verify the depth of the microchannels, the Veeco Wyko profilometer, which uses the phase change of light reflecting from various heights of similar materials to measure the uniformity of a flat surface or the horizontal distance between two adjacent surfaces, was used. The channel depth measurement shown in Figure 5.5 verifies the depth of the microchannels to be ~350μm, which is a sufficient channel depth for obtaining the desired microchannel heat sink thermal resistance, as discussed in Chapter 2.

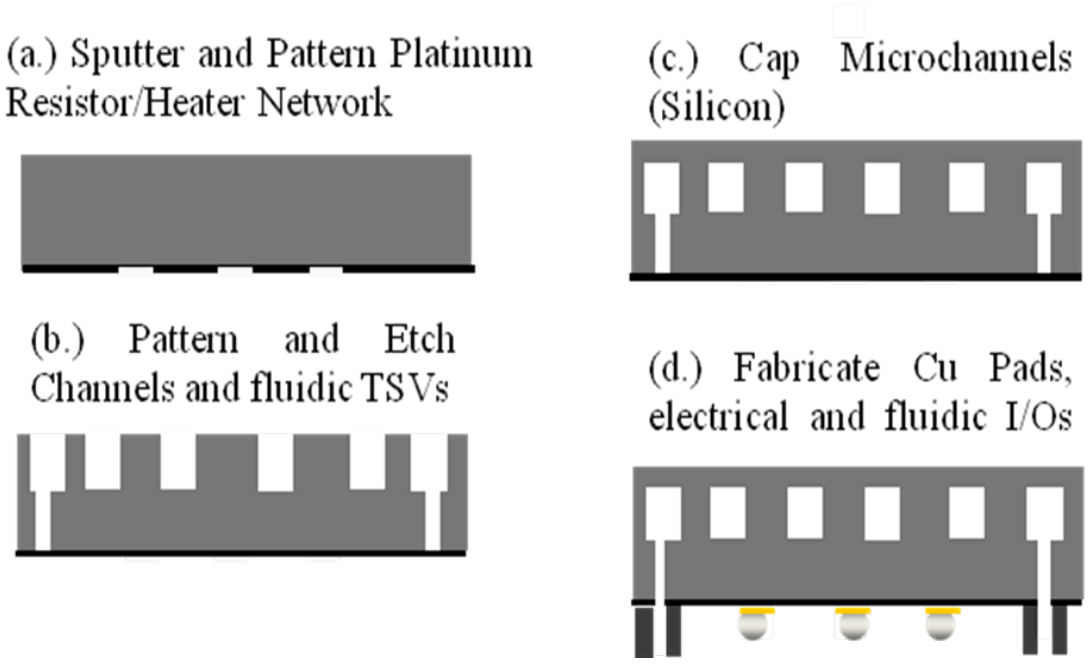


Figure 5.4: Schematic of wafer-level integration of microchannels, fluidic through-silicon vias, electrical and fluidic I/Os, and integrated platinum heaters/temperature sensors (top layer).

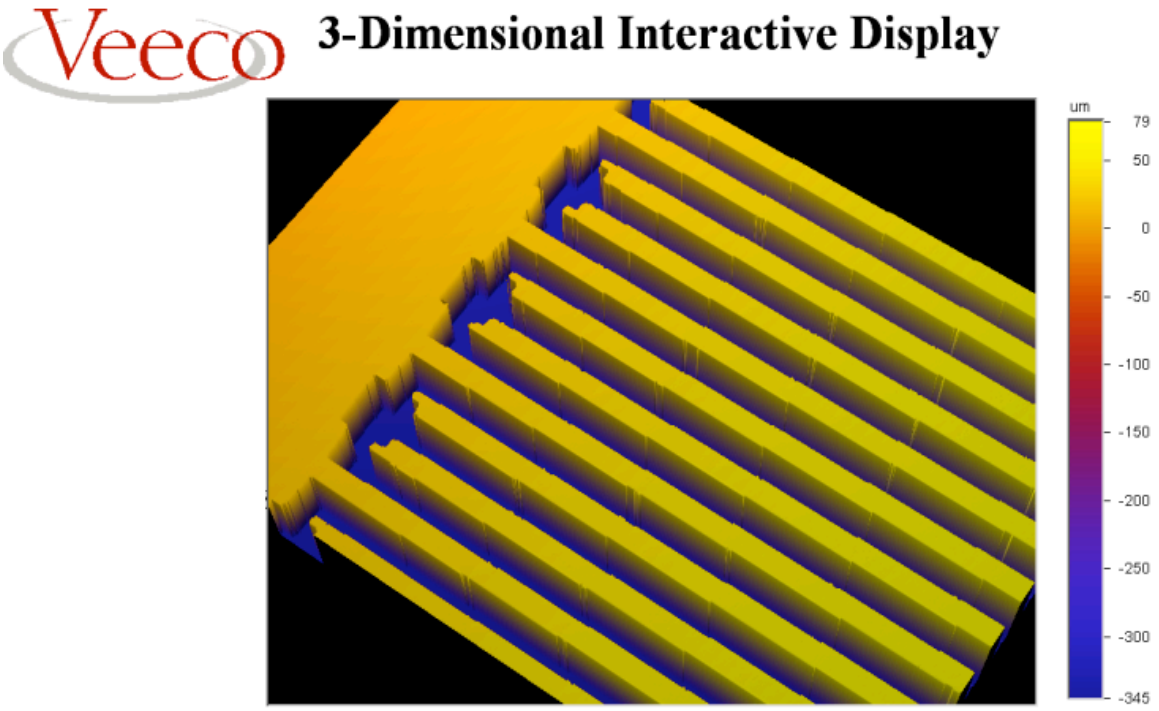


Figure 5.5: Veeco Wycko microscope measurement of microchannel depth.

5.3. Fabrication of Bottom Layer in 3D Chip Stack

Figure 5.6 shows the design layout schematic of the top layer in the 3D stack, and Figure 5.7 shows a photograph of the bottom layer in the 3D stack. The bottom side of this layer contains thin-film platinum resistors for heating and temperature sensing. The bottom side of this layer also contains copper pads, which enable power to be supplied to the heaters. This layer also contains a silicon-capped microchannel heat sink with integrated fluidic TSVs in the silicon cap. The top side of this layer contains copper pads which are used as a bonding site for the next chip in the 3D stack. Additionally, four larger copper electrode pads are present on the top side for supplying power to the thin-film platinum heaters of the next chip in the 3D stack.

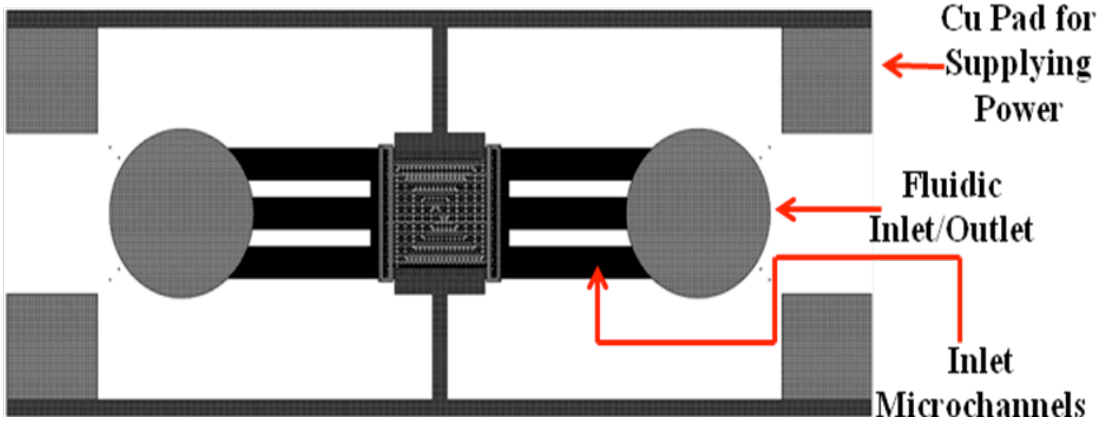


Figure 5.6: Schematic of top view of mask design with integrated (bottom chip).

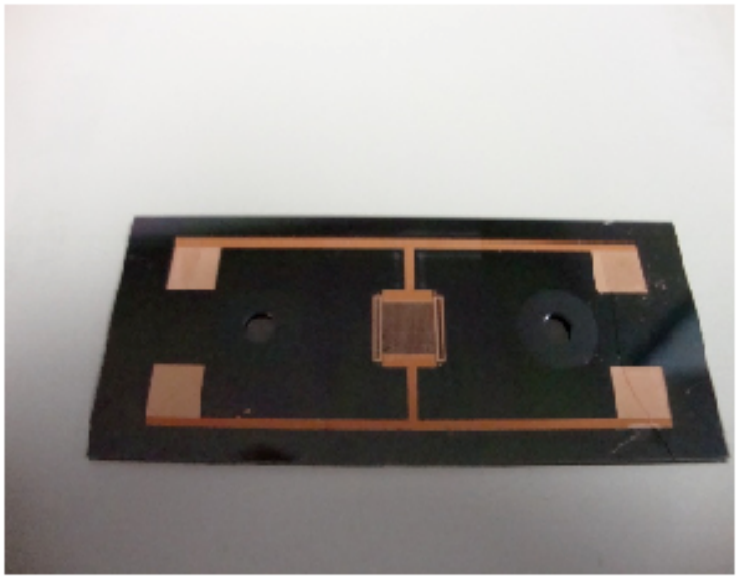


Figure 5.7: Photograph of the bottom layer in the 3D stack.

Figure 5.8 outlines the fabrication process flow for fabrication of the top layer of the 3D chip stack. A summary of the fabrication process for the chip on the bottom layer includes fabrication of the platinum resistor network (Figure 5.8a), etching of microchannels and fluidic inlet and outlet channels in the wafer (Figure 5.8b), capping

the microchannels with a silicon capping wafer (Figure 5.8c), and fabrication of copper pads on the top and bottom sides of the wafer (Figure 5.8d), deposition and patterning of oxide and copper bonding pads on the top side that enables assembly of the next chip in the 3D stack (Figure 5.8e), deposition and patterning of a dielectric layer (solder or polymer) for containing solder during flip-chip assembly, and etching the silicon capping layer to expose the fluidic inlet and outlet ports that are used for supplying fluid to the 3D chip stack (Figure 5.4g).

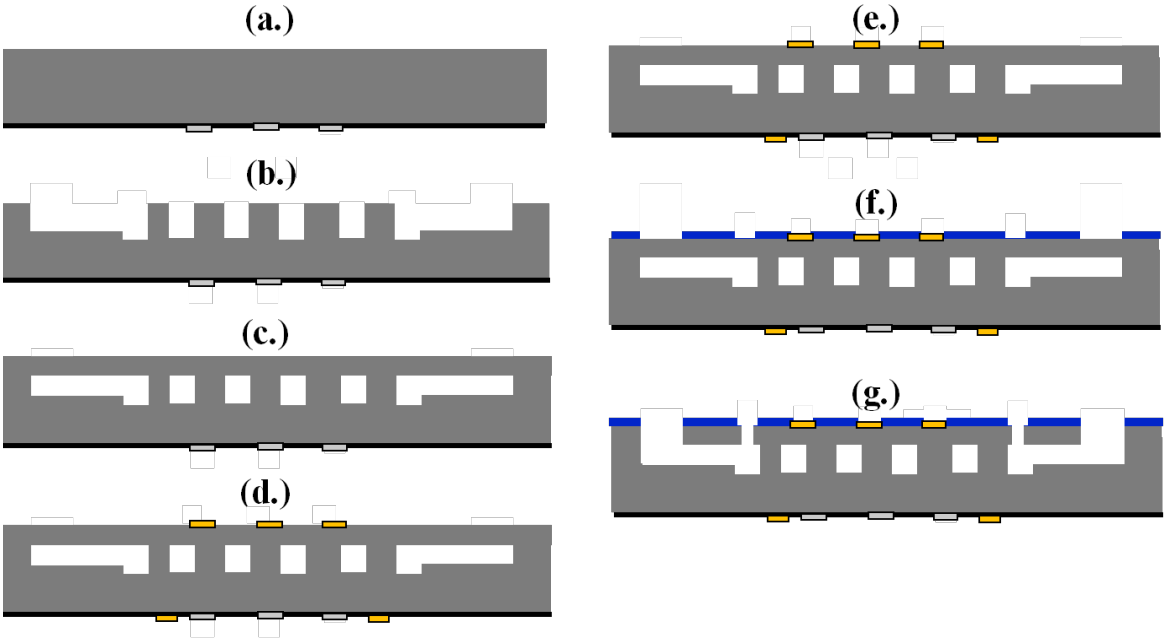


Figure 5.8: Schematic of wafer-level integration of microchannels, fluidic TSVs, fluidic inlets/outlets, platinum heaters, and copper bonding pads (bottom layer).

Figure 5.9 shows a SEM image of the microchannels heat sink that is fabricated in the bottom silicon capped layer. The larger fluidic channels on the left and right sides of the microchannel heat sink are used for routing liquid to the microchannels on the bottom layer and ultimately to the entire 3D chip stack.

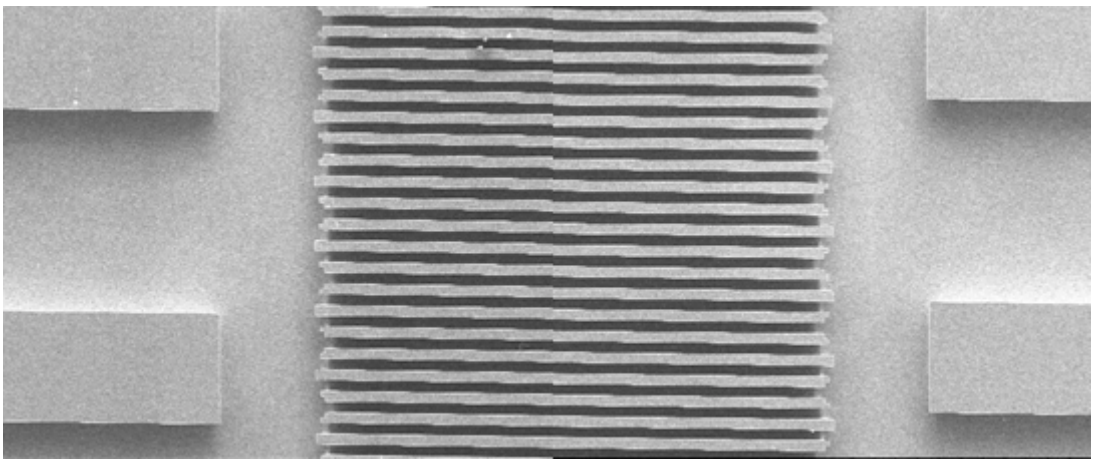


Figure 5.9: SEM image of microchannels in the 3D chip stack bottom layer, where inlet and outlet channels are on the left and right sides of the microchannel heat sink (middle).

5.4. Fluidic Connectivity within the 3D Chip Stack

Figure 5.10 shows a photograph of the multi-layer 3D stack. The features of the assembled microfluidic chip includes a silicon-capped microchannel heat sink, integrated fluidic TSVs, electrical and fluidic I/Os on the bottom side of the chip, and thin-film platinum heaters on the bottom side of the chip. "Nanoports" (Upchurch Scientific, Inc.) are used to attach fluidic tubing to the fluidic inlet and outlet and are bonded to the 3D stack, as shown in Figure 5.10, Figure 5.11, and Figure 5.12. Thus, cooling fluid can be pumped to the fluidic nanoport inlet on the bottom layer, circulated through each chip in the 3D stack, and pumped out of the fluidic nanoport outlet.

Figure 5.11 shows a schematic of a fluidic tube that originates from a mechanical pump and a liquid reservoir. Thus, cooling fluid can be pumped to the fluidic nanoport inlet on the silicon carrier bottom layer, circulated through each chip in the 3D stack, and pumped out of the fluidic nanoport outlet into a liquid reservoir.

Fluidic continuity and fluidic sealing for the 3D microfluidic network was verified and demonstrated by stacking two microfluidic chip layers, as shown in the configuration shown in Figure 5.11. After assembling the chips in the 3D stack, DI water was circulated through the 3D stack for 1 hour at flow rates ranging from 10 ml/min to 100 ml/min.

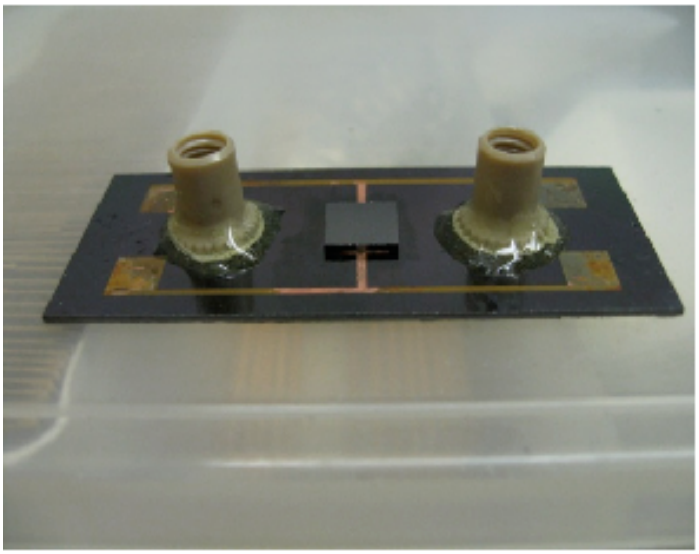


Figure 5.10: Photograph of the multi-layer 3D stack.

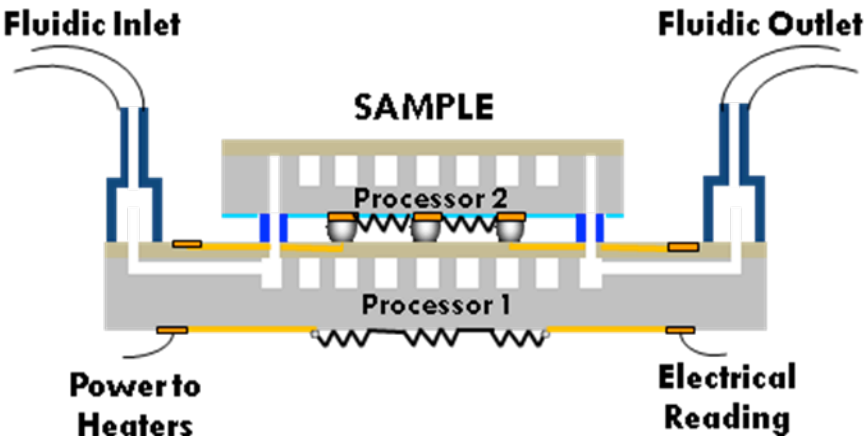


Figure 5.11: Schematic representation of the multi-layer 3D stack.

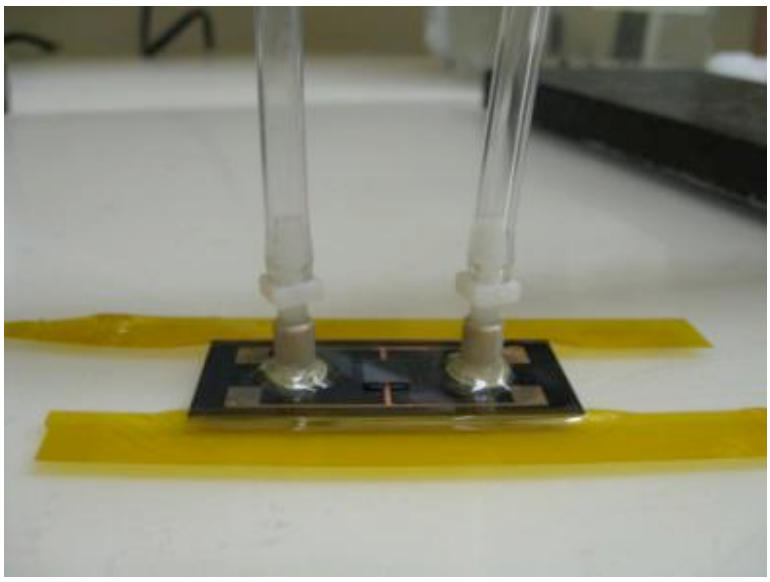


Figure 5.12: Photograph of nanoports and fluidic tubing attached to the 3D stack for fluidic continuity testing.

5.5. Platinum Heater / Thermometer Design and Fabrication

Thin-film platinum resistors are fabricated on the bottom side of each chip of the 3D stack (Figure 5.13). When applying a current source to the resistors, the resistors serve as heating sources which simulate heat dissipated by transistors and interconnects on a microprocessor. The change in resistance of the resistor can be measured and used to calculate the change in chip temperature. A schematic of the mask layout for the platinum heater structure is shown in Figure 5.14, and the characteristics of the platinum resistors/heaters can be found in Table 5.1. The platinum heaters that are integrated on the bottom side of each chip were designed in order to be able to dissipate a heat flux equivalent to 100W/cm^2.

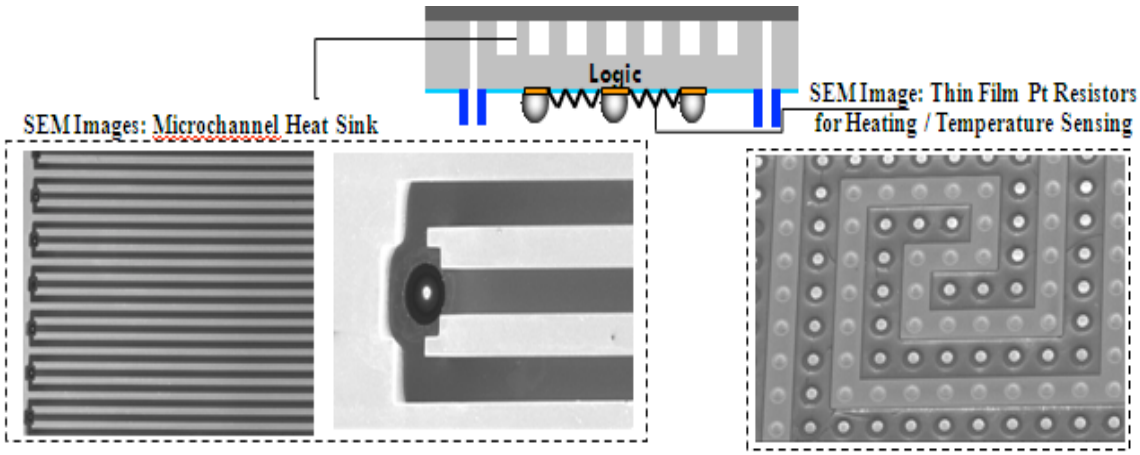


Figure 5.13: SEM images of (left) microchannel heat sink and (right) integrated thin-film platinum resistors and electrical I/Os.

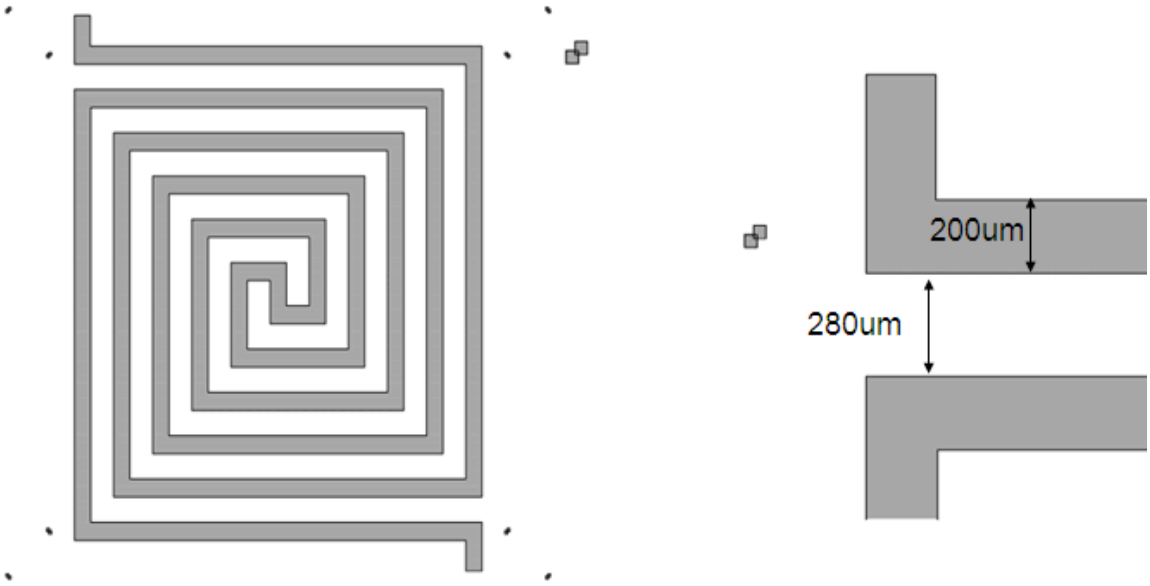


Figure 5.14: SEM images of (left) microchannel heat sink and (right) integrated thin-film platinum resistors and electrical I/Os.

Change of DC resistance of the platinum heaters was verified to be a linear function of the temperature. To characterize the temperature dependence of the Ti/Pt resistors, the sample was heated to various temperatures in a small oven and the DC resistance of the individual heaters was then measured. Figure 5.15a and Figure 5.15b show the measurement results that verify the linear relation between the heater resistance

and the temperature. The slope of the R-T curves is approximately 1.8 - 2Ω/°C, which yields sufficient sensitivity for resistance measurement using a digital multimeter. Good consistence was also observed when testing different chips with integrated platinum heaters fabricated on the chip.

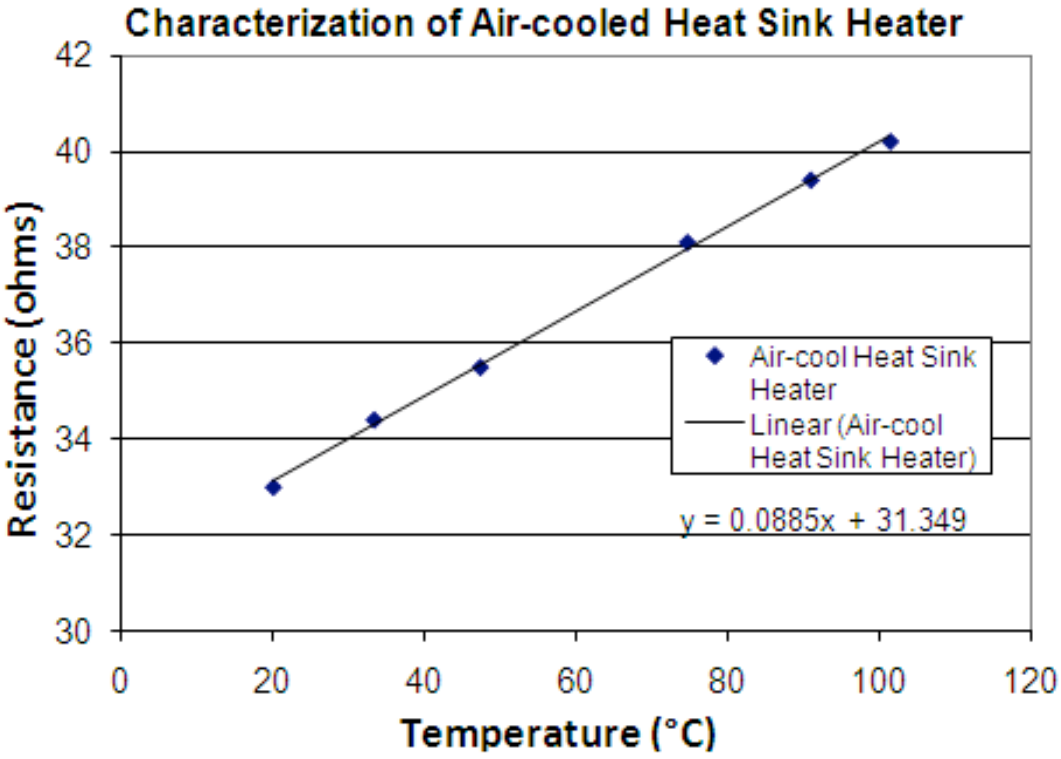


Figure 5.15a: Change of DC resistance of the heater as a linear function of temperature (ACHS).

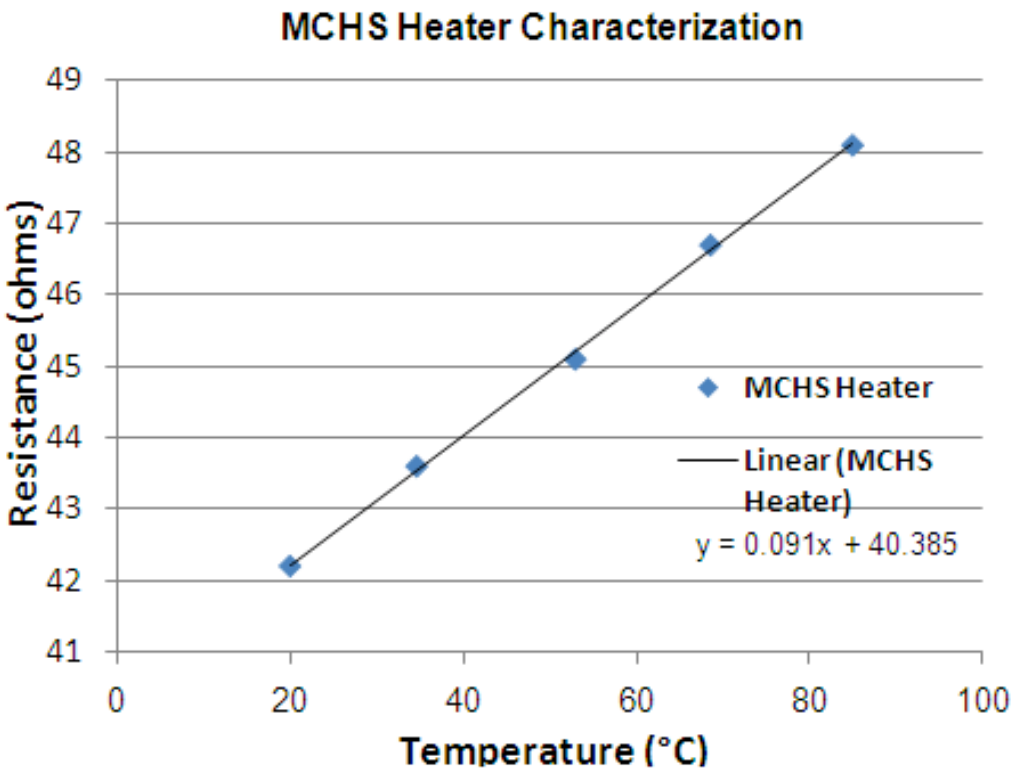


Figure 5.15b: Change of DC resistance of the heater as a linear function of temperature (MCHS).

Table 5.1: Thin-film platinum heater characterization.

Heater Dimensions				
Heating Area	**Wire Resistance**	**Applied Current**	**Applied Power**	**Power Density**
0.36 cm^2	**36 ohms**	**1 A**	**36 W**	**100 W/cm^2**

5.6. Electrical Connectivity in the 3D Chip Stack

The ability to achieve simultaneous electrical connectivity between multiple layers in the 3D stack was demonstrated by stacking chips that contain platinum resistors, electrical I/Os, and copper pads, as shown in Figure 5.16. After assembly, resistance measurements were taken by probing the copper pad electrodes on each layer in the 3D

stack. The resistance measurement of the top layer in the stack was measured to be approximately 37.1Ω, which is approximately the desired resistance measurement for the calculated resistor wire resistance shown in Table 5.1.

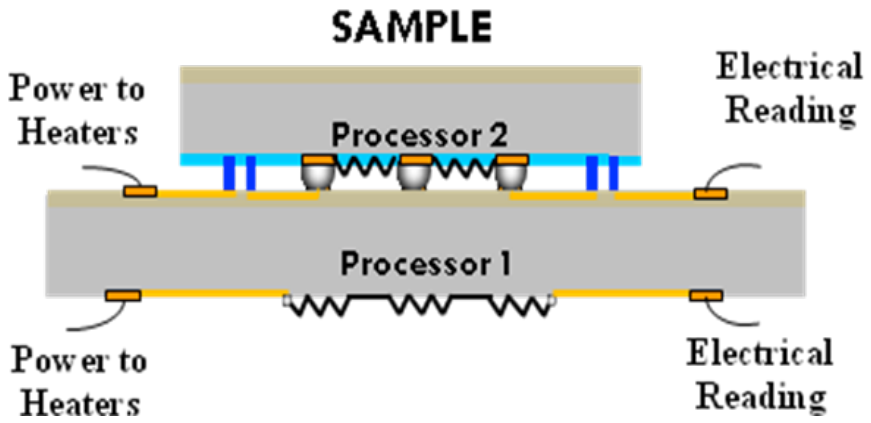


Figure 5.16: Experiential setup for measuring multi-layer electrical connectivity.

5.7. Experiential Thermal Measurement Comparison of an Air-cooled Heat Sink vs. a Microchannel Heat Sink

5.7.1. Experiential Thermal and Fluidic Testing Setup

The equipment required for thermal-fluidic testing and characterization includes a mechanical liquid pump, a digital flow meter for monitoring liquid flow rates, a differential pressure gauge for measuring pressure drop, thermocouples to measure the inlet and outlet temperatures of the cooling liquid, and a data logger to collect data during

thermal cycling of the chips in the 3D chip stack. Figure 5.17and Figure 5.18 show a schematic and photograph of the experiential setup.

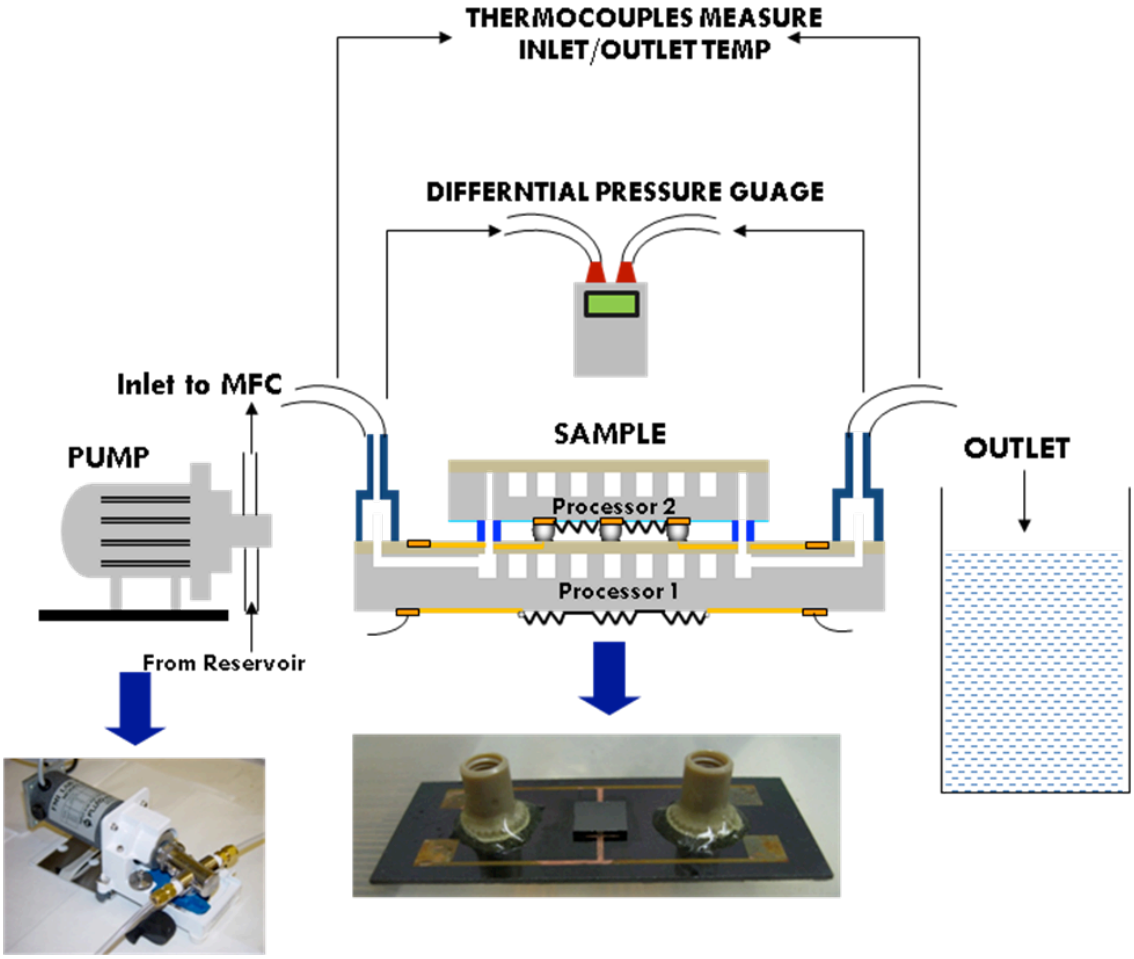


Figure 5.17: Schematic of the thermal test-bed experiential setup.

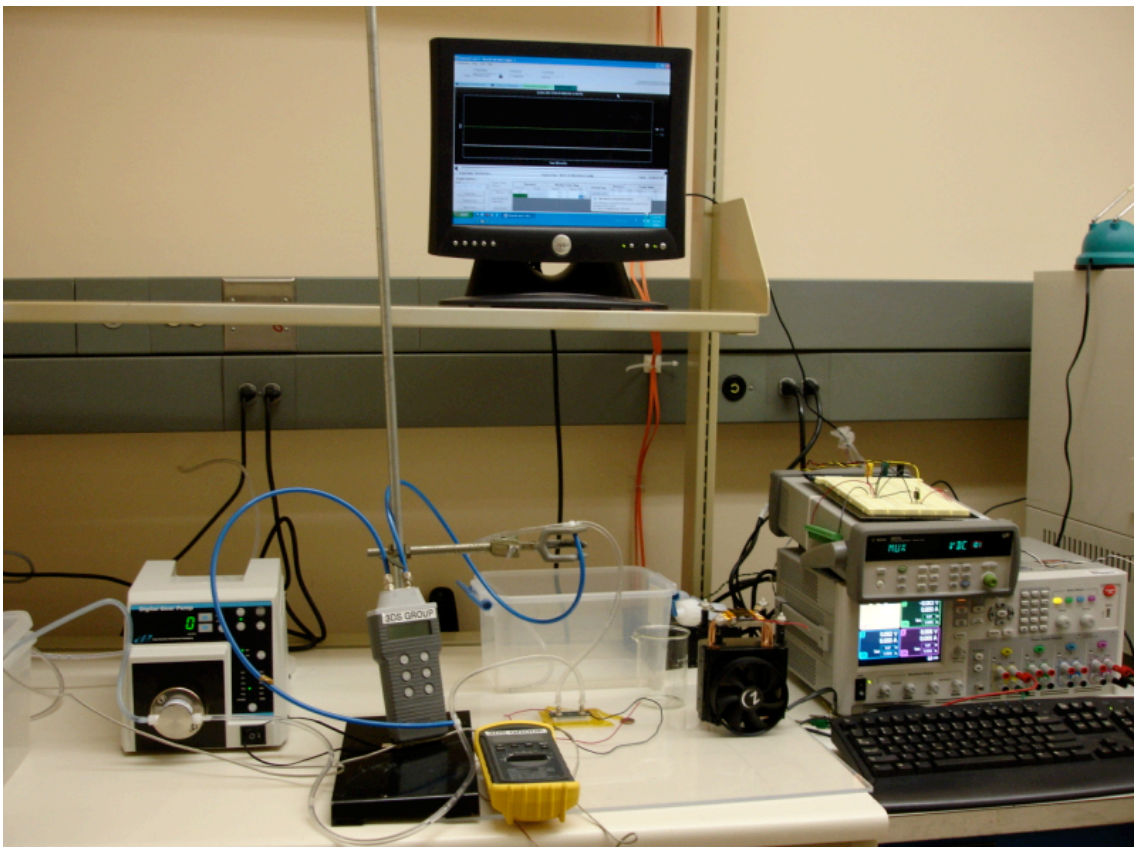


Figure 5.18: Photograph of the thermal test-bed experiential setup.

Microfluidic chips containing all of the components that were described in the previous sections were connected to the experimental setup to enable thermal and fluidic measurements. Additionally, a chip containing a platinum resistor network identical to the resistor network on the microfluidic chips was connected to an air-cooling heat sink (ACHS).

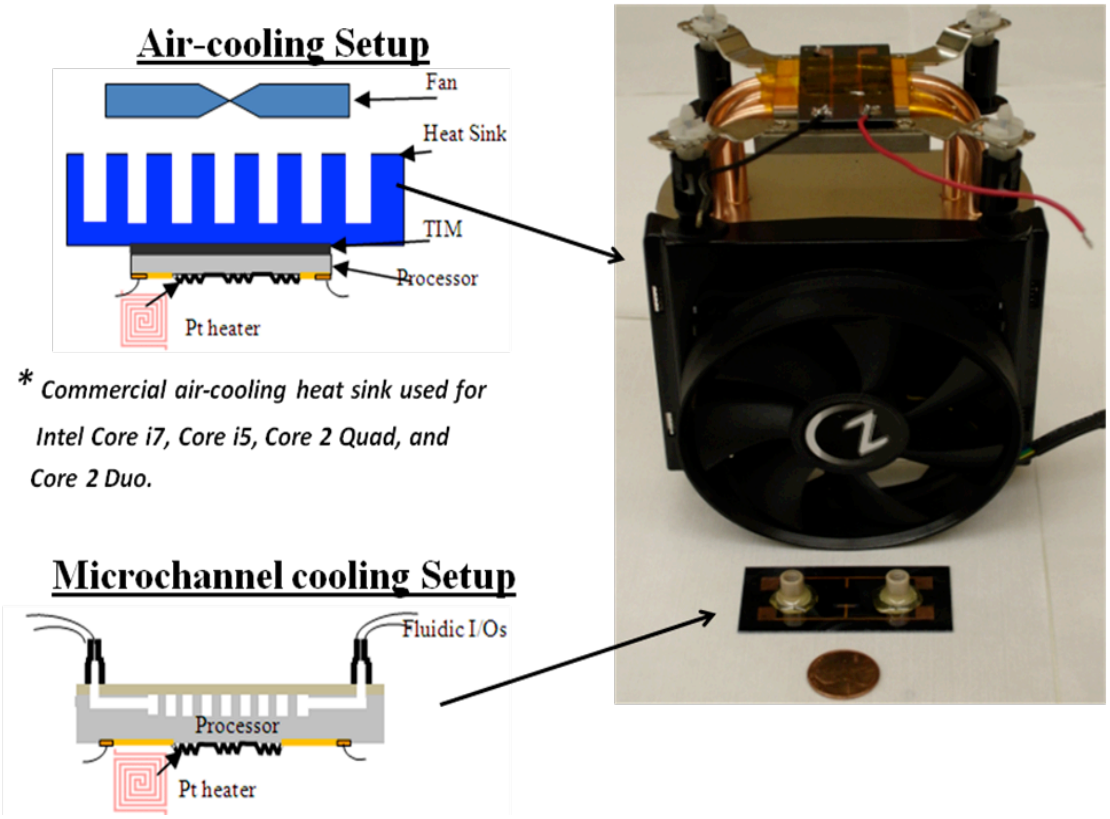


Figure 5.19: Schematic of ACHS and MCHS thermal testing setup.

5.7.2. Heat Sink Volume Comparison for Air-cooling vs. Microchannel Liquid Cooling

By placing the MCHS sample and the ACHS sample side-by-side, we can clearly see the volume difference of the two cooling technologies. For comparison, the dimensions of the MCHS are (0.6 x 0.6 x 0.02)cm, while the dimensions of the ACHS are (13 x 10 x 6)cm. The volume of the two heat sinks differs by a factor of 10^5, which is rather significant. The volume of the two heat sink technologies differs by a factor of 10^5. Using MCHS technology enables the reduction of cooling hardware size from inches to microns.

Figure 5.20: Heat sink volume comparison between the Intel i7 air-cooling heat sink and the microchannel heat sink.

Table 5.2: Heat sink volume comparison between the Intel i7 air-cooling heat sink and the microchannel heat sink.

Technology	Volume
Air-cooling Heat Sink	**(13 x 10 x 6) cm^3**
Microchannel Heat Sink	**(0.6 x 0.6 x 0.03) cm^3**

5.7.3. Thermal Resistance Analysis for Air-cooled Heat Sink vs. Microchannel Heat Sink

In the ACHS experiment, we use a commercially available CPU cooler which consists of 3 copper heat pipes and 45 aluminum fins that is designed for the Intel i5/i7 CPU. The ACHS sample is tested while the fan is rotating at its maximum speed (2500rpm $\pm$15). The corresponding air flow is 54.8 CFM.

For the MFHS testing, we used the sample with an embedded micropin-fin heat sink, which is fabricated as described in the previous section. The thermal measurements are made at two flow rates: 50 ml/min and 75 ml/min. The dissipated power density for both the ACHS and the MFHS was increased to ~100W/cm^2. The total heated area is 0.6cm $\times$ 0.6cm.

The experimental results clearly indicate the performance gains offered by liquid cooling. Figure 5.21 shows the on-chip temperature rise as a function of localized heating power under various two DI water flow rates of 50ml/min and 75ml/min (heating area of ~0.36 cm^2). As expected, when increasing the flow rate to 75ml/min, the temperature of the chip and thermal resistance of the microchannel heat sink decrease. However, as shown in the graph, the difference in chip temperature is not substantial. It can be assumed that the thermal resistance component R_{heat}, the resistance due to heating of the cooling fluid, which is disproportional to the fluid flow rate, is not the dominant thermal resistance component for the testing parameters previously described. It is likely that R_{conv}, the convective resistance, which is dependent on the heat transfer coefficient of

the cooling fluid and the area of the surfaces of the microchannels in contact with the cooling fluidic is the dominant thermal resistance component.

A summary of the experiential thermal measurements is shown in Table 5.3. The ACHS was shown to have a thermal resistance of 0.518°C/W at an average chip temperature of 77.6°C. The microchannel heat sink was shown to have a thermal resistance of 0.296°C/W at an average chip temperature of 49.9°C when cooling fluid is circulated through the microchannels at a flow rate of 50ml/min, and the microchannel heat sink is shown to have a thermal resistance of 0.27°C/W at an average chip temperature of 48.5°C when cooling fluid is circulated through the microchannels at a flow rate of 75ml/min.

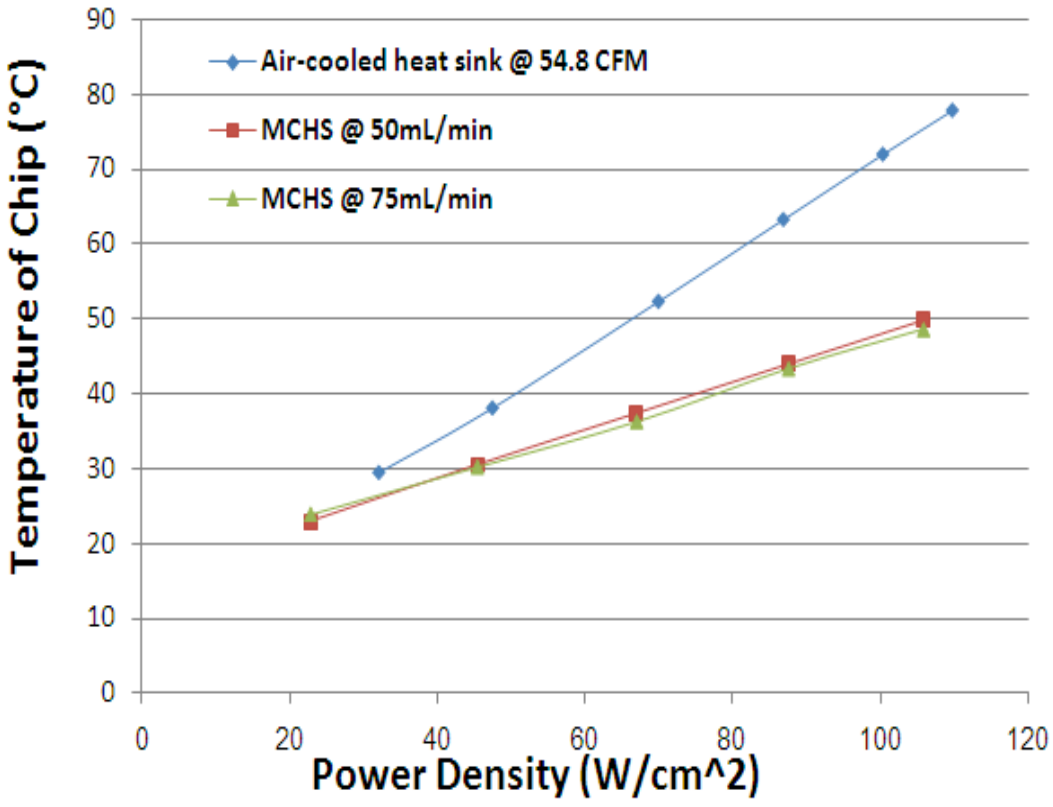


Figure 5.21: On-chip temperature rise as a function of localized heating power under various DI water flow rates (heating area of ~0.36 cm^2).

Table 5.3: Comparison of heat sink thermal resistance and chip average junction temperature for air cooling vs. microchannel liquid cooling.

	ACHS @ 54.8 CFM (~2500 rpm)	MCHS @ 50 ml/min	MCHS @ 75 ml/min
Thermal Resistance ($^oC \cdot cm^2/W$)	**0.518**	**0.296**	**0.270**
Localized power density (W/cm^2)	**109.6**	**105.7**	**105.9**
Avg. Junction Temperature (^oC)	**77.6**	**49.91**	**48.54**

5.8. Hydraulic Analysis of Microchannel Heat Sink

While circulating fluid through the microchannels in the 3D chip stack, a differential pressure gauge was used to measure the pressure drop in a single microfluidic chip and the pressure drop in a two-layer 3D chip stack. Additionally, the pressure drop was measured at various fluidic flow rates in order to analyze the impact of the flow rate on the pressure drop in the microchannels. Figure 5.22 shows the results of the measured pressure drop in a single microfluidic chip as a function of fluidic flow rate, and Figure 5.23 shows the pressure drop in a two-layer 3D chip stack as a function of fluidic flow rate.

As expected, in both cases, the pressure drop increases as the fluidic flow rate increases. Furthermore, it is important to note that the average pressure drop across the 3D chip stack is approximately twice the amount of the average system pressure drop for a single chip. Consequently, the fluidic flow rate will have to be increased to supply a sufficient amount of fluid for every layer that is added to the 3D chip stack. Increasing

the fluidic flow rate for each additional layer ultimately means that the pressure drop of the 3D system increases for each additional layer in the 3D stack.

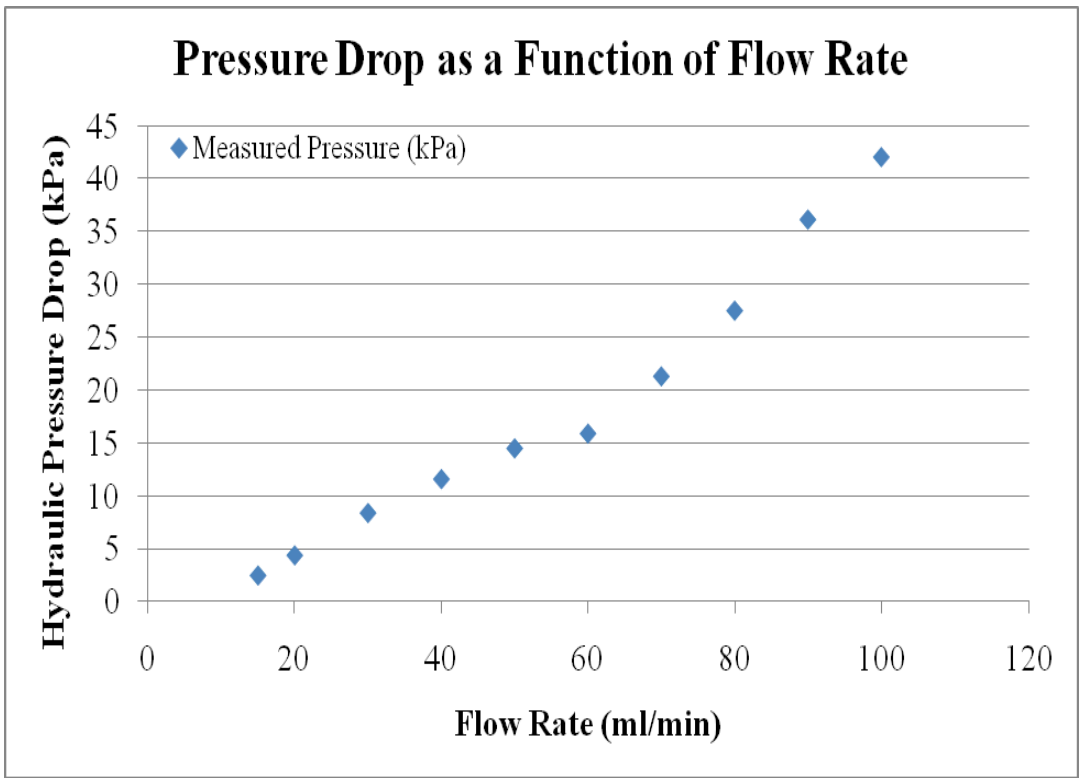


Figure 5.22: Pressure drop as a function of flow rate for a single microfluidic chip.

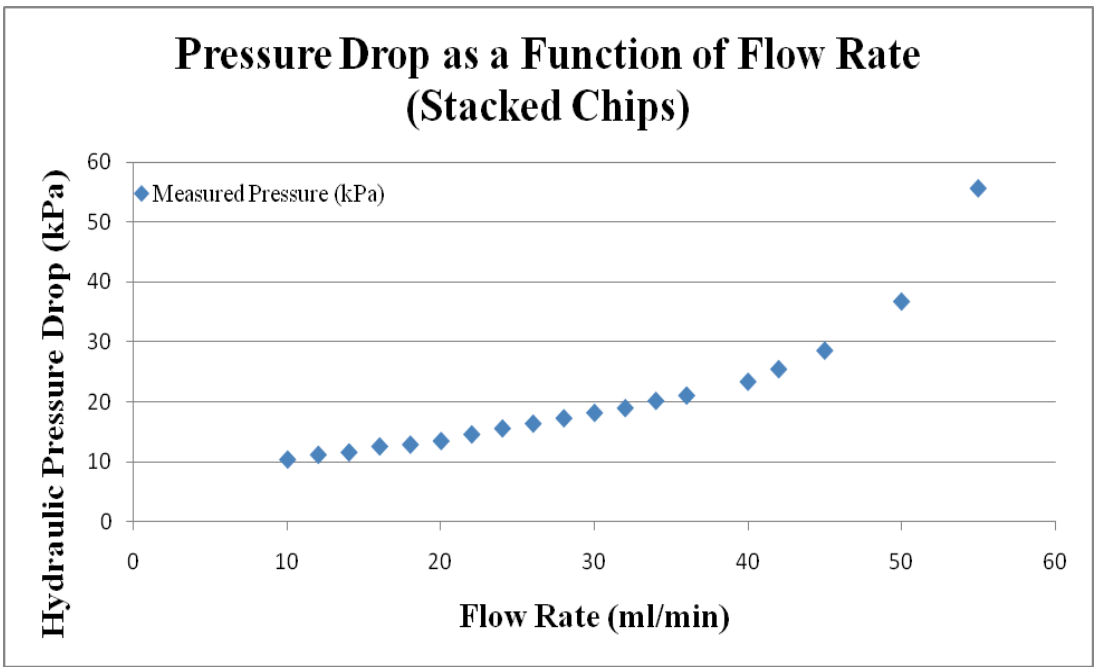


Figure 5.23: Pressure drop as a function of flow rate for a 3D stack of microfluidic chips (two layers).

5.9. Microfluidic Pin-fin Heat Sink

Although microchannel heat sink technology has been the primary focus of this research, alternative heat sink technologies were also investigated. An alternative heat sink technology to the microchannel heat sink is the pin-fin heat sink [5.1-5.4], which consists of an array of staggered circular pin-fin structures (Figure 5.24 and Figure 5.25) [5.5]. The 3D liquid cooling platform that has been developed enables the fabrication and thermal testing of alternative heat sink structures by changing one masking step in the process flow.

Preliminary fabrication and thermal analysis reveal that the pin-fin heat sink technology enables the fabrication of heat sink architecture with a much shorter height, while maintaining a similar thermal resistance as the microchannel heat sink. This result

is important because if electrical TSVs can be integrated in the pin-fin heat sink, electrical TSV fabrication will be easier due to the pin-fin heat sink being a shorter structure. Additionally, as previously discussed, shorter, high-aspect ratio electrical TSVs are preferred for signaling. Thinner and shorter TSVs result in faster interconnects, larger bandwidth density, and lower power consumption.

Table 5.4 summarizes the trade-offs between thermal resistance and pressure drop when comparing a microchannel heat sink to a pin-fin heat sink. The experiential results for the pin-fin heat sink are obtained from [5.5], and the experimental results for the microchannel heat sink are obtained from the most recent thermal measurements for microchannel heat sink analysis done in this work.

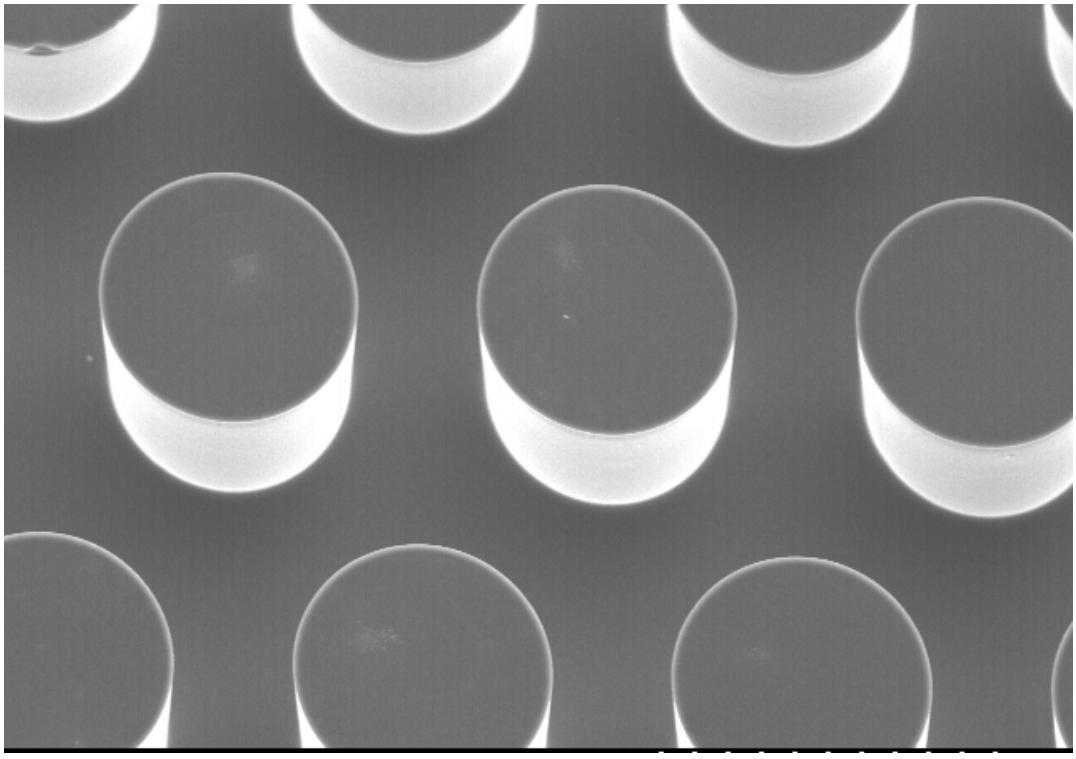


Figure 5.24: Top view of a SEM image of an array of micro pin-fins [5.5].

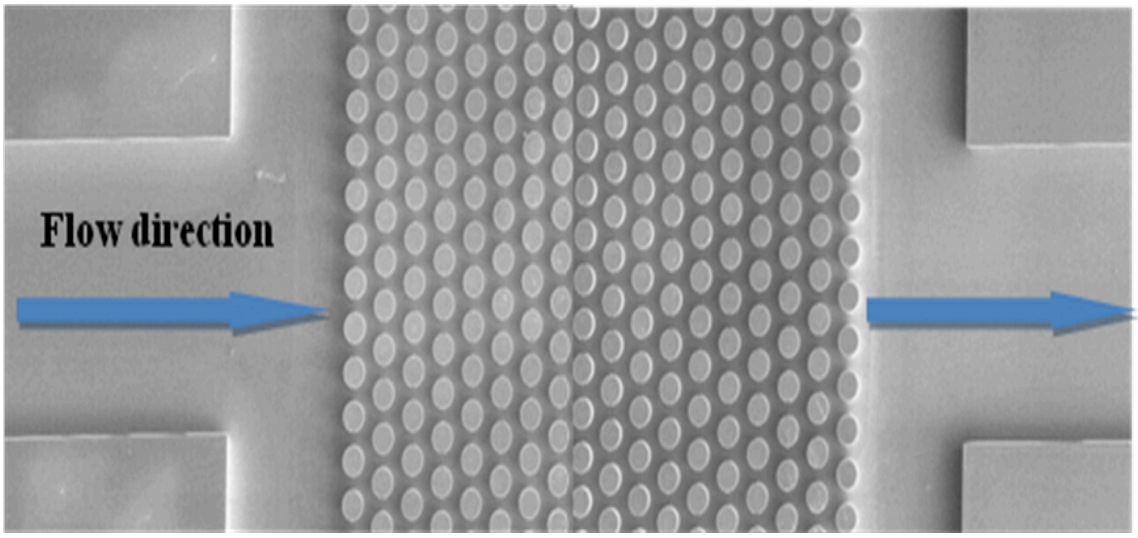


Figure 5.25: Top view SEM image of a micro pin-fin heat sink etched onto the back side of a silicon chip. Inlet and outlet channels that are used for routing cooling fluid to the pin-fin heat sink are shown on the left and right sides of the pin-fin heat sink [5.5].

Table 5.4: Comparison of microchannel and micro pin-fin heat sinks [5.5].

Heat Sink Technology	R_{tot} ($^oC/W$)	ΔP (kPa)	Flow Rate (ml/min)	Geometry
Pin-fin	**0.269**	**28.23**	**70**	**D=150µm, Pitch=225µm, H_{fin}=200µm**
Microchannel	**0.27**	**18**	**75**	**Ww=Wc=80µm H_{ch}= 350µm**

A staggered pin-fin heat sink is shown to have a thermal resistance as low as 0.269^{o}C/W, when circulating cooling liquid at a flow rate of 70 ml/min in a heat sink where the pin-fins have a height of 200µm. The microchannel heat sink is shown to have a thermal resistance of 0.27^{o}C/W, when circulating cooling liquid at a flow rate of 75 ml/min in a heat sink where the microchannels have a height of 350µm. While the pressure drop in the microchannel heat sink is lower than that of the pin-fin heat sink, the height of the pin-fin heat sink is only 57% of the height of the microchannel heat sink. Consequently, ease of electrical TSV fabrication and improved electrical TSV

performance could be achieved by implementing a pin-fin heat sink as the cooling solution for thermal management of high-performance microprocessors in a 3D chip stack [5.5].

5.10. Summary

Chapter 5 describes the experimental thermal measurement test-bed for evaluating a 3D inter-layer liquid cooling platform that has been developed. Experimental thermal testing results for an air-cooled chip and a liquid-cooled chip are compared. The on-chip integrated microchannel heat sink is shown to have a thermal resistance of >0.28 °C/W and cooling of >100W/cm^2 high-power density chip at an average junction temperature of less than 50°C is demonstrated. Electrical and fluidic interconnection between layers is also demonstrated. Cooling liquid is circulated through the 3D stack at flow rates of up to 100 ml/min.

Preliminary fabrication results for an alternative pin-fin heat sink technology are demonstrated, and the advantages of the pin-fin heat sink compared to the microchannel heat sink technology are discussed.

CHAPTER 6

CONCLUSION AND FUTURE WORK

This chapter provides a summary of the key results presented in the dissertation. Additionally, ideas regarding how this work may be extended in future research efforts are discussed.

6.1. Opportunities for Future Work

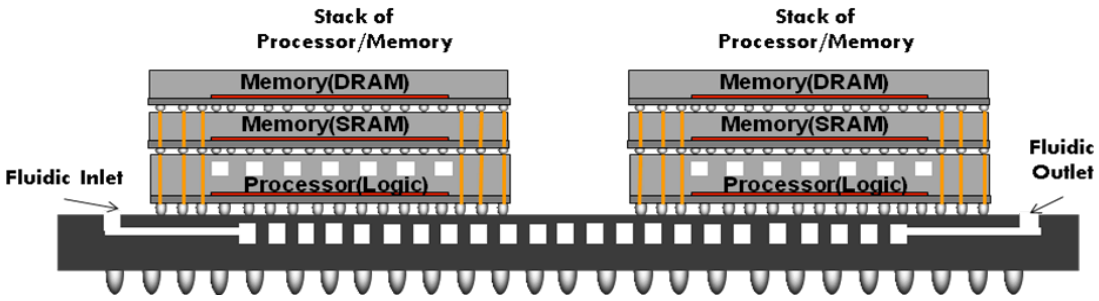
1. High density C4 electrical I/Os and integrated fluidic I/Os

In this work, an electrical I/O density of 1600/cm^2 is demonstrated. However, according to ITRS projections, high-performance chips in a 3D stack may have up to 9000 die-to-die bonds by the year 2022 [1.11]. Consequently, high-density electrical I/O interconnections will be necessary. There is an opportunity for future work to demonstrate high density electrical I/O interconnections integrated with fluidic I/O interconnections.

2. Demonstration of silicon carrier for supplying liquid to multiple 3D chip stacks

This work demonstrates fluid being supplied to the microchannels in the 3D chip stack by inlet channels that are fabricated in the bottom layer of the 3D stack. According to the ITRS, as shown in Table 1.2, there could be up to 10 high-performance chips in a 3D package by the year 2022 [1.11]. Having this many chips in a package could require that there be multiple 3D chip stacks that contain high-performance processors. Consequently, if microfluidic cooling were implemented as the cooling solution, the

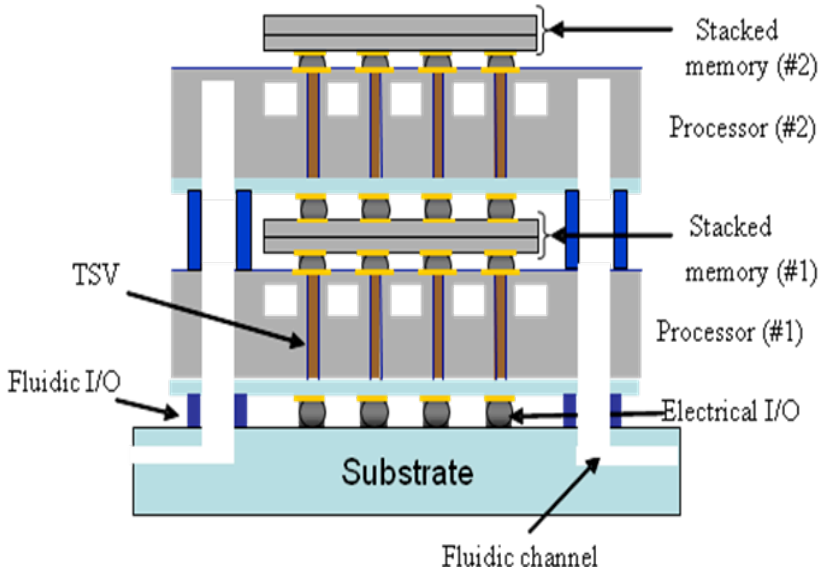
substrate on which the 3D ICs are stacked will be an important component of the 3D system. There is an opportunity for future experimental work in the implementation of a silicon carrier with integrated electrical and microfluidic interconnect networks. Within the silicon carrier, integrated fluidic interconnections can be developed to enable the routing of a coolant to multiple stacks of 3D ICs bonded on the silicon carrier.



3. Demonstration of polymer fluidic I/Os that supply liquid to multiple CPU chips in the 3D chip stack

As the design of 3D chip stacks that contain high-performance microprocessors becomes more complex, future 3D stacks have the potential to include multiple memory chips and multiple processor chips, such as the configuration shown in Figure 6.X.

In order to route fluid to high-performance processors in the 3D stack, a fluidic I/O technology that can traverse longer distances may be required (equivalent to the thickness of multiple memory chips). There is an opportunity to stack multiple memory and processor chips, while using polymer fluidic I/Os to supply liquid to multiple processor chips in the 3D stack.



4. Independent control of liquid coolant supplied to each layer of the 3D stack

In this work, fluidic is supplied to microchannels in the 3D chip stack by inlet channels that are fabricated in the bottom layer of the 3D stack. Because the inlet channels are in the bottom layer of the stack, fluid is easily supplied to the microchannels in the bottom layer of the stack. For fluid to be circulated to channels in each ascending layer, a sufficient fluid flow rate (and pumping power) must be applied to the microfluidic system in order for channels in the ascending layers in the stack to receive a sufficient amount of fluid for cooling. Alternative system configurations should be investigated to analyze the benefits of independent fluid flow to each level in the 3D stack.

6.2. Conclusion

Three-dimensional integration is a promising technology that offers many advantages including increased device density, shorter interconnect distances, system performance enhancements, decreased system form factor, and integration of

heterogeneous technologies in the same chip stack. However, heat removal is a primary limiter of stacking high-performance microprocessors in a 3D chip stack. This research has demonstrated the design, fabrication, assembly, and experimental testing of a 3D integration platform that can support the heat removal requirements for high-performance chips.

6.2.1. Development of Inter-layer Liquid Cooling Platform for Thermal Management of 3D Integrated Circuits

Using microchannel inter-layer liquid cooling to facilitate cooling on each strata allows chips to be arranged in the 3D stack as needed to support the most efficient heat removal and power delivery methods. The proposed microchannel liquid cooling scheme can be used when stacking multiple processors, as this scheme significantly reduces the overall thermal resistance of the cooling system, removes thermal resistances associated with TIMs, reduces chip cooling hardware size from inches to microns, and enables cooling of >100W/cm^2 of each high-power density chip.

Back-end-of-the-line (BEOL) compatible, wafer-level batch fabrication and micromachining technologies are used to fabricate the necessary electrical and thermal interconnects for the proposed 3D platform. Each silicon die of the 3D stack contains a monolithically integrated microchannel heat sink, through-silicon fluidic vias used for fluidic routing in the 3D stack, solder bumps, and microscale fluidic I/Os on the side of the chip opposite to the microchannel heat sink. Fabrication results of the individual components and integration of the components is demonstrated. Fabrication processes for integrating microchannel heat sinks and electrical through-silicon vias are also demonstrated.

6.2.2. Compact Physical Modeling to Determine the Design Trade-offs for Microchannel Heat Sink and Electrical TSV Integration

In order to determine how to design the microchannel heat sink to meet future ITRS high-performance chip cooling requirements, compact physical modeling is used to analyze the impact of microchannel geometry and fluid flow rates on thermal resistance and pressure drop of the heat sink. Compact physical modeling is also used to explore the electrical TSV performance and microchannel heat sink cooling trade-offs when integrating microchannel heat sinks and electrical TSVs in a 3D chip stack.

Modeling results show that increased microchannel cooling capability requires increased wafer thickness. However, TSV fabrication becomes more difficult and TSV electrical performance decreases as wafer thickness increases. Furthermore, electrical TSV density increases as the width of microchannel wall increases, which decreases the number of microchannels that can be fabricated on the chip and thereby decreases cooling capability. Analyzing the trade-offs of microchannel heat sink cooling performance enables a better understanding of how to design a 3D system that contains integrated microchannel heat sinks and electrical TSVs.

6.2.3. Integrated Electrical and Fluidic I/O Technologies for 3D Inter-layer Cooling

In the demonstrated 3D cooling platform, microscale fluidic interconnection between strata is enabled by through-wafer fluidic vias and fluidic I/O interconnects. The fabrication and process integration techniques are outlined for three distinct fluidic I/O technologies including a C4 pipe fluidic I/O, an air-gap C4 fluidic I/O, and a polymer pipe fluidic I/O interconnect technology. Characterization of the electrical and fluidic I/O interconnect structures is performed, and an electrical I/O density of ~1600/cm^2 is

demonstrated. The advantages and disadvantages of the three fluidic I/O technologies are discussed.

6.2.4. 3D Chip Stacking Using Electrical and Fluidic I/O Interconnects

Significant challenges in using microfluidic cooling in a 3D chip stack are the flip-chip bonding processes required to stack microfluidic chips and the ability to seal the fluidic interfaces in the 3D stack in order to prevent fluid leakage.

The ability to assemble chips with integrated electrical and fluidic I/Os and seal fluidic interconnections at each strata interface is demonstrated using three assembly and fluidic sealing techniques. Assembly results show the stacking of up to four chips that contain integrated electrical and fluidic I/O interconnects. Fluidic testing is performed by circulating fluid through the 3D stack at flow rates up to 100ml/min, with no fluid leakage observed.

6.2.5. Thermal and Fluidic Testing of the 3D Cooling Platform

Chapter 5 describes the experimental thermal measurement test-bed for evaluating the 3D inter-layer liquid cooling platform that has been developed. Experimental thermal testing results for an air-cooled chip and a liquid-cooled chip are compared. The on-chip integrated microchannel heat sink is shown to have a thermal resistance of >0.28 °C/W and cooling of >100W/cm^2 high-power density chip at an average junction temperature of less than 50°C is demonstrated. Microchannel heat sink cooling shows a significant junction temperature and heat sink thermal resistance reduction compared to air-cooling.

Preliminary fabrication results for a pin-fin heat sink technology are demonstrated, and the advantages of the pin-fin heat sink compared to the microchannel heat sink technology are discussed.

APPENDIX A

PUBLICATIONS BASED ON PRESENTED RESEARCH

Conference Proceedings:

[1] **C.R. King,** J. Zaveri, H. S. Yang, M. S. Bakir, and J. D. Meindl, "Electrical and Fluidic C4 Interconnections for Inter-layer Liquid Cooling of 3D ICs," 60th Electronic Components and Technology Conference, Las Vegas, NV, June 2010.

[2] **C.R. King**, J. Zaveri, H. S. Yang, M. S. Bakir, and J. D. Meindl, "Electro-fluidic C4 Interconnections for Inter-layer Liquid Cooling of 3D ICs," SRC TECHCON, Austin, TX, September 2009.
-Received Packaging and Cooling "Best in Session" Paper Award

[3] **C.R. King,** D. Sekar, M. Bakir, B. Dang, J. Pikarsky, J. Meindl, "3D Stacking of Chips with Electrical and Microfluidic Interconnects," in Proc. IEEE 58th Electronic Components and Technology Conference, Lake Buena Vista, FL, May 27-30, 2008.
-Received ECTC Motorola Electronic Packaging Fellowship Outstanding Paper Award

[4] **C.R. King,** D. Sekar, M. Bakir, B. Dang, J. Pikarsky, J. Meindl, "3D Chip Stacking with Inter-layer Liquid Cooling," SRC TECHCON, Austin, TX, November 2008.

[5] **C.R. King,** D. Sekar, M. Bakir, B. Dang, J. Pikarsky, J. Meindl, "Assembly Techniques for Microfluidic Networks in Three-dimensional Integrated Circuits," SRC TECHCON, Austin, TX, September 10-12, 2007.

[6] Y. Zhang, **C. R. King**, J. Zaveri, Y. J. Kim, V. Sahu, Y. Joshi, M. S. Bakir, **"**Coupled Electrical and Thermal 3D IC Centric Microfluidic Heat Sink Design and Technology**,"** in Proc. IEEE 58th Electronic Components and Technology Conference, Lake Buena Vista, FL, May 31 - June 3, 2011.

[7] J. Zaveri, **C. King Jr.**, H.S. Yang, M.S. Bakir, "Wafer-level Batch Fabrication of Silicon Microchannel Heat Sinks and Electrical Through Silicon Vias for 3D ICs," IMAPS 42nd International Symposium on Microelectronics, San Jose, CA, November 2009. *-Received IMAPS Best Student Paper Award*

[8] J. Zaveri, **C.R. King,** H. S. Yang, and M. S. Bakir, "Wafer-level Batch Fabrication of Silicon Microchannel Heat Sinks and Electrical Through-silicon Vias," SRC TECHCON, Austin, TX, September 2009.

[9] D. Sekar, **C. King,** B. Dang, M. Bakir, J. Meindl, "Removing heat from 3D stacked chips," Future Fab International, Vol. 29, vol. 4, pp. 80-85, April 2009. (*invited*)

[10] D. Sekar, **C. R. King,** B. Dang, T. Spencer, H. Thacker, P. Joseph, M. Bakir and James Meindl," A 3D-IC Technology with Integrated Microchannel Cooling," IEEE International Interconnect Technology Conference, Burlingame, CA, June 1-4, 2008. -*Received IITC Best Student Paper Award*

[11] M. S. Bakir, **C. King**, D. Sekar, H. Thacker, B. Dang, G. Huang, A. Naeemi, and J. D. Meindl, "3D heterogeneous integrated systems: liquid cooling, power delivery, and implementation," in Proc. IEEE Custom Integrated Circuits Conference, 2008.

[12] M. S. Bakir, **C. King**, D. Sekar, and B. Dang, "Electrical, Optical, Thermal Interconnect Networks for 3D Heterogenous Integrated Systems," in Proc. IEEE Avionics, Fiber-Optics and Photonics Conference, 2008.

[13] M. S. Bakir, P. A. Thadesar, **C. King**, J. Zaveri, H. S. Yang, C. Zhang, Y. Zhang, "Revolutionary Innovation in System Interconnection: New Era for the IC," in Proceedings of SPIE Photonics West, January 2011.

[14] T. Shodeinde, M.S. Bakir, **C. R. King**, "Sidewall Metallization of High Aspect Ratio Perpendicular Polymer Structures for Chip I/O Interconnections," National Nanotechnology Infrastructure Network (NNIN) REU Convocation, Cornell University, Ithaca, NY, August 2006.

Journal Publications:

[1] B. Dang, M. Bakir, D. Sekar, **C. King**, and J. Meindl, "Single and 3D chip cooling using microchannels and microfluidic chip input/output (I/O) interconnects," IEEE Trans. Adv. Packaging, January 2010.

[2] M. Bakir, G. Huang, D. Sekar, and **C. King**,"3D system integration: power delivery, cooling, and signaling," IETE Technical Review, November 2009. (invited)

[3] J. Lai, H. Yang, H. Chen, **C. King**, J. Zaveri, R. Ravindran, and M. Bakir, "Improved through-silicon-via fabrication for thick wafers containing MEMS and sensor devices," J. of Microelectromechanics & Microengineering, 2010.

Patents:

[1] **C. R. King**, J. Zaveri, M. S. Bakir, and J. D. Meindl, "Air-Gap C4 Fluidic I/O Interconnects and Methods of Fabricating Same," filed March 2012, Serial No.: 13/416,948, *patent pending*.

[2] M. S. Bakir, D. Sekar, **C.R. King**, B. Dang, J. Meindl, "3D ICs with Microfluidic Interconnects," issued April 19, 2011, patent number 7,928,563.

Book Chapter:

[1] B. Dang, M. Bakir, D. Sekar, **C. King,** and J. Meindl, "Single and 3D Chip Cooling using Microchannels and Fluidic I/Os," in *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*, M. Bakir and J. Meindl (Eds.), Artech House, 2008. (invited)

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