POLYLITHIC INTEGRATION USING FUSED-SILICA STITCH-CHIPS FOR RF/MM-WAVE SYSTEMS: SIMULATION, FABRICATION, AND CHARACTERIZATION

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POLYLITHIC INTEGRATION USING FUSED-SILICA STITCH-CHIPS FOR RF/MM-WAVE SYSTEMS: SIMULATION, FABRICATION, AND CHARACTERIZATION

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To my family

for their infinite caring, support, understanding,

and most importantly, LOVE.

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3GPP 3rd Generation Partnership Project

5G Fifth-Generation

AiP Antenna in Package

AJP Aerosol Jet Printing

AMD Advanced Micro Devices

BEOL Back End Of Line

BiCMOS Bipolar CMOS

CMI Compressible MicroInterconnect

CMOS complementary metal-oxide semiconductor

COTS commercial-off-the-shelf

CoWoS Chip-on-Wafer-on-Substrate

CPW Coplanar Waveguide

CTE coefficient of thermal expansion

D2D Die-to-Die

DA Driver Amplifier

DSP Digital Signal Processing

DUT Device Under Test

EMIB Embedded Multi-die Interconnect Bridge

EUV Extreme Ultra-Violet

eWLB Embedded Wafer-Level Ball-grid array

FE Front-End

FinFET Fin Field-Effect Transistor

FR2 Frequency Range 2

GaAs Gallium Arsenide

GaN Gallium Nitride

HBM High Bandwidth Memory

HEMT High-Electron-Mobility Transistor

HI Heterogeneous Integration

HPC high performance computing

IBM International Business Machines

IC integrated circuit

ICP Inductive Coupled Plasma

IMC intermetallic compound

imec Interuniversity MicroElectronics Centre

InFO Integrated Fan-Out

InP Indium Phosphide

IP intellectual property

KGD Known Good Die

LE-DPAM Laser-Enhanced Direct Print Additive Manufacturing

LNA Low Noise Amplifier

LTCC Low Temperature Co-fired Ceramics

MECA Metal-Embedded Chip Assembly

MMIC Monolithic Microwave Integrated Circuit

PA Power Amplifier

PECVD Plasma-Enhanced Chemical Vapor Deposition

PI-FSSC polylithic integration using fused-silica stitch-chips

PMC Perfect Magnetic Conductor

RDL redistribution layer

RF Radio Frequency

SEM Scanning Electron Microscopy

Si Silicon

SiC silicon carbide

SoC System on Chip

SOLT Short-Open-Load-Thru

TDR Time Domain Reflectometry

TEM Transverse ElectroMagnetic

TIM thermal interface material

TRL Thru-Reflect-Line

TSMC Taiwan Semiconductor Manufacturing Company

UF UnderFill

SUMMARY

Packaging innovations are driven by applications today that include artificial intelligence and Fifth-Generation (5G) wireless communication. For Radio Frequency (RF)/mm-wave systems in 5G, it is critical to manage the losses and the impedance at the package-level. Given the high-loss and significant impedance mismatch caused by current wire/ribbon bonding technologies, a low-loss and impedance-matched fused-silica stitch-chip technology is proposed and studied in this dissertation to replace lossy wire/ribbon bonds for RF/mm-wave systems packaging. In addition, the stitch-chip technology is demonstrated for the first time using active Monolithic Microwave Integrated Circuit (MMIC) chiplets.

Firstly, the RF characterization using a thru-only and an L-2L de-embedding technique is validated to extract the S-parameters and frequency-dependent parasitics of the stitch-chip channel and Compressible MicroInterconnect (CMI). The CMI's fabrication processes are developed on the fused-silica substrate for the first time. The measurements are compared with state-of-the-art, which show lower loss than Silicon (Si)-based technologies and similar loss as other technologies, such as glass interposer technology, organic substrate technology, and Integrated Fan-Out (InFO) technology.

Secondly, to explore impedance matching using the stitch-chip technology, a passive testbed using a high-resistivity silicon package substrate is utilized. To minimize the impedance discontinuity at the interface of the stitch-chip and the package substrate, an RF-mechanical co-design methodology for the CMI is established. A stitch-chip is designed, fabricated, and assembled on the package substrate to characterize its impedance through Time Domain Reflectometry (TDR), which shows a significant impedance improvement compared with an equivalent wire-bond. The fused-silica stitch-chips accommodate pad pitch differences, package material differences, and die thickness variance.

Thirdly, an embedded Low Noise Amplifier (LNA) single-chip module using the fused-silica stitch-chip technology is experimentally demonstrated, which can be developed fur-

ther for RF/mm-wave multi-chip module. The linear gain performance of the module is measured and used to calculate the package and interconnect losses. The return-losses are also measured. The module performance is comparable to or better than state-of-the-art. Steady-state thermal simulations are also performed to understand the module's thermal capability. The case studies, including Die-to-Die (D2D) interconnect length, the transition of stitch-chip to package, and power supply interconnect on the stitch-chip, are performed for the RF/mm-wave multi-chip module using the stitch-chip technology.

Lastly, two frequency-dependent parasitics extraction methodologies up to 100 GHz are reviewed for fine-pitch ($<$50 μm) off-chip I/O that can be potentially utilized in the stitch-chip technology. The impact of underfill, substrate, I/O pitch scaling, and I/O ground-signal configuration are explored and compared among solder bump, micro-bump, and hybrid-bond. When the pitch is within 50 μm to 30 μm, the solder bump shows higher electrical parasitics than the micro-bump. Hybrid-bond shows the lowest electrical parasitics that can enable low-loss and fine-pitch signal routing at 2-10 μm pitch. Adding more ground I/Os around the signal I/Os can be a potential solution to reduce I/O resistance and inductance.

CHAPTER 1
INTRODUCTION AND BACKGROUND

5G wireless technology has become a key driver for semiconductor technology development beyond 2020, as shown in Figure 1.1 by Taiwan Semiconductor Manufacturing Company (TSMC). This fact was amplified as the need to connect people remotely significantly increased in 2020 due to the COVID-19 pandemic. Millimeter-wave technology is a critical component in 5G wireless communication, which is revolutionary in terms of the data transfer speed and extremely low latency [2], [3]. The fast data rates and low latencies in such 5G wireless systems require mm-wave frequency bandwidth between 24.25 GHz to 52.6 GHz, which is called Frequency Range 2 (FR2) defined by 3rd Generation Partnership Project (3GPP). However, the high-frequency bandwidth leads to the increasing complexity of mm-wave system packaging and interconnection as maintaining characteristic impedance and low-loss interconnection in common package transitions and materials presents many hurdles.

In this chapter, the driving design and technology factors in mm-wave systems, such as 5G RF Front-End (FE), are discussed in detail. The evolution of packaging architectures for RF/mm-wave systems and their interconnection challenges are reviewed. To overcome the challenges in RF/mm-wave system packaging, a polylithic integration technology using fused-silica stitch-chips is designed, fabricated, assembled, and tested; this effort, along with the integration of the stitch-chips with active mm-wave chiplets, represents the main focus of this thesis.

1.1 From Monolithic to Polylithic Integration

Moore's law predicts transistor density increase based on economic benefits [4]. Such increase in transistor density also significantly boosts the computing capability and enables

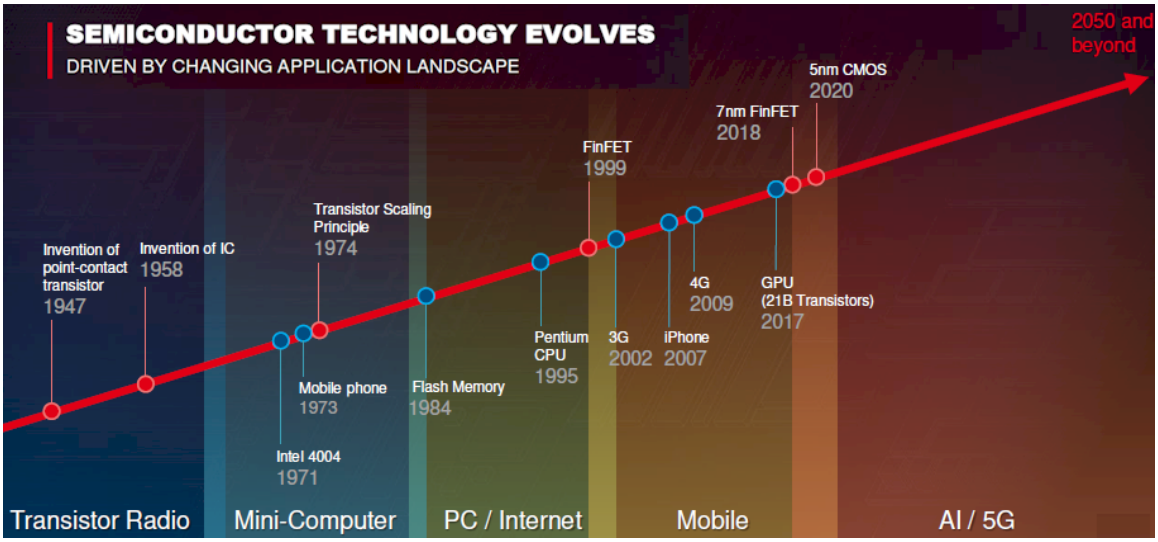
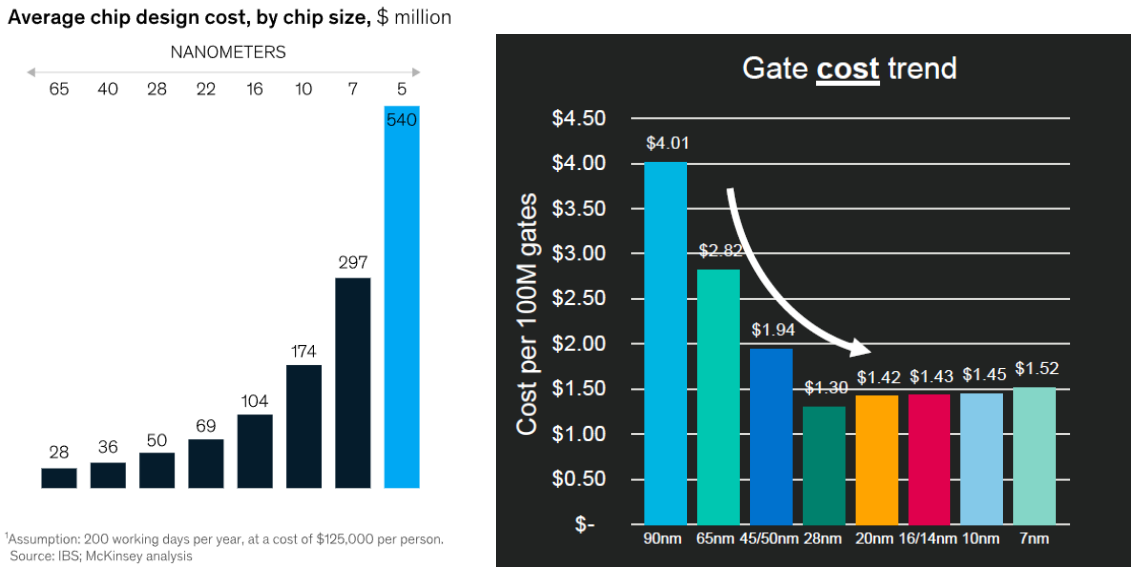


Figure 1.1: Application driving semiconductor technology evolution [1]

the integration of multiple functionalities into one single chip (System on Chip (SoC)). Transistor density scaling was enabled by transistor geometric size scaling till the 1990s and then by device innovation, such as strained gate channel, high-K metal gate channel, and Fin Field-Effect Transistor (FinFET) [5]. The increased device complexity resulted in increased process complexity, which requires advanced technologies such as Extreme Ultra-Violet (EUV) lithography and materials, which in turn rapidly increases the design cost for next-generation technology nodes. As shown in Figure 1.2a and [6], the design cost for 5 nm technology is approximately 1.82 times higher than 7 nm technology. The ever-increasing design and fabrication costs are neutralizing the expected cost-reduction benefits from continued technology scaling. For example, as reported by Marvell Technology and shown in Figure 1.2b, the cost per 100M gates appears to have stopped decreasing beyond 20 nm technology.

This phenomenon is attributed to the slowing down of process technology nodes development, as shown in Figure 1.3. In Figure 1.3a, AMD states that the industry is unlikely to follow Moore's Law in a sustainable manner [9], and [10] reports a similar vision.

Ever-larger die areas are needed for the integration of multiple functionalities into a single chip (SoC) to meet the ever-increasing computing needs as captured in Figure 1.4.

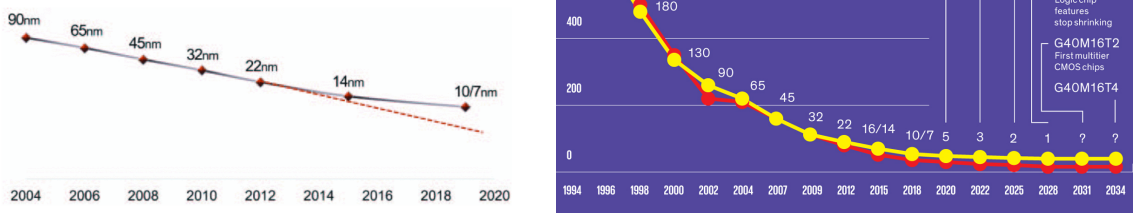


(a) (b)

Figure 1.2: (a) Average design cost of technology from IBS; McKinsey analysis [7] and (b) gate cost trend with semiconductor technology node [8]

However, as shown in Figure 1.4, the current die size has reached the lithographic reticle limit ($\sim$858 mm^2), which is the practical area limit size of silicon die that can be manufactured. Although mask stitching technology has been developed for passive devices and demonstrated to manufacture the second-generation Chip-on-Wafer-on-Substrate (CoWoS) interposer technology of TSMC with 1200 mm^2 area (1.5x larger than a full reticle size die) [11], there can be some extreme challenges for production facilities and design flexibility, especially for active devices. In addition, a larger die increases the possibility of defects on the die, which can result in lower manufacturing yield and higher costs.

In Gordon Moore's paper "Cramming More Components onto Integrated Circuits", Moore states that interconnecting functions at the package level to build larger systems could be more economical than continued monolithic integration [4]. Inspired by his prediction and given the aforementioned challenges of monolithic integration (SoC), technology innovation at the package level, such as polylithic integration or HI is being pursued today in both academia and industry. For digital applications, HI has provided an aggressive transistor count scaling timeline compared to a monolithic integration, as shown in



(a) (b)

Figure 1.3: (a) Approximate introduction dates of technology nodes predicted by Advanced Micro Devices (AMD) [9] and (b) next-generation technology nodes development trend [10]

Figure 1.5. For example, in Figure 1.5, TSMC's CoWoS technology provides more aggressive transistor scaling by integrating High Bandwidth Memory (HBM) [11].

HI has already proven to be a cost-efficient system integration method. By reducing the size of each die/chiplet for HI, the overall yield of the system increases and the overall cost reduces. Such cost-benefits of HI are more apparent when compared with a monolithic die with similar circuit blocks, as captured in Figure 1.6a. In addition, HI unlocks a mix-and-match methodology for system integration, which drives the cost even lower. For example, in [9], AMD splits and integrates core-complex dice (CCD) that are manufactured by a 7 nm process for significant improvements on transistor speed and power efficiency, while I/O die (IOD) is made by mature and cost-effective 12 nm process and set in the middle of the package. The overall cost of this configuration is compared with its monolithic equivalent, as shown in [9] and Figure 1.6b. Figure 1.6b shows the overall cost of implemention by HI is significantly lower than any monolithic counterpart across all potential configurations. Furthermore, Known Good Die (KGD) testing before final integration can be utilized for HI to improve system yield and reduce overall cost along with better control of the system performance.

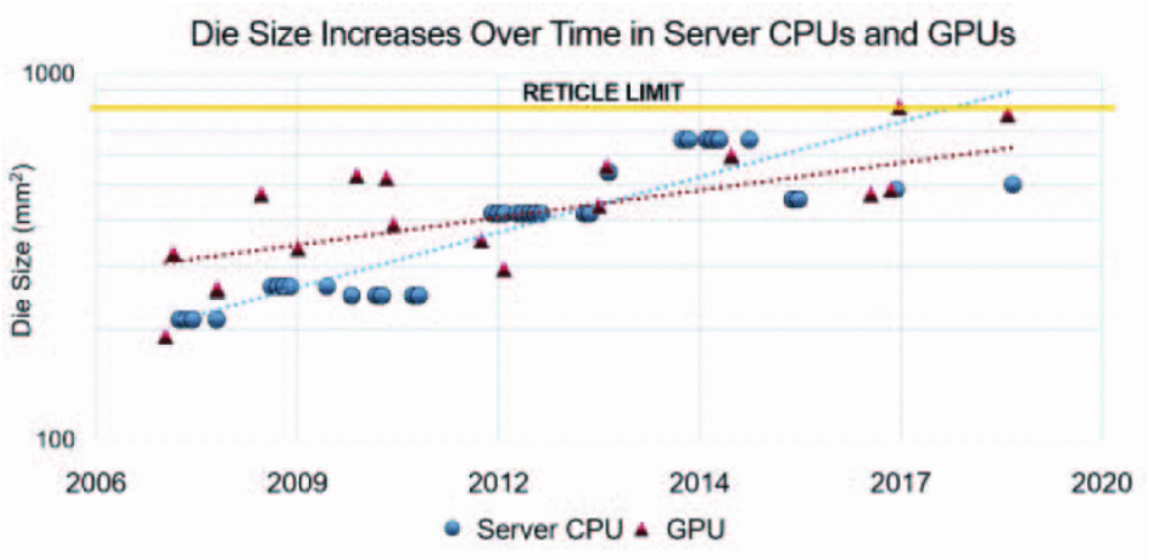


Figure 1.4: Die size increasing for SoC [9]

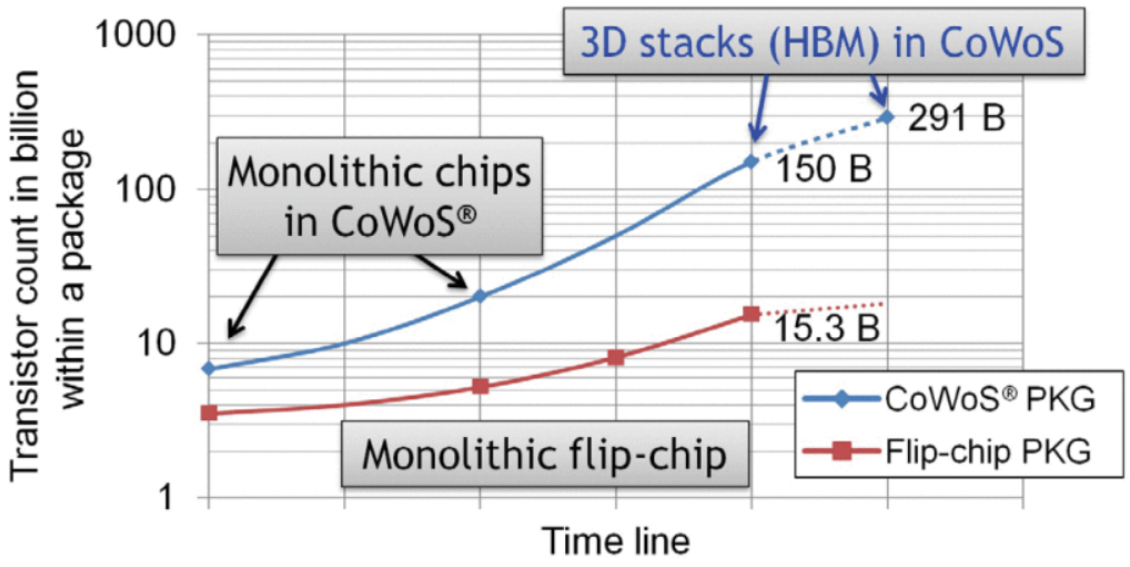
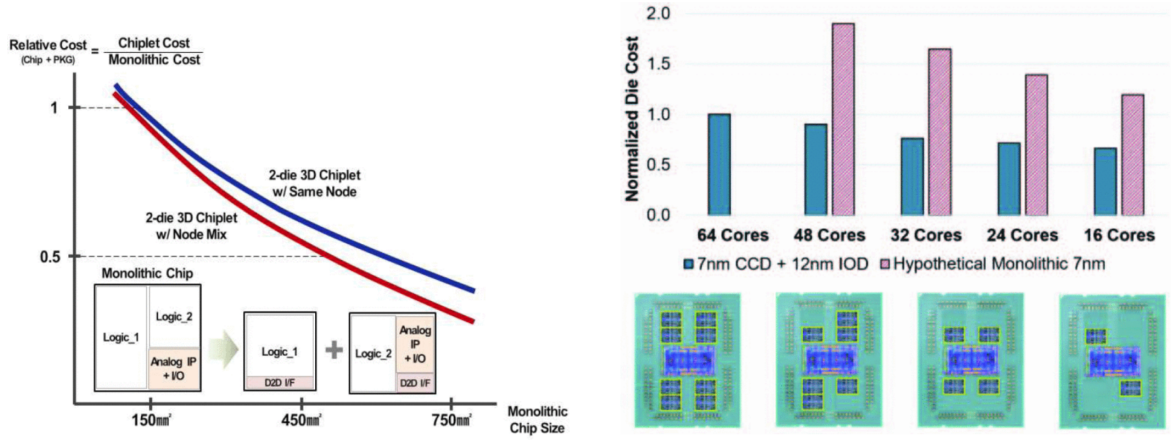


Figure 1.5: Transistor count comparison between Heterogeneous Integration (HI) pathway and its monolithic pathway [11]



(a) (b)

Figure 1.6: (a) Relative cost of HI against monolithic counterpart with chip size [12] and (b) normalized cost comparison between HI and hypothetical monolithic die for AMD EPYC™ processor [9]

1.1.1 Motivation of polylithic integration for RF/mm-wave systems

Besides device scaling, yield, and cost challenges, monolithic integration of an SoC lacks material and device integration flexibility, requires long time-to-market, and has poor thermal management for RF/mm-wave system packaging [13]. In addition, RF and I/O circuits will not be fully optimized if monolithically integrated with digital compute and memory because the requirements for RF, I/O, and digital are quite different [14]. For example, digital applications require optimization for density, power efficiency, and data rate, while RF/mm-wave systems need optimization for passives, higher voltage, and higher speed.

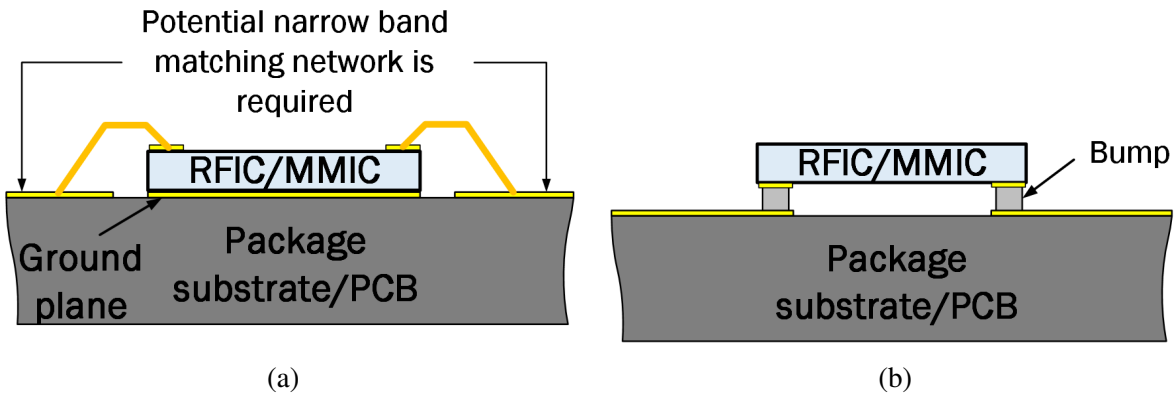
In contrast, the circuit mix-and-match methodology of polylithic integration or HI enables multi-chiplet interconnection and packaging for RF/mm-wave systems, where the chiplets or passives are made using different materials and processes such as Gallium Arsenide (GaAs)/Gallium Nitride (GaN) High-Electron-Mobility Transistor (HEMT) chiplets integrated with Si chiplet [15]. For example, an RF beamforming system consists of passives (e.g., an antenna array), RF/mm-wave LNA and Power Amplifier (PA) chiplets, and digital backend (e.g.,Si Digital Signal Processing (DSP)) [16]. Polylithic integration or HI enable the decoupling of the manufacturing constraints as well as the optimization of

the individual circuit functions such that RF/mm-wave chiplets, I/O chiplets, and digital chiplets are each electrically optimized separately and fabricated using process nodes optimized for the intended function [3], [13], [14], [17], [18]. This is the main motivator of polylithic integration for several applications including RF/mm-wave systems.

1.1.2 Requirements of interconnects in polylithic integration for RF/mm-wave systems

Given most components in RF/mm-wave systems scale with the operating frequency and wavelength, polylithic integration is developing towards highly-integrated and miniaturized modules, which drives new packaging paradigms [19]. For example, to avoid undesired grating lobes in the antenna radiation pattern, the antenna element's spacing should not be larger than the half wavelength (e.g., maximum 5 mm at 30 GHz). This in turn requires tight integration for LNA, PA, passives, and antenna elements, which presents significant challenges for the packaging. The packaging and integration requirements can be formulated as follows:

- Low-loss and low-parasitics interconnects are critical. For example, antenna element feed lines and interconnects between beamforming integrated circuit (IC)s and frequency conversion ICs should be able to route mm-wave signals with negligible loss and parasitics to improve the antenna efficiency [16], [20].
- Sufficient power transmission between the analog/RF ICs and the antenna elements require impedance matching throughout the signal path [3], [16].
- Miniaturization of the RF/mm-wave modules into smaller packages by densely integrating actives and passives.
- Reworkable interconnects that can reduce KGD testing cost and improve system assembly yield.
- Chiplet-based module integration for system functional scalability, intellectual property (IP) re-use, and lower time-to-market.



(a) (b)

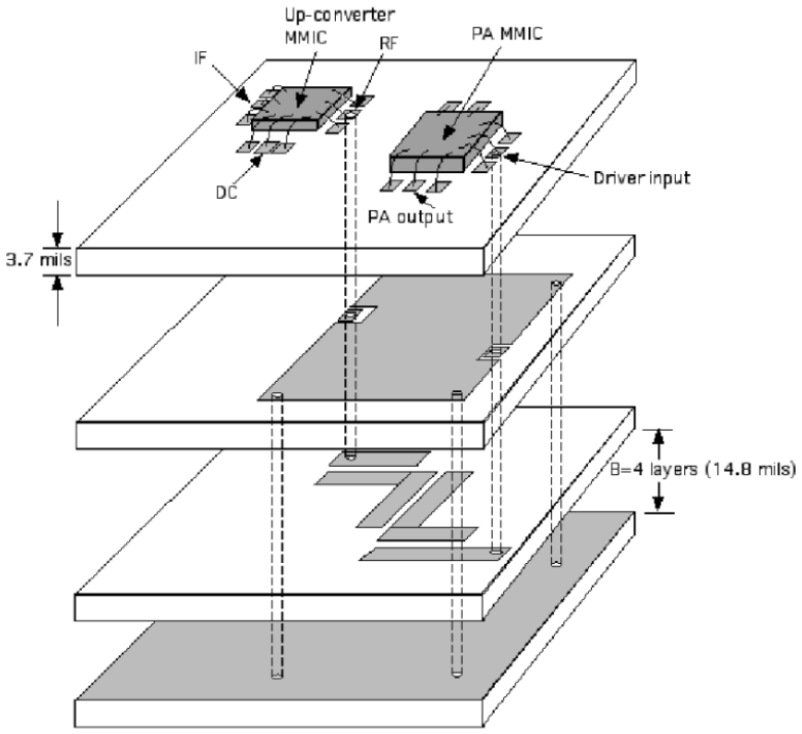
Figure 1.7: Packaging architecture schematics for RF/mm-wave systems: (a) wire-bonded module and (b) flip-chip module

1.2 Landscape of Prior Packaging Architectures for RF/mm-Wave Systems

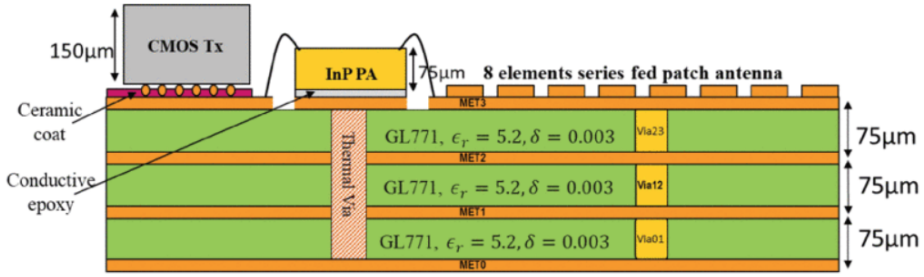
A landscape of current RF/mm-wave packaging technologies is reviewed in this section. As will be shown, there is a trend towards miniaturizing RF/mm-wave system packages to enable shorter interconnects, which intrinsically leads to better frequency response.

1.2.1 Architecture using wire-bonding

A conventional packaging architecture that is widely used in the packaging industry is the wire-bonded module, as shown in Figure 1.7a. Typically, an RFIC or MMIC die is attached on top of the ground plane of the package substrate, and wire bonds are utilized to connect die pads with package pads. Passives such as antenna array and filters can also be integrated on the package substrate to construct a fully integrated RF/mm-wave module, as shown in Figure 1.8. In Figure 1.8a [21], two MMIC dice (up-converter MMIC and PA) are wire-bonded on top of a multilayer Low Temperature Co-fired Ceramics (LTCC) package, while a filter is designed and integrated at the bottom layers of the package. The length of the wire bond is approximately 1 mm and is estimated to have a 2 dB loss at 14 GHz [21], [22]. In Figure 1.8b from [23], a Indium Phosphide (InP) PA die is attached on the ground plane on a LTCC package and wire bonded to the nearby antenna array. The wire is 450 μm long and requires a dedicated impedance-matching network to operate with the 135 GHz PA.

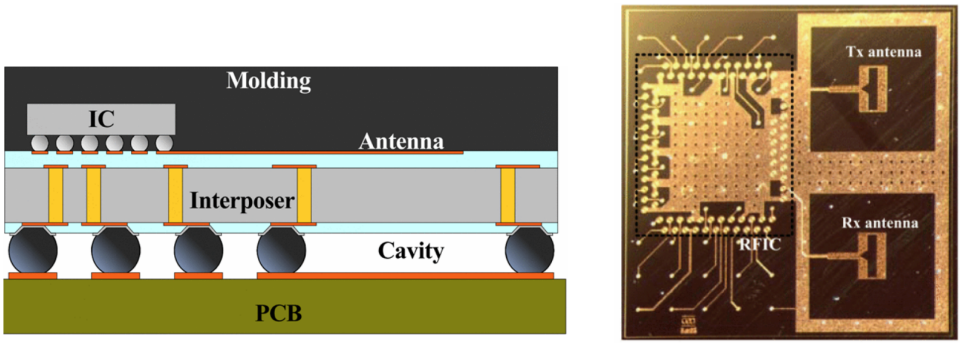


(a)



(b)

Figure 1.8: (a) An filter integrated underneath MMIC in a LTCC package [21] and (b) antenna array integrated on a LTCC package and next to InP PA die [23]



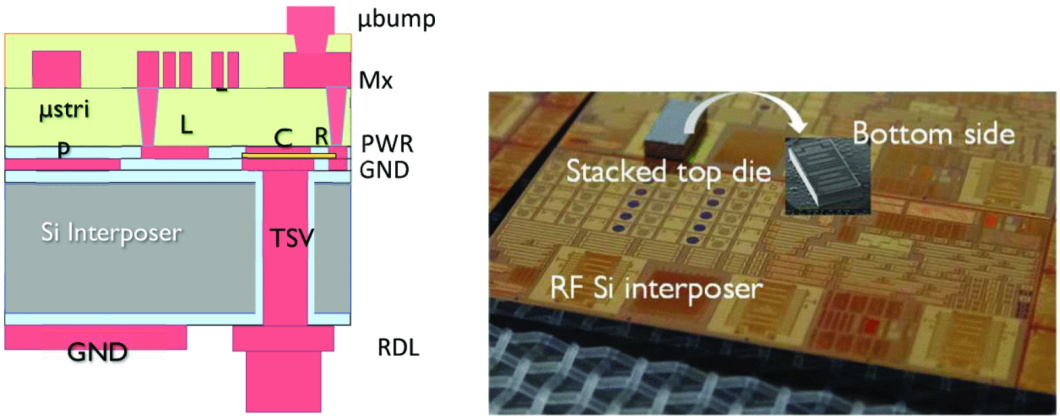
(a) (b)

Figure 1.9: High resistivity Si interposer technology for RF transceiver module from CEA-LETI [24]: (a) cross-sectional schematic and (b) bottom view

1.2.2 Architecture using flip-chip

To reduce the interconnect length and form factor, packaging architectures using flip-chip are also widely investigated in the packaging industry, as shown in Figure 1.7b. The RFIC or MMIC die is flipped and bonded (faced down) onto the package substrate; this places the device layer on the die in very close proximity to the package substrate. The I/O interconnects that can be used to bond the die and the package substrate include solder bumps with a diameter range of 100 μm to 300 μm, copper pillars with a diameter of below 50 μm, and hybrid bond with around 10 μm diameter for future dense RF/mm-wave signal routing. Similar to wire-bonded modules, passives can also be integrated into the package.

The first example is conventional Si interposer technology. The Si interposer technology is widely studied and used for digital computing applications such as high performance computing (HPC). For RF/mm-wave system packaging, the technology has been adapted by using relatively costly high resistivity Si to reduce high-frequency dielectric loss. For example, CEA-LETI demonstrated a 60 GHz transceiver module on high resistivity Si interposer technology: a 65 nm complementary metal-oxide semiconductor (CMOS) RFIC transceiver die was flip-chip bonded using solder balls (80 μm diameter) on the Si interposer with antennas at the side and then molded in a low-loss molding compound [24], as shown in Figure 1.9. Recently, imec demonstrated a cost-effective RF Si interposer using



(a) (b)

Figure 1.10: RF Si interposer technology from Interuniversity MicroElectronics Centre (imec) [25]: (a) cross-sectional schematic and (b) top view

CMOS grade Si substrate [25], as shown in Figure 1.10. The substrate loss is shielded by a 1 μm thick well-designed ground plane between the polymer dielectric and the substrate, and an 18 μm thick polymer dielectric layer is utilized to lower parasitic capacitance, which leads to line loss being as low as 0.3 dB/mm at 150 GHz [25]. The RFIC is expected to be flip-chip bonded using μbump (pitch in a range of 20-40 μm). In general, Si interposer technology using flip-chip is typically utilized for RF/mm-wave IC made by CMOS or Bipolar CMOS (BiCMOS) process and can provide fine-pitch mm-wave signal routing.

LTCC package can also be used with flip-chip technology to realize CMOS RFIC packaging. LTCC package benefits from its large number of metal layers, low coefficient of thermal expansion (CTE), and high thermal conductivity, which leads to flexibility of multilayer passive integration and better thermal robustness but suffers from larger I/O pitch ($>$125 μm) and size scalability due to dimensional limit of its screen-printing process and alignment accuracy [3]. One example is a 60 GHz phased-array system fully integrated into a LTCC package demonstrated by IBM [26], as shown in Figure 1.11a. An RFIC is flip-chip bonded to the bottom of the package through C4 bumps, while antenna arrays are at the top [26].

Besides the inorganic substrate materials used in the package (e.g., LTCC and Si), or-

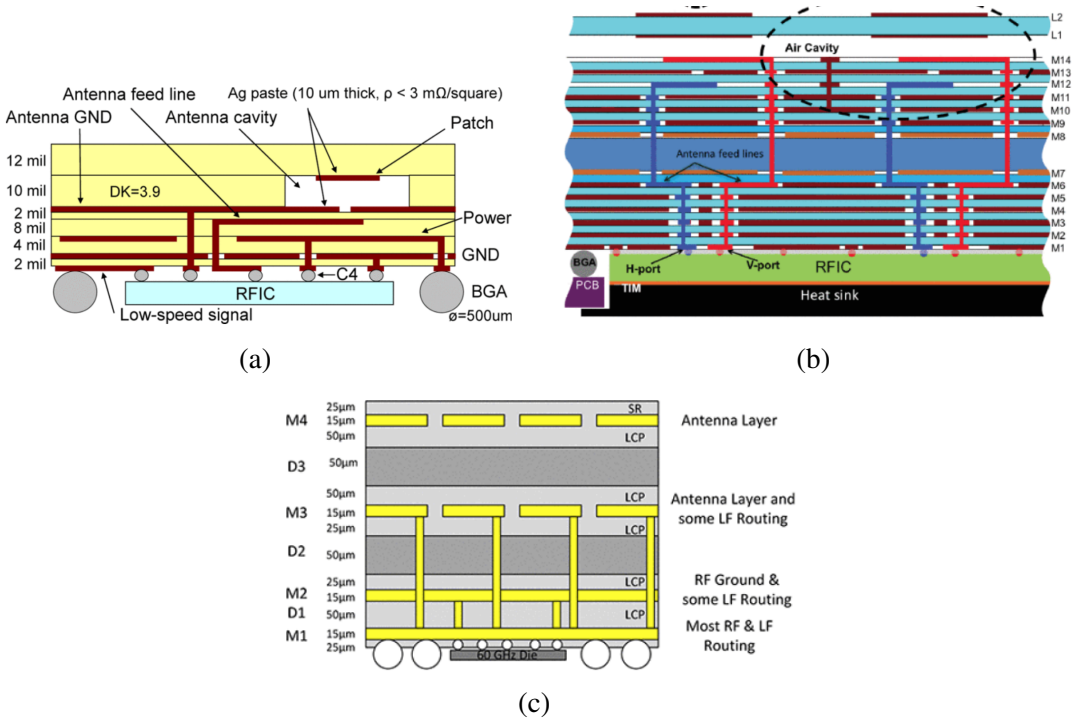


Figure 1.11: Cross-sectional schematics of non-Si packaging architectures using flip-chip technique: (a) LTCC package example from International Business Machines (IBM) [26], (b) organic package example from IBM [20], (c) organic package example from Intel [27]

ganic substrate materials are often used as well. The RF/mm-wave ICs are typically flip-chip bonded at the bottom of the package through solder balls or μbumps, while antenna or passives are fabricated at the top. The interconnects go through multilayers in the package to build the connections between the antenna or passives and the ICs. The organic substrate has low relative cost due to the current high volume manufacturing and possesses lower dielectric constant and loss tangent than Si and LTCC with the drawbacks of lacking fine-pitch interconnect routing as Si interposer technology. The examples are shown in Figure 1.11b from IBM [20] and Figure 1.11c from Intel [27].

1.2.3 Fan-out or IC embedding

A high-power amplifier die made of GaAs or GaN typically has two metal layers (one at the top of the substrate and one at the bottom), both of which require electrical connections in the package. However, flip-chip technology works better for CMOS or BiCMOS dice that

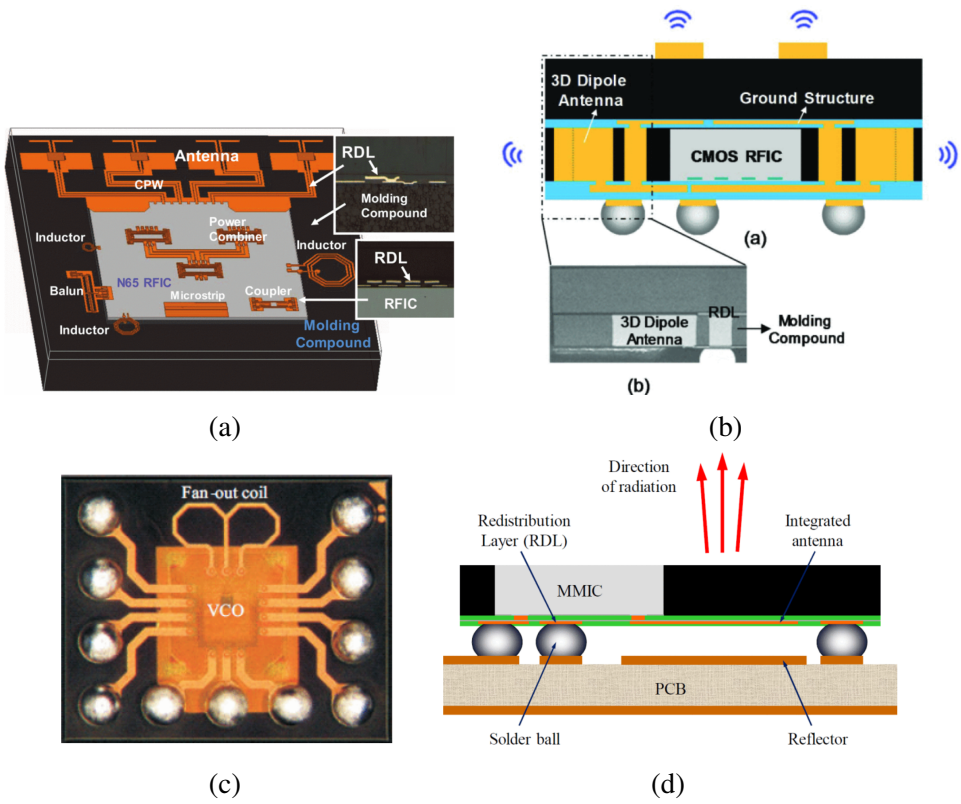


Figure 1.12: InFO wafer level packaging technology: (a) high-performance passives [28] and (b) Antenna in Package (AiP) module [29], and Embedded Wafer-Level Ball-grid array (eWLB) technology from Infineon: (c) 2D coil inductor demonstrated in eWLB [30] and (d) cross-sectional schematic of a 77 GHz transceiver module using eWLB [31]

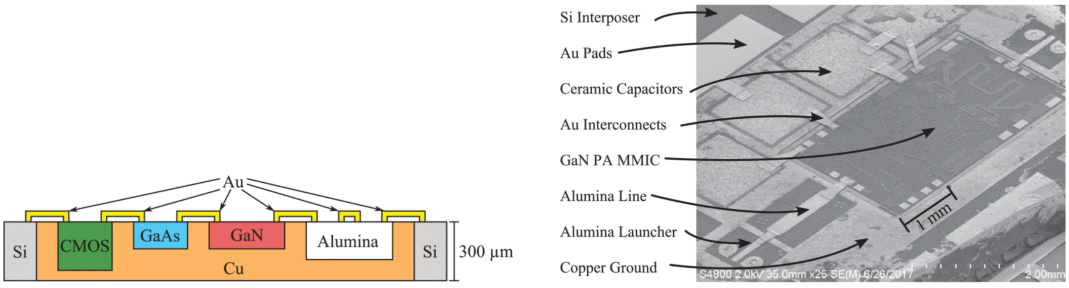
have only one-sided metal layers (Back End Of Line (BEOL)). Therefore, to further scale down the package size, decrease the length and the loss of interconnects, and incorporate with dice made of Si and III-V compound semiconductor processes, embedding IC and fan-out packaging architectures are evolving and become imperative. In such technologies, the dice are embedded in a package substrate or molded in polymer, and redistribution layer (RDL)s are formed directly on the die pads to fan out electrical signals from the die to the package.

There are two very important examples of fan-out packaging for RF/mm-wave systems in industry: InFO wafer level packaging from TSMC (as shown in Figure 1.12a and Figure 1.12b) and eWLB from Infineon (as shown in Figure 1.12c and Figure 1.12d). In [28] and [32], passives for RF/mm-wave systems, including inductor, antenna, transmission

lines, etc., are demonstrated using RDLs in an InFO package having low-loss dielectrics, fine-pitch and thick RDLs, and bumpless off-chip I/Os. The passives are measured to have a low loss (e.g., Coplanar Waveguide (CPW) has 0.35 dB/mm loss at 60 GHz) [28] and off-chip I/Os in InFO package are simulated to possess lower parasitics (e.g., 75% lower resistance) than μbump counterpart [32]. The InFO technology is also demonstrated as antenna in package modules for 5G applications [29], [33]. Although there are several potential challenges including die shifting and warpage [34], eWLB has been demonstrated with integrated 2D and 3D passives [30] and as 77 GHz transceiver module [31]. A 50 Ω CPW (minimum width/spacing is 15 μm) in eWLB package is measured to have 0.3 dB/mm attenuation at 80 GHz [31] and a ground-signal-ground through molding via (300 μm pitch and 100-150 μm diameter) is measured to have less than 0.5 dB loss up to 40 GHz [30]. The advancements in next-generation eWLB technology are multi-RDL for high-density signal routing and passives integration, lower thickness (0.5 mm) for portability, large size (12 mm $\times$ 12 mm) for more complicated system packaging, and 3D integration [35].

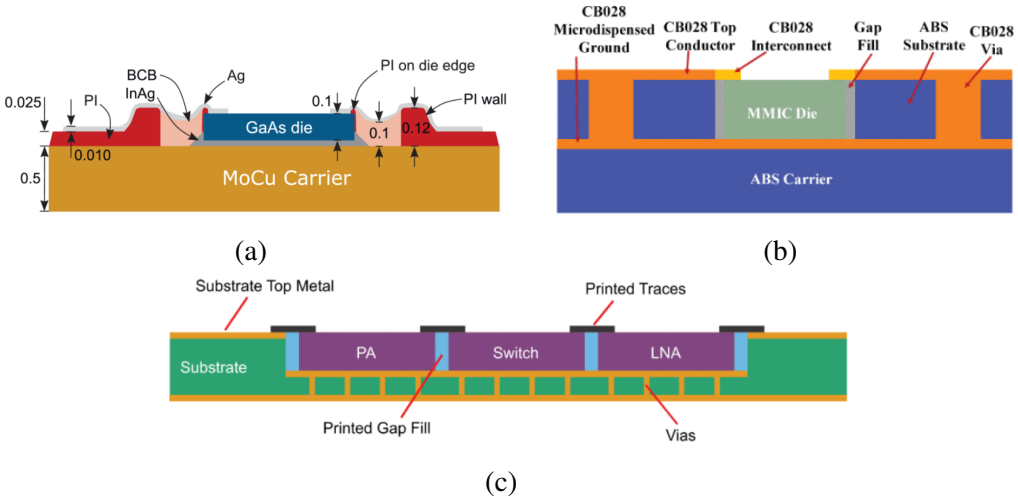
For embedding IC architecture, there are multiple advancements. HRL Laboratories developed Metal-Embedded Chip Assembly (MECA) technology to embed GaN PA circuits in high-resistivity Si or silicon carbide (SiC) interposer with backside metallization as ground and heat spreader [36]. The technology is proposed to enable the embedding of different dice, including CMOS, GaAs, GaN, and alumina dice, in a copper heat spreader which is also embedded in a Si interposer, as shown in [37] and Figure 1.13. The dice are interconnected with $\sim$360 μm long gold bridges, which are simulated to have less than 0.5 dB loss up to 100 GHz [37].

Additive manufacturing techniques for rapid prototyping of embedded ICs system are another recent advancement. Inkjet printing has been utilized to print interconnects for RF/mm-wave dice, which are embedded in an organic substrate as a front-end multi-chip module (Ka-band), as shown in Figure 1.14c and [38]. The interconnects printed in [38] are around 400 μm long. To enable multi-level and conformal printing, Aerosol Jet Printing



(a) (b)

Figure 1.13: MECA process to integrate different technologies using embedding IC architecture [37]: (a) cross-sectional schematic and (b) Scanning Electron Microscopy (SEM) image of embedded GaN PA using MECA process



(a) (b)

(c)

Figure 1.14: Cross-sectional schematics of embedding IC architectures using additive manufacturing techniques: (a) AJP technique [39] (b) LE-DPAM technique [40], and (c) inkjet printing technique [38]

(AJP) technique and Laser-Enhanced Direct Print Additive Manufacturing (LE-DPAM) technique are often utilized to print packages or interconnects instead of the inkjet printing [39], [40]. These two techniques have been demonstrated in a commercial-off-the-shelf (COTS) attenuator module [39], as shown in Figure 1.14a and a COTS W-band GaAs LNA module [40], as shown in Figure 1.14b.

Finally, a passive die embedded in a glass substrate with an antenna on top is recently demonstrated for operating in the D-band from Georgia Tech [41], as shown in Figure 1.15. The die is embedded in the glass core and two-layer RDLs are directly built on the die to fan

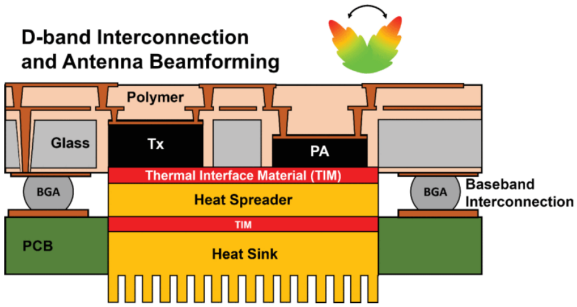


Figure 1.15: D-band module using die-embedded glass substrate [41]

out the RF signal to nearby antennas. The interconnects for die to package (two staggered vias and one RDL) are approximately 300 μm in length.

1.2.4 Interconnect challenges in prior packaging architectures

There are several challenges for the interconnects used in the aforementioned packaging architectures to meet the demands of interconnects in RF/mm-wave systems, which were summarized in section 1.1.2.

Firstly, although wire bonding and ribbon bonding techniques are mature and can be used for quick assembly, the wire bond's and the ribbon bond's geometry are not easy to predict and model, which creates a design challenge, especially for high-frequency applications. In addition, both wire-bond and ribbon-bond introduce high parasitic inductance at high frequencies, which requires capacitors designed on the package as a matching network to compensate. However, such compensation results in a reduction of operational bandwidth, which is not acceptable for wide-band applications and further increases the complexity of the design and fabrication [42]. Also, the matching network may increase package area overhead [43], which creates a challenge for the miniaturization of packaged RF/mm-wave modules. Moreover, a significant impedance mismatch [44] and radiation loss [45] compounded with the aforementioned design challenges and complexity causes significant challenges when using wire or ribbon bonding for future RF/mm-wave system packaging.

Secondly, the flip-chip technique can significantly decrease the interconnect length and cause less impedance discontinuity for wide-band applications. However, the flip-chip technique has a strict requirement on surface flatness for acceptable assembly yield and requires the package to withstand high-pressure and high-temperature bonding processes [46]. From a thermal perspective, the flip-chip technique naturally causes poor thermal dissipation, which prevents its wide usage for high-power applications such as PA die integration [47]. From an electrical perspective, the flip-chip technique introduces circuit performance detuning as it changes the dielectric environment of the active circuits on RF/mm-wave dice [48], which increases the assembly complexity such as tuning of underfill's dielectric properties [49]. In addition, the poor reworkability of the flip-chip technique creates a challenge to KGD methodology to improve the assembly yield and further lower cost.

Finally, die shifting and warpage are common challenges in fan-out technology [34], which may lower interconnect reliability and require more advanced process flow to compensate [50]. Interconnects fabricated by additive manufacturing techniques may have a worse resolution (10 μm), heavily depending on tool capability, and large process variations that cause inconsistency in the package electrical performance [39], which may need to be addressed further for the miniaturization of RF/mm-wave system module.

1.3 Polylithic Integration using Fused-Silica Stitch-Chips

To address the interconnects challenges in prior packaging architecture and meet the interconnects requirements for RF/mm-wave system packaging, a polylithic integration using fused-silica stitch-chips (PI-FSSC) technology is proposed in this thesis for RF/mm-wave chiplet-based module, as shown in Figure 1.16.

Firstly, similar to the trend of IC embedding in RF/mm-wave system packaging, COTS MMICs are embedded in cavities of the package substrate for smaller form factor and shorter interconnects. A shared RF internal ground plane is exposed at the bottom of the

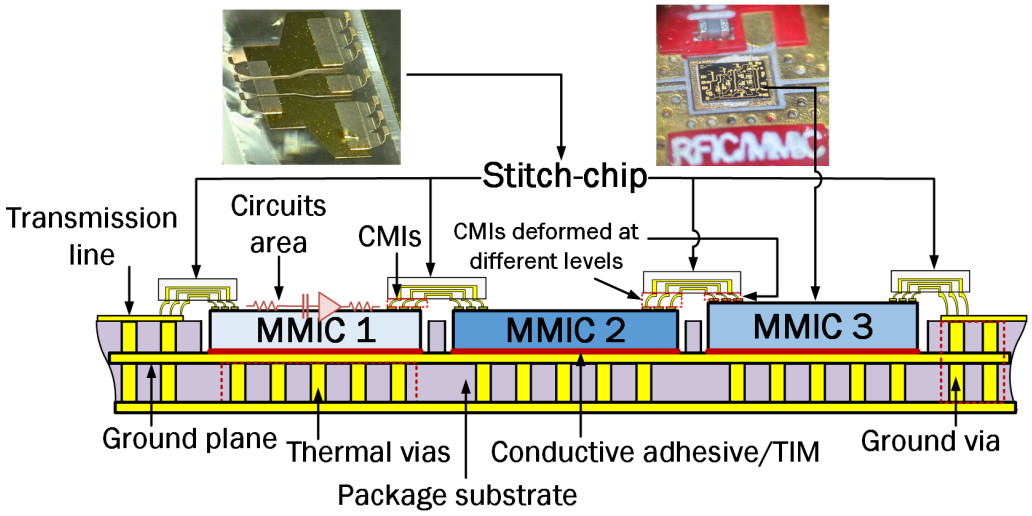


Figure 1.16: A schematic of the proposed polylithic integration using fused-silica stitch-chips

cavities. The MMICs are mounted on the ground plane by a conductive adhesive film that can also be used as thermal interface material (TIM). Structures such as thermal vias and heat sinks can be directly attached underneath the ground plane for better thermal management.

Secondly, fused-silica stitch-chips are utilized as die-to-die and die-to-package interconnects with the following features:

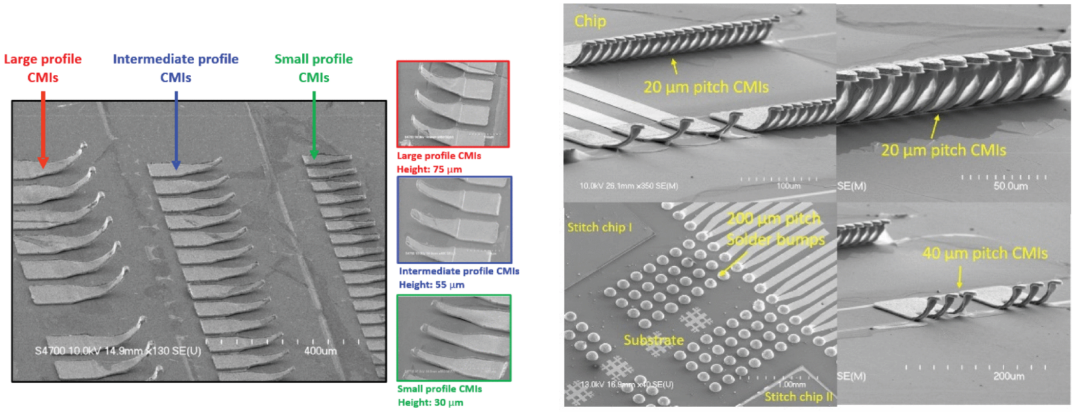
- Fused-silica is selected as the stitch-chip's substrate material for its low dielectric constant and loss tangent.
- The impedance of the stitch-chip is controlled to match the die pads' impedance for wide-band applications.
- Photolithography processes are utilized to fabricate the stitch-chip, which enables the fine-pitch scaling of the stitch-chip interconnects.
- Simplified and reworkable assembly process of stitch-chip enables complex RF/mm-wave system integration with improved assembly yield.

1.3.1 Compressible microinterconnects

Off-chip I/O is a vertical interconnect on the stitch-chip that is used to mate the die pads and stitch-chip's lateral interconnects (i.e. transmission lines). To realize simplified and reworkable assembly of the stitch-chip, CMI is selected as the off-chip I/O in current PI-FSSC technology.

CMI is a vertically flexible interconenct that is developed in [51] to enable HI of multi-die systems [52]. The CMI deforms elastically in a vertical direction with a pressure contact mechanism during assembly and provides temporary electrical connections, which are distinct from conventional metallurgical bonding such as solder bumps and microbumps. Currently, this type of interconnects are commonly used in die-level testing, socket system, interposer assembly [53], [54].

The mechanical flexibility of the CMI has been shown to improve thermomechanical reliability and mitigate thermal-induced package warpage due to CTE mismatch of different materials used in a single package [55], [56]. In addition, the assembly process for the CMI does not require high-temperature and high-assembly force, and intermetallic compound (IMC) does not form during the process. This is contrary to metallurgical bonding using solder, which may cause mechanical reliability issues such as cracking or delamination [57]. The CMI's ability to be compressed can make the stitch-chip adapt to the thickness variance of different dice/chiplets, which eliminates the strict requirement on the surface planarity for conventional flip-chip bonding. As shown in Figure 1.16, MMIC 3 is thicker than the MMIC 2, which causes the CMIs on the same stitch-chip to deform at different levels to compensate such die thickness variance. Furthermore, as the CMI provides a temporary connection, the stitch-chip can be easily detached from the package substrate and the die can be removed afterward. As such, system assembly can follow KGD strategy to improve system assembly yield and reduce assembly cost. CMIs, as pressure-based interconnects, are envisioned to be agnostic to the metal used on the receiving pads (Cu, Au, and Al pads, for example).



(a) (b)

Figure 1.17: SEM images of different fabricated CMI designs: (a) 30 μm, 55 μm, and 75 μm high CMI and (b) 20 μm and 40 μm pitch CMI [52]

The fabricated CMI has been proven to be free of plastic deformation in experiments: it can recover its original profile after 5000 cycles of 30 μm indentations [52]. Multiple heights and different in-line pitches of the CMIs have already been demonstrated to show the scalability of such off-chip I/O technology [52], as shown in Figure 1.17. Furthermore, a 30 μm by 30 μm pitch CMI array has also been fabricated and demonstrated in [58].

1.3.2 I/O scaling motivation

However, the CMI technique is not the only bonding technique for the proposed PI-FSSC technology. Other techniques such as solder bumping, microbumping using solder-capped copper pillar, and hybrid bonding can also be applied to the stitch-chip. These bonding techniques are commonly used in digital applications with the trend of further down-scaling pitches to achieve lower I/O delay and power consumption. The pitch scaling trend for such interconnects is shown in Figure 1.18. The scaling trend also matches the I/O requirements of future RF/mm-wave systems operating in the terahertz band because the size of the components and their spacing generally scale with the wavelength, which results in a tighter area on the package to route I/O. In addition, as the dielectric loss becomes more predominant at the terahertz band, low-loss and low-parasitic interconnects are critical to

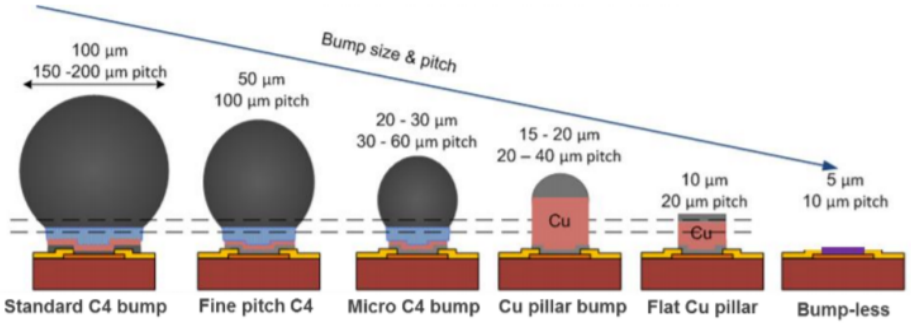


Figure 1.18: Off-chip I/O pitch scaling trend [59]

RF/mm-wave system performance. Therefore, an investigation of pitch scaling on RF performance of these alternative bonding techniques is needed.

1.4 Research Objective and Contribution

The main objective of this research is to develop a fused-silica stitch-chip technology for polylithic integration of RF/mm-wave dice/chiplets. The main contributions of this thesis can be summarized as follows:

- **Characterization methodology for fused-silica stitch-chip components:** RF characterization of the CMIs and CPWs used in the fused-silica stitch-chip is performed with de-embedding design and parasitics extraction. The CMI's fabrication process is demonstrated on the fused-silica substrate for the first time. All results are compared with state-of-the-art.

- **CMI RF-mechanical co-design and stitch-chip impedance design for embedding RF/mm-wave chiplets:** An RF-mechanical co-design of the CMI is integrated in the stitch-chip design flow to optimize the CMI's performance. In addition, an impedance study is also added in this design flow to study the assembly impact on the stitch-chip's impedance. Samples are fabricated accordingly and compared with conventional wire-bonding technique.

- **COTS chiplet-based module demonstration using the fused-silica stitch-chip:**

The fused-silica stitch-chips are assembled on active RF/mm-wave front-end die/chiplet for the first time to demonstrate their RF performance. The chiplet-based module is characterized to understand package impact on die performance and results are benchmarked with state-of-the-art. A thermal analysis is also conducted to understand the module's thermal handling capability.

- **Parasitics study and benchmarking of alternative off-chip I/Os for the stitch-chip:** With the vision of pitch scaling trend of off-chip I/Os, alternative off-chip I/Os including solder bump, microbump, and hybrid bond are studied in terms of frequency-dependent parasitics. A benchmarking of these off-chip I/Os is also included.

1.4.1 Thesis statement

To address the high-loss of wire/ribbon-bonds and overcome the strict assembly process of flip-chip for RF/mm-wave system packaging, this thesis introduces and develops a novel low-loss, low-parasitic, and impedance-matched fused-silica stitch-chip technology for RF/mm-wave chiplet-based packages. Key features also include a small form factor, the ability to rework, and the ability to enable system functional scalability.

1.5 Organization of this Thesis

The remainder of this thesis is organized as follows:

- Chapter 2 discusses the baseline design of the fused-silica stitch-chip and de-embedding testbed design. The CMI's fabrication processes are demonstrated on fused-silica substrate. RF characterization is performed to acquire loss and parasitics of the stitch-chip channel and CMI, which are compared with state-of-the-art.
- Chapter 3 explores the RF-mechanical co-design and impedance study (TDR simulations and measurements) for CMI and assembled stitch-chip, respectively. Samples

for these designs are fabricated and RF characterized. The results are compared with wire bonding and other existing technologies.

- Chapter 4 demonstrates a LNA single chip module using the fused-silica stitch-chips. Module design, die-attaching, and stitch-chip assembly are elaborated in this chapter. The RF characterization is conducted on this module to obtain linear gain and return loss. Steady-state thermal analysis is performed to understand the module's potential for higher power RF/mm-wave die integration.

- Chapter 5 explores the stitch-chip and package substrate design for a multi-chip module, including D2D interconnect length study, the study of the transition from stitch-chip to package, and power supply interconnect on the stitch-chip for the first time. The assembly and RF characterization for this multi-chip module are also discussed in this chapter.

- Chapter 6 reviews the parasitic extraction methods of alternative off-chip I/Os for the stitch-chip and investigates the pitch scaling impact on these off-chip I/Os' parasitics. Different ground-signal configurations for these I/Os are also studied for RF/mm-wave applications. All results are summarized and benchmarked.

- Chapter 7 summarizes the key conclusions in this thesis and discusses potential future work.

CHAPTER 2

RF CHARACTERIZATION OF FUSED-SILICA STITCH-CHIPS AND COMPRESSIBLE MICROINTERCONNECTS

In this chapter, baseline designs of the stitch-chip are discussed, including CPW and CMI designs. De-embedding testbeds are designed, fabricated, and assembled. RF characterization is conducted on these testbeds to obtain measured S-parameters and interconnect parasitics extractions for both the stitch-chip channel and the CMIs. To further understand the electrical performance of the stitch-chip channel and the CMI, their losses and parasitics are benchmarked to other technologies.

2.1 Fused-Silica Stitch-Chip Baseline Design

Figure 2.1 shows a schematic of a fused-silica stitch-chip model in ANSYS HFSS. In the model, a 500 μm long CPW is made on a fused-silica substrate (dielectric constant $\sim$3.9 and loss tangent $\sim$0.0002). Off-chip I/Os (e.g., 100 μm pitch 30 μm high CMIs) are set on both ends of the CPW.

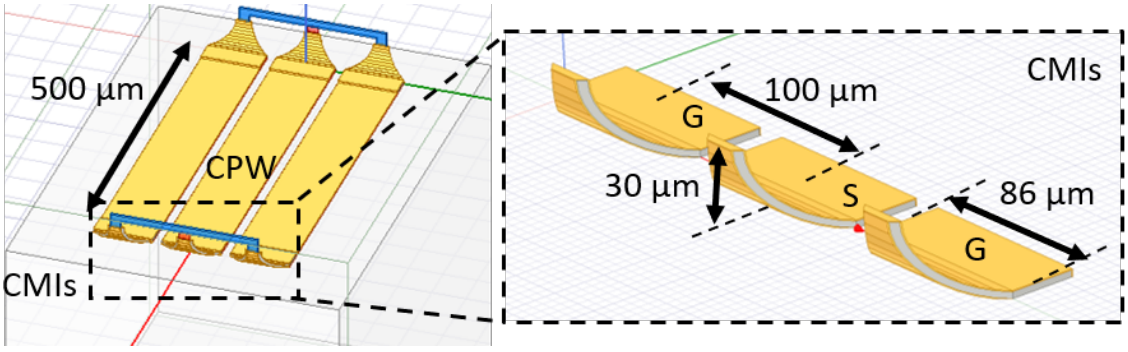


Figure 2.1: An example of a baseline fused-silica stitch-chip in ANSYS HFSS

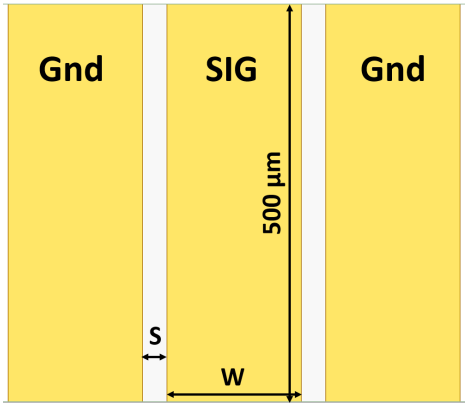


Figure 2.2: Top view of a CPW

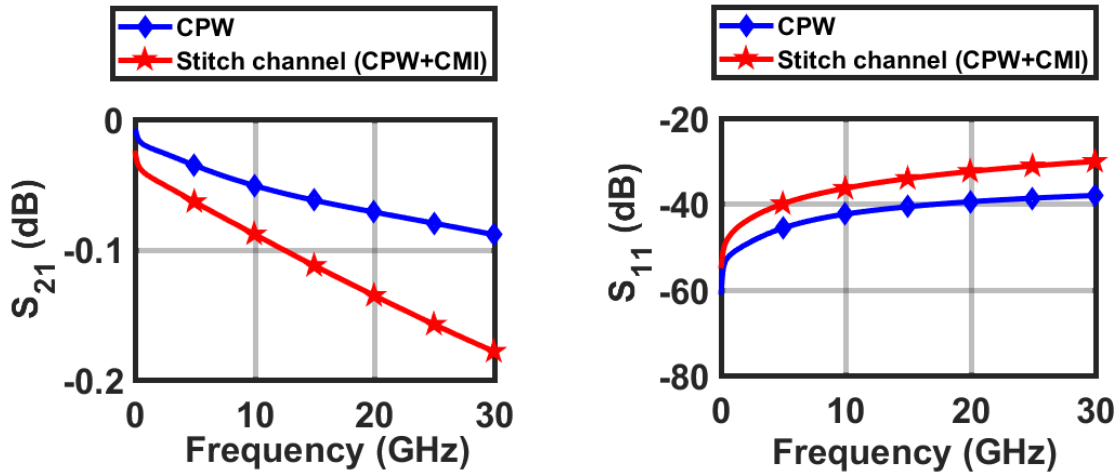
Table 2.1: Design parameters of multi-pitch CPWs and corresponding characteristic impedance.

Pitch (W+S, μm)	W (μm)	S (μm)	Impedance (Ω) across 50 GHz
200	170	30	~52
150	128	22	~52
100	85	15	~52
50	41	9	~53

2.1.1 CPW design

The design objective is to achieve 50 Ω characteristic impedance for the CPW to match the impedance of the RF/mm-wave chiplet pads. To accommodate multiple pitches used in RF/mm-wave systems, the CPWs are designed with different pitches. All designs are performed in ANSYS HFSS up to 50 GHz.

Figure 2.2 shows a top view of the designed CPWs on the fused-silica substrate. The design parameters are the center signal trace width (W) and the edge-to-edge spacing (S) between the center signal trace and adjacent ground (reference) traces. The pitch is defined as the summation of W and S. The design parameters at different pitches are summarized in Table 2.1. Other dimensions and materials in the designs are summarized as follows: 1) the fused-silica substrate is 500 μm thick; 2) the CPWs are made using 1.5 μm thick copper covered with 0.5 μm thick gold; 3) the length of the CPWs is 500 μm. Wave ports are used



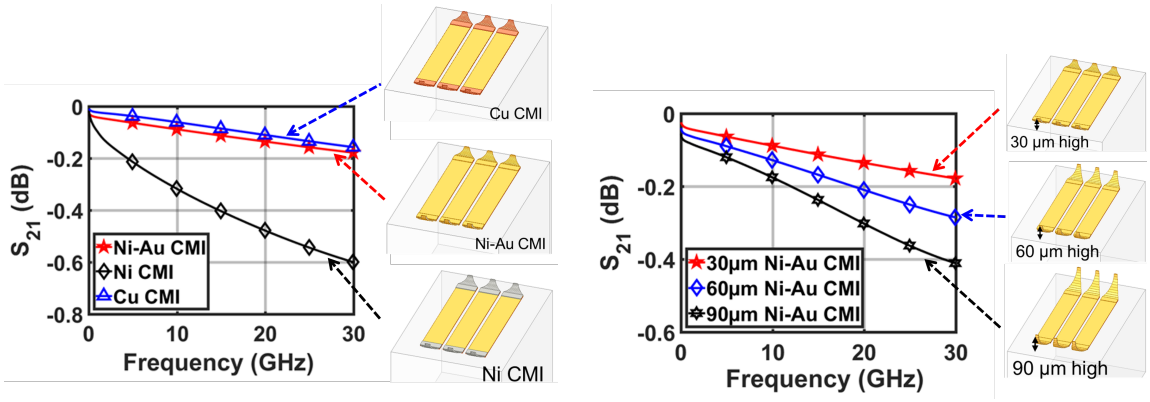
(a) (b)

Figure 2.3: CMIs impact on the S-parameters of the total stitch-chip channel in Figure 2.1: (a) insertion loss (S_{21}) and (b) return loss (S_{11})

to excite Transverse ElectroMagnetic (TEM) fields at the ends of the CPWs.

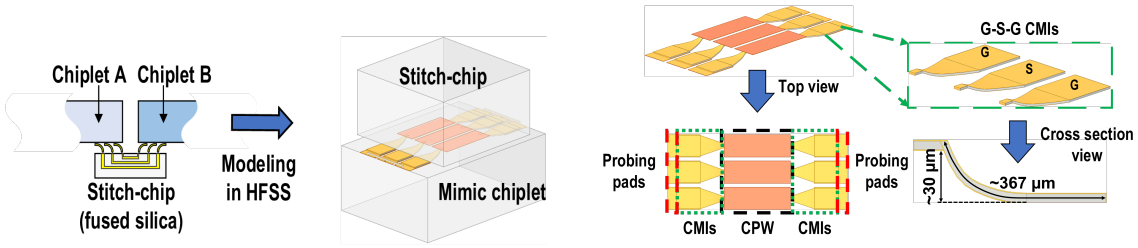
2.1.2 CMIs design

The integration of the CMIs on the CPW has minimal impact on the total stitch-chip channel loss. For the stitch-chip design in Figure 2.1, Figure 2.3 depicts the simulated S-parameters up to 30 GHz before and after integrating the CMIs on the CPW. A maximum 0.1 dB difference is observed for the insertion loss. Next, the material and height of the CMIs in Figure 2.1 are varied in the simulation. As shown in Figure 2.4a, copper CMIs exhibit the lowest insertion loss up to 30 GHz, while nickel CMIs show the highest insertion loss. However, a simple gold coating on the nickel CMIs can improve the insertion loss close to the copper CMIs. Moreover, as shown in Figure 2.4b, the total channel insertion loss changes by approximately 0.3 dB up to 30 GHz with the tallest CMIs (90 μm high). The dimensions of the CMIs would mostly depend on the requirements of the end application.



(a) (b)

Figure 2.4: Insertion loss of (a) CMIs with different materials and (b) CMIs with varied heights

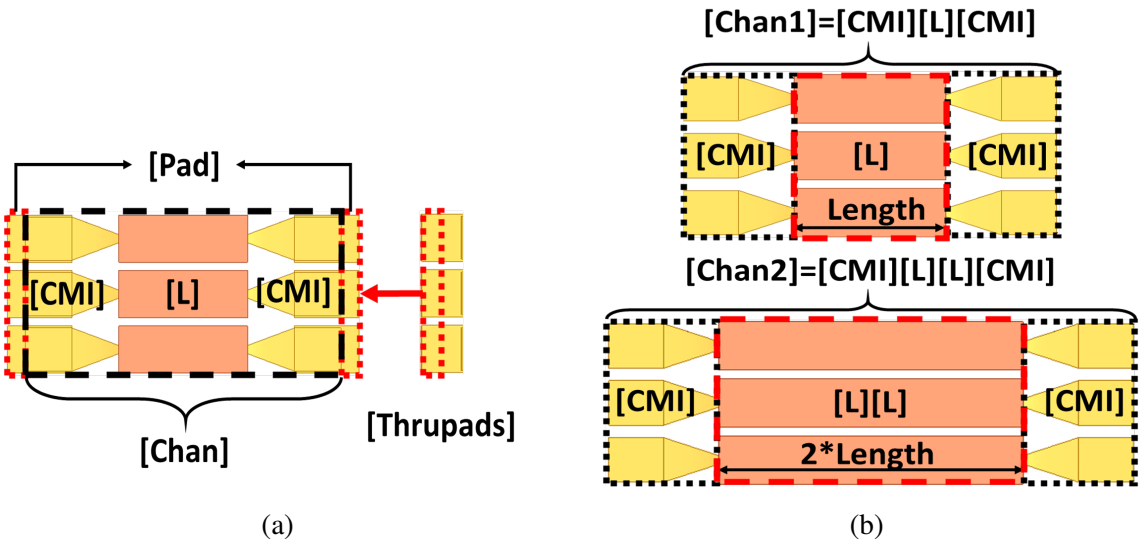


(a) (b)

Figure 2.5: Testbed HFSS modeling: (a) modeling procedure and (b) schematic of a stitch-chip channel (hide substrate material) and ground-signal-ground CMIs

2.2 De-Embedding Testbed Design

A testbed, which emulates a fully assembled stitch-chip system, is designed in ANSYS HFSS, as shown in Figure 2.5. Fused-silica (dielectric constant ∼3.9 and loss tangent ∼0.0002) is selected as substrate material for both stitch-chip and mimic chiplet for its low-loss characteristics. CPWs are designed on the stitch-chip as follows: a center 170 μm wide signal trace is 30 μm spaced from the adjacent ground (reference) traces; all traces are modeled as 1.5 μm thick copper covered with 0.5 μm thick gold. These dimensions result in approximately 50 Ω characteristic impedance up to 40 GHz. Two ground-signal-ground (G-S-G) sets of gold-coated NiW CMIs (NiW's Young's modulus: 180 GPa, yield strength: 1.93 GPa [60]) with probing pads (170 μm $\times$ 250 μm) are designed on the mimic



(a) (b)

Figure 2.6: De-embedding techniques used in the design: (a) thru-only de-embedding and (b) L-2L de-embedding

chiplet. The gold coating of the CMIs is to prevent oxidation [61] and reducing the RF loss because of its higher conductivity and larger skin depth at high frequencies. Note that these CMIs can be designed on the stitch-chip as well. The CMIs are 30 μm tall and $\sim$367 μm in length, as shown in Figure 2.5b. A curved sidewall in the CMI's cross-sectional view enables the out-of-plane mechanical flexibility [51]. The top view in Figure 2.5b shows a stitch-chip channel (Device Under Test (DUT)) consisting of two probing pads, one CPW, and two sets of CMIs.

2.2.1 De-embedding technique

A thru-only de-embedding technique [62] is selected to extract the stitch-chip channel's loss due to its simplicity. L-2L de-embedding technique [65], [66] is chosen to obtain the CMI's loss rather than the Thru-Reflect-Line (TRL) de-embedding technique or the open-short de-embedding technique. The TRL technique is expected to have S-parameters measurement errors due to the difficulty of determining the reference impedance [63] and the open-short technique suffers from frequency band limitation [64]. The pros and cons of these de-embedding techniques are summarized in Table 2.2.

Table 2.2: Summary of RF de-embedding techniques.

Technique	**Benefit**	**Limitation**
Thru-only [62]	Simple de-embedding structure for pads	The pads should be much smaller than interested wavelength
TRL [63]	Accurate up to 60 GHz	Challenge of acquiring reference impedance for 3D transitions
Open-short [64]	Simple de-embedding structure	Limited frequency band
L-2L [65], [66]	Simple de-embedding structure	Validation needed for non-TSV 3D transitions

As shown in Figure 2.6, the thru-only de-embedding technique [62] is utilized to remove the probing pads' parasitics from the measurement and extract the loss information of the stitch-chip channel, while CMIs' loss information is extracted by the L-2L de-embedding technique [65], [66].

As shown in Figure 2.6a, the loss information of the stitch-chip channel is extracted by removing the parasitics of the probing pads through ABCD-matrix computation (two by two matrix) as follows [62]:

$$[Thrupads] = [Pad][Pad] \tag{2.1}$$

$$[DUT] = [Pad][Chan][Pad] \tag{2.2}$$

$$[Chan] = \sqrt{[Thrupads]}^{-1}[DUT]\sqrt{[Thrupads]}^{-1} \tag{2.3}$$

where $[Pad]$ represents the pads' ABCD-matrix, and $[Chan]$ is the ABCD-matrix of the stitch-chip channel.

As shown in Figure 2.6b, the loss information of the CMI-only structure is extracted by the L-2L de-embedding technique, which requires two testbeds: one with L-length (500 μm long) CPW and the other with 2L-length (1000 μm long) CPW on the stitch-chips. The ABCD-matrices of these testbeds after removing the probe pads' parasitics are denoted as $[Chan1]$ and $[Chan2]$, while $[CMI]$ and $[L]$ are the ABCD-matrices of the CMIs and the

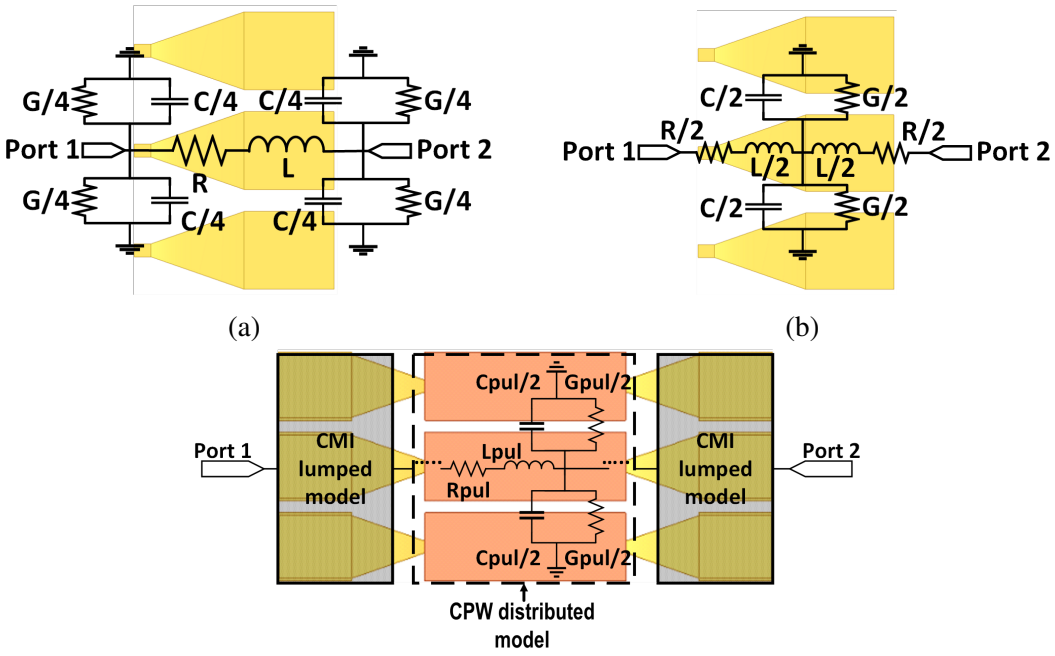


Figure 2.7: Parasitics models for different target structures (top view): (a) Π-lumped model for CMI-only, (b) T-lumped model for CMI-only, and (c) combined model for the total stitch-chip channel (a distributed model for CPW and a lumped model for CMIs)

L-length CPW, respectively. The L-2L de-embedding technique [65], [66] is implemented and described using the ABCD-matrix form (two by two matrix) as follows:

$$[Chan1] = [CMI][L][CMI] \tag{2.4}$$

$$[Chan2] = [CMI][L][L][CMI] \tag{2.5}$$

$$[CMI] = \left(\sqrt{[Chan1]^{-1}[Chan2][Chan1]^{-1}}\right)^{-1} \tag{2.6}$$

2.2.2 Parasitics extraction

The parasitics of the stitch-chip channel and CMI-only structure can be extracted using their ABCD-matrices. Such extraction requires accurate parasitics modeling of these structures, which is determined by the wavelength (λ) and the target structure's physical length. If the physical length is shorter than or comparable to $\lambda/10$, the lumped parasitics models can be used, otherwise, the distributed parasitics model should be used. The wavelength can be

calculated as follows:

$$\lambda = c/(\sqrt{\varepsilon_r} f) \tag{2.7}$$

where c is the speed of the electromagnetic wave in vacuum, ε_r is the relative permittivity of the surrounding medium, and f is the selected frequency. To simplify the calculation, two cases are considered for the testbed: one assumes that the medium is only air, while the other assumes only fused-silica. The effective ε_r will be between these two calculated cases and so will λ. Therefore, λ/10 is within the range of $\sim$380 μm to $\sim$750 μm at 40 GHz, which implies that the lumped parasitics models can be used for the CMI-only (typical length less than 380 μm) and the distributed parasitics model will be used for CPWs. A combined parasitics model that leverages both the CMIs' lumped models and the CPWs' distributed model is proposed for the total stitch-chip channels (i.e., CMIs+CPW+CMIs).

Figure 2.7a and Figure 2.7b show the lumped models (Π-model and T-model) for the CMI-only structure. A two-port Y-matrix (converted from the ABCD-matrix) of a CMI-only structure is used for the Π-lumped model and can be expressed as follows:

$$[\mathbf{Y}] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{2.8}$$

where Y_{11} and Y_{22} are the input admittances seen through these two ports respectively. Y_{12} and Y_{21} are the transfer admittances between these two ports. The parasitic resistance (R), inductance (L), conductance (G), and capacitance (C) can be calculated [67]:

$$R_Y = real\left(\frac{-2}{Y_{12} + Y_{21}}\right) \tag{2.9}$$

$$L_Y = \frac{imag\left(\frac{-2}{Y_{12}+Y_{21}}\right)}{2\pi f} \tag{2.10}$$

$$G_Y = real(Y_{11} + Y_{22} + (Y_{12} + Y_{21})) \tag{2.11}$$

$$C_Y = \frac{imag(Y_{11} + Y_{22} + (Y_{12} + Y_{21}))}{2\pi f} \tag{2.12}$$

where f is the frequency. Similarly, the parasitics extracted from the T-lumped model and Z-matrix can be calculated [67]:

$$R_Z = real(Z_{11} + Z_{22} - (Z_{12} + Z_{21})) \tag{2.13}$$

$$L_Z = \frac{imag(Z_{11} + Z_{22} - (Z_{12} + Z_{21}))}{2\pi f} \tag{2.14}$$

$$G_Z = real\left(\frac{2}{Z_{12} + Z_{21}}\right) \tag{2.15}$$

$$C_Z = \frac{imag\left(\frac{2}{Z_{12}+Z_{21}}\right)}{2\pi f} \tag{2.16}$$

The extracted CMIs' parasitics are then input into the combined model, as shown in Figure 2.7c, to obtain the parasitics of the total stitch-chip channels. In Figure 2.7c, two CMIs' lumped model blocks and one CPW's distributed model block are connected to represent the combined model. The CPW's distributed model in Figure 2.7c is a cascade of a per-unit-length (pul) element that is calculated from the ABCD-matrix of the CPW. The CPW's propagation constant γ and characteristic impedance Z_0 are also calculated from the ABCD-matrix [67]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} cosh(\gamma l) & Z_0 sinh(\gamma l) \\ \frac{1}{Z_0} sinh(\gamma l) & cosh(\gamma l) \end{bmatrix} \tag{2.17}$$

$$Z_0 = \sqrt{\frac{B}{C}} \tag{2.18}$$

$$\gamma = \frac{cosh^{-1}(A)}{l} \tag{2.19}$$

where l is the physical length of the CPW. Next, the parasitics of the CPW can be calculated with the γ and the Z_0 [67]. The parasitics of the total stitch-chip channel (CMIs+CPW+CMIs)

are a summation of the parasitics of the CMIs and the CPW:

$$R_{tot} = R_{CPW} + 2R_{CMI} = l \times real(\gamma Z_0) + 2R_{Z/Y} \tag{2.20}$$

$$L_{tot} = L_{CPW} + 2L_{CMI} = l \times \frac{imag(\gamma Z_0)}{2\pi f} + 2L_{Z/Y} \tag{2.21}$$

$$G_{tot} = G_{CPW} + 2G_{CMI} = l \times real\left(\frac{\gamma}{Z_0}\right) + 2G_{Z/Y} \tag{2.22}$$

$$C_{tot} = C_{CPW} + 2C_{CMI} = l \times \frac{imag\left(\frac{\gamma}{Z_0}\right)}{2\pi f} + 2C_{Z/Y} \tag{2.23}$$

where f is the frequency; $R_{Z/Y}$, $L_{Z/Y}$, $G_{Z/Y}$, and $C_{Z/Y}$ are the parasitics from CMIs' lumped models.

2.3 Stitch-Chip and Mimic Chiplet Fabrication and Assembly

The designed CPW on the stitch-chip is fabricated using a lift-off process, as shown in Figure 2.8. To prepare the bare fused-silica substrate for fabrication, a plasma descum process is utilized followed by acetone/methanol/isopropanol rinse. Next, an NR71-3000P photoresist layer is spin-coated on the substrate and soft-baked. The photoresist is patterned

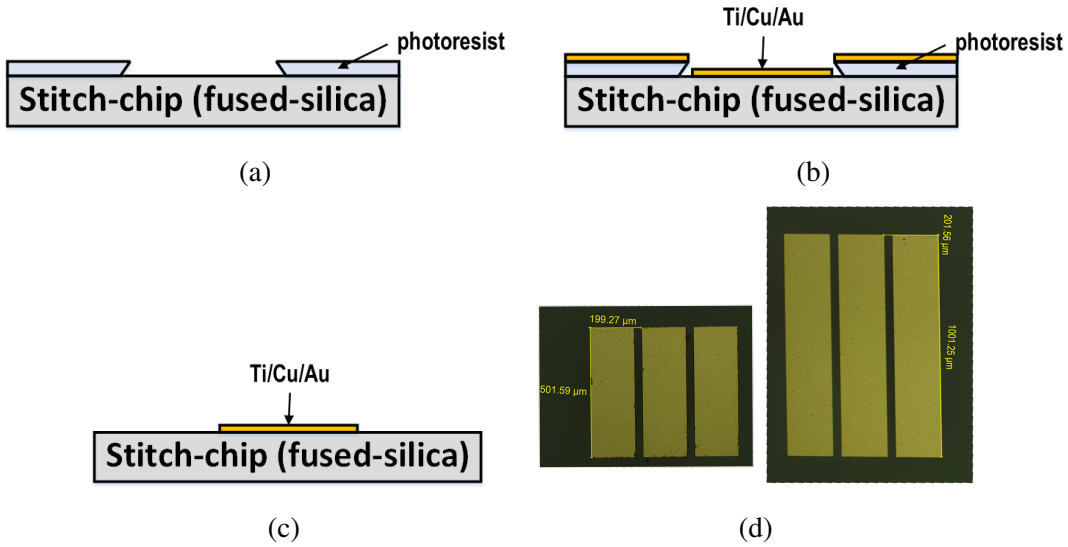


Figure 2.8: Fabrication of CPW: (a) photoresist patterning, (b) metal deposition, (c) lift-off, and (d) fabricated CPWs with 200 μm pitch and 500 μm/1000 μm length

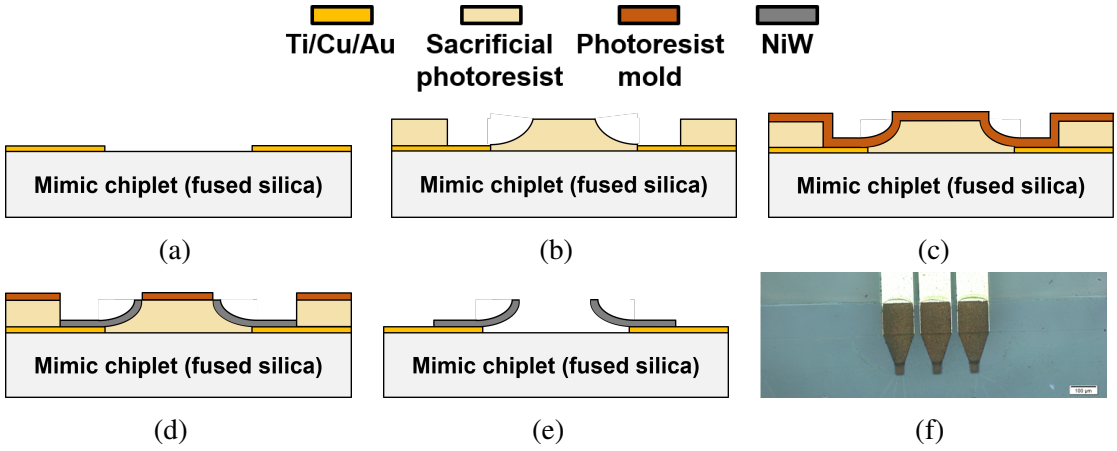


Figure 2.9: Mimic chiplet (the chiplet with fabricated probe pads and CMIs) fabrication process: (a) probing pads' lift-off, (b) photoresist patterning after pads' lift-off, (c) photoresist spray coating after seed layer sputtering, (d) photoresist molding and electroplating, (e) CMI releasing, and (f) a top view of CMIs in microscope

through lithography, post-exposure-baked, and developed, as shown in Figure 2.8a. Then, 15 nm thick titanium (Ti), 1.5 μm thick copper (Cu), and 0.5 μm thick gold (Au) layers are deposited sequentially through E-beam evaporation, as shown in Figure 2.8b. Note that the thin Ti layer is required to promote the adhesion of the metals to the wafer. Finally, the wafer is left in an acetone bath to perform a lift-off process. As shown in Figure 2.8d, 200 μm pitch CPWs with 500 μm length and 1000 μm length are fabricated on the fused-silica substrate to form the stitch-chips.

The fabrication of the probing pads and CMIs are summarized in Figure 2.9. Firstly, a lift-off process is performed for the probing pads on a fused-silica substrate, as shown in Figure 2.9a. Next, a sacrificial photoresist layer (AZ40XT-11D) is spin-coated to have $\sim$30 μm thickness and soft-baked. The edge bead of the photoresist layer is removed to improve fabrication yield. Next, the photoresist is patterned, post-exposure-baked, and developed to obtain a curved sidewall profile [51]. Ti/Cu/Ti seed layers are sputtered and another photoresist layer (AZP4620) is spray-coated and patterned as a mold for electroplating. Next, the top Ti seed layer is etched away to expose the Cu seed layer. NiW electroplating is performed to form the CMIs' bodies on the Cu seed layer. The photoresist layers and

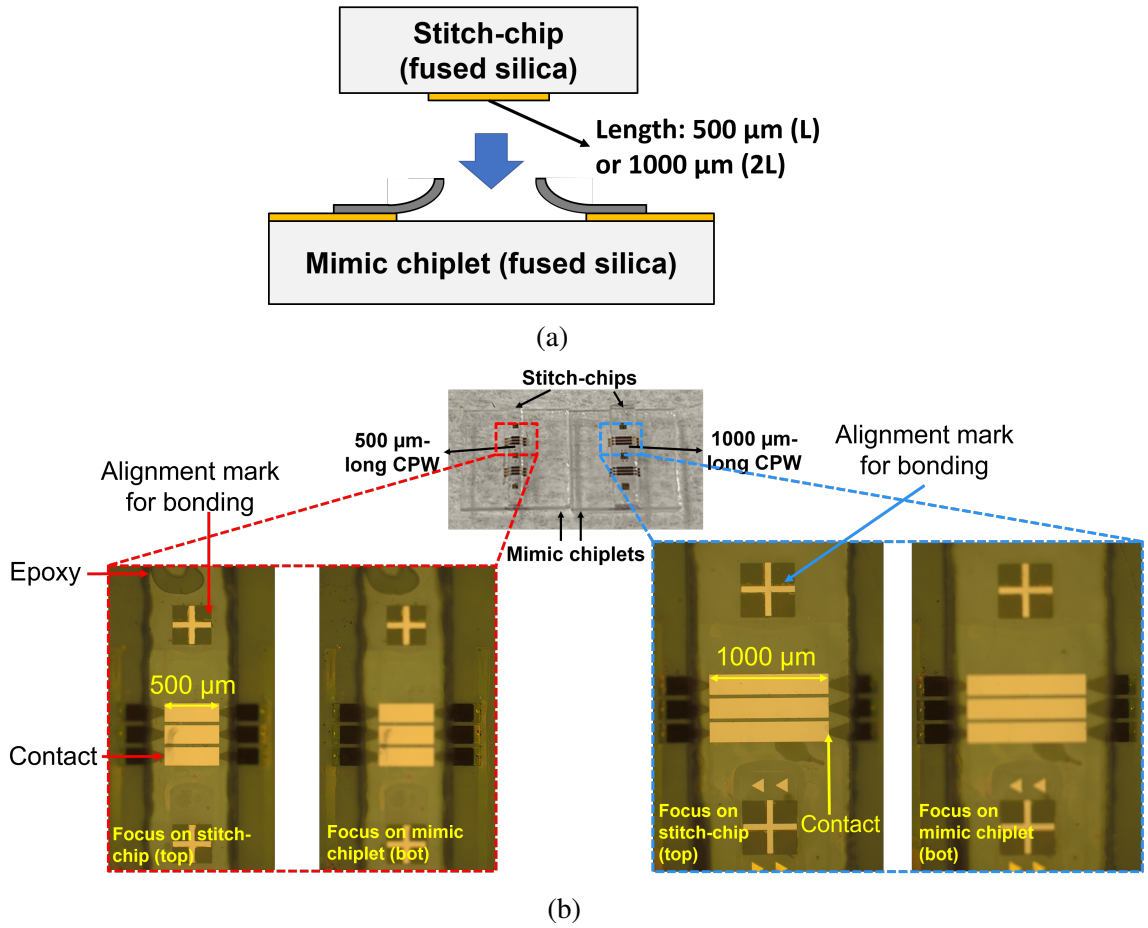


Figure 2.10: Testbed assembly process and results: (a) schematic of flip-chip bonding of the stitch-chip and the mimic chiplet and (b) top-views of the assembled testbed

the seed layers are then removed to release the CMIs. Finally, electroless gold plating is implemented to cover all conductive surfaces. Figure 2.9f shows a top-view micrograph of fabricated ground-signal-ground CMIs.

The fabricated mimic chiplet is assembled with two different fabricated stitch-chips (one with 500 μm long CPWs and the other with 1000 μm long CPWs) using a flip-chip bonder (Finetech FINEPLACER lambda), as shown in Figure 2.10a. Epoxy is applied at the edges of the chips to hold both the stitch-chip and the mimic chiplet together for demonstration purposes (epoxy does not leak inside the conductor region). The assembled two testbeds are shown in Figure 2.10b. During assembly, the CMI's tip would contact with the CPWs on the stitch-chip and deform elastically as needed to build robust electrical

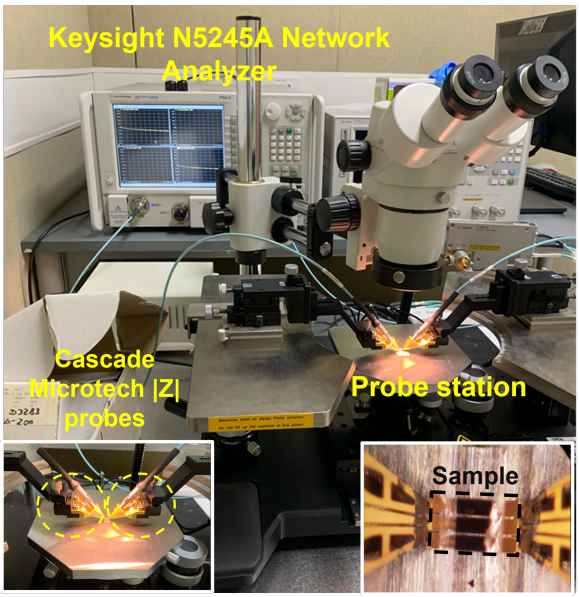


Figure 2.11: RF measurement setup for the assembled testbeds

interconnections.

2.4 RF Characterization

RF characterization up to 40 GHz is implemented for the assembled testbeds using a Keysight N5245A PNA-X network analyzer in a Faraday cage, as shown in Figure 2.11. Short-Open-Load-Thru (SOLT) calibration with Cascade Microtech CSR-8 calibration substrate is utilized to move the measurement reference planes to the tips of two Cascade Microtech 200 μm pitch ground-signal-ground |Z| probes. The probes are manually landed on the probing pads of the assembled testbeds. Next, the S-parameters of the assembled testbeds (as shown in Figure 2.10b) and the thru-pads structures are measured.

2.4.1 Stitch-chip channel loss and parasitics

The measured S-parameters of the assembled testbeds and the thru-pads structures are converted to ABCD-matrices for pads' parasitics de-embedding. After removing the pads' parasitics, the resulting measured ABCD-matrices are converted back to S-parameters and plotted with the simulated results in Figure 2.12 and Figure 2.13. In Figure 2.12a, the dif-

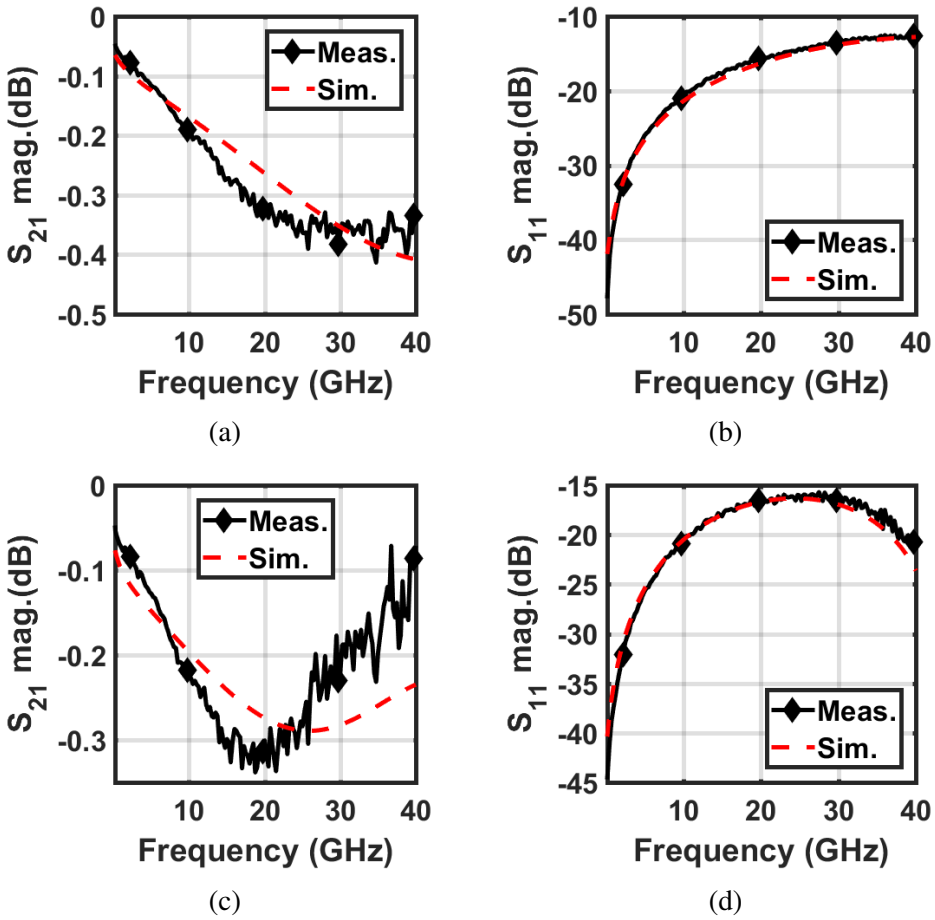


Figure 2.12: Measured S-parameters of stitch-chip channels (CMIs+CPW+CMIs): (a) 500 μm long stitch-chip channel insertion loss **magnitudes**, (b) 500 μm long stitch-chip channel return loss **magnitudes**, (c) 1000 μm long stitch-chip channel insertion loss **magnitudes**, and (d) 1000 μm long stitch-chip channel return loss **magnitudes**

ference between the measured insertion loss (0.33 dB at 20 GHz) and the simulated value (0.26 dB at 20 GHz) is around 0.82%, which demonstrates a good correlation between simulation and measurement. The stitch-chip channels exhibit $<$ 0.42 dB insertion loss up to 40 GHz. In Figure 2.12c, the testbed may be susceptible to background noise, as seen by the ripples at high frequencies. In addition, the stitch-chip channels show acceptable return loss (return loss $>$ 12.7 dB).

Note that in Figure 2.12a and Figure 2.12c, 1000 μm long stitch-chip channel shows lower insertion loss than the 500 μm long channel beyond approximately 20 GHz. Such phenomenon could result from the 1000 μm long channel's lower return loss at high fre-

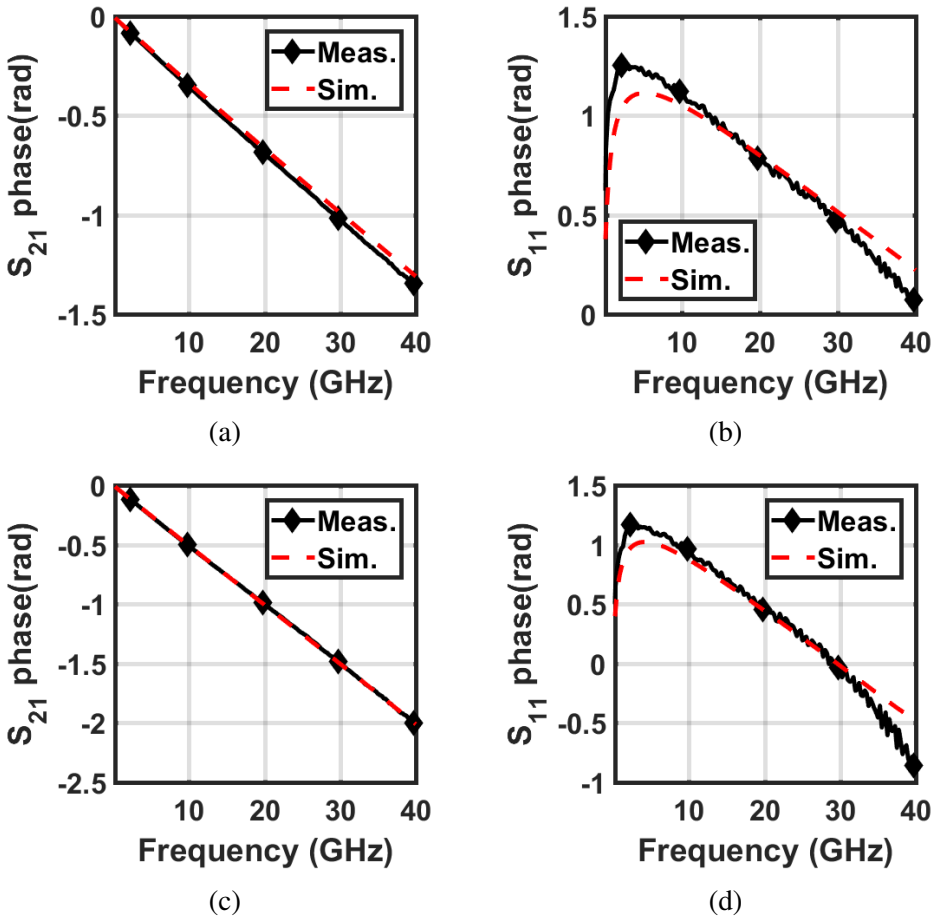


Figure 2.13: Measured S-parameters of stitch-chip channels (CMIs+CPW+CMIs): (a) 500 μm long stitch-chip channel insertion loss **phase**, (b) 500 μm long stitch-chip channel return loss **phase**, (c) 1000 μm long stitch-chip channel insertion loss **phase**, and (d) 1000 μm long stitch-chip channel return loss **phase**

quencies due to potential resonance around 40 GHz (more inductance and capacitance from longer channel cause resonance to shift to a lower frequency), as shown in Figure 2.12d. Generally, lower return loss leads to a lower reflection coefficient and higher transmission coefficient, which translates to lower insertion loss.

A 500 μm long stitch-chip channel's parasitics are also extracted, as shown in Figure 2.14. Figure 2.14b and Figure 2.14c show a good correlation between the measurement and the simulation. However, Figure 2.14a shows the discrepancy which mostly results from the overlook of the contact resistance between the CMI and the CPW in the simulation due to its complexity in the actual assembly. In addition, the measured resistance

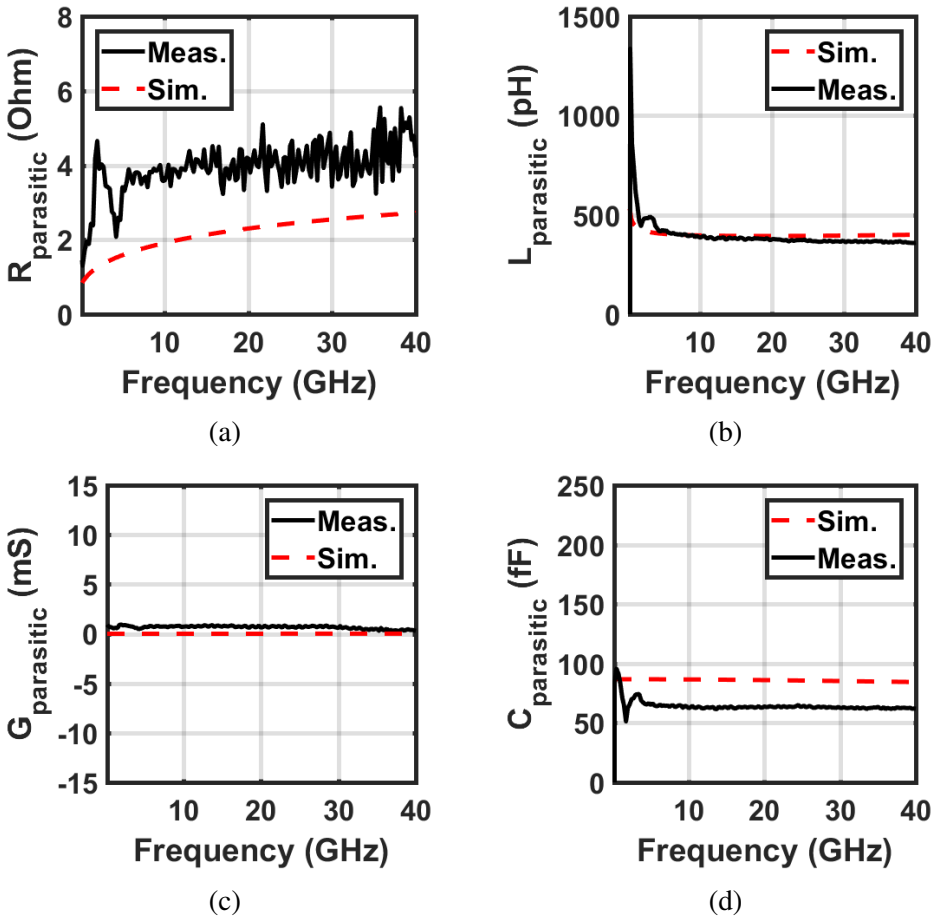


Figure 2.14: Parasitics extraction of 500 μm long stitch-chip channels: (a) resistance, (b) inductance, (c) conductance, and (d) capacitance

and capacitance could suffer from SOLT calibration error for such wideband calibration [68] and process variations (e.g., fabricated dimensions differ from hard mask design). The ripples of the measured resistance could result from the high-frequency noise during measurements. The 500 μm long stitch-chip channel is measured to have 4.68 Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz. The inductance and capacitance remain relatively constant across the 40 GHz bandwidth, while the resistance increases due to skin depth.

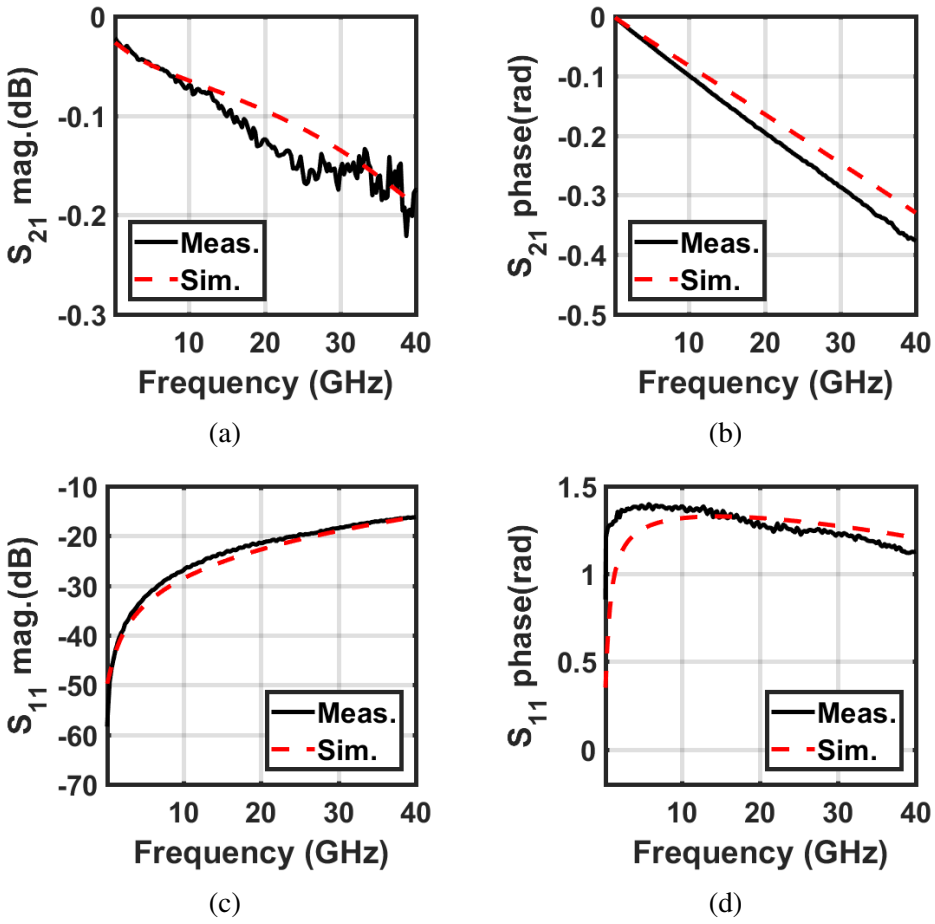


Figure 2.15: Measured S-parameters of CMIs using L-2L de-embedding: (a) insertion loss **magnitude**, (b) insertion loss **phase**, (c) return loss **magnitude**, and (d) return loss **phase**

2.4.2 Ground-signal-ground CMIs loss and parasitics

The ABCD-matrix of ground-signal-ground CMIs, which are 30 μm high and $\sim$367 μm long as shown in Figure 2.5b, can be obtained with the L-2L de-embedding method and converted back to S-parameters (up to 40 GHz), as shown in Figure 2.15. A good correlation between the simulation and the measurement is achieved for the magnitude and the phase of the S-parameters. The mismatches may result from the measurement noise and process variations in the testbeds (e.g., electroplated metal thickness variation). The CMIs' return loss is better than 16.2 dB up to 40 GHz and the insertion loss is less than 0.2 dB.

The measured S-parameters of the CMIs are converted to the Z/Y-parameters to use the

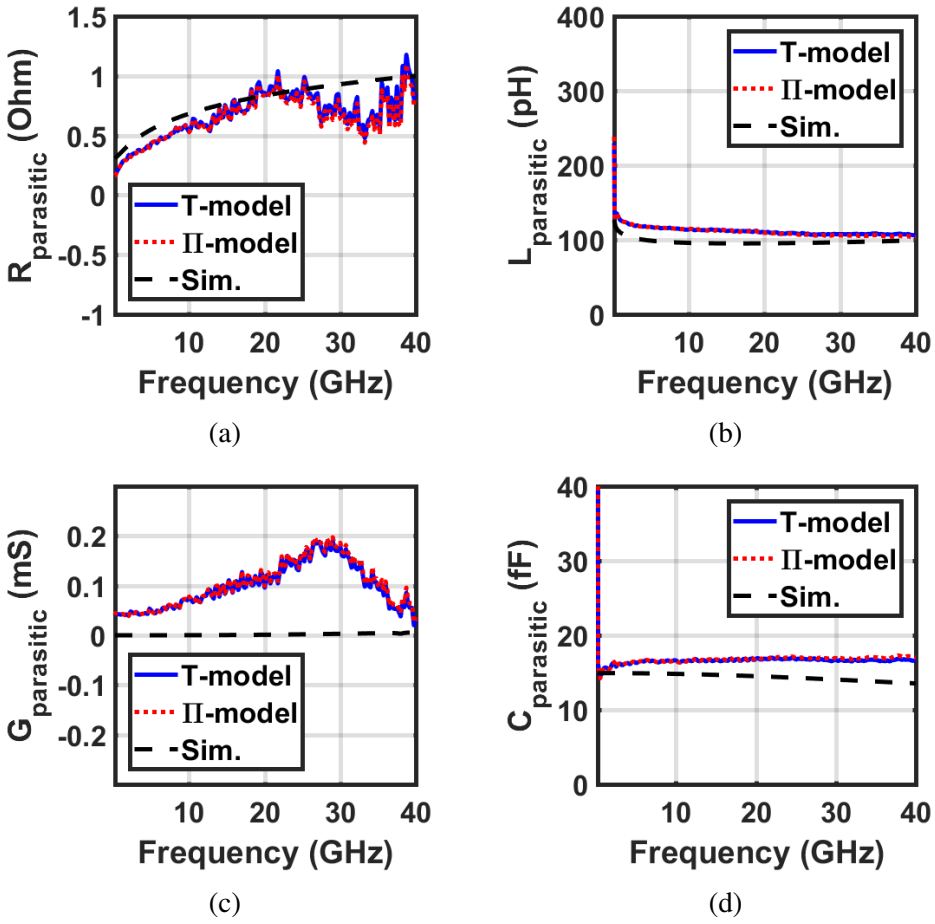


Figure 2.16: Parasitics extraction of CMIs using the lumped models: (a) resistance, (b) inductance, (c) conductance, and (d) capacitance

lumped models for parasitics extraction. The ground-signal-ground CMIs' parasitics are shown in Figure 2.16. Because CMIs are electrically short up to 40 GHz, the results from the two lumped models are similar. Table 2.3 summarizes the measured and simulated parasitics of different CMI designs at 28 and 39 GHz. CMIs' parasitics decrease with pitch scaling except for resistance because DC resistance increases due to the smaller cross-sectional area of the conductor. In Figure 2.16a, the measurement shows larger fluctuations at high frequencies ($>\sim$20 GHz) due to the measurement noise. The measurement can be susceptible to calibration error [68] and process variations, which causes a mismatch with the simulation. In Figure 2.16c, the measurement and the simulation are divergent: each CMI is designed to be surrounded by air, which leads to virtually zero conductance;

Table 2.3: Summary of CMIs' parasitics at selected RF/mm-wave frequencies.

	28 GHz				39 GHz			
Pitch/height (μm)	**R (Ω)**	**L (pH)**	**G (μS)**	**C (fF)**	**R (Ω)**	**L (pH)**	**G (μS)**	**C (fF)**
200/30 (meas.)	0.71	106	170	17	0.99	105	70	17.2
200/30 (sim.)	0.91	96.3	2.5	14.2	0.99	98.9	5.2	13.6
200/60 (sim.)	0.92	102	0.7	14	1	106	4.4	13
150/30 (sim.)	0.96	96	3	12.5	1.01	94.5	1.4	12.9
50/30 (sim.)	1.67	71.6	9.9	8.9	1.75	69.1	16	9.4

however, photoresist residuals could appear between signal-CMI and ground-CMI after sacrificial photoresist layer removal and seed layer etching, which may increase the CMIs' conductance; moreover, the fused silica underneath CMIs' pads could also increase the measured conductance, which is not fully accounted for in the simulation.

2.5 RF Performance Benchmarking

2.5.1 Signal channels

Table 2.4 compares the insertion loss of signal channels in different technologies for RF/mm-wave chiplets packaging, including high-resistivity (HR) silicon interposer technology, glass interposer technology, and organic substrate technology. The fused-silica stitch-chip signal channel shows relatively lower insertion loss than the HR silicon interposer channel because of the lower dielectric constant and loss tangent. A simulation is performed for low-resistivity (LR) silicon interposer technology as well for reference: CPWs with 50 Ω characteristic impedance are designed on the silicon substrate (10 S/m conductivity) with 1 μm thick silicon dioxide; solder bumps are implemented as off-chip I/Os at the ends of the CPWs. The fused-silica stitch-chip technology demonstrates an approximate 3.8 dB

Table 2.4: Loss performance benchmarking of signal channels in different technologies.

Technology	**Channel length /pitch**	**Off-chip I/O /height**	**Insertion loss**
High resistivity silicon interposer [69]	1 mm/-	-/-	0.94 dB @ 40 GHz
Glass interposer [70]	1.86 mm/188 μm	-/-	$\sim$0.56 dB @ 28 GHz
Organic substrate [71]	1.35 mm/-	Au bumps/50 μm	$\sim$0.3 dB @ 40 GHz
InFO [28]	4 mm/-	-/-	1.12 dB @ 39 GHz
Silicon interposer (sim.)	1 mm/200 μm	Solder bumps/30 μm	$\sim$3.8 dB @ 28 GHz $\sim$4.0 dB @ 39 GHz
EMIB [72], [73] (shown as reference)	1 mm/$\sim$4 μm	Microbumps and vias/-	$\sim$14 dB @ 25 GHz
This work (meas.)	1 mm/200 μm	CMIs/30 μm	$\sim$0.2 dB @ 28 GHz $\sim$0.2 dB @ 39 GHz
This work (sim.)	1 mm/4 μm	CMIs/30 μm	$\sim$1.15 dB @ 25 GHz

loss improvement to the LR silicon interposer technology. Compared with glass interposer technology, organic substrate technology, and InFO wafer-level packaging, the fused-silica stitch-chip technology shows similar insertion loss.

Furthermore, to compare with Embedded Multi-die Interconnect Bridge (EMIB), the stitch-chip channel scales to have a similar fine pitch. The newly generated stitch-chip channel model is simulated to obtain S-parameters. The comparison between the stitch-chip channel and EMIB is included in Table 2.4. Stitch-chips with fine-pitch channels show lower insertion loss than EMIB by approximately 13 dB. The EMIB's large loss is partly due to the small cross-sectional area of the traces and lossy Si substrate [72].

Table 2.5 compares the extracted parasitics of the stitch-chip channel with other technologies. The stitch-chip channel possesses similar capacitance but higher inductance and resistance than eWLB. However, eWLB requires precise die positioning, die shift control, and package warpage control during processing [34]. For digital applications, as shown in Table 2.5, the stitch-chip channel's parasitics are compared among Si-based technologies. Note that only traces' parasitics are reported for the Si interposer channels, while

Table 2.5: Parasitics benchmarking of signal channels in different technologies.

Technology	**Typical trace length/pitch**	**Off-chip I/O/height**	**R (Ω)**	**L (nH)**	**C (pF)**
Si interposer [74]	3 mm/4∼6 μm (Microstrip)	Microbumps/-	33.87∼36.94 (28&39 GHz)	0.78	0.63
Si interposer [75]	10 mm/20 μm (CB-CPW)	-/-	15 (3.5 GHz)	2.9	1.6
EMIB [73]	<10 mm/4 μm (Microstrip)	Microbumps and vias/-	-	-	-
eWLB [76]	-/107 μm (CPW)	-/-	∼0.78/mm (10 GHz)	∼0.27/mm	∼0.12/mm
This work (meas.)	0.5 mm/200 μm (CPW)	CMI/30 μm	4.68∼4.99 (28&39 GHz)	0.36	0.062
This work (sim.)	0.5 mm/4 μm (CPW)	CMI/30 μm	10.12∼11.03 (28&39 GHz)	0.26	0.067

both traces' and CMIs' parasitics are included for the stitch-chip channels in this work. The lower parasitics of the stitch-chip channels result from shorter channel lengths and low-loss substrate material.

2.5.2 Off-chip I/Os

A benchmarking of the CMIs in this work, including measurement, simulation, and optimization (lowest loss while minimizing equivalent stress during assembly), with other off-chip I/O technologies for RF/mm-wave frequencies is reported, as shown in Table 2.6. The optimization is realized by shortening the CMI's length but fixing pitch and height while keeping mechanical compliance in a reasonable range. For similar pitch (approximate 150 to 200 μm) and height (30 to 35 μm), the CMIs show comparable or lower insertion loss than solder bumps [77] or Au bumps [79]. For example, the CMIs (150 μm pitch and 30 μm height) possess similar insertion loss (approximate 2.45% difference) as solder bumps with the same dimensions from [77]. The measurement of the CMIs in this work (30 μm high and ∼367 μm long) shows relatively higher resistance (340 mΩ at 2.5 GHz) and inductance

Table 2.6: Comparison of off-chip I/Os (including pads) for RF/mm-wave frequencies.

Off-chip I/O	**Pitch/height (μm)**	**Insertion loss**	**R (mΩ)**	**L (pH)**	**C (fF)**
Solder bumps [77]	150/30	<0.4 dB up to 40 GHz	-	-	-
Solder bumps [78]	300/55	-	11.7 (2.5 GHz)	66	-
Au bumps [79]	155$\sim$180/35	<0.2 dB up to 35 GHz	-	-	-
Flip-chip bumps [80]	>100/20	<0.4 dB up to 40 GHz	-	90	86
Au bumps [48]	100/22	<0.3 dB up to 90 GHz	-	-	-
CMIs (meas.)	200/30	<0.22 dB up to 40 GHz	340 (2.5 GHz)	113.5	17
CMIs (sim.)	150/30	<0.18 dB up to 40 GHz	509.3 (2.5 GHz)	98.9	12.5
CMIs optimization (best value)	200/30	<0.14 dB up to 40 GHz	>94.4 (2.5 GHz)	>12.9	>14.8

(113.5 pH up to 14.5 GHz), while the simulated resistance and the measured inductance of the solder bumps (300 μm pitch and 55 μm high) are 11.7 mΩ at 2.5 GHz and 66 pH up to 14.5 GHz [78]. However, CMIs may possess other benefits over conventional solder bumps, such as free of IMC formation, free of bridging with pitch scaling, and enabling simple rework. Moreover, CMIs do not require underfill to assemble, which leads to even lower conductance and capacitance. To further optimize the CMI's electrical performance, a material with higher conductivity and larger skin depth at high frequencies (e.g., copper) might be utilized as the core material to form the CMI's body during fabrication.

2.6 Conclusion

In this chapter, a testbed that emulates a fully assembled fused-silica stitch-chip technology is characterized. The RF loss performance and parasitics of fused-silica stitch-chip

channels and CMIs are characterized using the thru-only and L-2L de-embedding techniques, respectively. Stitch-chip modeling, de-embedding design, fused-silica stitch-chip fabrication, assembly, RF characterization, and benchmarking are reported.

The RF characterization suggests that the 500 μm long fused-silica stitch-chip channels possess extremely low loss ($<$0.42 dB insertion loss up to 40 GHz) and low parasitics (4.68Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz). CMIs' S-parameters (up to 40 GHz) and parasitics are extracted for the first time and the results indicate that the CMIs (200 μm pitch and 30 μm height) possess $<$0.2 dB insertion loss and $>$16.2 dB return loss, which are comparable or lower than solder bumps.

To this end, the fused-silica stitch-chip technology shows lower loss than Si-based technologies and similar loss as other technologies, such as glass interposer technology, organic substrate technology, and InFO technology, which indicates its potential to be used for RF/mm-wave system packaging.

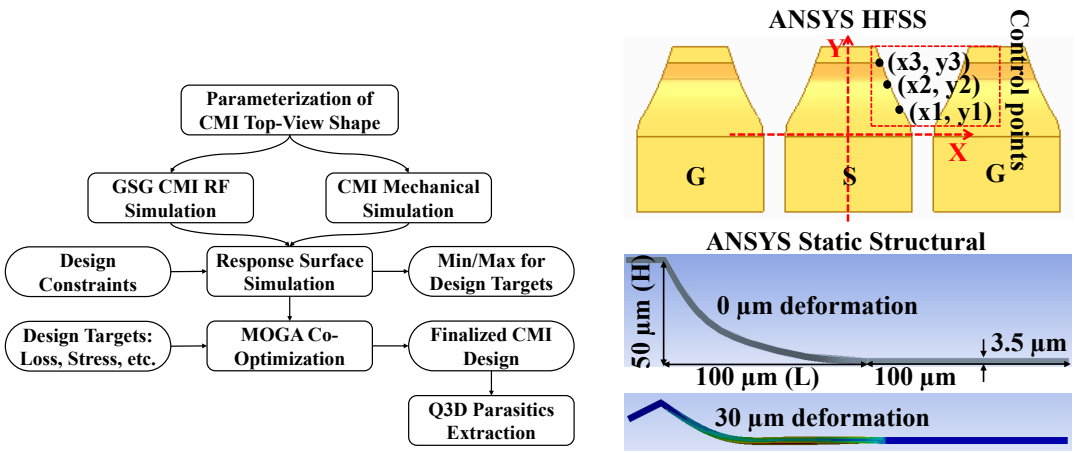
CHAPTER 3
STITCH-CHIP TECHNOLOGY DEVELOPMENT FOR EMBEDDING RF/MM-WAVE CHIPLETS

As shown in Figure 1.16, instead of wire-/ribbon-bonds, stitch-chips with low-loss, low-parasitics, and impedance-matched interconnects are utilized to bridge the chiplets and the substrate without matching networks for seamless multi-chiplet integration. The stitch-chips only need to be assembled on the chiplet's edges where I/Os are located, which reduces the coupling between the stitch-chip and the chiplets, and avoids circuit detuning.

Taller CMIs are needed for the stitch-chips to compensate for any non-planarity between the chiplets and the package substrate. It is also critical that the signal reflection between the stitch-chips and the chiplets (i.e., reflection due to CMIs) should be minimized to improve the RF signal transition. Therefore, an RF-mechanical co-design to optimize the tall CMIs (50 μm tall) is discussed in this chapter. In addition, the impedance design of the stitch-chip is conducted through TDR, and the package substrate coupling is studied as well. A passive testbed substrate, which emulates non-planarity in the package, and newly designed stitch-chips are fabricated and assembled. The newly assembled testbeds are characterized to demonstrate the RF performance and compared with wire bonds.

3.1 Advanced Stitch-Chip Design for Embedding RF/mm-wave Chiplets

The fused-silica stitch-chip consists of two components. One component is CMIs that can deform elastically during assembly to compensate for any surface non-planarity between chiplets (e.g., MMIC 3 is thicker than MMIC 2 in Figure 1.16) and the package substrate. The second component is CPWs with different pitches at their ends to compensate for pitch mismatch between chiplets' pads and package substrates' pads.



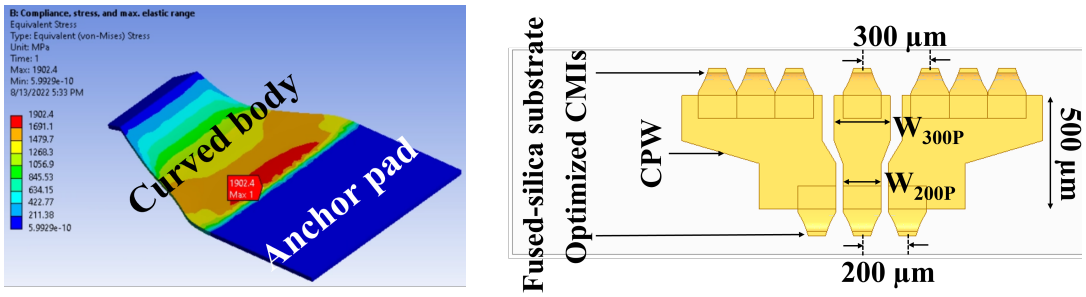
(a) (b)

Figure 3.1: CMI RF-mechanical co-design: (a) co-design procedure and (b) parameterized model details.

3.1.1 CMI RF-mechanical co-design

A co-design methodology involving RF and mechanical simulations is proposed for the CMIs that are utilized in the fused-silica stitch-chip technology for embedding COTS RF/mm-wave chiplets. As shown in Figure 3.1a, the first step is to parameterize CMI shape: the top-view shape of the CMI's curved body is defined by splines that are determined by three control points in ANSYS HFSS, as shown in Figure 3.1b. Next, the design is imported to ANSYS Static Structural and exhibits a curved profile in cross-sectional view, as shown in Figure 3.1b. Coordinate boundaries of the control points are then set as design constraints to prevent non-physical geometries. The CMI is made using NiW (180 GPa Young's modulus, 1.93 GPa yield strength) with electroless gold. The final CMI's shape is obtained by optimizing the coordinates of the three control points to achieve the lowest return loss (>10 dB), the lowest insertion loss (<1 dB), and the lowest equivalent stress (<1.93 GPa) using Direct Optimization modules with Multi-Objective Genetic Algorithm (MOGA) in ANSYS Workbench.

The optimized CMI is 200 μm in pitch and 50 μm tall and is designed to compensate for 30 μm non-planarity in the package through its elastic deformation and can be further



(a) (b)

Figure 3.2: (a) Local stress within CMI during compression and (b) top view of the stitch-chip design in ANSYS HFSS

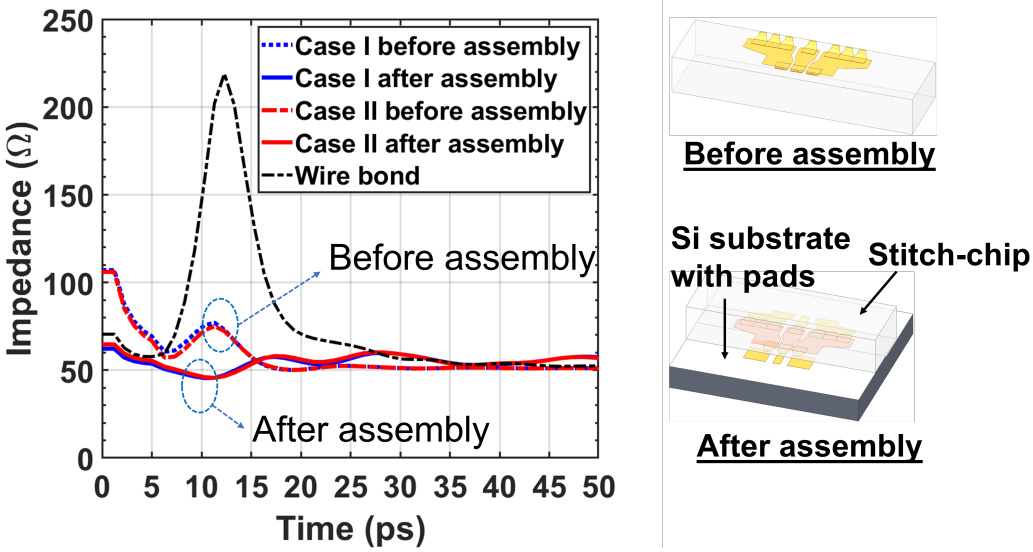


Figure 3.3: Impedance simulations of the stitch-chip designs before and after assembly

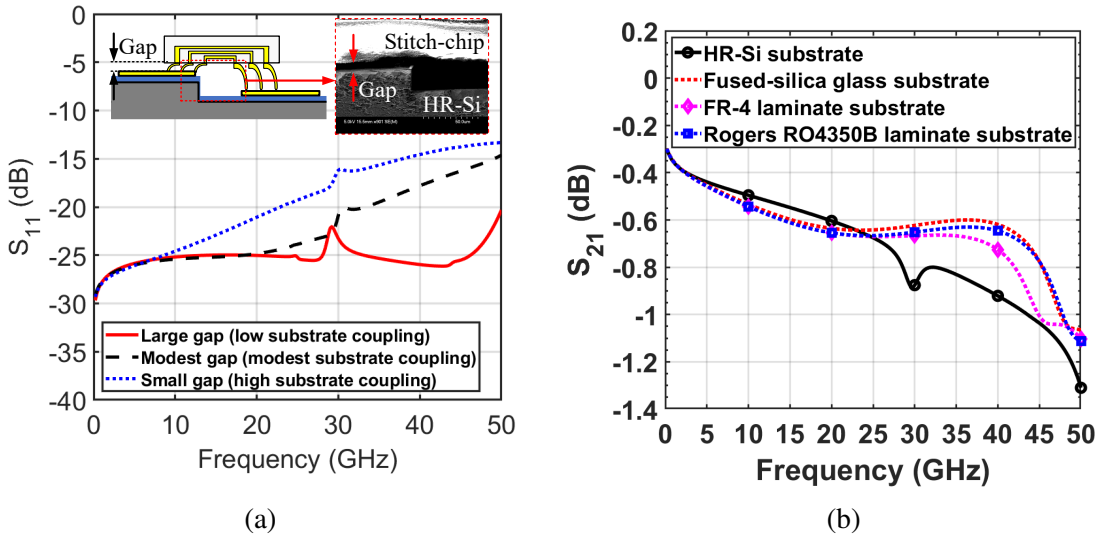
scaled for different bond pad pitches and die height variance [58] with cavity co-design. In Figure 3.2a, the local maximum stress is at the center of the CMI between the anchor pad and the curved body and does not exceed the yield strength (1.93 GPa). For 65 GHz bandwidth, it is optimized to have >12.2 dB return loss, <0.4 dB insertion loss, <0.7 Ω, 25 pH, and 21 fF, which minimize the impedance mismatch between the stitch-chips and the chiplets.

3.1.2 Impedance design

As a potential dielectric loading due to stitch-chip flip-chip assembly may impact the impedance of the stitch-chip, an impedance simulation accounting for the dielectric loading should be performed for the stitch-chip to minimize signal reflection. As shown in Figure 3.2b, a generalized stitch-chip is built on a 500 μm thick fused-silica substrate (dielectric constant: 3.9, loss tangent: 0.0002) and consists of a CPW with different pitches at its ends where the optimized CMIs are located. The CPW with different pitches at its ends can compensate for pitch mismatch between chiplet pad and the package substrate pad. The CPW is modeled with 300 nm thick Cu and 100 nm thick Au on the surfaces. One optimized CMI design is located at the ends of the CPW's signal trace, while multiple optimized CMIs are placed on reference traces to reduce the inductance. The impedance design parameters are the width of the center signal conductor at 200 μm pitch side (W_{200P}) and at 300 μm pitch side (W_{300P}). Two optimized stitch-chip design cases (Case I: W_{200P}=170 μm, W_{300P}=248 μm; Case II: W_{200P}=174 μm, W_{300P}=258 μm) are simulated to obtain the impedance before and after assembly through TDR simulations. The impedance simulation results are shown in Figure 3.3. As seen in Figure 3.3, CMI's transition increases the inductance and the impedance for the stitch-chip before assembly. The stitch-chip assembly introduces dielectric loading, which reduces the impedance to an average $\sim$55 Ω. Note that the high impedance is designed on purpose for the stitch-chip before assembly. The two optimized stitch-chip design cases (Case I and Case II) show similar impedances close to 50 Ω after assembly, while a wire bond shows extremely high impedance due to its high parasitic inductance.

3.1.3 Substrate coupling degradation

As shown in the insets of Figure 3.4a, there is a gap between the stitch-chips and the package substrates after the assembly, which determines the substrate coupling level: 1) low coupling/large gap (28 μm), 2) modest coupling/gap (13 μm), and 3) high coupling/small



(a) (b)

Figure 3.4: (a) The effect of assembly gap (substrate coupling effect) between stitch-chip and package substrate on return loss and (b) simulated insertion loss variance when the same stitch-chip assembles on different package substrates

gap (8 μm). Figure 3.4a depicts the simulated return loss degradation due to the substrate coupling effect. In Figure 3.4a, a small gap results in a large capacitive coupling from the substrates, which varies the stitch-chip channel's impedance and leads to impedance mismatch and return loss degradation. However, the worst substrate coupling case still exhibits $>$10 dB simulated return loss up to 50 GHz.

In addition to the gap-induced substrate coupling, different package substrate materials on which the stitch-chips are assembled could be another source of coupling degradation. The variance of the simulated insertion loss of the same stitch-chip assembled on different package substrate materials is shown in Figure 3.4b. Materials, such as high resistivity Si, glass, FR-4, and Rogers high-frequency substrate, are selected for this study because of their common usage in RF/mm-wave applications. A maximum 0.2 dB variance on the loss is observed. Such minimal variance can be caused by the short stitch-chip channel (500 μm length) and small variance of dielectric constants ($\sim$4) of package substrate materials for RF/mm-wave applications.

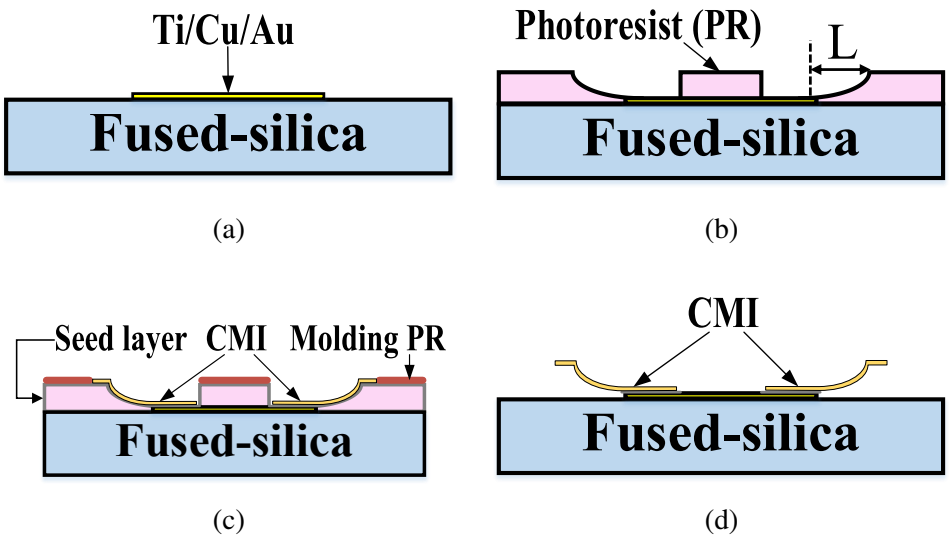


Figure 3.5: Stitch-chip fabrication: (a) lift-off for CPW, (b) photoresist patterning, (c) seed layer sputtering, photoresist molding, and CMI electroplating, and (d) CMI releasing.

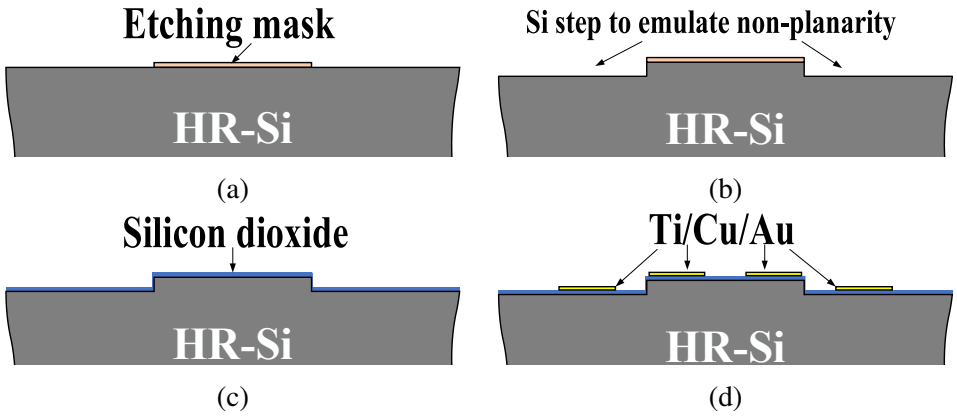


Figure 3.6: Testbed substrate fabrication: (a) etching mask patterning, (b) Inductive Coupled Plasma (ICP) etching, (c) Plasma-Enhanced Chemical Vapor Deposition (PECVD) oxide layer, and (d) probing pads lift-off.

3.2 Fabrication and Assembly

To fabricate such 50 μm tall CMIs, the previous CMI fabrication processes are adjusted. Passive testbed substrates are also fabricated for the RF characterization of the newly designed stitch-chips.

The stitch-chip fabrication is shown in Figure 3.5. Firstly, the CPW is fabricated using the lift-off process on a 4-inch fused-silica wafer. Next, descum and prebaking processes

are performed to clean the wafer surface and promote photoresist adhesion. A 50 μm thick photoresist is then coated and soft-baked. The photoresist is then rehydrated by 30 to 45 minutes, exposed and post-exposure baked. After developing. the photoresist has a curved sidewall, as shown in Figure 3.5b. Note that it is important that the soft-baking time and post-exposure baking time are optimized to eliminate potential resist cracking. An edge bead removal is also used after the photoresist coating to improve the uniformity (around 50% improvement) of the photoresist and yield. A Ti/Cu/Ti seed layer is sputtered to cover the surface and another photoresist layer is spray-coated and patterned for NiW electroplating. The patterning of the spray-coated photoresist requires the optimization of dose and development. The electroplating will deposit NiW in the openings of the spray-coated photoresist layer to form the CMIs' bodies, as shown in Figure 3.5c. The CMIs are then released by etching the seed layer and removing the photoresist layers, as shown in Figure 3.5d. Finally, electroless Au plating is performed to cover all conductive surfaces and prevent NiW oxidation.

The passive testbed substrate to evaluate the performance of the stitch-chip is fabricated, as shown in Figure 3.6. Four-inch high resistivity Si wafers ($>$10K Ω·cm and thickness of 300 μm) are used. Firstly, a photoresist mask is patterned, as shown in Figure 3.6a. An ICP etching is performed to create steps (16.7 μm deep) for emulating the non-planarity in a package, as shown in Figure 3.6b. Next, 1 μm thick silicon dioxide is deposited using PECVD, as shown in Figure 3.6c. Finally, the lift-off process is utilized to fabricate probing pads, as shown in Figure 3.6d.

The fabricated stitch-chips are picked and aligned by a flip-chip bonder (Finetech FINEPLACER lambda). Next, as shown in Figure 3.7c, the stitch-chips are assembled on the Si substrates by the bonder with 1 N force. The edges of the stitch-chips are held with the substrates by cured non-conductive epoxy for demonstration purposes. Figure 3.7d shows a top view of the assembled stitch-chip testbed. For comparison, wire bonding is implemented on the same substrates using a gold wedge bonder, as shown in Figure 3.7a

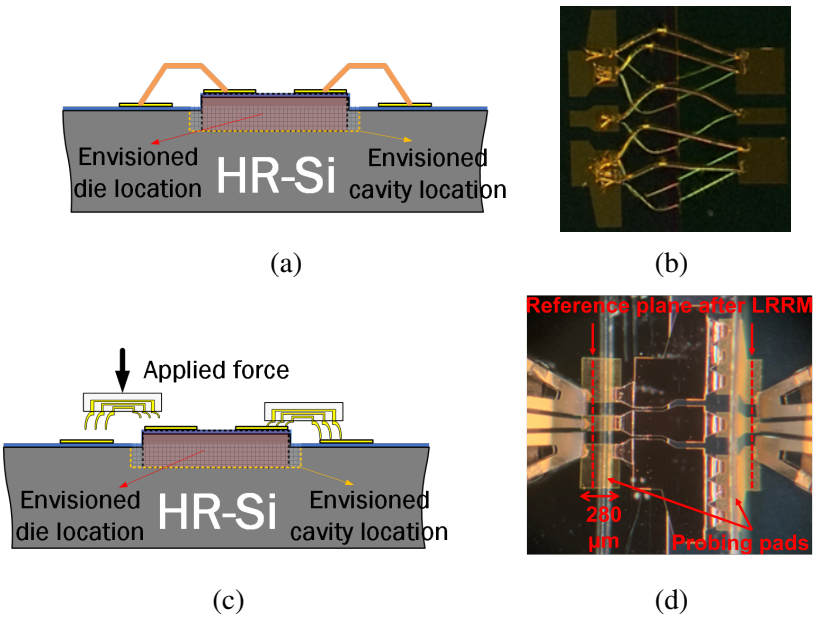


Figure 3.7: Testbed assembly process: (a) a cross-sectional schematic of the wire-bonding testbed and (b) an angled view of the wire-bonds, (c) a cross-sectional schematic of stitch-chip flip-chip assembly, and (d) a top-view of the assembled stitch-chip testbed

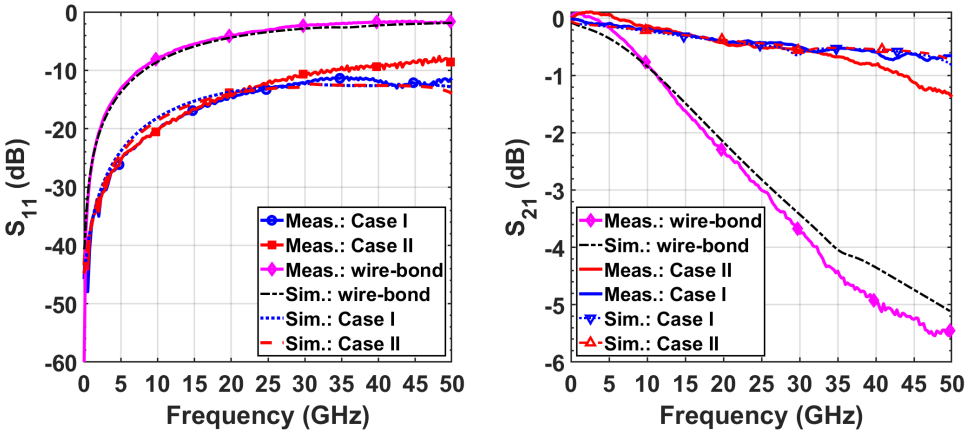
and Figure 3.7b. The gold wires have a 1 mil diameter and approximately 1 mm length. Multiple wire bonds are formed on the reference conductors to reduce inductance.

3.3 RF Characterization and Benchmarking

3.3.1 Measurement of assembled stitch-chip

The Keysight N5245A PNA-X is used to measure return loss and insertion loss up to 50 GHz of the assembled testbeds. As shown in Figure 3.7d, two Cascade Microtech 200 μm pitch GSG $|Z|$ probes are directly landed on 280 μm long probing pads and line-reflect-reflect-match (LRRM) calibration is performed after probing to move the measurement reference planes to the probes' tips.

The results are shown in Figure 3.8. The measurements are correlated well to simulations where the process variation and flip-chip misalignment are measured and utilized to tune the simulation results. In Figure 3.8a, wire bonds degrade the return loss significantly ($>$1.8 dB up to 50 GHz) because of their high parasitic inductance. When comparing two



(a) (b)

Figure 3.8: (a) Return loss measurement and (b) insertion loss measurement of assembled stitch-chip, compared with wire-bonding

stitch-chip cases, Case I with narrower CPWs shows better return loss than Case II with wider CPWs: Case I exhibits $>$11.34 dB measured return loss up to 50 GHz, which is a 3.46 dB improvement from Case II. Non-negligible impedance reduction induced by the aforementioned substrate coupling can decrease the impedance of total signal transition through the stitch-chips, which can be mitigated by intentional high inductance and impedance design of using narrower CPWs. Note that such broadband low return loss can be realized for the assembled stitch-chips without any impedance matching network that may be required by wire-bonds, which would occupy a large package/chip area.

In Figure 3.8b, the wire-bond is measured to have $<$5.49 dB insertion loss up to 50 GHz. Stitch-chip Case I with narrower CPWs demonstrates $<$0.66 dB insertion loss up to 50 GHz, which is a 0.72 dB improvement from Case II with wider CPWs. The performance can be improved further by increasing the thickness and shortening the length of stitch-chip channels on lower-loss stitch-chip substrates.

In Figure 3.9, the measured impedances of the optimized stitch-chips and wire-bonds are obtained by the calculations of the measured S-parameters. The optimized stitch-chips show the measured impedances to be much closer to 50 Ω (average 46.85 Ω) than the wire-bond (maximum $\sim$170 Ω), which indicates a significant impedance matching improvement

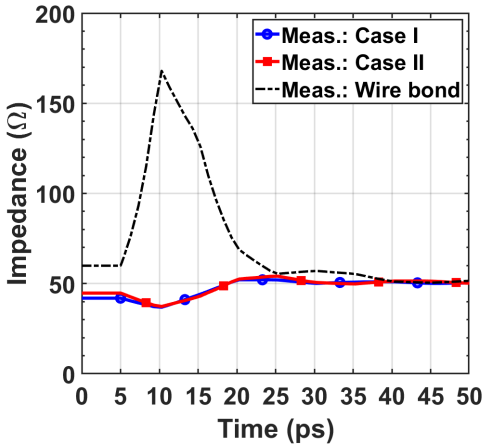


Figure 3.9: Calculated TDR from measured S-parameters

established by the stitch-chip technology.

3.3.2 Benchmarking to existing technologies

Table 3.1 compares the stitch-chip technology with state-of-the-art for RF/mm-wave applications. While the wire bonding technology shows significant loss, especially at high frequencies, the stitch-chip technology exhibits much lower insertion loss (i.e. 4.55 dB improvement) and return loss (i.e. 9.54 dB improvement) within the same bandwidth. In addition, the stitch-chip technology can realize broadband impedance matching without extra matching network design. In contrast, a matching network that can only support a narrow bandwidth and be designed on the package substrate is required by the wire-bonding technology to minimize signal reflection. The matching network may also prevent multi-chiplet module size reduction, which is not a challenge of the stitch-chip technology.

The stitch-chip technology utilizes the photolithography process on the fused-silica substrates, which can realize extremely finer pitch I/O and high design freedom for impedance matching without sacrificing losses, while flip-chip technologies using organic laminate substrates may confront a challenge of I/O pitch scaling [82]. In addition, chip-first technologies assemble chiplets before the interconnect fabrication, which may impair the chiplets performance [83]. The stitch-chip technology may show similar or minimal additional loss,

Table 3.1: Performance comparison between stitch-chip technology and state-of-the-art in RF/mm-wave chiplets modules.

Technology	**Bandwidth (GHz)**	**Insertion loss (dB/mm)**	**Return loss (dB)**	**Impedance design**	**Re-workability**	**Non-planarity compensation**
Stitch-chip (Chip-last)	DC-50	$<$0.94	$>$11.34	Optimization	Yes	Yes
Wire-bond (Chip-last)	DC-50	$<$5.49	$>$1.8	Matching network	Limited	-
Wire-bond [81] (Chip-last)	0.1-20	$<$16.6	$>$5	Matching network	Limited	-
Flip-chip [82] (Chip-last)	75-110	$<$7.01	$>$12	Limited	No	No
Inkjet printing [38] (Chip-first)	10-40	$<$6.25	$>\sim$8	Challenge	Limited	Yes
Aerosol jet printing [39] (Chip-first)	DC-50	$<$0.74 as average	-	Challenge	Limited	Yes

when compared with technologies using additive manufacturing. However, additive manufacturing may confront impedance design challenges because interconnect dimensions and quality heavily depend on tool capability. The interconnect dimensions and quality may also deviate because of potential significant process variation, which leads to the degradation of the electrical performance and non-negligible impedance discontinuity [39].

3.4 Conclusion

In this chapter, the fused-silica stitch-chip technology is demonstrated on passive high-resistivity silicon substrates with intentional non-planarity for the first time. The CMI's RF-mechanical co-design for the lowest RF losses and equivalent stress is developed to minimize the impedance mismatch between the stitch-chip and the die/package substrate. The impedance design of the assembled stitch-chip is studied with an investigation of the

substrate coupling effects including the degradation due to a small assembly gap between the stitch-chip and the package substrate, and the performance variance due to different package substrate materials. The stitch-chip is also designed to compensate pitch mismatch of the die pad and package pad. The optimized designs are fabricated, assembled, characterized, and benchmarked.

For 65 GHz bandwidth, the CMI is optimized to compensate for 30 μm non-planarity in the package and have $>$12.2 dB return loss, $<$0.4 dB insertion loss, $<$0.7 Ω, 25 pH, and 21 fF. The assembled stitch-chip is optimized to achieve approximately 55 Ω impedance through TDR. The worst package substrate coupling still exhibits $>$10 dB return loss up to 50 GHz and a maximum 0.2 dB insertion loss variance due to different package substrate materials is observed. The RF characterization of the assembled stitch-chip suggests that $<$0.66 dB insertion loss and $>$11.34 dB return loss up to 50 GHz can be measured for 500 μm long stitch-chip channels, which indicates a significant loss reduction from wire-bonding technology. The optimized stitch-chips show the measured impedances much closer to 50 Ω (average 46.85 Ω) than the wire-bond (maximum $\sim$170 Ω), which indicates a significant impedance matching improvement.

To this end, an RF-mechanical co-design for the CMI and impedance design for the assembled stitch-chips that can compensate for the pad pitch difference between die and the package substrate are developed to improve the stitch-chip's performance further. Compared with wire-bonding, the stitch-chip technology's scalable interconnects are promising for multi-chiplet integration for RF front-end modules.

CHAPTER 4
EMBEDDED MMIC SINGLE CHIP MODULE ENABLED BY FUSED-SILICA STITCH-CHIP TECHNOLOGY

Following the RF characterization of the stitch-chip technology using the passive testbeds in the previous chapter, a new demonstration of the technology using an active MMIC single-chip is presented, including design, layout, assembly, and characterization, in this chapter. A COTS chiplet (HMC-ALH369 LNA die from Analog Devices Inc. operating within 24 to 40 GHz) is selected for this purpose. In addition, thermal simulations are performed to evaluate the thermal capability of this module. The results are also benchmarked to state-of-the-art technologies.

4.1 Module Design

The design workflow of the single chip module can be described as three steps: (1) design of conductor-backed CPW on the package substrate, (2) design of the package cavity for embedding the bare die, and (3) module layout.

4.1.1 Conductor-backed CPW on package substrate

A conductor-backed CPW is designed on the top copper layer of the package substrate using ANSYS HFSS. As shown in Figure 4.1, the width of the center signal trace and the edge-to-edge distance between the center signal trace and adjacent reference planes are 170 μm and 130 μm respectively, which results in approximately 50 Ω impedance. Through-package vias are used to connect the top reference planes and bottom ground planes and function as RF shielding: the via pitch is smaller than a quarter of the interested wavelength (i.e. wavelength at 40 GHz) to prevent electric-field leakage and resonance [84].

The through-package via diameter (d) is swept in HFSS to study its impact on the

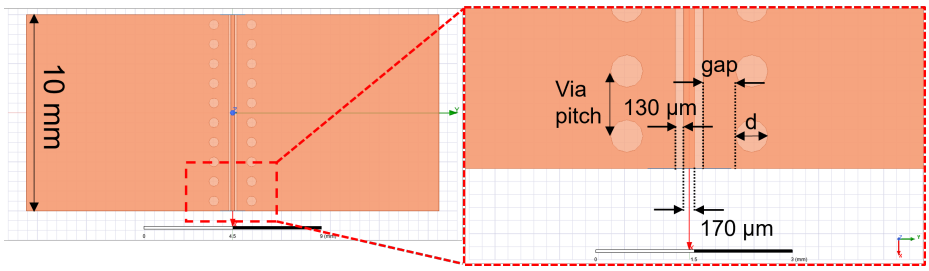
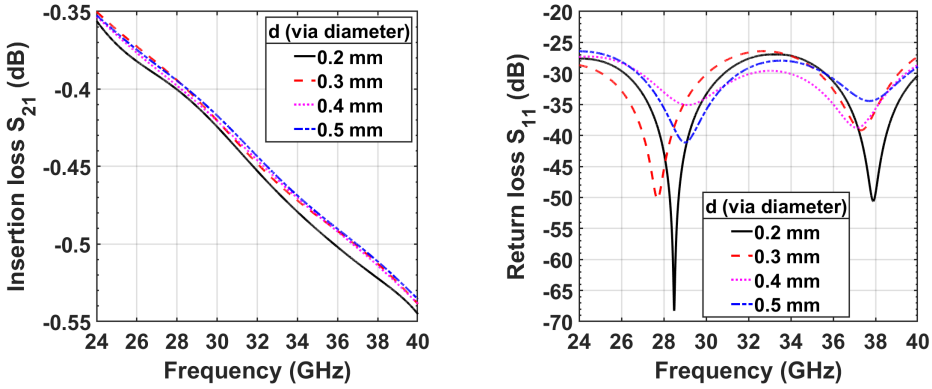


Figure 4.1: A top view of conductor-backed CPW

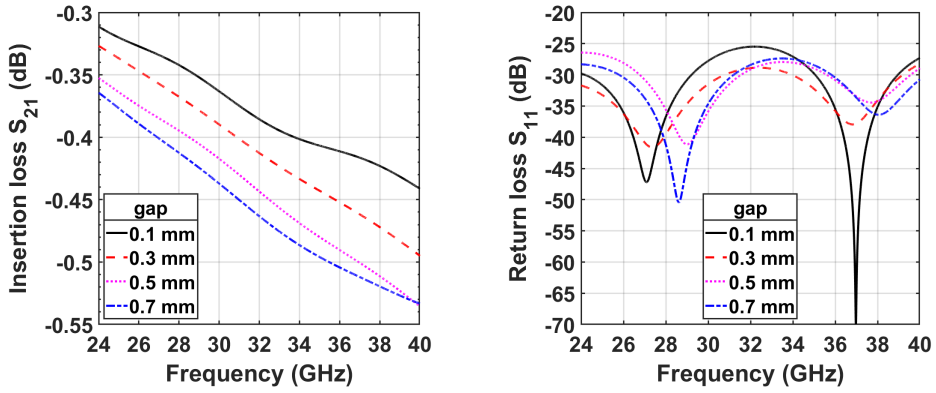


(a) (b)

Figure 4.2: Through-package via diameter's impact on (a) insertion loss and (b) return loss of conductor-backed CPW within LNA bandwidth (24-40 GHz)

losses of the conductor-backed CPW when the gap (gap) between the via and reference plane edge is fixed as 0.5 mm, as shown in Figure 4.1. In Figure 4.2, via diameter has a negligible effect on insertion loss and return loss: the 10 mm long conductor-backed CPW shows <0.55 dB insertion loss and >26 dB return loss up to 40 GHz. Note that the process variations of the conductor-backed CPW, such as copper roughness and dimension variation, are not considered in the simulation. As shown in Figure 4.3, decreasing the gap of through-package via and reference conductor's edge reduces the conductor-backed CPW's insertion loss (<0.44 dB up to 40 GHz), while the return loss keeps similar.

To this end, the conductor-backed CPW is designed as follows: center signal trace width is 170 μm; edge-to-edge distance between the signal trace and the adjacent reference planes is 130 μm; the through-package vias that connect top reference planes and bottom ground planes have 0.2 mm diameter, 0.6 mm pitch, and are 0.1 mm away from reference



(a) (b)

Figure 4.3: Impact of gap between through-package via and reference plane's edge on (a) insertion loss and (b) return loss of conductor-backed CPW within LNA bandwidth (24-40 GHz)

plane's edge.

4.1.2 Cavity design and die-package simulation

A die-package simulation is performed using ANSYS HFSS and Keysight ADS to study the impact of cavity design on module's RF performance. As shown in Figure 4.4, a cavity is created in the substrate, where a dummy GaAs (dielectric constant: 12.9) LNA die model is mounted using a conductive epoxy film on the internal copper layer that is at the bottom of the cavity. Note that the model was generated by cutting out a final package model into

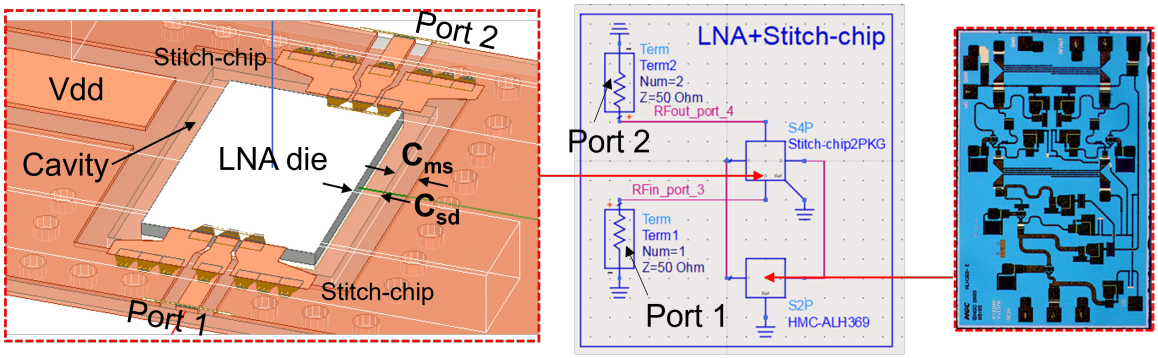


Figure 4.4: An angled view of die embedded in cavity and circuit simulation schematic of the module

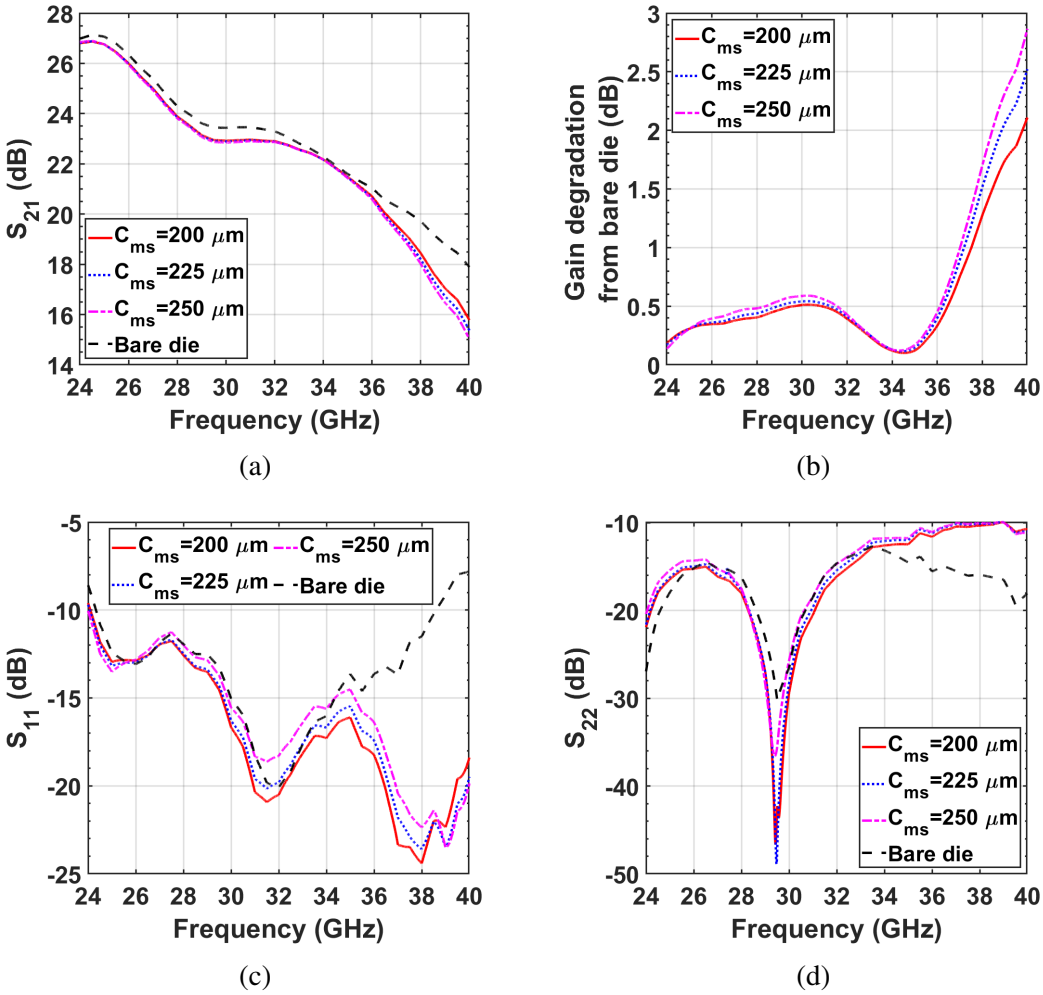


Figure 4.5: The impact of the clearance of reference plane edges to cavity edges (C_{ms}) on (a) gain, (b) gain degradation, (c) input return loss, and (d) output return loss of active module simulation

a smaller local region to decrease simulation time and computing resources. The cavity design depends on a clearance of surrounding reference plane edges to cavity edges (C_{ms}) and a clearance of cavity edges to the LNA die edges (C_{sd}). Note that ground vias are distributed all around the cavity to eliminate the cavity loop resonance [83]. The stitch-chips, which are designed as shown in Chapter 3, are assembled to connect the LNA die pad to the conductor-backed CPW on the package substrate. In Figure 4.4, the simulated S-parameters are shown: port 1 is located at the conductor-backed CPW's end, which is close to LNA RF input side; port 2 is located at the conductor-backed CPW's end, which is close

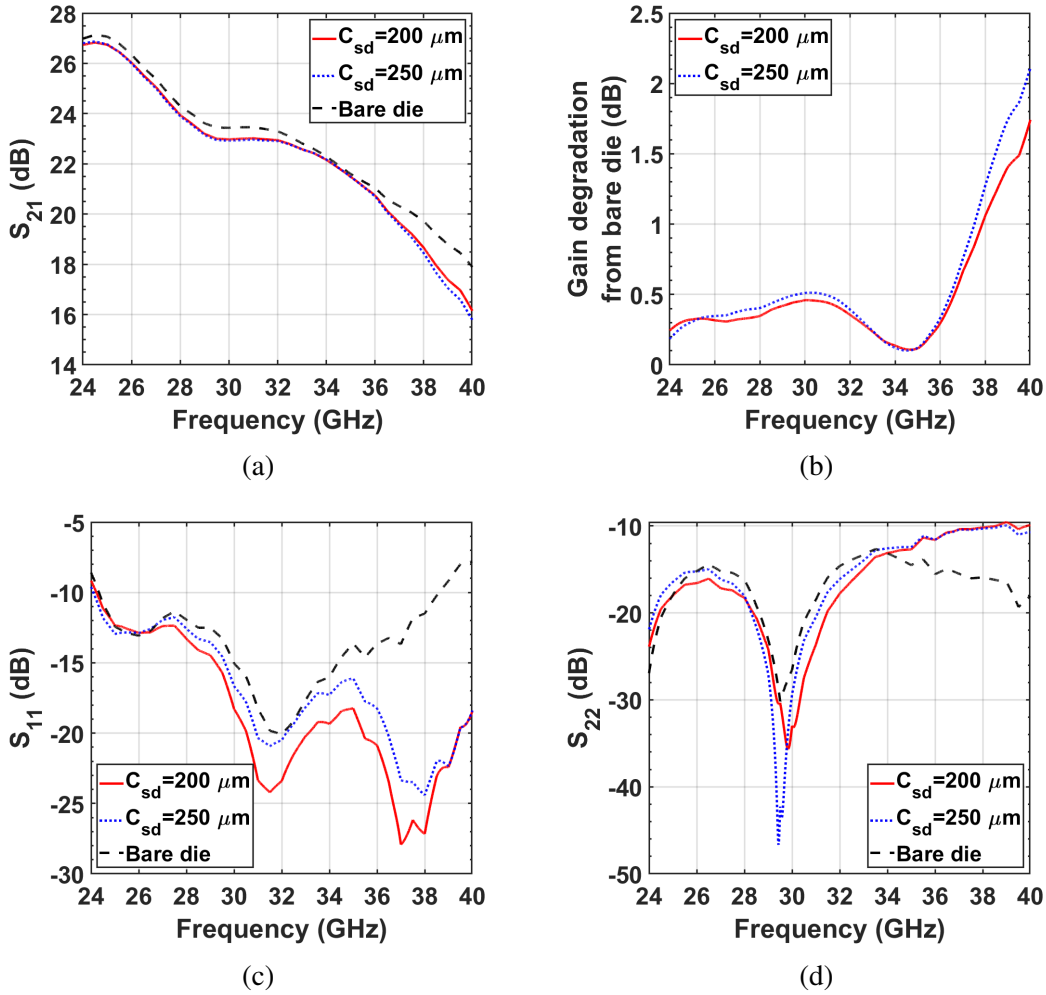


Figure 4.6: The impact of the clearance of cavity edges to die edges (C_{sd}) on (a) gain, (b) gain degradation, (c) input return loss, and (d) output return loss of active module simulation

to LNA RF output side. As shown in the middle of Figure 4.4, the simulated S-parameters are then imported into Keysight ADS and connected to the LNA die's S-parameters for an active module simulation. Figure 4.4 also shows how the ports map from ANSYS HFSS to Keysight ADS.

Figure 4.5 and Figure 4.6 show the embedded LNA die performance when the two clearances of the cavity design are optimized based on manufacturing limits. S_{21} represents the embedded LNA die's gain between port 2 (Figure 4.4) and port 1 (Figure 4.4), while S_{11} and S_{22} are return losses at port 1 and port 2, respectively. Figure 4.5a illustrates the

gain of the embedded LNA die with respect to different C_{ms} values. Bare die's gain from the datasheet is also added as a reference. The gain degradation is calculated by subtracting the embedded die's gain from the bare die's gain, as shown in Figure 4.5b. It is suppressed to 2.1 dB at 40 GHz when the top reference planes are 200 μm away from the cavity's edges (i.e. C_{ms} = 200 μm). In addition, S_{11} and S_{22} of the embedded LNA die follow the bare die data until approximately 35 GHz and show the lowest values when C_{ms} = 200 μm, as shown in Figure 4.5c and Figure 4.5d. Figure 4.6a shows the impact of C_{sd} on the embedded LNA die's gain. The embedded LNA die's gain is degraded by 1.7 dB when the die edges is 200 μm separated from the cavity's edges (i.e. C_{sd} = 200 μm) in Figure 4.6b. As shown in Figure 4.6c and Figure 4.6d, when C_{sd} = 200 μm, the embedded die's S_{11} and S_{22} show the lowest values especially at high frequencies. To this end, the two clearances (C_{ms} and C_{sd}) are both designed as 200 μm for lower gain degradation and return losses.

4.1.3 Module layout and simulation setup

The layout of the package substrate, which contains conductor-backed CPW as RF input and output traces and the cavity for embedding the LNA die, is performed using Altium Designer. The top view of the layout is shown in Figure 4.7a, and Figure 4.7b illustrates the stackup of the package substrate. Table 4.1 shows the RF and thermal material properties of the stackup. The designed cavity is milled out through the RO4350B layer and an internal copper layer is exposed at the bottom of the cavity. An active die (such as HMC-ALH369 LNA die from Analog Devices Inc.) can be embedded in the cavity. The designed conductor-backed CPWs are located close to the RF input/output pads of the LNA die. The bypass capacitor pads are placed close to the die for power delivery. As shown in Figure 4.7b, through-package vias are utilized to connect the bottom three copper layers and ground/reference planes to the top copper layer. The through-package vias function as RF shielding for the high-frequency signals (0.2 mm diameter and 0.6 mm pitch) and stitching vias to shorten the return path and improve thermal transfer (0.3 mm diameter and 0.6 mm

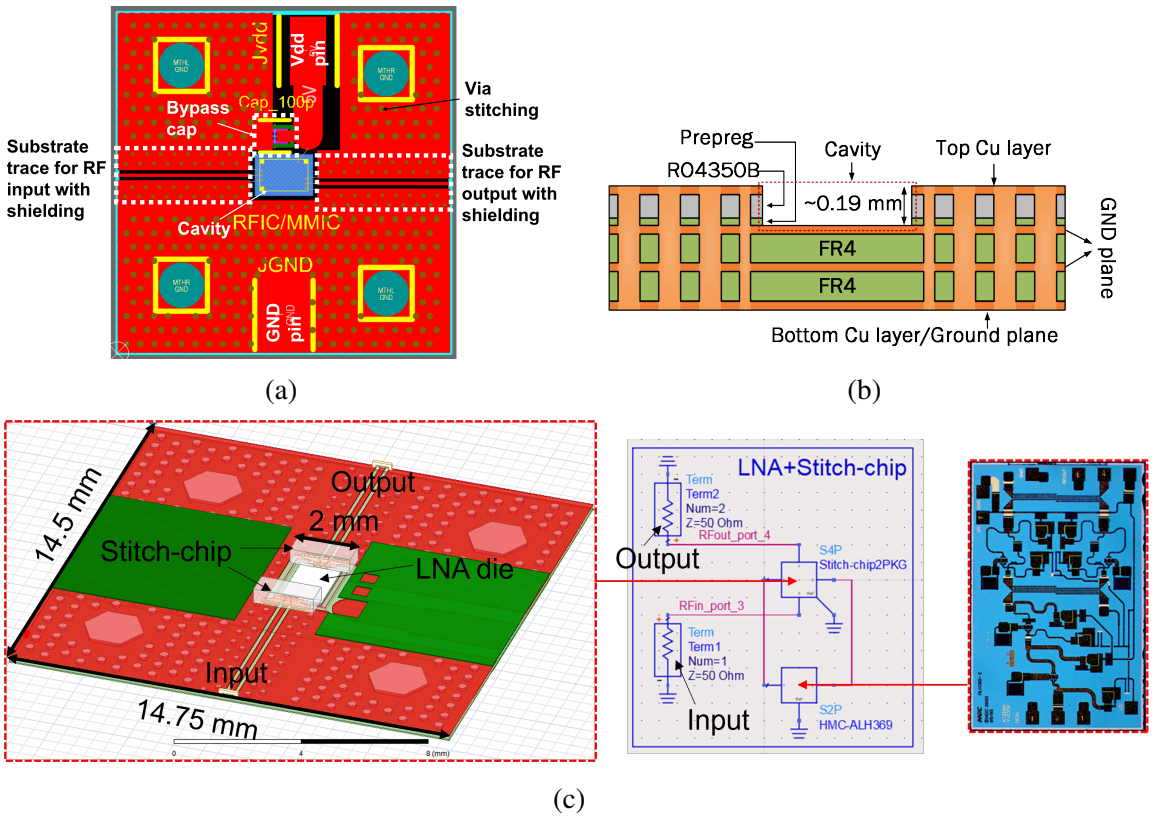


Figure 4.7: (a) Top view of package substrate layout, (b) a cross-sectional schematic of the package substrate, and (c) assembled package substrate model in HFSS and simulation with LNA die's S-parameters using Keysight ADS

pitch).

The package substrate layout is then exported as an ANSYS EDB file, which is imported into ANSYS HFSS 3D Layout and ANSYS HFSS. The dummy LNA die model and stitch-chip models are imported and assembled on the package substrate, as shown in Figure 4.7c. Next, the S-parameters of this assembled package are imported into Keysight ADS to simulate with LNA die's S-parameters to verify the module's RF performance. A schematic to show the simulation is depicted in Figure 4.7c. The simulation results will be discussed with the measurement results later in the chapter.

Table 4.1: Package Substrate Stack-Up and Material Properties

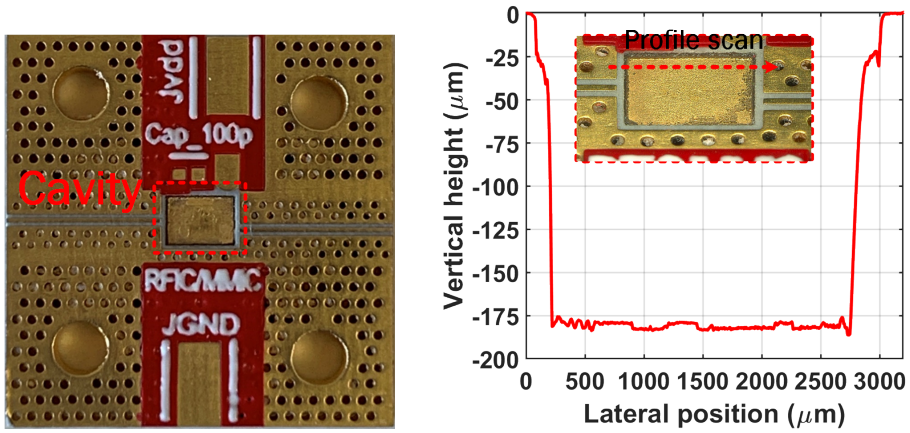
Material	**Thickness** (mm)	**Dielectric constant**	**Loss tangent**	**Thermal conductivity** ($Wm^{-1}K^{-1}$)
Copper	0.035	-	-	380
RO4350B	0.101	3.66	0.0037	0.69
FR4 prepreg	0.0565	4.4	0.02	0.25
Copper	0.035	-	-	380
FR4 core	1.83	4.4	0.02	0.25
Copper	0.035	-	-	380
FR4	0.1815	4.4	0.02	0.25
Copper	0.035	-	-	380

4.2 Module Assembly

Figure 4.8a shows a top view of a manufactured package substrate based on the layout, and Figure 4.8b shows the cavity profile that is measured by a Dektak 150 Profilometer. The distance between the cavity bottom and the top copper layer is approximately 180-190 μm.

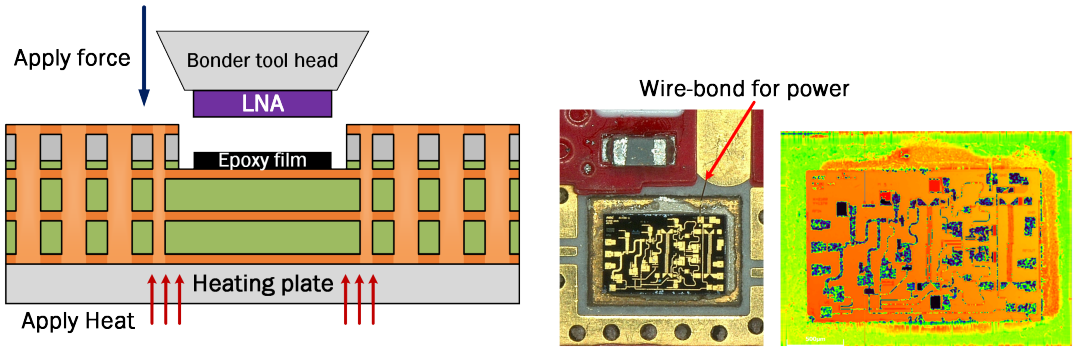
4.2.1 Die mounting

A 100 pF bypass capacitor is first assembled on the substrate through a reflow soldering process. Next, the 100 μm thick COTS LNA die (HMC-ALH369) is mounted inside the cavity using a 101.6 μm thick conductive epoxy film (LOCTITE ABLESTIK CF 3350), as shown in Figure 4.9a: the epoxy film is placed inside the cavity; the die is then aligned and placed on the epoxy film using a Finetech FINEPLACER lambda flip-chip bonder. Next, the epoxy film is cured at 175 °C for 30 minutes while the die is pressed with approximately



(a) (b)

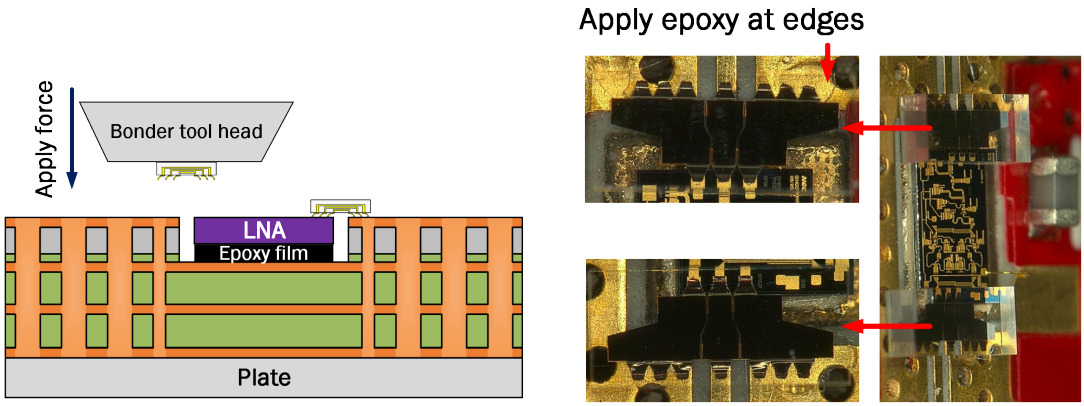
Figure 4.8: (a) A top view of manufactured package substrate and (b) profile characterization of the milled cavity



(a) (b)

Figure 4.9: (a) LNA die mounting process and (b) a top view and surface profile of the mounted die

0.1 N assembly force using the flip-chip bonder. Note that the bonder tool head is required to be as flat as possible, otherwise, the top surface of the die would be damaged after mounting and the die performance would be degraded. Figure 4.9b shows a top view and a confocal image of the mounted die surface. Note that the die's power pad is connected to the power trace on the package substrate by a wire bond. The confocal image shows similar color across the die's surface, which suggests that the bond line of the die is uniform because of the epoxy film.



(a) (b)

Figure 4.10: (a) Stitch-chip assembly process and (b) an angled view of assembled stitch-chips on the die

4.2.2 Stitch-chip assembly

The stitch-chips, whose design and fabrication are described in chapter 3, are assembled on the package substrate to form the electrical connections between the die and the package substrate. The stitch-chips are designed to compensate for the difference of the pitches of the die pads and package traces. Further, CMIs on the stitch-chips are designed to deform locally to compensate for any non-planarity within the package. As shown in Figure 4.10a, the stitch-chips are flipped (the CMIs are facing down) and picked by the flip-chip bonder. The flip-chip bonder is also utilized to align the stitch-chips to the die pad. Next, a small amount of epoxy is applied around the edges of the stitch-chips and the stitch-chips are pressed with 0.1 N force using the flip-chip bonder. Two stitch-chips are needed in this module for die input and output. The final assembled module is shown in Figure 4.10b.

4.2.3 Wire-bonding as reference

After the die is mounted inside the cavity, wire bonds can be utilized instead of the stitch-chips to connect the die's RF input/output pads to the package substrate traces for comparison. As shown in Figure 4.11, approximately 1 mm long gold wire-bonds (25.4 μm diameter) are used to connect the die's signal pads to center signal traces of the conductor-backed

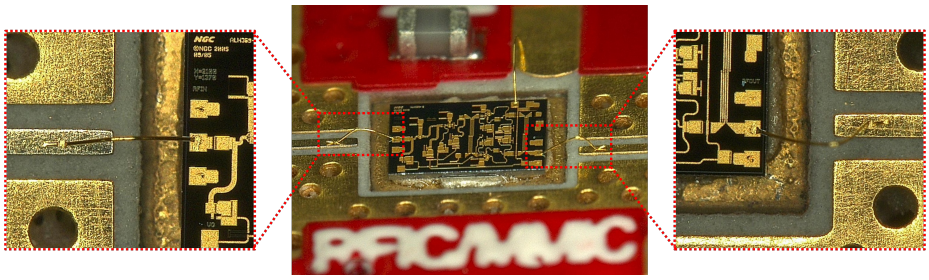
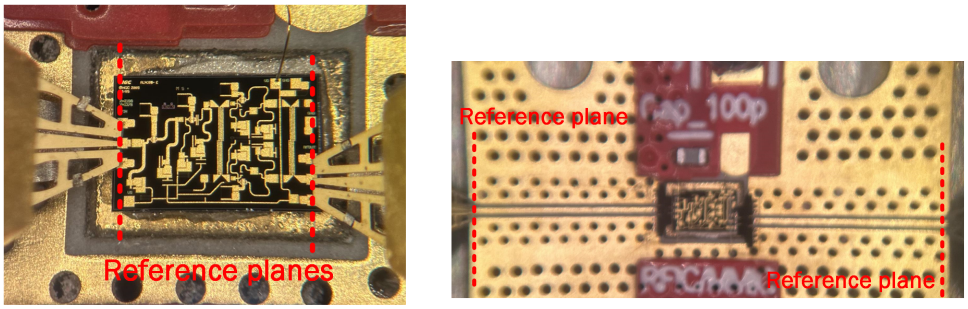


Figure 4.11: Connecting die's input and output to package substrate using wire-bonding instead of stitch-chips



(a) (b)

Figure 4.12: (a) Probing on embedded bare die and (b) probing on module

CPW on the package substrate. Note that the die's ground pads are already connected to the bottom ground plane of the die by through die vias, which are then connected to the package ground planes directly through the epoxy film. Therefore, there is no need to use additional wire bonds to connect the die's ground pads to the package ground.

4.3 RF Characterization and Benchmarking

Two RF measurements are performed on the module using stitch-chips: (1) an embedded bare die testing when two Cascade Microtech G-S-G $|Z|$ 200 μm pitch probes are directly landed on the LNA die's RF pads, as shown in Figure 4.12a and (2) whole module testing when two Cascade Microtech $|Z|$ 300 μm pitch probes landed on package substrate traces, as shown in Figure 4.12b. The RF measurements are conducted within the LNA bandwidth (24-40 GHz) using Keysight N5245B PNA-X with SOLT calibration to move the reference planes to the probes' tips, as shown in Figure 4.12.

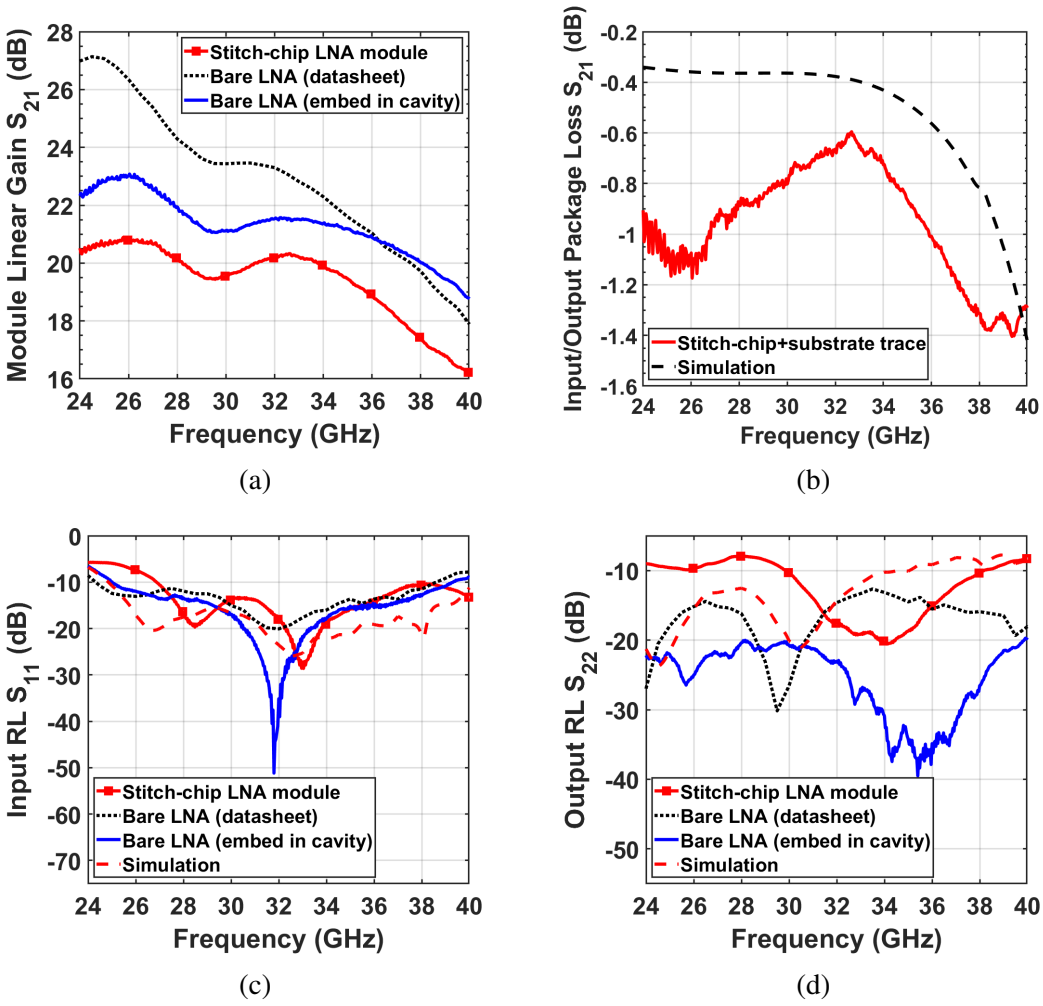


Figure 4.13: RF performance of LNA single chip module using stitch-chips (stitch-chip LNA module): (a) linear gain, (b) loss of one stitch-chip and one package conductor-backed CPW, (c) input return loss, and (d) output return loss

4.3.1 Linear gain degradation and return loss

The RF measurements of the LNA single chip module using stitch-chips are depicted in Figure 4.13. The bare LNA die's data from the datasheet is added as a reference to demonstrate the module's performance. The difference between the data from the datasheet and the embedded LNA die may result from the impact of embedding. As shown in Figure 4.13a, a maximum 2.5 dB package loss within the LNA bandwidth is observed, which is calculated by subtracting stitch-chip LNA module's linear gain from embedded bare LNA die's linear gain. Such package loss includes two stitch-chips and two RF signal traces

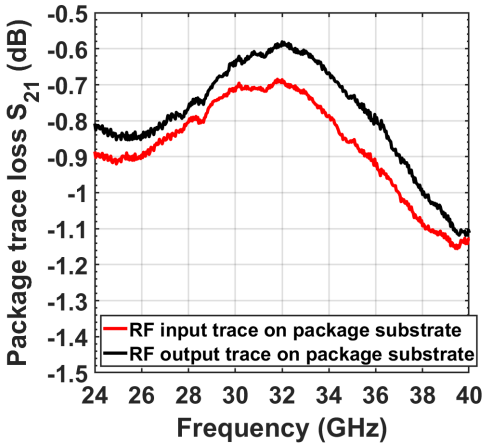


Figure 4.14: Loss measurement of RF traces on package substrate

on the package (RF input/RF output). In Figure 4.13b, the measured insertion loss of one stitch-chip and one RF signal trace on the package is $<$1.4 dB within the LNA bandwidth, while the RF signal trace on the package is measured to have $<$1.15 dB, as shown in Figure 4.14. Process variance of the organic package substrate, such as copper roughness, can result in a mismatch between the simulation and measurement.

Figure 4.13c and Figure 4.13d show the return losses of the LNA module using stitch-chips. The module's measured input return loss is well correlated with the data from the bare LNA die datasheet and from the bare die embedded in the cavity except for 32 GHz. The correlation suggests a minimal impact of the proposed stitch-chip technology on the signal reflection of the LNA die. As shown in Figure 4.13d, the stitch-chip LNA module shows a degradation in the output return loss, compared with the embedded bare LNA die in the cavity. However, it still possesses $>$8 dB within the LNA bandwidth. The mismatch between the simulation and the measurement may result from the substrate process variations, such as copper roughness.

4.3.2 Compare with wire-bonded module

The RF measurements are also performed on the LNA module using wire-bonding, which is shown in Figure 4.11 and the results are shown in Figure 4.15. The data from bare LNA's

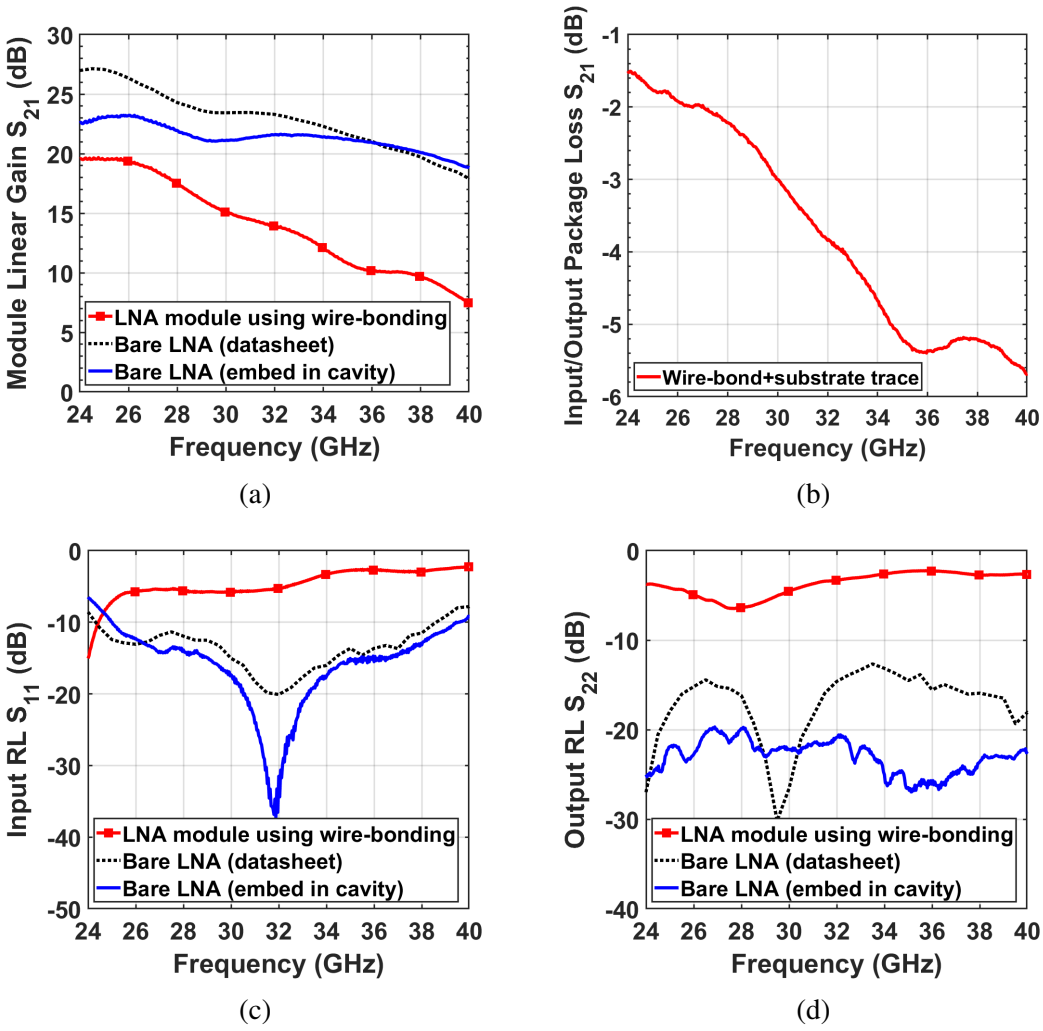


Figure 4.15: RF performance of LNA single chip module using wire-bonding: (a) linear gain, (b) loss of one wire-bond and one package conductor-backed CPW, (c) input return loss, and (d) output return loss

datasheet are also added. The module linear gain degrades significantly with frequency (e.g., the gain reduces to 7.5 dB at 40 GHz) because of wire bonding, as shown in Figure 4.15a. One wire-bond and one package conductor-backed CPW are measured to have <5.6 dB loss up to 40 GHz in Figure 4.15b. As shown in Figure 4.15c and Figure 4.15d, compared with the embedded bare die's return losses, using wire-bonding increases return losses significantly as well because of its high parasitic inductance.

To compare the stitch-chip technology with conventional wire-bonding technology for such LNA single chip module, the input/output package losses are calculated and in-

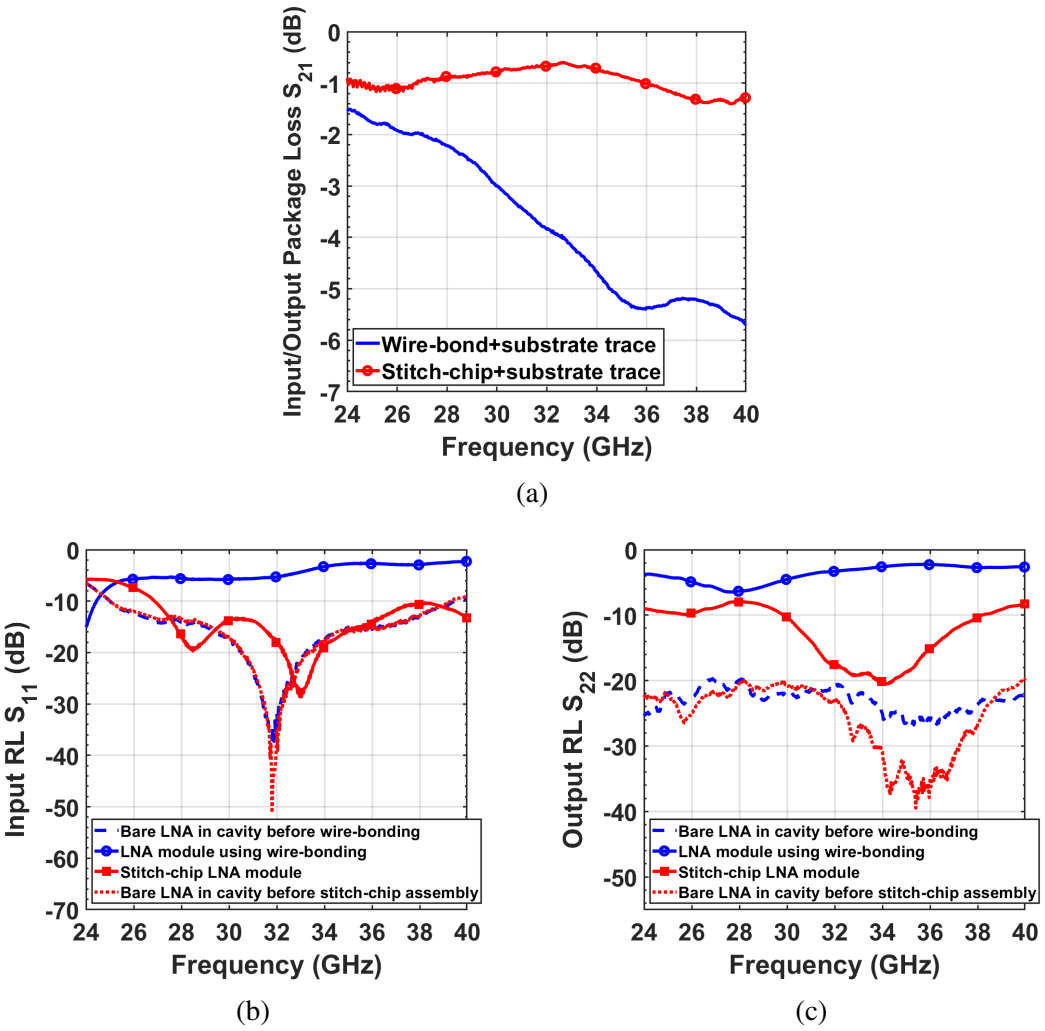


Figure 4.16: RF performance comparison between wire-bonded LNA module and stitch-chip LNA module: (a) package loss, (b) input return loss, and (c) output return loss

put/output return losses are plotted together in Figure 4.16. In Figure 4.16a, the stitch-chip technology demonstrates approximately 4.4 dB loss improvement at 40 GHz from wire-bonding technology. Note that the substrate trace losses are the same in the wire-bonded and stitch-chip modules assuming minimal variation because they are manufactured using the same design and in the same batch. Therefore, the stitch-chip technology is a major contribution to the 4.4 dB loss improvement. In addition, as shown in Figure 4.16b and Figure 4.16c, using stitch-chip technology leads to much lower signal reflection across the whole LNA bandwidth, compared to wire-bonding. Note that the embedded dice in the

Table 4.2: Performance benchmarking of technologies for the embedded RF chiplet module

Technology	**Die /substrate**	**Bandwidth (GHz)**	**Package loss (dB)**	**Interconnect loss (dB/mm)**	**Return loss (dB)**
Stitch-chip	GaAs LNA/glass, organic	24-40	<2.5	<0.23	>8
Wire-bonding	GaAs LNA/organic	24-40	<10.5	<0.9	>2
Inkjet-MCM [38]	GaAs LNA/organic	20-40	<5	-	>4
MECA [36],[37]	GaN PA/BCB, Si	8-12	<2.5	-	>8
LEDPAM [40]	GaAs LNA/ABS	65-110	<5.2	<0.54	>7.25
Si-embedded IC [83]	CMOS DA, multiplier/Si	80-100	-	<0.63	-
AJP-SCM [39]	GaAs attenuator/BCB, PI, MoCu	0-50	<2	<0.74	>5

modules using stitch-chip and wire-bond show similar input/output return losses before stitch-chip assembly or wire-bonding, which suggests that wire-bonding causes the higher return loss degradation.

4.3.3 Benchmarking to state-of-the-art

Table 4.2 summarizes the RF performance of recent embedded-chip technologies for single-chip or multi-chip module demonstrations. The package loss is calculated by subtracting the module's linear gain from the bare die's linear gain, while interconnect loss is defined as the per-unit-length loss of both the RF trace on the package substrate and the die-to-package transition. The return loss is measured on the package.

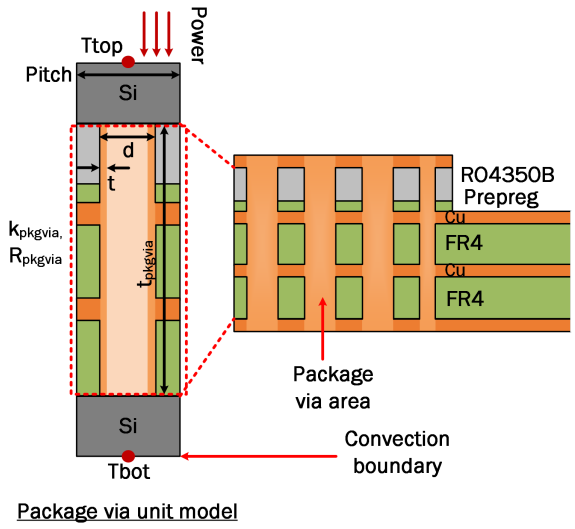


Figure 4.17: Thermal simulation setup schematic for the LNA single chip module

The LNA single chip module using stitch-chip technology shows superior package loss and return loss to a similar module using inkjet printing to fabricate the interconnects [38]. Furthermore, the stitch-chip technology establishes a similar or better RF performance than other additive manufacturing technologies, such as aerosol jet printing [39] and laser-enhanced direct print additive manufacturing (LEDPAM) [40]. Additive manufacturing suffers from potential performance degradation/variation and impedance discontinuity due to significant process variation from tool capability [39].

Metal-Embedded Chiplet Assembly (MECA) technology is demonstrated for MMIC to realize short fabrication cycle time and monolithic-like performance [36]. It also utilizes a copper layer at the bottom of the package substrate to perform thermal management when integrating high-power PA. The stitch-chip technology demonstrated in the LNA module shows comparable RF performance as the MECA technology. In addition, embedding CMOS Driver Amplifier (DA) and multiplier in a Si interposer is reported in [83].

4.4 Thermal Analysis

Steady-state thermal simulations are performed in ANSYS Workbench to evaluate the thermal performance of such LNA single chip module. It is computationally expensive for such

thermal simulations to take each through-package via into account. Therefore, as shown in Figure 4.17, the through-package via is simulated firstly as a unit model in the package substrate [85], which generates the effective thermal conductivity value of regions in the substrate that contain the vias. Next, these values are used as input into the thermal model of the module to acquire the LNA average temperature.

4.4.1 Package via unit model simulation

The unit model of the through-package via is shown in Figure 4.17. In the model, the through-package via is interfaced with 800 μm thick (t_{Si}) bulk silicon (σ_{Si}: 170 $Wm^{-1}K^{-1}$) at the top and bottom. The via has 0.6 mm pitch/width (p) as designed and assumes copper is fully filled inside. The diameters (d) are 0.2 mm for the shielding via and 0.3 mm for the stitching via in the package. Next, the top silicon temperature (T_{top}) and bottom silicon temperature (T_{bot}) are obtained by injecting a power density (PD) at the top silicon surface and applying a convection boundary condition at the bottom silicon surface. Therefore, the series thermal resistance of the via and the bulk silicon (R_{tot}) is:

$$R_{tot} = \frac{T_{top} - T_{bot}}{PD \times p^2} \tag{4.1}$$

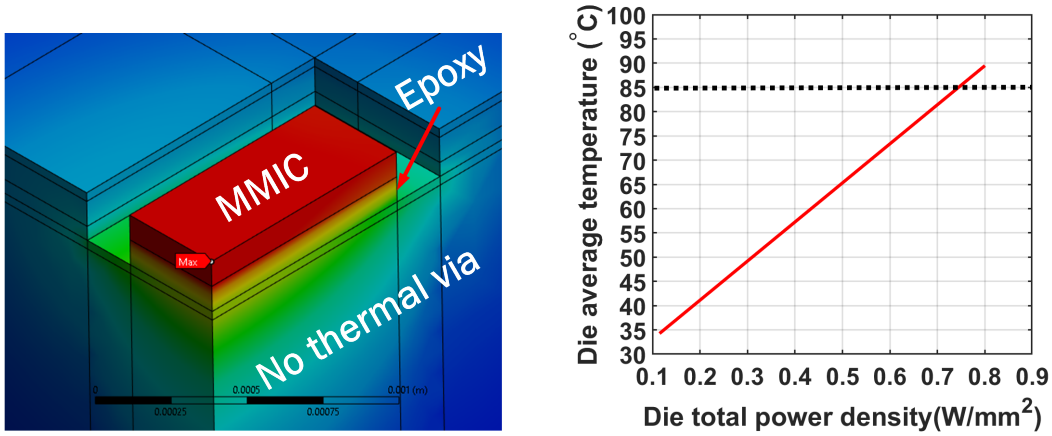
Because the bulk silicon thermal resistance (R_{Si}) can be calculated as follows:

$$R_{Si} = \frac{t_{Si}}{\sigma_{Si} \times p^2} \tag{4.2}$$

the effective thermal resistance and conductivity of the via model are derived:

$$R_{pkgvia} = \alpha \times (R_{tot} - 2R_{Si}) \tag{4.3}$$

$$k_{pkgvia} = \frac{t_{pkgvia}}{R_{pkgvia} \times p^2} \tag{4.4}$$



(a) (b)

Figure 4.18: Thermal simulation of LNA module: (a) thermal map of embedded LNA die in the cavity and (b) die average temperature with increasing die power density

where t_{pkgvia} is the through-package via height in Figure 4.17 and α is a correction factor for the thermal resistance, given the actual vias have a partial copper filling rather than the assumed full filling in the model. α can be calculated [86]:

$$\alpha = \frac{d^2}{4t(d-t)} \tag{4.5}$$

where t is copper plating thickness, which is 50 μm. Note that the effective thermal resistance (R_{pkgvia}) and conductivity (k_{pkgvia}) not only depend on the conductor but also take nearby laminate materials into account, as shown in Figure 4.17. The effective thermal conductivity of the substrate regions that contain the 0.2 mm and 0.3 mm through-package vias are 22.982 $Wm^{-1}K^{-1}$ and 37.876 $Wm^{-1}K^{-1}$, respectively.

4.4.2 Thermal analysis for module

Quarter symmetry is utilized to conduct the thermal analysis of such LNA single chip module for computation time reduction. The effective thermal conductivities that are calculated before are used as input in the model. The LNA's power density is applied at the top surface of the die geometry and air convection boundaries are applied at the top (10 $Wm^{-2}K^{-1}$),

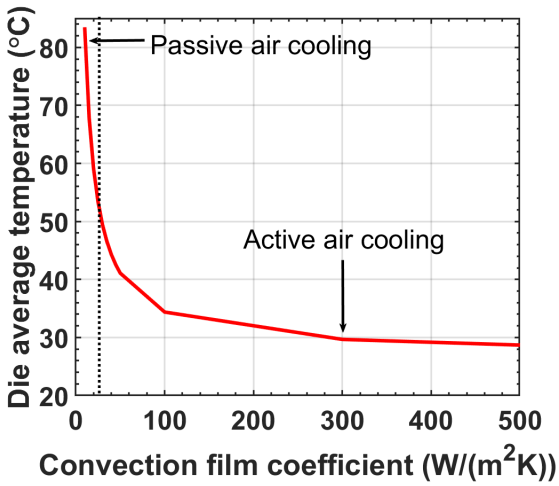


Figure 4.19: Peripheral air convection impact on die average temperature of the single chip module (die power density fixes as 0.75 W/mm^2)

bottom (5 $Wm^{-2}K^{-1}$), and lateral (10 $Wm^{-2}K^{-1}$) surfaces of the model. Figure 4.18a shows a perspective view of the temperature distribution around the embedded LNA die. A thick conductive epoxy film (7 $Wm^{-1}K^{-1}$) is used as die-attaching material in the actual assembly. As shown in Figure 4.18a, the heat is generated from the die and tends to spread to the bottom substrate. The average LNA die temperature is approximately 34.2 $^{\circ}C$. To understand the power handling capacity of the single chip module, the die power is increased to reach the 85 $^{\circ}C$ die temperature limit, which is a common maximum RF die operating temperature. As shown in Figure 4.18b, the die power density is approximately 0.75 W/mm^2 when the die average temperature is around 85 $^{\circ}C$, which implies the single chip module's potential to integrate higher-power die, such as driver amplifier or power amplifier.

To further reduce the die average temperature, active air cooling can be implemented at the top surface of the package, while natural air convection may not be efficient to extract heat out of the module. To this end, a preliminary study of the convection film coefficient (heat transfer coefficient) at the top surface is performed to emulate air cooling. As shown in Figure 4.19, the die average temperature decreases with a higher heat transfer coefficient. The die average temperature reduces to approximately 50 $^{\circ}C$ with around 20 $W/(m^2K)$

heat transfer coefficient and saturates when increasing the heat transfer coefficient even further. The results suggest that air cooling with a higher heat transfer coefficient is a promising method to extract heat efficiently for embedding much higher power RF die ($>$0.75 W/mm^2) in the module. In addition, as the device layer is at the top surface of the RF die, increasing the heat transfer coefficient or applying air cooling at the top surface of the module is apparently more effective than other thermal management methods.

4.5 Conclusion

In this chapter, an embedded LNA single-chip module using the fused-silica stitch-chip technology is demonstrated for the first time, including module design, assembly, and characterization.

Below 2.5 dB package loss and less than 1.4 dB interconnect loss including the stitch-chip and RF trace on the package are measured up to 40 GHz. The module's input return loss is similar to the bare die and the output return loss is better than -8 dB, which implies minimal signal reflection. The module using the stitch-chip technology is also compared with the module bonded by wire bonding and other state-of-the-art embedded RF chiplet modules. The stitch-chip reduces the package loss significantly ($\sim$8 dB), compared with wire-bonding, and possesses comparable or better performance than state-of-the-art (additive manufacturing technologies). Steady-state thermal simulations are conducted to evaluate the thermal performance of the module. The LNA die average temperature is simulated as 34.2 °C and the maximum power density that the module can handle when the die temperature reaches 85 °C is around 0.75 W/mm^2. Air cooling at the top package surface is promising to extract the heat from the package efficiently, which results in $>$36.01% lower die temperature.

To this end, it is shown that the fused-silica stitch-chip technology features lower loss interconnects than wire bonds for RF/mm-wave integration using an active die as a single chip module. This technology can be a promising solution to future mm-wave multi-chiplet

based modules.

CHAPTER 5

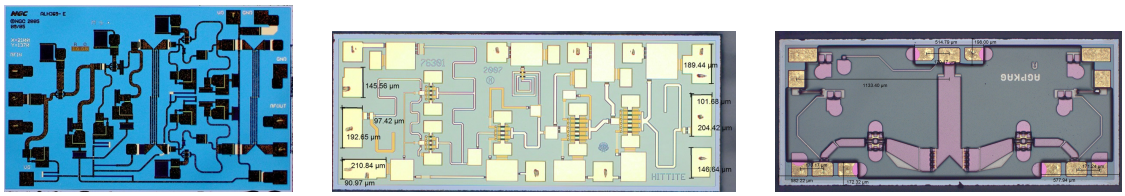
DEVELOPMENT OF STITCH-CHIP TECHNOLOGY FOR EMBEDDED MULTI-CHIP MODULE

To demonstrate the functional scalability of polylithic integration using fused-silica stitch-chip technology, this chapter further explores a co-design of the stitch-chip and a package substrate for a multi-chip module. A portion of a RF-front end including an LNA die, a DA die, and a switch die is investigated to build the multi-chip module using stitch-chips in this chapter.

5.1 Multi-Chip Module Design Overview

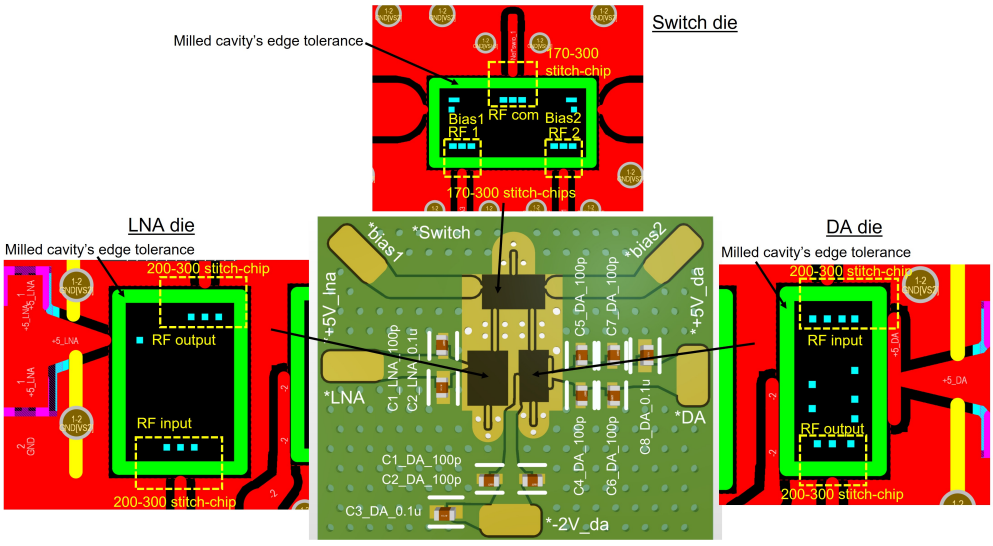
Three types of COTS mm-wave die (K/Ka-band) are selected to build the multi-chip module, as shown in Figure 5.1: (a) HMC-ALH369 LNA die from Analog Devices Inc. operating within 24 to 40 GHz, (b) HMC635 DA die from Analog Devices Inc. operating within 18 to 40 GHz, and (c) MASW-011144-DIE switch die from MACOM Technology Solutions operating within 20 to 40 GHz.

The dimensions of these three dice are summarized as follows: (a) the LNA die size is 2.1 $\times$ 1.37 mm^2 and 100 μm thick with 200 μm pitch RF pads, (b) the DA die size is 1.95 $\times$ 0.84 mm^2 and 100 μm thick with 200 μm pitch RF pads, and (c) the switch die size is

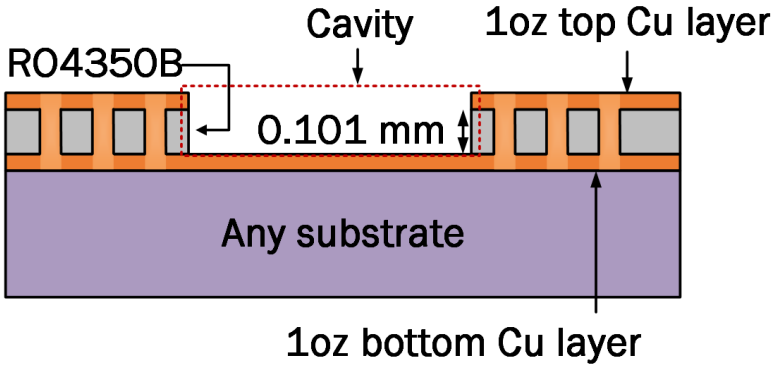


(a) (b) (c)

Figure 5.1: Top views of (a) HMC-ALH369 LNA die, (b) HMC635 DA die, and (c) MASW-011144-DIE switch die



(a)

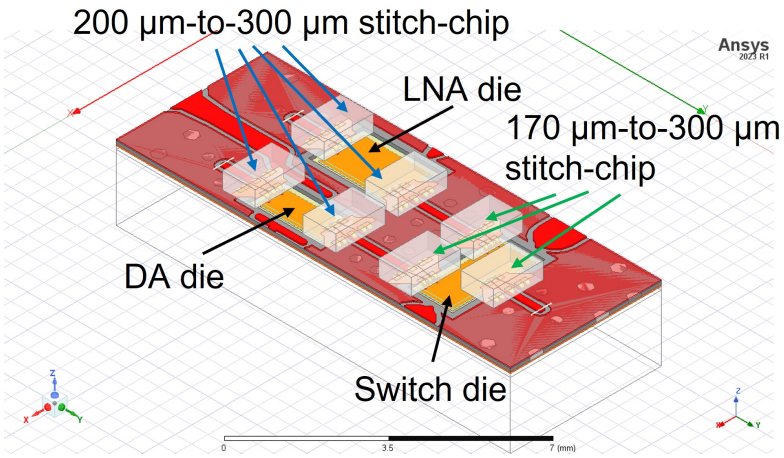


(b)

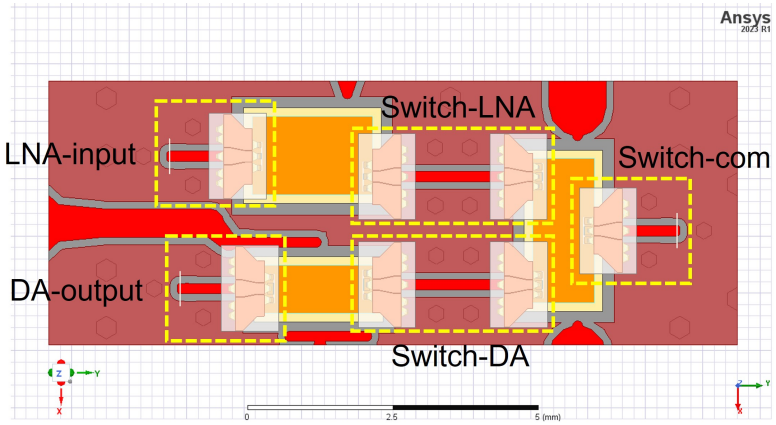
Figure 5.2: (a) A top view of a baseline multi-chip module layout and (b) the module cross-sectional view

2.52 $\times$ 1.08 mm^2 and 100 μm thick with around 170 μm pitch RF pads.

Based on the aforementioned die dimensions, a layout is performed using Altium Designer for a baseline multi-chip module package substrate. A top view of the layout and its cross-sectional stack-up are shown in Figure 5.2. In Figure 5.2a, three cavities (black regions) are milled out in the package substrate for embedding dice. Further, there are two RF chains in the module: switch to LNA RF chain and switch to DA RF chain. Seven stitch-chips are required to provide the connections between the dice and the package substrate. Ten bypass capacitors (seven 100 pF and three 0.1 μF surface-mounted capacitors in



(a)



(b)

Figure 5.3: (a) An angled view and (b) a top view of assembled HFSS model of the multi-chip module

0402 footprint) need to be assembled for power delivery. In Figure 5.2b, a 0.101 mm thick RO4350B dielectric layer with a top and a bottom copper layer is on a bottom substrate. The bottom copper layer provides the RF ground shielding. The bottom substrate can be a metal plate to achieve better heat spreading when integrating high-power die into this module without RF performance degradation. Plated vias that connect the bottom copper layer to the top copper layer function as RF shielding and maintain a low impedance and short return loops for power delivery.

The layout model is then imported into ANSYS HFSS following the workflow described in the previous section. The three cavities are opened in the model and three die

models having 50 Ω RF pads are embedded inside these cavities, as shown in Figure 5.3a. Note that the model is a cut out from the whole module to reduce computing resources for the simulation. While the stitch-chip designed in the previous section (200 μm-to-300 μm stitch-chip, as shown in Figure 5.3a) can be used to bridge LNA/DA dice to the package substrate, a new stitch-chip (170 μm-to-300 μm stitch-chip, as shown in Figure 5.3a) that can compensate for the pad pitch mismatch between the switch die and package substrate is necessary. This new stitch-chip design is achieved by using re-optimized 170 μm pitch and 50 μm high CMIs, which have >12.25 dB return loss, <0.39 dB insertion loss up to 65 GHz, and 30 μm elastic deformation range. The two types of stitch-chips are then assembled on the model, as shown in Figure 5.3a. In Figure 5.3b, there are five interconnects that need to be evaluated to optimize the module RF performance: (1) Switch-LNA interconnect represents a D2D interconnect that connects the switch die and the LNA die; (2) Switch-DA interconnect represents a D2D interconnect that connects the switch die and the DA die; (3) LNA-input interconnect represents a die-to-package interconnect at the LNA input side; (4) DA-output interconnect represents a die-to-package interconnect at the DA output side; (5) Switch-com interconnect represents a die-to-package interconnect at switch RF input/output side. Because the D2D interconnects are critical to RF performance of the whole multi-chip module, they are investigated in depth.

5.2 Design Case Investigation

5.2.1 Impact of die-to-die package traces

Figure 5.4 shows a top view of the two module D2D interconnects: Switch-LNA and Switch-DA interconnects. Each interconnect consists of one 200 μm-to-300 μm stitch-chip, one 170 μm-to-300 μm stitch-chip, and a package trace with an L-length between the two stitch-chips. The length of the package trace (L) is decreased to investigate its impact on reducing interconnect losses.

In this study, 2 mm, 1.5 mm, 1.3 mm, and 1.1 mm package traces are simulated within

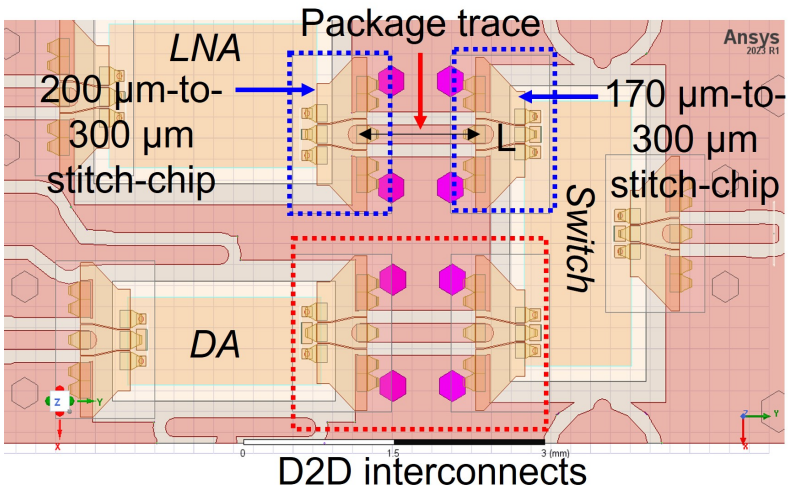


Figure 5.4: A top view of D2D interconnects in the multi-chip module

the interested bandwidth and the results are shown in Figure 5.5. In Figure 5.5a and Figure 5.5b, reducing the package trace length leads to a significant decrease in insertion loss: approximately 0.5 dB insertion loss at high-frequency is reduced and the insertion loss resonances are mitigated by shortening the package trace from 2 mm to 1.3 mm. A minimal improvement is observed when further shortening the package trace to 1.1 mm. Given the flip-chip bonder requirements for the assembly of 200 μm-to-300 μm and 170 μm-to-300 μm stitch-chips, the 1.3 mm package trace length is selected for the following study in this chapter.

In addition, Figure 5.5c and Figure 5.5d illustrate the impact of the package trace length on the return losses of the module D2D interconnects. Solid lines show the return losses at the switch die pads, which connect to the 170 μm-to-300 μm stitch-chip, while dotted lines represent the return losses at the LNA or DA die pads, which connect to the 200 μm-to-300 μm stitch-chip. As the package trace length reduces, the interconnects' parasitics decrease, which shifts the resonances of return loss to higher frequencies, as shown in Figure 5.5c and Figure 5.5d. Both interconnects show $>$17 dB return losses when the package trace length is 1.3 mm.

When decreasing the length of the package trace, it is critical to keep multiple RF

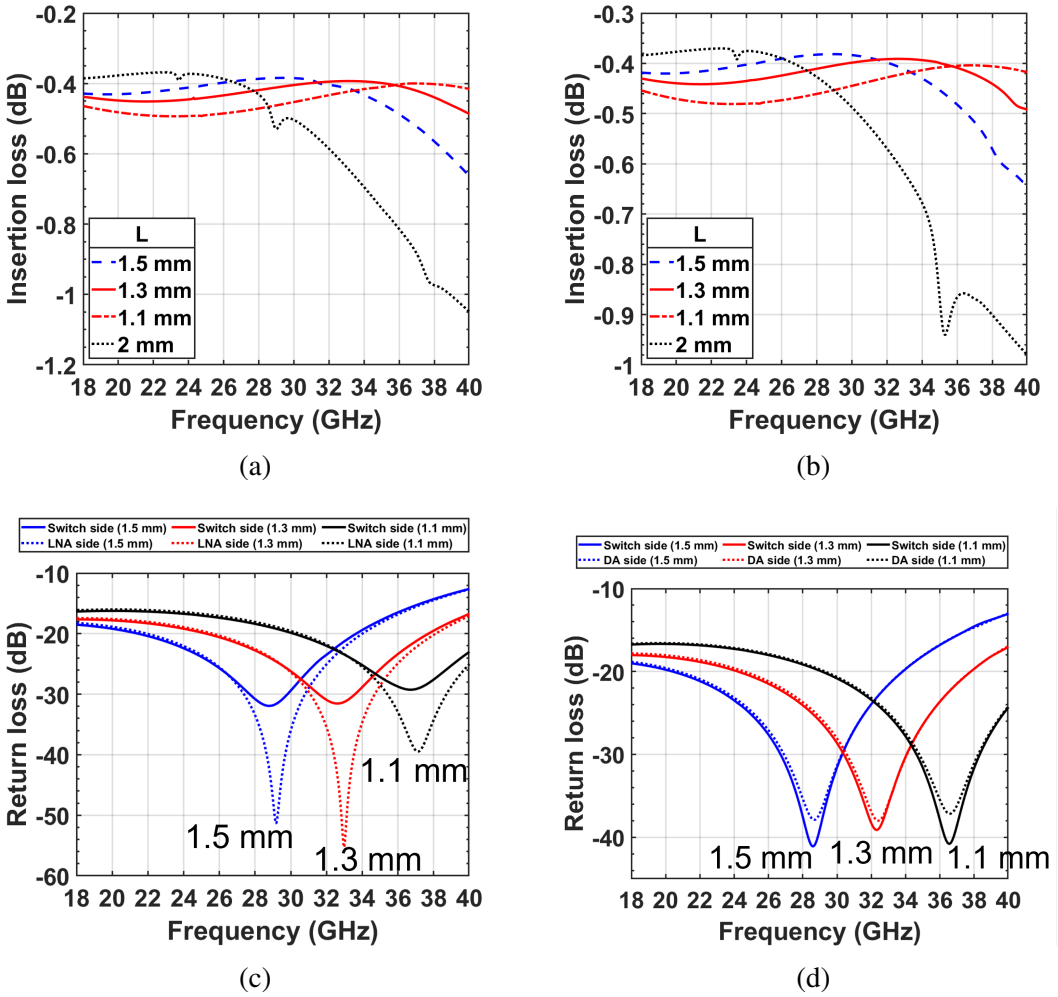


Figure 5.5: Impact of package trace length on insertion loss of (a) Switch-LNA interconnect and (b) Switch-DA interconnect and return loss of (c) Switch-LNA interconnect and (d) Switch-DA interconnect

shielding vias along the package trace to prevent any potential RF signal leakage, which may cause unwanted resonances in the insertion loss [84]. Figure 5.6a and Figure 5.6b show the cases where one or two vias are along each side of the package trace. As shown in Figure 5.6c and Figure 5.6d, the two vias case (via pitch is calculated as $\sim 0.15\lambda$) can prevent 'loss dip' in the insertion loss of the module D2D interconnects (red lines in figures) without degrading return loss significantly. This is because the via pitch is smaller than a quarter of the wavelength of interest (i.e. wavelength at 40 GHz), which can prevent electric-field leakage and unwanted resonance [84].

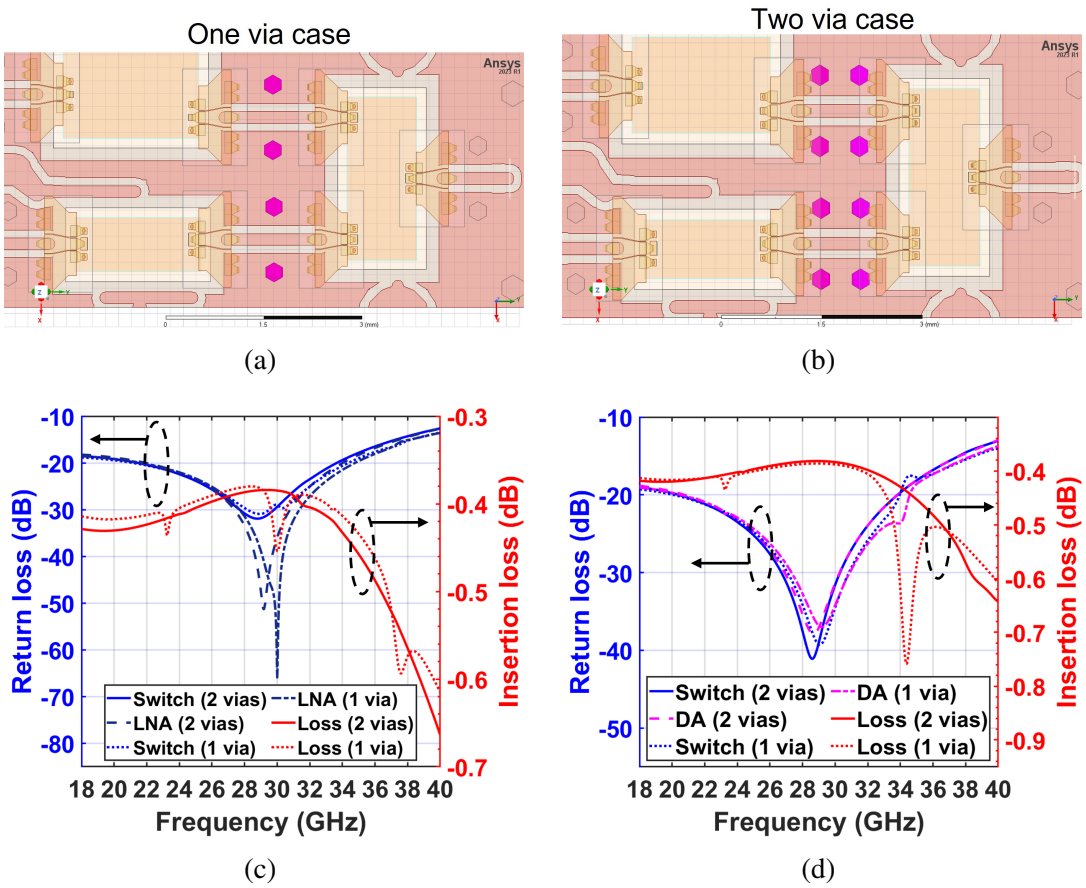
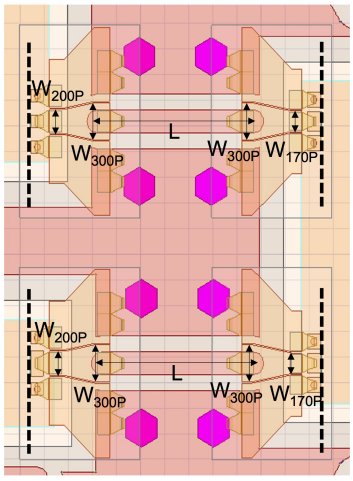


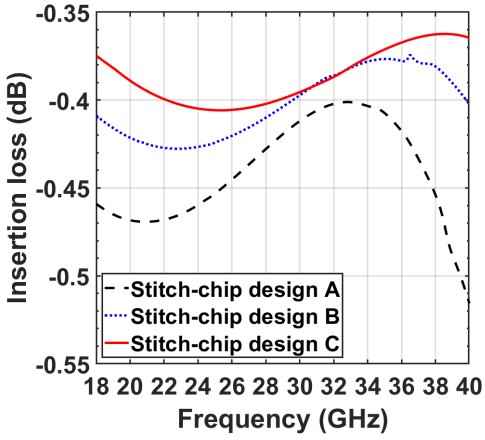
Figure 5.6: (a) One shielding via on each side of the package trace, (b) two shielding vias on each side of the package trace, (c) shielding via impact on Switch-LNA interconnect, and (d) shielding via impact on Switch-DA interconnect

5.2.2 Impact of stitch-chip design

When assembling stitch-chips on the package substrate, the unwanted capacitive coupling due to the package substrate will detune the stitch-chip performance, which may increase the module D2D interconnect losses. Therefore, the stitch-chip designs need to be optimized while accounting the complete D2D interconnects. As shown in Figure 5.7a, W_{200P}, W_{170P}, and W_{300P} are the width of the center signal conductors at the 200 μm pitch side, 170 μm pitch side, and 300 μm pitch side of the stitch-chips, respectively. Three stitch-chip designs are studied: (1) design A: W_{170P} = 160 μm, W_{200P} = 190 μm, W_{300P} = 290 μm; (2) design B: W_{170P} = 155 μm, W_{200P} = 185 μm, W_{300P} = 285 μm; (3) design C: W_{170P} =



(a)



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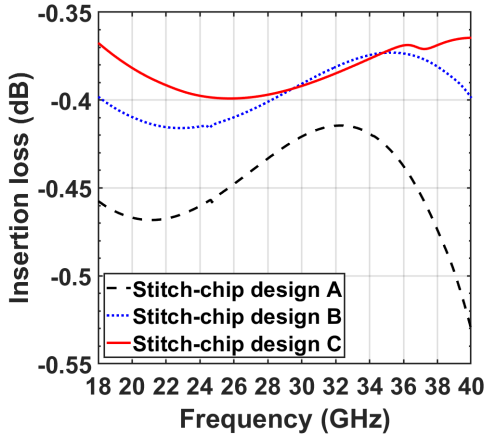

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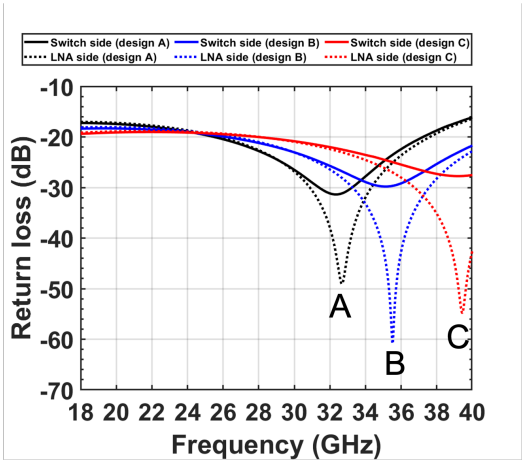
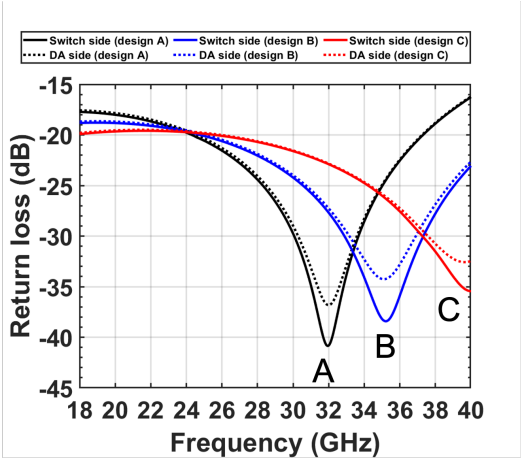
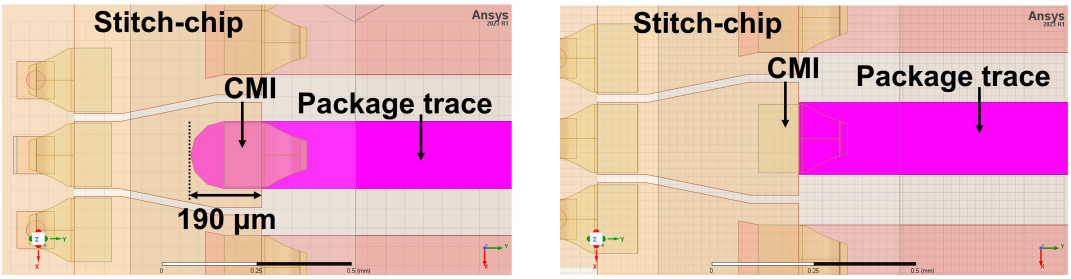


(d)



(e)

Figure 5.7: (a) Design parameters of the stitch-chip as part of the D2D interconnects, (b) Switch-LNA interconnect's insertion loss, (c) Switch-DA interconnect's insertion loss, (d) Switch-LNA interconnect's return loss, and (e) Switch-DA interconnect's return loss affected by stitch-chip design



(a) (b)

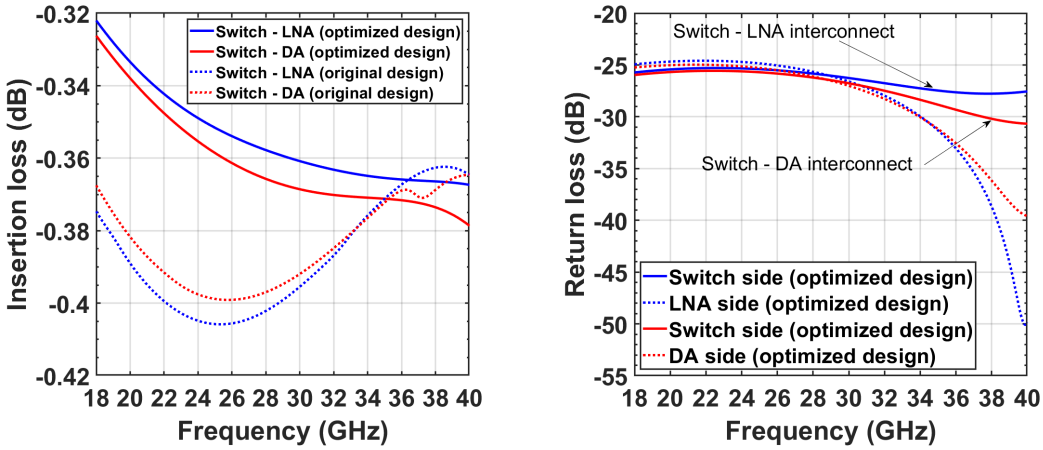
Figure 5.8: Stitch-chip to package trace transition: (a) original design with 190 μm stub underneath CMI and (b) optimized design without the stub underneath the CMI

150 μm, W_{200P} = 180 μm, W_{300P} = 280 μm.

Figure 5.7b and Figure 5.7c illustrate the insertion losses of the Switch-LNA D2D interconnect and the Switch-DA D2D interconnect with these three different stitch-chip designs. The lowest insertion loss is observed with stitch-chip design C for both module D2D interconnects (<0.41 dB loss is achieved). In addition, Figure 5.7d and Figure 5.7e show the stitch-chip design impact on the return losses of the two D2D interconnects. The D2D interconnects with stitch-chip design C are simulated to have >19 dB return losses. Stitch-chip design with a narrow center signal conductor (design C) can reduce the significant capacitive coupling between the stitch-chip and the package substrate, which improves the insertion losses and shifts the resonances of the return losses to higher frequencies than other designs.

5.2.3 Impact of transition between stitch-chip and package trace

The transition between the stitch-chip and the package substrate (specifically the package trace) is critical to minimize RF signal reflection through the module D2D interconnects. As shown in Figure 5.8a, a 190 μm stub on the original package trace is underneath the CMI of the stitch-chip to provide enough space for CMI mating with the package trace. However, the inductive stub may result in impedance-mismatch at the transition of the CMI to the package trace, which will increase the reflection loss. Therefore, an optimized



(a) (b)

Figure 5.9: (a) Impact of optimized stitch-chip to package transition on D2D interconnect insertion loss and (b) return losses of the D2D interconnect with optimized stitch-chip to package transition

transition design is proposed by cutting out the inductive stub, as shown in Figure 5.8b. The insertion losses of these two transition designs are plotted in Figure 5.9a: the optimized transition design results in a slight improvement in insertion loss (<0.38 dB within 18-40 GHz). Figure 5.9b illustrates the return losses at each die side when using the optimized transition design. The optimized transition design enables >24 dB return losses, while the original transition design only achieves >19 dB return losses, which is 5 dB worse than the optimized one.

5.2.4 Power supply interconnect design on stitch-chip

As shown in Figure 5.10a, the power supply pad on the DA die is close to the RF input pads, which requires a power supply interconnect to be integrated onto the stitch-chip. Figure 5.10b shows the Switch-DA D2D interconnect and its assembled stitch-chip with a power supply interconnect. The power supply interconnect is 0.7 mm long and 0.24 mm wide. The CMIs are located at the ends of the interconnect as off-chip I/Os to mate with the power pad of the DA die and power supply trace on the package substrate. The simulation results are depicted in Figure 5.10c. Within the DA bandwidth, the additional power supply

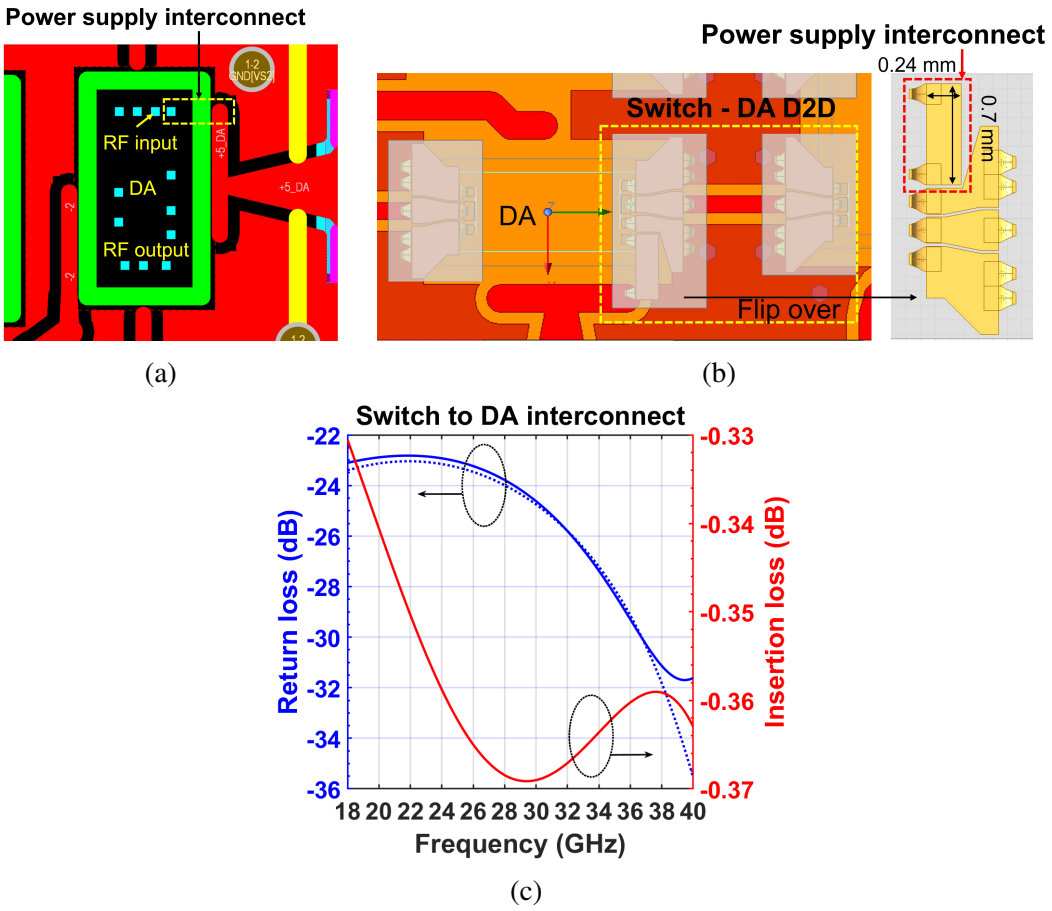


Figure 5.10: (a) Package layout around the DA die: the power supply pad is very close to the RF input pad, (b) stitch-chip design with additional power supply interconnect, and (c) Switch-DA D2D interconnect losses when using the stitch-chip design with additional power supply interconnect

interconnect has minimal impact on the whole D2D interconnect losses: the return loss is simulated to be better than 23 dB, which indicates 1 dB degradation from the stitch-chip design without the power supply interconnect; the insertion loss is less than 0.37 dB, which is similar to the design without the power supply interconnect.

5.3 Multi-Chip Module's Linear Gain Simulation with Active Dice

The simulated S-parameters of the whole multi-chip module with the optimized stitch-chips can be imported into Keysight ADS to perform simulations with the S-parameters of the active COTS dice, which are provided by vendors.

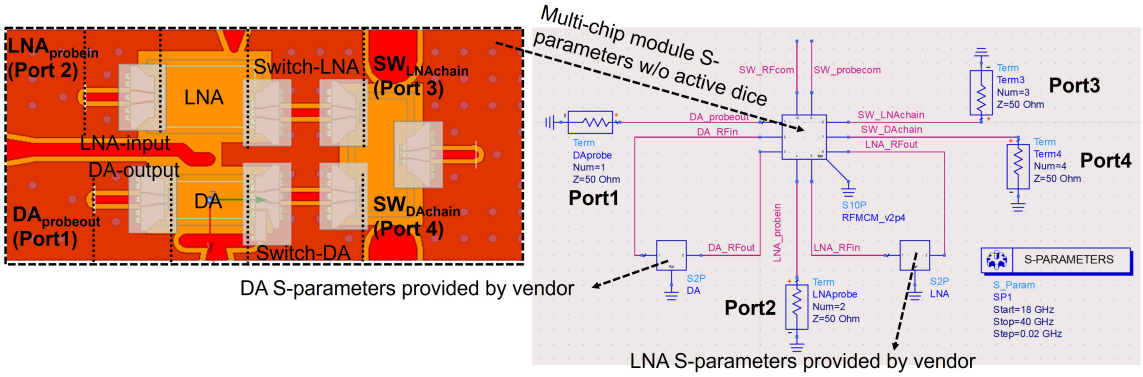


Figure 5.11: Simulation setup for packaged LNA/DA dice in the multi-chip module

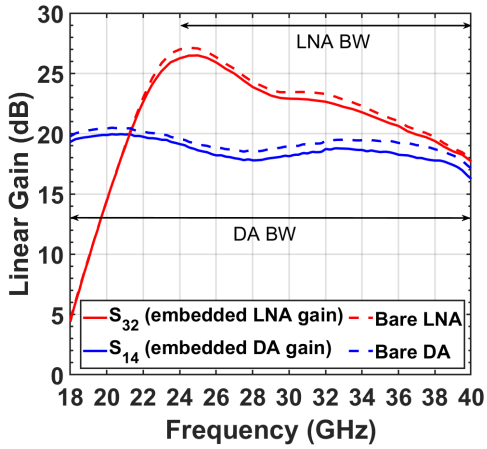


Figure 5.12: Linear gain degradation when 'embedded' LNA and DA dice into the cavities

5.3.1 Linear gain of LNA and DA dice embedded in the module

The performance of the LNA and the DA dice are simulated when they are embedded into this multi-chip module using the stitch-chips. As shown in Figure 5.11, simulated S-parameters of the module are imported into Keysight ADS and connected to the vendors' S-parameters of the LNA and DA dice accordingly. A four-port network is simulated within 18-40 GHz to cover the operating bandwidths of the LNA and DA; the ports' locations are marked in Figure 5.11. An LNA-switch RF chain between Port2 and Port3 includes LNA-input interconnect, LNA, and Switch-LNA D2D interconnect, while an DA-switch RF chain between Port1 and Port4 includes DA-output interconnect, DA, and Switch-DA D2D interconnect.

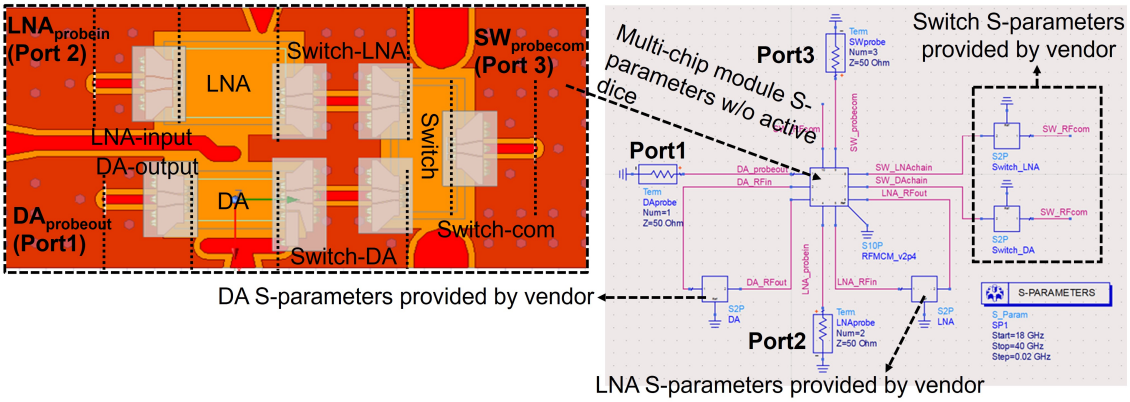


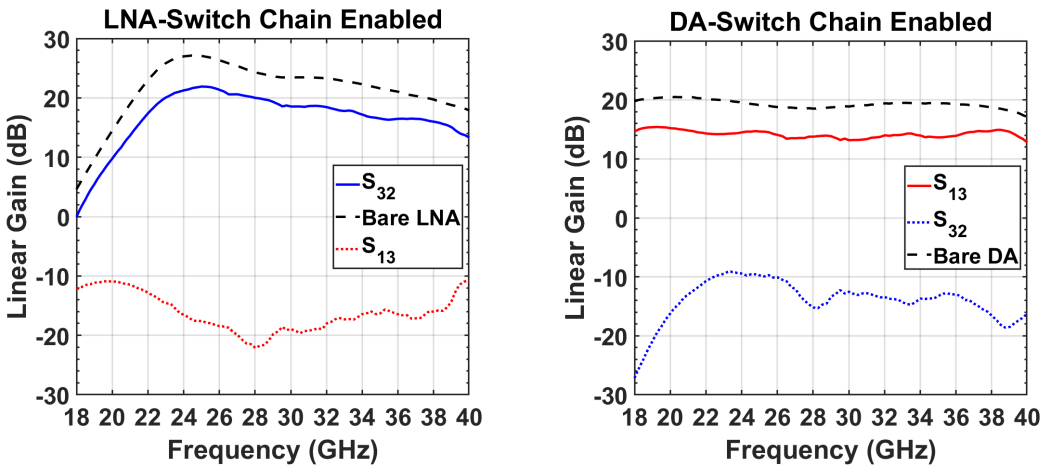
Figure 5.13: Simulation setup for the complete multi-chip module including LNA, DA, and switch

The simulated linear gains are depicted in Figure 5.12. S_{32} represents the gain between Port3 and Port2 (LNA-switch RF chain) and S_{14} represents the gain between Port1 and Port4 (DA-switch RF chain). The S-parameters of the bare dice are also plotted in the figure for reference. When embedding dice into the module using stitch-chips, the linear gain degradations are less than 0.73 dB for the LNA and less than 0.98 dB for the DA, which implies the negligible losses of the module interconnects using the fused-silica stitch-chips.

5.3.2 Linear gain of whole multi-chip module

The switch die's S-parameters from the vendor are then imported into Keysight ADS to simulate the whole multi-chip module, as shown in Figure 5.13. The whole module is a three-port network and port locations are marked in Figure 5.13. The LNA-switch RF chain between Port2 and Port3 consists of LNA-input interconnect, LNA, Switch-LNA D2D interconnect, switch, and Switch-com interconnect. The DA-switch RF chain between Port1 and Port3 consists of DA-output interconnect, DA, Switch-DA D2D interconnect, switch, and Switch-com interconnect.

Figure 5.14 shows the simulation results when the multi-chip module works into two scenarios: (1) the switch is biased to enable the LNA-switch chain while disabling the other; (2) the switch is biased to enable the DA-switch chain while disabling the other. As



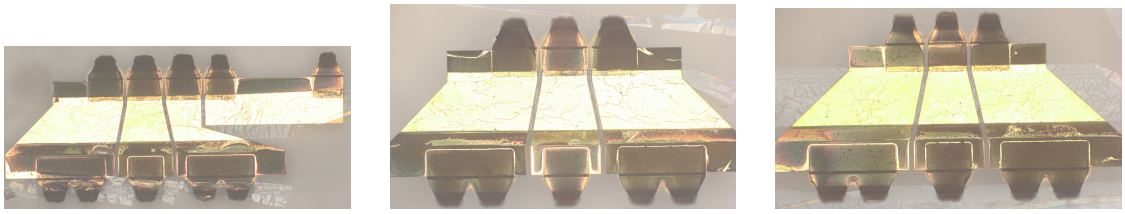
(a) (b)

Figure 5.14: Linear gain degradation of the whole multi-chip module using fused-silica stitch-chip technology: (a) when enabling LNA-switch RF chain and disabling DA-switch RF chain and (b) when enabling DA-switch RF chain and disabling LNA-switch RF chain

shown in Figure 5.14a, when enabling the LNA-switch chain, the linear gain degradation (S_{32} vs. bare LNA) is less than 5 dB, while the DA-switch chain, which is switched off, has a high-loss of >10.5 dB. A similar linear gain degradation (S_{13} vs. bare DA) is also observed (<5 dB) when enabling DA-switch chain and disabling the other, as shown in Figure 5.14b. Note that when including the switch die in this simulation, there is a significant increase in the linear gain degradation, which is attributed to the loss of the switch die device itself. For example, the poor switch die's RF signal isolation may lead to unwanted coupling between the two chains, which may cause impedance mismatching and degrade the linear gain further.

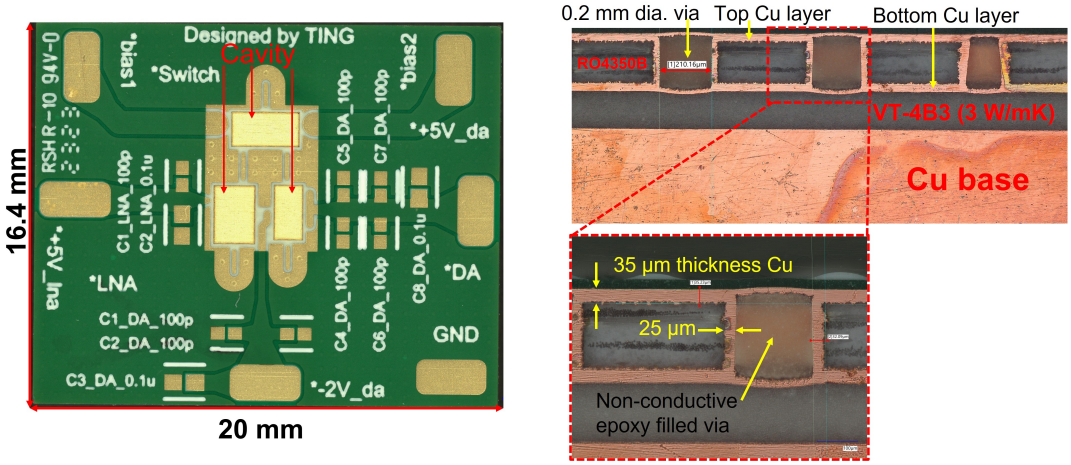
5.4 Stitch-Chip Fabrication and Multi-Chip Module Assembly

The stitch-chip fabrication is shown in Chapter 3. The 170 μm-to-300 μm stitch-chip and 200 μm-to-300 μm stitch-chip are diced into 1.5 mm $\times$ 1 mm chiplets. The 200 μm-to-300 μm stitch-chip with power supply interconnect is diced into 1.8 mm $\times$ 1 mm chiplets. The top views of these three types of stitch-chips are shown in Figure 5.15.



(a) (b) (c)

Figure 5.15: Top view of fabricated stitch-chips for the multi-chip module: (a) 200 μm-to-300 μm stitch-chip with power supply interconnect, (b) 200 μm-to-300 μm stitch-chip, and (c) 170 μm-to-300 μm stitch-chip



(a) (b)

Figure 5.16: Multi-chip module substrate: (a) top view and (b) stack up

5.4.1 Multi-chip module assembly

Figure 5.16 shows a top view and a cross-sectional view of the designed multi-chip module package substrate. The board is 20 mm in length and 16.4 mm in width. The three cavities are milled out in the middle of the board. As shown in Figure 5.16b, a 168 μm thick RO4350B laminate with top and bottom copper layers (35 μm thickness) is set on a copper base using thermal conductive adhesives (VT-4B3) for efficient heat spreading. The top copper layer is used to route RF signal, power, and ground, while the bottom copper layer is used as a ground plane, which is connected to the top ground through 0.2 mm epoxy-filled via; the side wall plating thickness of the via is 25 μm.

As shown in Figure 5.17, the depth of the three cavities is approximately 200 μm, as

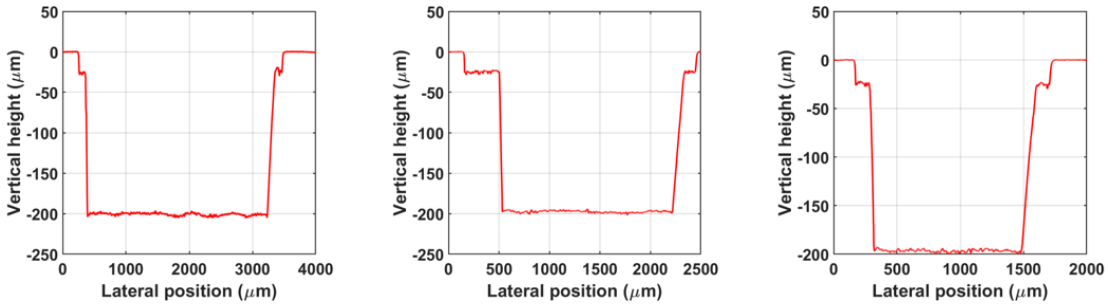


Figure 5.17: Cavity profile scan: (a) switch cavity profile, (b) LNA cavity profile, and (c) DA cavity profile

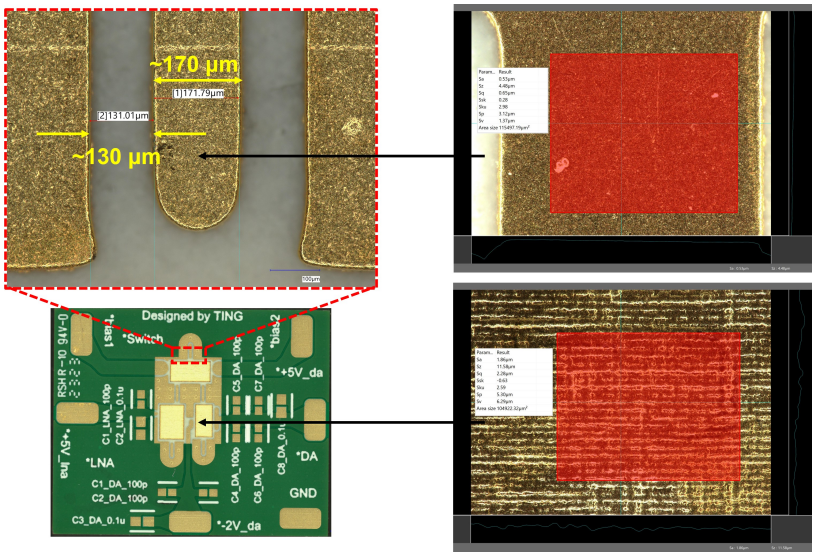


Figure 5.18: Trace dimensions and surface roughness

designed. Figure 5.18 shows that the width of the package substrate's RF trace and its spacing from the ground trace are approximately 170 μm and 130 μm, respectively. The areal surface roughness for the RF trace is 0.65 μm while the copper plane that is exposed at the bottom of the cavities has a 2.28 μm areal surface roughness.

Ten bypass capacitors are mounted on the substrate using solder reflow and six copper wires are soldered on the substrate for power supply connections. Next, conductive epoxy films are attached inside the cavities. The LNA, DA, and switch dice are aligned and mounted on the conductive epoxy films using a Finetech FINEPLACER lambda flip-chip bonder. Note that the epoxy films have 100 μm thickness and the die thicknesses are 100

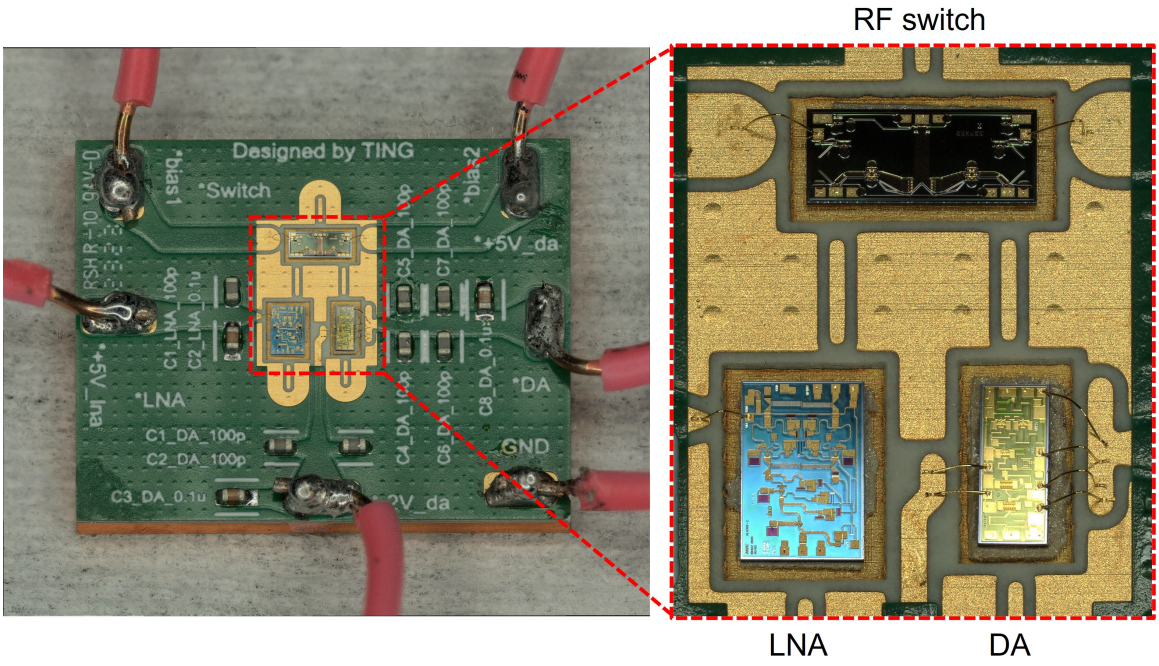


Figure 5.19: Assembled multi-chip module before stitch-chips assembly

μm as well, which leads to a total height of 200 μm that is equal to the depth of the cavity (i.e., the top surfaces of the dice are coplanar with the top surface of the package substrate). The bonder applies 3.5 N to the dice, and the substrate is heated to 125 °C for 30 minutes to fully cure the epoxy film. Note that the curing temperature is reduced from the previous 175 °C to 125 °C because of VT-4B3's lower glass transition temperature (130 °C). Next, nine wire-bonds are added to connect the power pads of the dice to the substrate's power interconnects. Note that one wire-bond on the DA die for bare die testing will be taken off eventually and its power connection will be provided by the 200 μm-to-300 μm stitch-chip. The assembled multi-chip module without stitch-chips is shown in Figure 5.19.

5.5 Stitch-Chip Assembly and RF Characterization

To measure this multi-chip module, the stitch-chips are assembled one by one on each die. The bare die testing for LNA and DA is done using two Cascade Microtech G-S-G $|Z|$ 200 μm pitch probes to directly probe on the die's RF pads when the die is embedded inside the

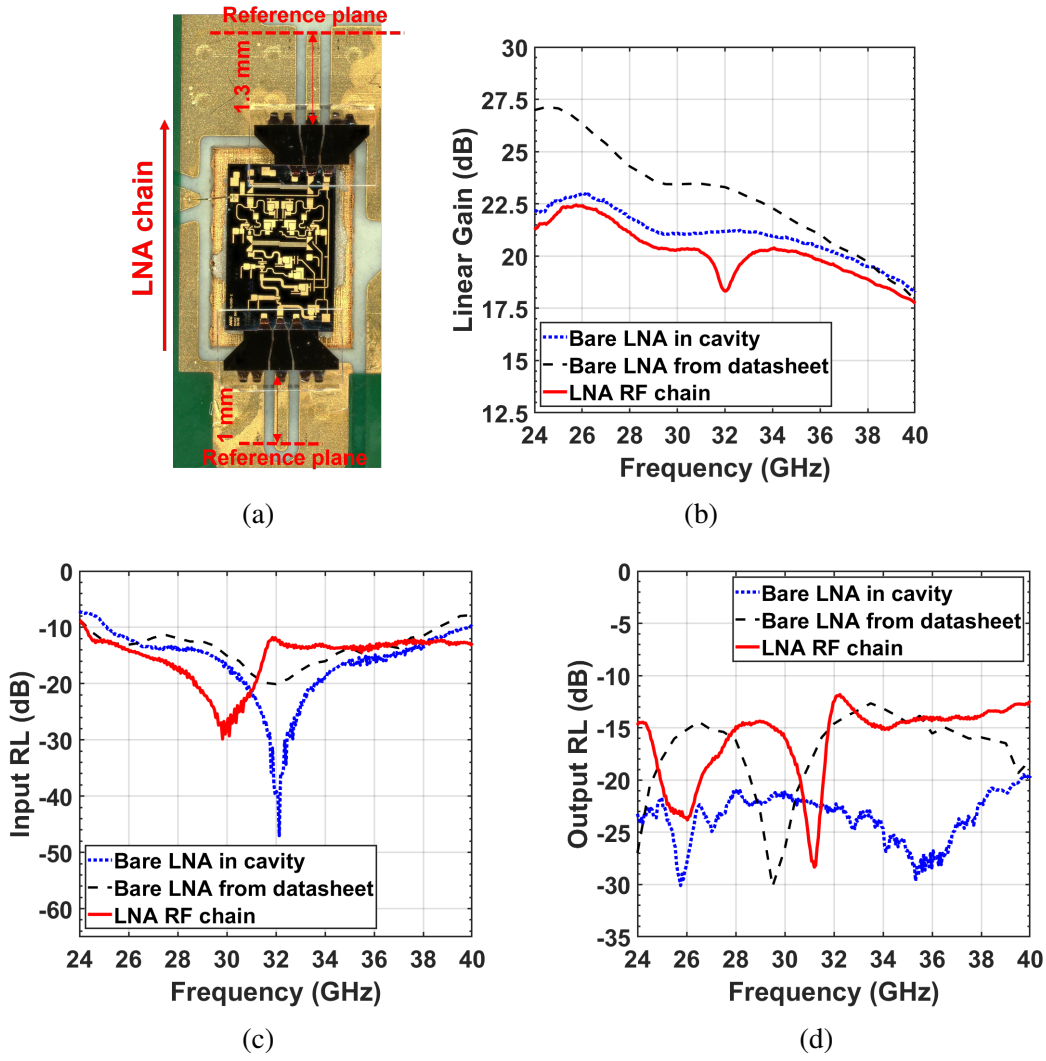


Figure 5.20: LNA RF chain measurement (without switch die): (a) top view, (b) linear gain, (c) input return loss, and (d) output return loss

cavity. The on-package testing is accomplished using two Cascade Microtech G-S-G $|Z|$ 300 μm pitch probes to probe the package substrate after the stitch-chips are bonded onto the package. Keysight N5245B PNA-X is used for the RF measurements from 18 GHz to 40 GHz. SOLT calibration is used to move the reference planes to the probes' tips. Three DC supplies with a shared common ground are utilized for powering the three dice.

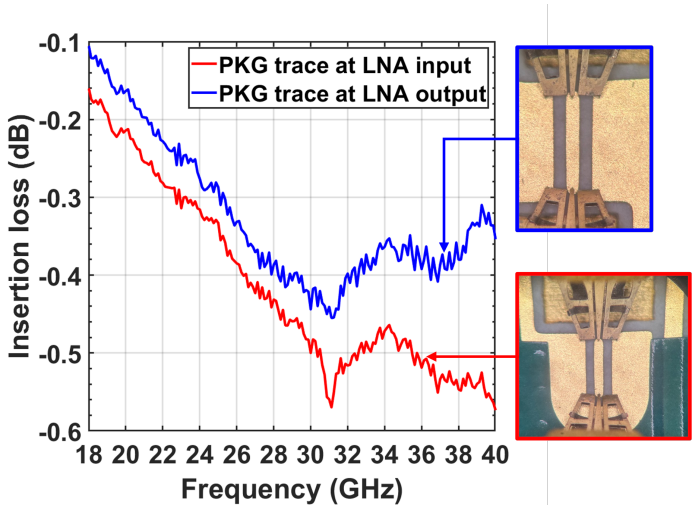


Figure 5.21: The insertion losses of package RF traces in module

5.5.1 LNA RF chain measurement

Two 200 μm-to-300 μm stitch-chips are flip-chip bonded on the LNA die's RF input/output pads, as shown in Figure 5.20a. The measurement reference planes are also marked in Figure 5.20a. The LNA RF chain includes a 1.3 mm long package trace, two 200 μm-to-300 μm stitch-chips, the LNA die, and a 1 mm long package trace. Figure 5.20b shows the linear gain of this LNA chain with bare LNA die performance as a reference. Note that the measurement of the bare LNA die in the cavity is different from the datasheet, which results from the lower drain biasing voltage used in measurements due to the long power supply trace on the package. The LNA RF chain has a similar linear gain performance, compared to the measurement of the bare LNA die embedded in the cavity except for 32 GHz. The dip at 32 GHz may result from package trace resonance caused by the variation of probe location. This implies that the total interconnect loss (package traces and two stitch-chips) is approximately 1 dB within the LNA bandwidth. Furthermore, the insertion losses of the package traces are shown in Figure 5.21, which is the major contributor to the total interconnect loss. Figure 5.20c and Figure 5.20d illustrate the input return loss and output return loss of the LNA chain, whose performance is not degraded by the stitch-chips and is close to the datasheet. The return losses are better than -10 dB within the LNA

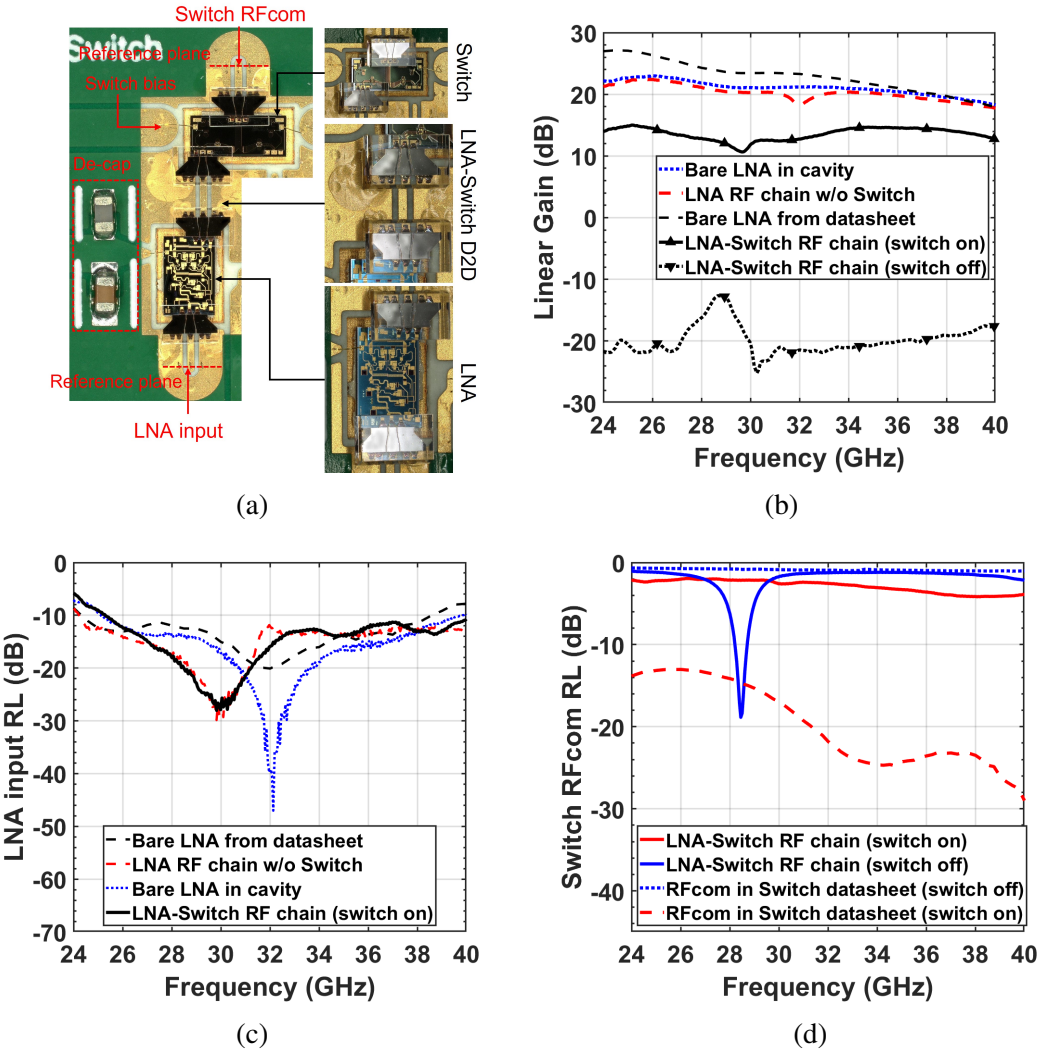


Figure 5.22: Full LNA-Switch RF chain measurement: (a) top view, (b) linear gain, (c) input return loss, and (d) output return loss

bandwidth. Compared with the datasheet, the resonance frequencies in the return losses shift because of the package parasitics change due to the stitch-chips assembly. To this end, the stitch-chips and package show minimal impact on return losses as well as linear gain in this multi-chip module.

5.5.2 LNA-Switch RF chain measurement

Another two 170 μm-to-300 μm stitch-chips are flip-chip bonded on the switch die's RF-com and RF1 pads to build the full LNA-Switch RF chain, as shown in Figure 5.22a. The

reference planes of the measurement are marked at the LNA input side and switch RFcom side in the figure. The full chain measurement includes two 1 mm long package traces, four stitch-chips, LNA-Switch D2D interconnects, LNA die, and switch die. As shown in Figure 5.22c, adding the switch die and its stitch-chips does not change the LNA input return loss. However, it degrades the output return loss to around 2-4 dB at switch die's RFcom side, compared with the bare switch die's return loss from the datasheet, as shown in Figure 5.22d. Such degradation may result from the high capacitive coupling between the stitch-chip and switch-die at RFcom side due to the large overlap area. The output return loss degradation leads to a linear gain reduction when comparing the measurements of LNA RF chain without switch and full LNA-Switch RF chain in Figure 5.22b. In addition, the switch die is able to control the chain. When turning it off, the chain shows larger than 10 dB loss across the LNA bandwidth, as shown in Figure 5.22b.

5.5.3 Preliminary measurement of DA

As shown in Figure 5.23, two preliminary measurements are performed for the DA chain: bare die measurement when the DA die is embedded in the cavity and measurement when the RF pads of the DA die are wire-bonded to the package traces. The reference planes are marked in the figures. For the bare die measurement, the RF pads of the DA die are directly probed, as shown in Figure 5.23a, while the other measurement includes a 1 mm long package trace, a 1.3 mm long package trace, two 1 mm long wire-bonds, and the DA die, as shown in Figure 5.23b.

As shown in Figure 5.23c, the bare DA die in the cavity shows roll-off linear gain beyond approximately 36 GHz when compared with the datasheet, which may result from the actual cavity milling larger than the design. Specifically, as discussed in Chapter 4, a bigger cavity leads to linear gain roll-off at high frequencies, as shown in Figure 4.6b. The actual clearance between the die edge and cavity edge is around 0.2 mm, while the designed clearance is 0.15 mm. As expected, wire-bonds at DA die's input and output degrade return

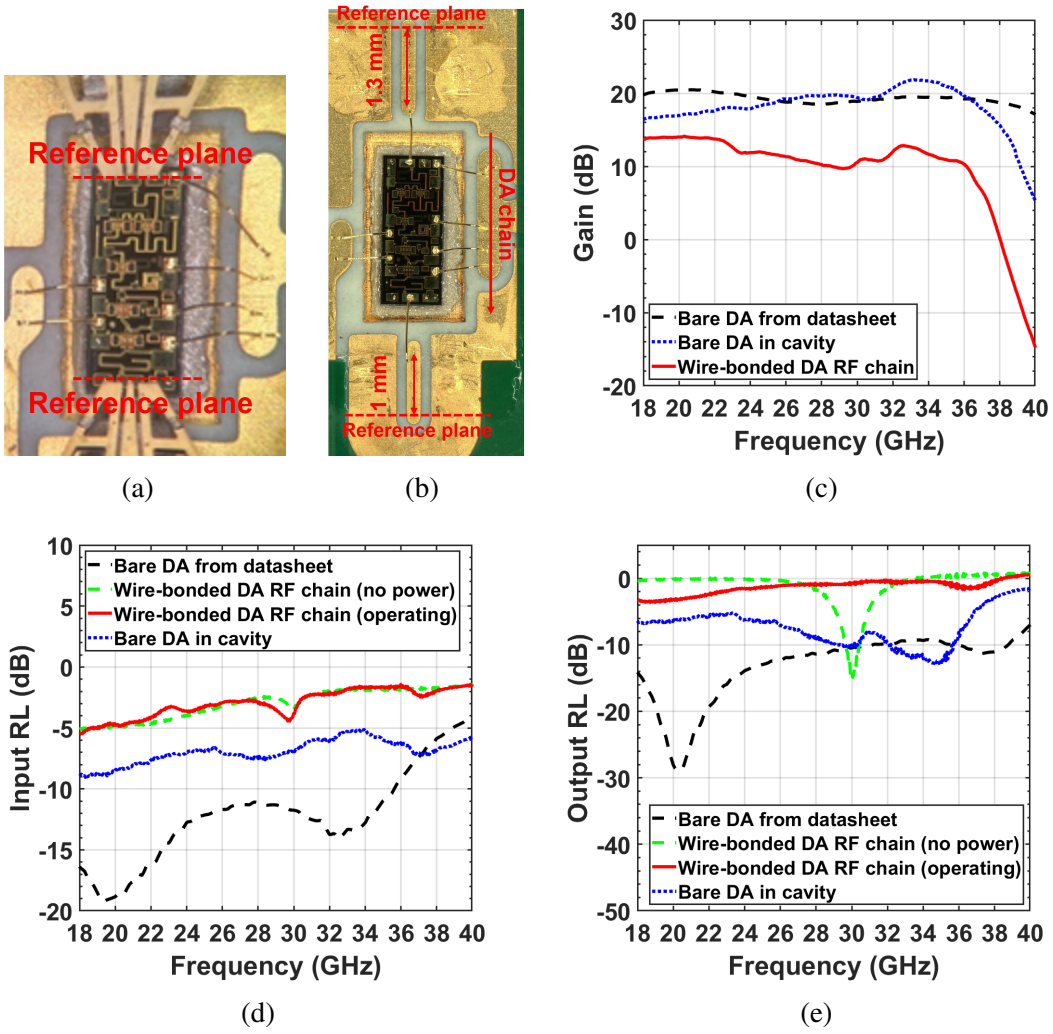


Figure 5.23: Preliminary measurements for the DA die: (a) top view of the bare DA die in cavity, (b) top view of wire-bonded DA die in the cavity, (c) linear gain measurement, (d) input return loss measurement, and (e) output return loss measurement

losses significantly, as shown in Figure 5.23d and Figure 5.23e, which results in an even larger linear gain reduction. In addition, the ground vias nearby the cavity may be too far from the embedded DA die's ground pad (∼0.86 mm), which results in large ground inductance and degrades impedance matching, linear gain, and bandwidth.

5.6 Conclusion

In this chapter, the stitch-chip technology is further developed for multi-chip modules. D2D interconnect and its stitch-chip design are investigated along with stitch-chip to package transition study and preliminary exploration of power supply interconnect integration on the stitch-chip. The module is assembled (including stitch-chips) and RF measurements are performed for the LNA and switch RF chain and the DA die.

The total LNA RF chain using stitch-chips is measured to have less than 1 dB package loss within the LNA bandwidth (24-40 GHz) except a resonance dip at 32 GHz, which may be due to the resonance of the RF traces on the package substrate. The return losses are better than -10 dB, which are not degraded from the bare die performance. The resonances in the return losses shift because of the parasitics change from the stitch-chips assembly.

A fully functional LNA-switch RF chain using stitch-chips is demonstrated for the first time. The switch die is able to control the chain and a fair gain reduction is observed due to the potential impedance mismatching at the switch die's RFcom (input/output). Such impedance matching may be due to the large capacitive coupling between the stitch-chip and the switch die, which causes a return loss degradation at the switch die's RFcom (input/output).

A preliminary measurement is performed for the DA die as well. The DA die's linear gain rolls off beyond 36 GHz when embedding the DA die inside the cavity. Such phenomenon may result from two reasons: (1) the actual cavity size is larger than the design, which may cause higher gain reduction at high frequencies, as shown in Chapter 4; (2) the ground vias nearby the cavity may be too far from the embedded DA die, which may cause large ground inductance and degrade impedance matching, linear gain, and bandwidth.

CHAPTER 6

INVESTIGATION OF OTHER OFF-CHIP I/O IN POLYLITHIC INTEGRATION

Alternative off-chip I/Os (e.g. solder bump, micro-bump [87], and hybrid-bond [88], [89], [90], [91]) may be able to replace the CMIs in the stitch-chip technology for RF/mm-wave systems only when their RF performance are well-studied, which can be evaluated by frequency-dependent parasitics. However, conventional parasitics models [77], [92] are frequency-independent and there are only a few articles reporting the frequency-dependent parasitics of off-chip I/Os. In addition, RF/mm-wave applications beyond 5G require much higher signal routing density, which is currently limited by the pitch of the off-chip I/Os: for example, while 0.4/0.4 μm fine-pitch line/spacing (L/S) of lateral interconnects can already be achieved [11], off-chip I/Os' pitch scaling is behind and is in the range of 50 μm to 2 μm [93], [94], [95], [96]. To this end, it is necessary to fully study the pitch scaling impact on frequency-dependent parasitics of off-chip I/O technologies.

RF/mm-wave simulations are utilized in this chapter to extract the frequency-dependent parasitics and perform off-chip I/O technology benchmarking. The impact of underfill, substrate, pitch scaling, and ground-signal configurations on the parasitics are also investigated in this chapter.

6.1 Parasitics Extraction of Off-Chip I/O

One of the mainstream off-chip I/O technologies is micro-bump technology using solder-capped Cu pillar [87], whose ANSYS HFSS model is shown in Figure 6.1. The model consists of two off-chip I/Os in the ground-signal (G-S) configuration. In Figure 6.1, the signal (S) I/O is terminated by 50 Ω impedance and excited by wave ports. The Perfect Magnetic Conductor (PMC) is set as a boundary condition for lateral surfaces.

In Figure 6.1, dia, p, h_{solder} and h_{CuP} are I/O diameter, I/O pitch, solder's height, and

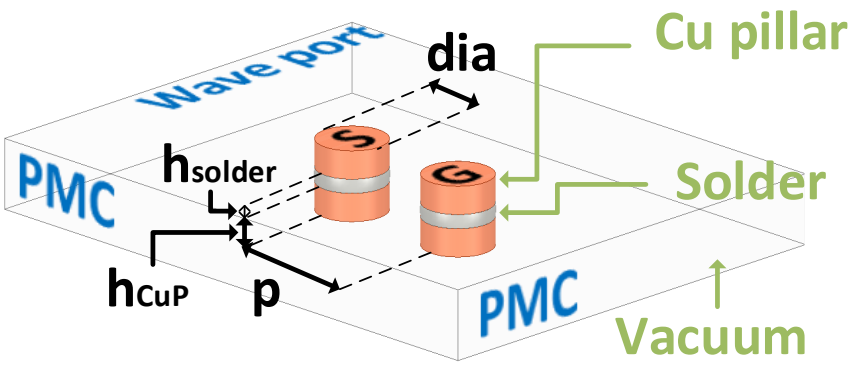


Figure 6.1: HFSS model of a typical off-chip I/O in ground-signal configuration

Table 6.1: Dimensions of the off-chip I/Os in Figure 6.1.

p	dia	h_{solder}	h_{CuP}
50 μm	25 μm	5 μm	10 μm

Table 6.2: Material properties used in the model of Figure 6.1.

Material	ε_r	μ_r	$tan\delta$	σ
Vacuum/air	1	1	0	0
Underfill	3.74 @ 1 kHz	1	0.011 @ 1 kHz	5 pS/m @ DC
Copper	1	0.999991	0	5.8E7 S/m
Solder	1	1	0	7E6 S/m

pillar's height, respectively. The initial values of these design parameters are set based on the open literature [87], [97] and summarized in Table 6.1. Table 6.2 shows relative permittivity (ε_r), relative permeability (μ_r), loss tangent ($tan\delta$), and conductivity (σ) of materials used in the model. The frequency-dependent material properties of a capillary flow underfill for flip-chip are also summarized in Table 6.2.

6.1.1 Numerical calculation

The parasitic resistance (R_{tot}) of the I/O in Figure 6.1 involves DC resistance (R_{DC}) and AC resistance (R_{AC}) as follows:

$$R_{tot} = \sqrt{R_{DC}^2 + R_{AC}^2} \tag{6.1}$$

where R_{DC} is a loop DC resistance of both signal and ground I/Os. Each has two pillars' resistances ($2 \times R_{pillar}^{DC}$) and the middle solder's resistance (R_{solder}^{DC}):

$$R_{DC} = 2 \times (2 \times R_{pillar}^{DC} + R_{solder}^{DC}) \tag{6.2}$$

The DC resistance calculation is elaborated in Appendix A.

When the frequency is much higher than the skin-effect onset frequency (ω_δ) [98] (i.e., skin depth is well-established), the R_{AC} can be calculated as follows:

$$R_{AC} = 2 \times R_{pillar}^{AC} + R_{solder}^{AC} \tag{6.3}$$

The AC resistance calculation is elaborated in Appendix A.

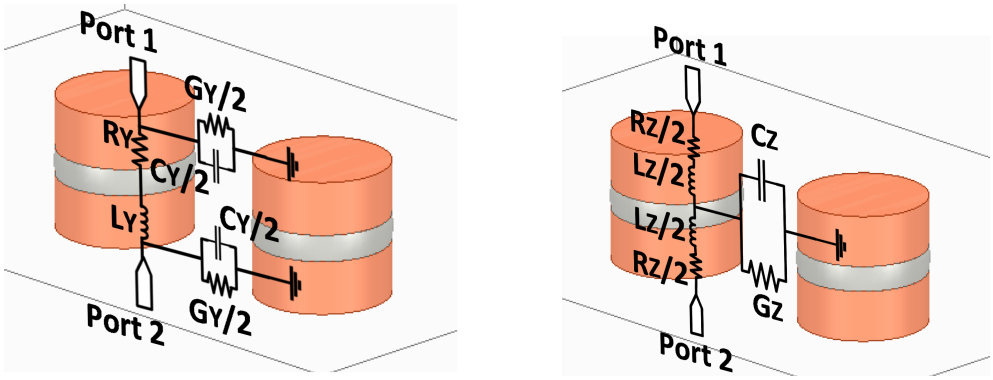
The parasitic inductance (L_{tot}) can be derived from two-wire transmission line formula [99] and high-frequency internal impedance [100] with R_{AC}:

$$L_{tot} = \frac{\mu_0(2h_{CuP} + h_{solder})}{\pi} \cosh^{-1}(p/dia) + \frac{R_{AC}}{2\pi f} \tag{6.4}$$

where μ_0 is the vacuum permeability and f is the frequency. In addition, partial inductance concept (i.e., L_{tot} is calculated by self-inductance L_s and mutual-inductance L_m) could be used [100], [101]:

$$L_{tot} = 2(L_s - L_m) + \frac{R_{AC}}{2\pi f} \tag{6.5}$$

The calculation using the partial inductance concept is introduced in Appendix A.



(a) (b)

Figure 6.2: Lumped parasitics models for off-chip I/O: (a) Π-model and (b) T-model

Because of the high conductivity of copper and solder, the parasitic conductance (G_{tot}) and parasitic capacitance (C_{tot}) can be calculated as follows [99]:

$$G_{tot} = \frac{\sigma_m}{\varepsilon_m} C_{tot} \tag{6.6}$$

$$C_{tot} = (2h_{CuP} + h_{solder}) \frac{\mu_0 \varepsilon_m}{L_{tot}/(2h_{CuP} + h_{solder})} \tag{6.7}$$

where σ_m and ε_m are the conductivity and the permittivity of the medium surrounding the I/Os, respectively. At high frequencies, L_{tot} becomes frequency-independent and the equations become:

$$G_{tot} = (2h_{CuP} + h_{solder}) \frac{\pi \sigma_m}{\cosh^{-1}(p/dia)} \tag{6.8}$$

$$C_{tot} = (2h_{CuP} + h_{solder}) \frac{\pi \varepsilon_m}{\cosh^{-1}(p/dia)} \tag{6.9}$$

6.1.2 Simulation-based parasitics extraction

The simulated S-parameters from the model in Figure 6.1 are used with lumped circuit models (Π- or T-model) [67] shown in Figure 6.2 to extract the parasitics of the off-chip I/O. Adaptive meshing at 100 GHz and a discrete frequency sweep from 200 MHz to 100

GHz are performed. The simulated S-parameters are firstly converted to Y/Z-parameters:

$$[\mathbf{Y}] = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{6.10}$$

$$[\mathbf{Z}] = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \tag{6.11}$$

Next, Y-parameters (corresponding to Π-model, as shown in Figure 6.2a) are used for the extraction as follows [67]:

$$R_Y = \mathrm{Re}\left(\frac{-2}{Y_{12}+Y_{21}}\right) \tag{6.12}$$

$$L_Y = \frac{\mathrm{Im}\left(\frac{-2}{Y_{12}+Y_{21}}\right)}{2\pi f} \tag{6.13}$$

$$G_Y = \mathrm{Re}(Y_{11}+Y_{22}+(Y_{12}+Y_{21})) \tag{6.14}$$

$$C_Y = \frac{\mathrm{Im}(Y_{11}+Y_{22}+(Y_{12}+Y_{21}))}{2\pi f} \tag{6.15}$$

where f is the frequency. Similarly, Z-parameters (corresponding to T-model, as shown in Figure 6.2b) are used to extract the parasitics as follows [67]:

$$R_Z = \mathrm{Re}(Z_{11}+Z_{22}-(Z_{12}+Z_{21})) \tag{6.16}$$

$$L_Z = \frac{\mathrm{Im}(Z_{11}+Z_{22}-(Z_{12}+Z_{21}))}{2\pi f} \tag{6.17}$$

$$G_Z = \mathrm{Re}\left(\frac{2}{Z_{12}+Z_{21}}\right) \tag{6.18}$$

$$C_Z = \frac{\mathrm{Im}\left(\frac{2}{Z_{12}+Z_{21}}\right)}{2\pi f} \tag{6.19}$$

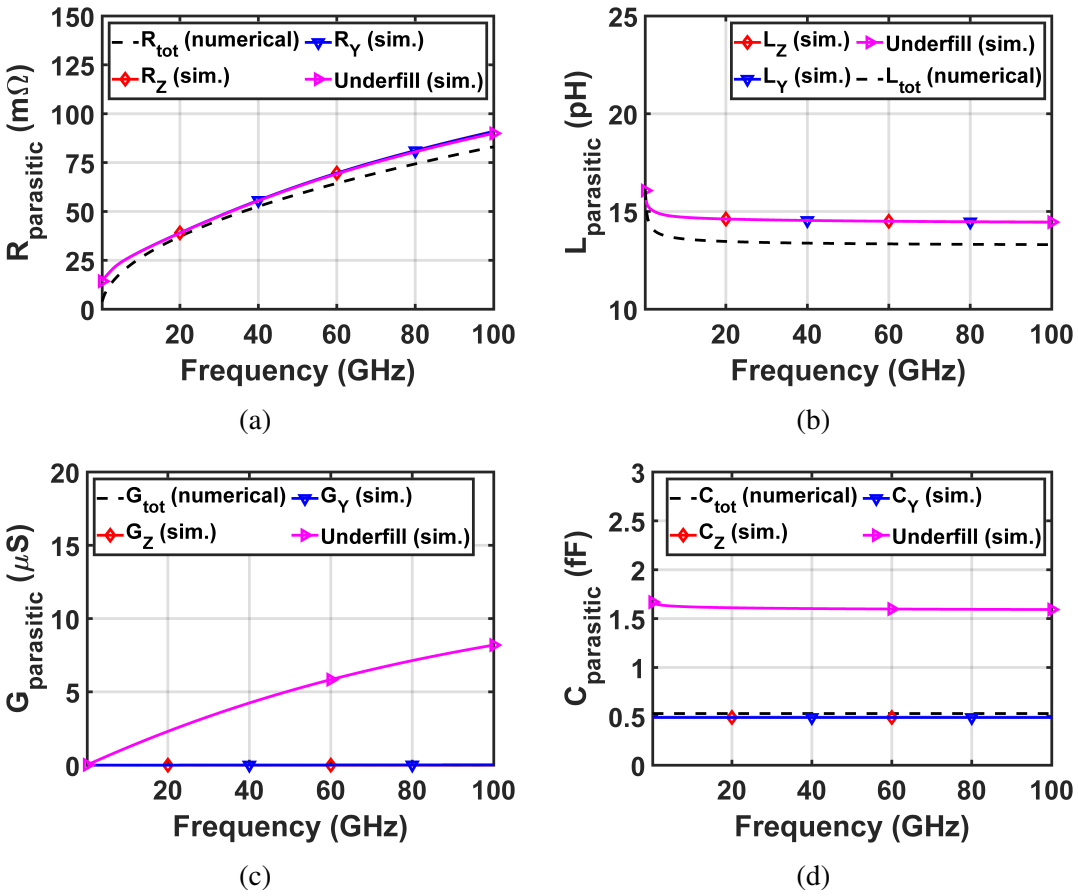


Figure 6.3: Extracted parasitics from numerical calculation and simulation for 50 μm pitch G-S off-chip I/O (micro-bump): (a) parasitic resistance, (b) parasitic inductance, (c) parasitic conductance, and (d) parasitic capacitance

6.2 Frequency-Dependent Underfill and Substrate Effects

6.2.1 Underfill effect

UnderFill (UF) is commonly utilized to fill around off-chip I/Os to improve their mechanical reliability (e.g., local stress reduction) [102]. However, the UF introduces more parasitics, and to study this effect, the vacuum/air in the model is replaced with the UF whose frequency-dependent material properties are modeled by the Djordjevic-Sarkar model [103]: the UF's material properties at 1 kHz in Table 6.2 are input in the Djordjevic-Sarkar model to obtain the material properties across the full bandwidth. The UF will have a larger impact

Table 6.3: Parasitics of 50 μm pitch G-S off-chip I/Os (micro-bumps) at selected frequencies.

	R (mΩ)	**L (pH)**	**G w/o UF (nS)**	**G w/ UF (μS)**	**C w/o UF (fF)**	**C w/ UF (fF)**
10 GHz	29.5	14.7	4.9	1.2	0.5	1.6
20 GHz	38.9	14.6	6.8	2.3	0.5	1.6
100 GHz	89.9	14.5	26.2	8.2	0.5	1.6

on the conductance and capacitance (due to its high conductivity and permittivity) than the resistance and inductance, which are mostly related to dimensions and conductors' material properties from Equation 6.1 to Equation 6.5.

Simulated parasitics (R_Z, L_Z, G_Z, C_Z, R_Y, L_Y, G_Y, and C_Y) and numerical calculated parasitics (R_{tot}, L_{tot}, G_{tot}, and C_{tot}) are extracted and depicted with one UF case (simulation only) in Figure 6.3. The simulated parasitics are $<$8% different from the numerical calculated parasitics (Equation 6.1 to Equation 6.9). In Table 6.3, the parasitics at 10 GHz, 20 GHz, and 100 GHz of the 50 μm pitch G-S I/Os' are shown. The resistance is directly proportional to the square root of the frequency because of the skin depth effect. According to Equation 6.4, the inductance decreases with the frequency and falls to a constant ($\sim$14.5 pH) when the second term in Equation 6.4 becomes negligible at high frequencies. There are increases in the conductance and capacitance due to the UF: (1) the conductance reaches $\sim$8.2 μS for UF case, while it is around zero ($\sim$nS) without underfill; (2) the capacitance increases to $\sim$1.6 fF because of UF's higher permittivity.

6.2.2 Substrate effect

As shown in Figure 6.4, 500 μm thick Si substrates (10 S/m conductivity) with 1 μm silicon dioxide are included in the model for updating the numerical calculation and simulation to investigate the substrate effect on off-chip I/O's parasitics. The frequency-dependent material properties are also generated by the Djordjevic-Sarkar model.

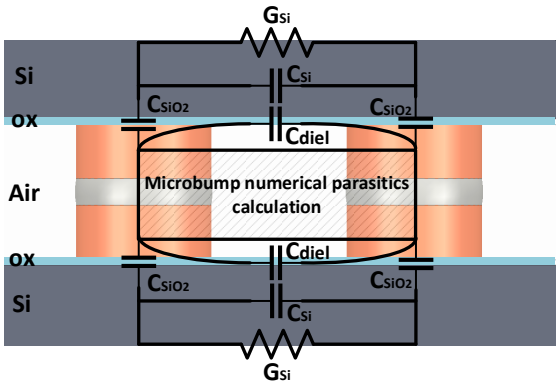


Figure 6.4: Updated numerical calculation model for off-chip I/O (micro-bump) with Si substrate (10 S/m conductivity)

The substrates introduce additional capacitances including fringe capacitance between pillars (C_{diel}), the capacitance of pillar-to-substrate (C_{SiO_2}), and substrate capacitance (C_{Si}) whose calculations are elaborated in Appendix B. Next, similar to [104], the capacitance and conductance with frequency-dependence due to the substrate effect can be calculated as follows:

$$C_{sub} = C_{diel} + \frac{\omega^2 C_{SiO_2} C_{Si}(C_{SiO_2} + 2C_{Si}) + 2C_{SiO_2} G_s^2}{4G_s^2 + \omega^2 (C_{SiO_2} + 2C_{Si})^2} \tag{6.20}$$

$$C_{total+sub} = C_{tot} + 2C_{sub} \tag{6.21}$$

$$G_{sub} = \frac{\omega^2 C_{SiO_2}^2 G_s}{4G_s^2 + \omega^2 (C_{SiO_2} + 2C_{Si})^2} \tag{6.22}$$

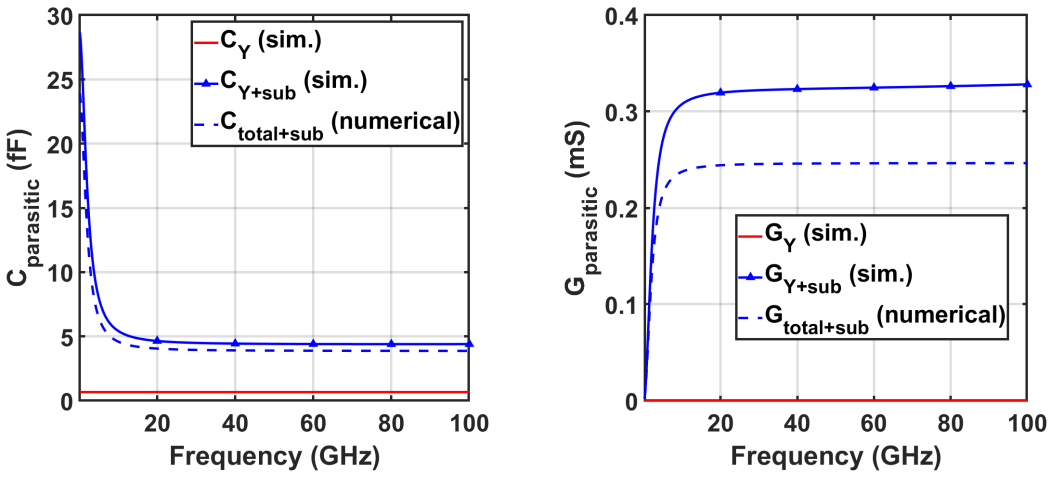
$$G_{total+sub} = G_{tot} + 2G_{sub} \tag{6.23}$$

where

$$G_s = dia \times \frac{\sigma_{Si}[1 + (1 + 10h_{Si}/dia)^{-0.5}]}{2F(h_{Si})} \tag{6.24}$$

where σ_{Si} is the conductivity of Si.

In Figure 6.5, a simulation-only case without substrate effect (i.e. G_Y and C_Y), the conductance with substrate effect, and capacitance with substrate effect (i.e. $G_{total+sub}$ and $C_{total+sub}$ from the numerical calculation with the modified model, G_{Y+sub} and C_{Y+sub}



(a) (b)

Figure 6.5: Parasitic capacitance and conductance for 50 μm pitch G-S off-chip I/O (micro-bump) with Si substrate: (a) capacitance and (b) conductance

from the S-parameters simulation method) are shown. As shown in Figure 6.5a, the capacitance increases by approximately 6.64 times at high frequencies because of the substrates. Simulation (C_{Y+sub}) and numerical calculation ($C_{total+sub}$) are correlated well (12.0% difference) and capture the phenomenon of interfacial polarization at the Si-silicon dioxide interface. At low frequencies (<10 GHz), most of the electric fields are confined in the thin silicon dioxide layer, which results in large capacitance; as frequency increases, the electric fields penetrate into the Si substrate, and the capacitance becomes the thin silicon dioxide capacitance in series with the substrate capacitance, which falls to a constant value. In Figure 6.5b, the conductance increases due to Si substrates' higher conductance, which implies that using high resistivity Si can decrease the conductance. Although there is a mismatch between simulation (G_{Y+sub}) and numerical calculation ($G_{total+sub}$), the two methods are able to capture the frequency-dependent trend of the conductance. The difference may result from the underestimation of the thin silicon dioxide capacitance (C_{SiO_2}) in Equation 6.22 (e.g., the fringe capacitances from pillar to Si substrate are ignored).

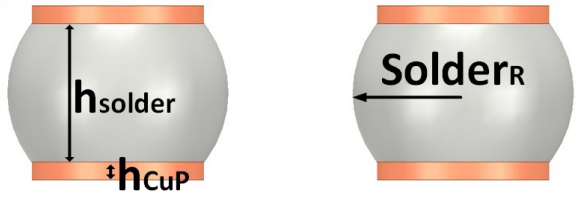


Figure 6.6: The cross-sectional view of solder bumps in HFSS

6.3 Impact of Off-Chip I/O Pitch Scaling

To study the impact of pitch scaling, two assumptions are used to set up the simulation: the diameter (dia) of the I/O pad or pillar is fixed as half of the pitch (p), and the total I/O height (i.e., $h_{CuP} \times 2 + h_{solder}$) is fixed, except for hybrid bonding, for I/O technologies benchmarking purpose.

6.3.1 Pitch scaling of solder bump

To derive a solder bump model, the model in Figure 6.1 is modified by increasing the solder amount with fixed total I/O height (i.e., $h_{CuP} \times 2 + h_{solder}$ is fixed) and changing solder geometry. Increasing the solder amount can be translated to increase a defined solder ratio r as follows:

$$r = \frac{h_{solder}}{h_{solder} + 2 \times h_{CuP}} \tag{6.25}$$

As solder geometry becomes a truncated sphere after reflow, as shown in Figure 6.6, the solder geometry is changed with a parameter named the solder sphere radius ($Solder_R$). The $Solder_R$ is calculated as follows [105]:

$$Solder_R = \frac{\sqrt{h_{solder}^4 + 4h_{solder}^2 (dia/2)^2}}{2h_{solder}} \tag{6.26}$$

For the pitch scaling study, the solder ratio r is assumed as 0.8, which leads bump height to fall in a reasonable range of around 20 μm [48].

According to Equation 6.26, bridging may happen between adjacent solder bumps and

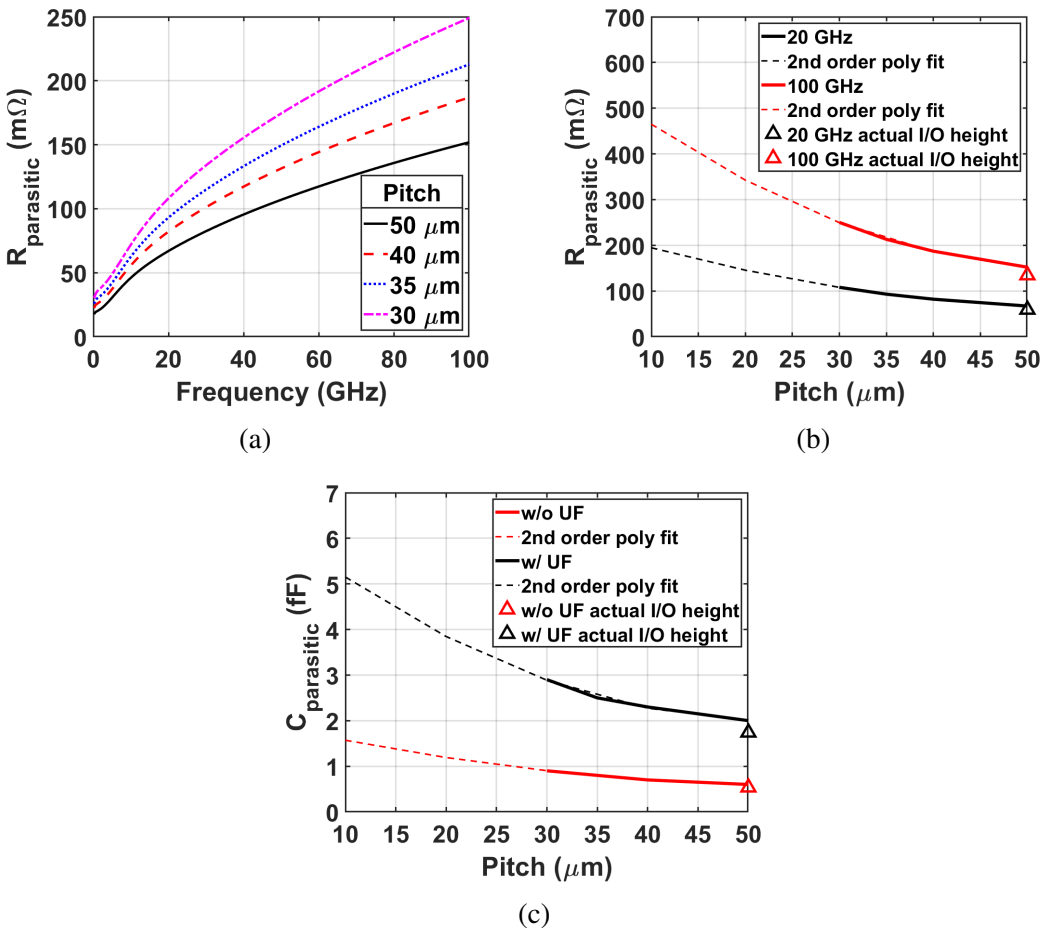


Figure 6.7: Impact of solder bump pitch scaling on (a) frequency-dependent resistance, (b) resistance at 20 GHz and 100 GHz with varied pitches, and (c) capacitance with varied pitches

electrically short them when pitch scales below approximately 23 μm. Hence, the pitch is only swept from 50 μm to 30 μm in the simulation, while a polynomial fit is utilized to predict the parasitics for 30 μm to 10 μm pitch assuming no bridging. Only Π- or T-model is used to extract the parasitics because the two models generate similar results. The resistance and capacitance are impacted significantly by the scaling. As shown in Figure 6.7a and Figure 6.7b, when pitch decreases from 50 μm to 30 μm, the resistance at 20 GHz increases 61.2% and is predicted as around 194.5 mΩ at 10 μm pitch. As shown in Figure 6.7c, the capacitance at 10 μm pitch is 1.5 fF without UF, which is $\sim$3X of 50 μm case, while UF increases the capacitance to 5.2 fF, which is $\sim$2.6X of 50 μm case. Note that

the substrate effect and the capacitive coupling between bumps and adjacent redistribution layers on substrates may also affect the capacitance. In Figure 6.7b and Figure 6.7c, data points using experimentally demonstrated 50 μm pitch solder bump's height and diameter from [48] are also shown as references. The model in this work shows similar resistance ($<$11.6% difference) and capacitance ($<$13.2%), compared to the references. The difference may result from conductor and dielectric material properties variance. Moreover, pitch scaling has a negligible impact on inductance and conductance. The inductance is around 10-12.4 pH, while the conductance at 20 GHz is around 0.5 nS without UF and 3-4.2 μS with UF.

6.3.2 Pitch scaling of micro-bump

There is a lower possibility of bridging when a less solder amount is used, which leads to micro-bump technology where solder-capped Cu pillars are used as fine-pitch off-chip I/Os. The pitch of the micro-bump in Figure 6.1 is swept from 50 μm to 10 μm for the simulation and the parasitics are extracted using Π- or T-model. The resistance and capacitance results are shown in Figure 6.8.

In Figure 6.8a and Figure 6.8b, the resistance at 20 GHz increases 1.67 times when pitch decreases from 50 μm to 30 μm. When the pitch continues scaling to 10 μm, the resistance increases to 192 mΩ, which is 3.1 times higher than 30 μm pitch. Such phenomenon implies that pitch scaling has a more significant impact on the finer pitch micro-bump, especially for 10-20 μm pitch as shown in Figure 6.8b. However, as shown in Figure 6.8c, the pitch scaling has a limited impact on capacitance. Note that the substrate effect and the capacitive coupling between bumps and adjacent redistribution layers on the substrate may still impact the capacitance. In Figure 6.8b and Figure 6.8c, data points using experimentally demonstrated 20 μm pitch micro-bump's height and diameter from [106] are also shown as references. The 20 μm pitch micro-bump has a lower height ($\sim$13 μm), which results in lower resistance and capacitance than the model in this work. Moreover, pitch

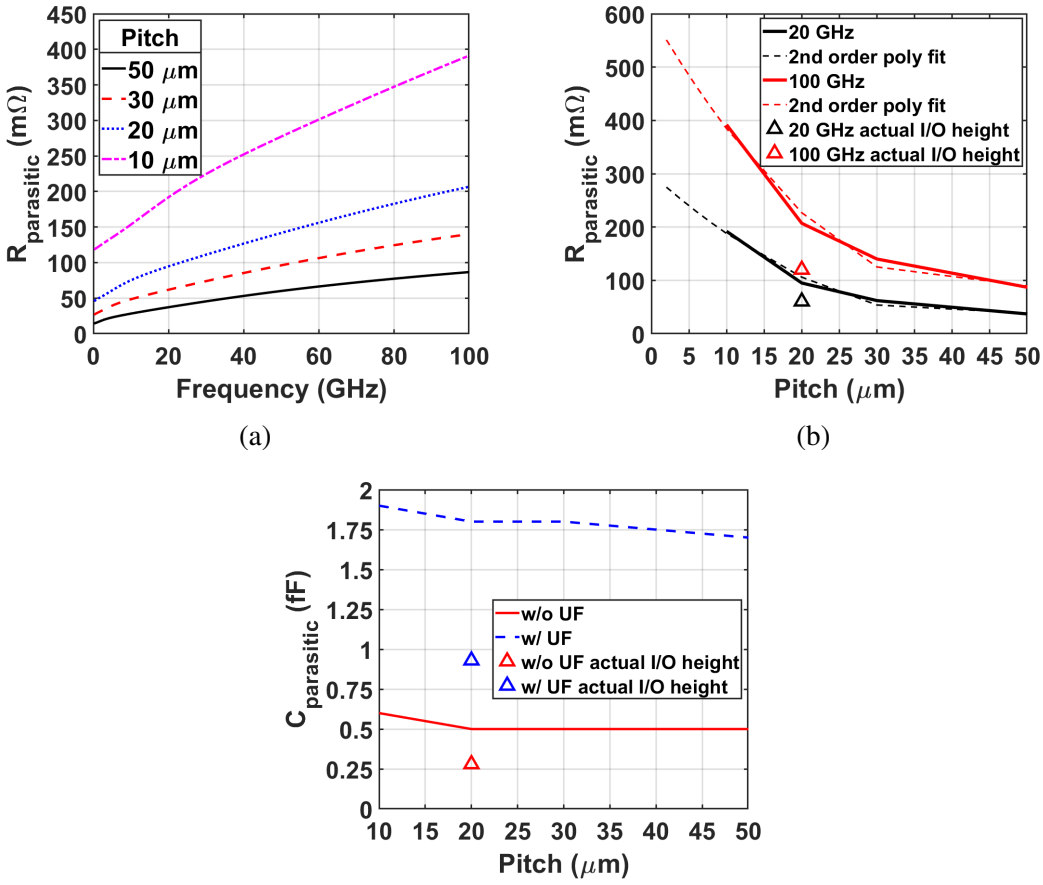


Figure 6.8: Impact of micro-bump pitch scaling on (a) frequency-dependent resistance, (b) resistance at 20 GHz and 100 GHz, and (c) capacitance

scaling has a negligible impact on inductance and conductance. The micro-bump inductance is around 13-13.7 pH and the conductance at 20 GHz is around 0.3 nS without UF and 2.5-2.8 μS with UF.

6.3.3 Pitch scaling of hybrid-bond

Pitch scaling beyond 10 μm pitch may bring about issues of potential solder extrusion and bridging between adjacent I/Os [88] for micro-bump technology. Cu/oxide hybrid bonding [89], [90] is widely investigated for sub-10 μm pitch to solve the aforementioned issues. To this end, the model in Figure 6.1 is modified by changing the vacuum/air to silicon dioxide

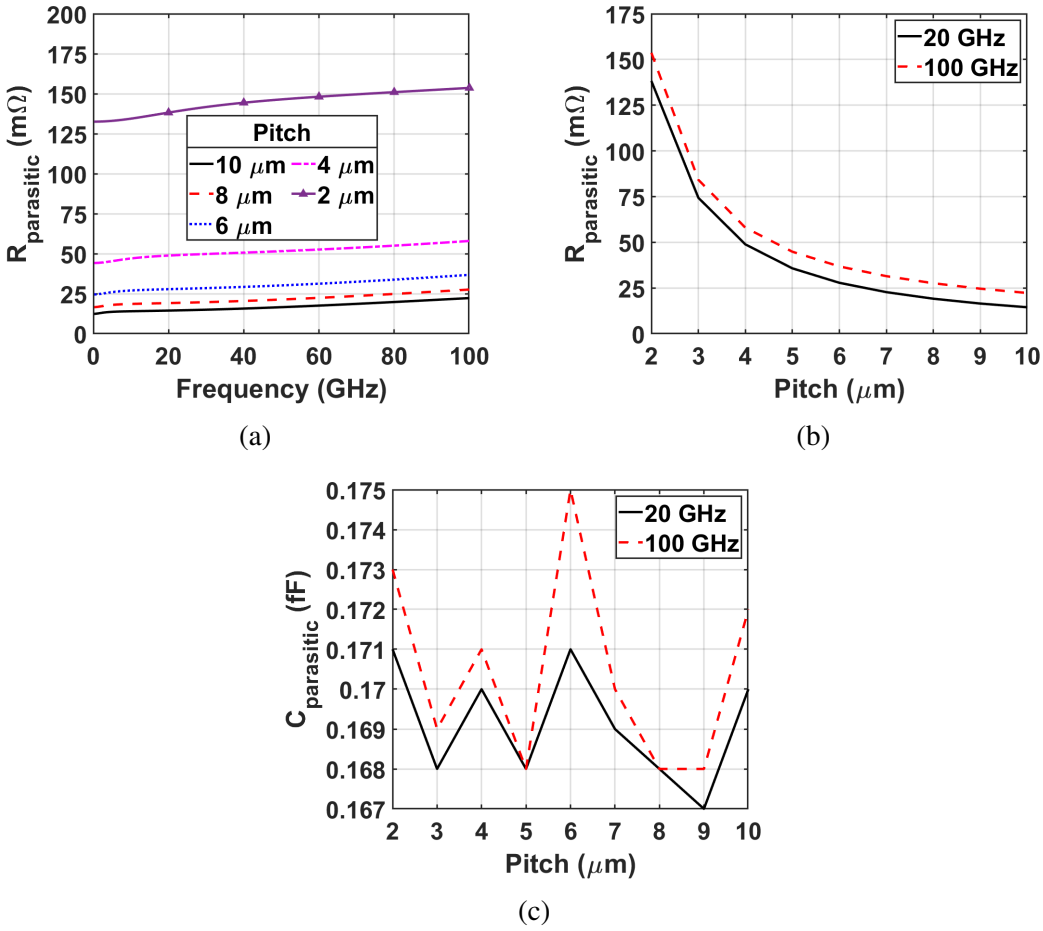
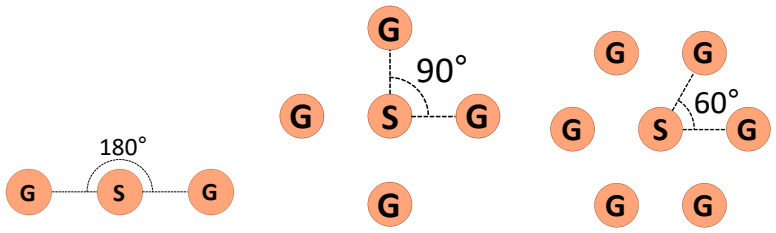


Figure 6.9: Impact of hybrid-bond pitch scaling on (a) frequency-dependent resistance, (b) resistance at 20 GHz and 100 GHz, and (c) capacitance at 20 GHz and 100 GHz

[88] and by replacing the middle solder with copper. The pitch is swept from 2 μm to 10 μm in the simulation. The single I/O height (h_{CuP}) is reduced to a reasonable value as 1 μm [90] and the total I/O height ($h_{CuP} \times 2$) becomes 2 μm.

In Figure 6.9a and Figure 6.9b, the resistances at 20 GHz and 100 GHz are close (<35.1% difference), which implies that the frequency dependence of hybrid-bond's resistance is minimal because DC resistance may be a major contributor of its resistance. The resistance at 20 GHz raises from 14.4 mΩ (10 μm pitch) to 138.2 mΩ (2 μm pitch), which shows a significant increase due to the aggressive I/O pitch scaling. Such aggressive I/O pitch scaling does not show a significant impact on capacitance, as shown in Figure 6.9c.



(a) (b) (c)

Figure 6.10: The top views of different ground-signal I/O's configurations: (a) one signal I/O with two ground I/Os (S2G), (b) one signal I/O with four ground I/Os (S4G), and (c) one signal I/O with six ground I/Os (S6G)

The capacitance maintains a relatively constant of around 0.17 fF. In addition, pitch scaling has limited impacts on inductance and conductance. The inductance is approximately 1.1 pH and the conductance is approximately 1.5 nS at 20 GHz for different pitches.

However, there are fabrication and assembly challenges for hybrid bonding during pitch scaling. For fabrication, a low temperate ($< 250°C$) hybrid bonding process is needed for applications such as DRAM packaging to prevent degrading device performance. Extremely low surface defect level and high precision alignment are also essential to the bonding yield for extremely fine-pitch hybrid bonding.

6.4 Impact of Off-Chip I/O Ground-Signal Configuration

The configuration of ground and signal I/Os is another factor that affects the parasitics of off-chip I/Os. As shown in Figure 6.10, three configurations are studied by modifying the model in Figure 6.1: one signal I/O surrounded by (1) two ground I/Os (S2G), (2) four ground I/Os (S4G), and (3) six ground I/Os (S6G).

6.4.1 Micro-bump

The pitch between signal and ground micro-bumps is initially 50 μm and further scaled to 30 μm. S6G configuration has the lowest resistance for both pitches, as shown in Figure 6.11a. With the same configuration, 30 μm pitch micro-bumps possess $\sim$1.5X higher

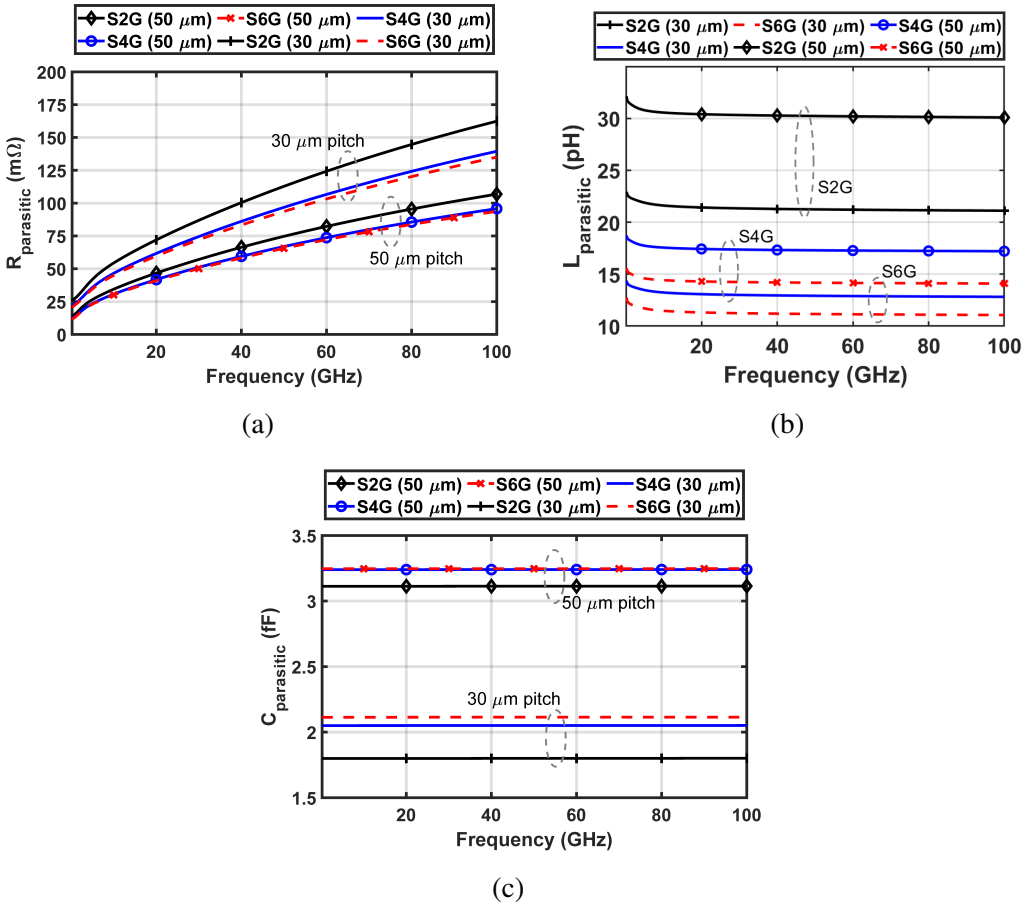


Figure 6.11: Parasitic (a) resistance, (b) inductance, and (c) capacitance of micro-bump with different ground-signal configurations and varied pitches

resistance than 50 μm pitch micro-bumps. The resistance reduces with more ground micro-bumps surrounding the signal micro-bump: the reduction is approximately 10% from S2G to S4G and becomes negligible from S4G to S6G. Because the signal micro-bump's surface current tends to distribute close to the surrounding ground micro-bumps, more ground micro-bumps would make the surface current distribute more uniformly, which mitigates the proximity effect. In addition, more ground micro-bumps establish extra return paths in parallel, which decreases the total loop resistance.

The inductance decreases with more ground micro-bumps for both pitches, as shown in Figure 6.11b. The inductance of the S4G with both pitches reduces by approximately 39%-43% from the S2G. From S4G to S6G, the inductance reduces by approximately 13.7%-

18.1%. The self-inductance of the ground micro-bumps reduces and the mutual inductance between the signal and the ground micro-bumps is unchanged when more ground micro-bumps exist [107]. Therefore, the loop inductance, which is the summation of the self and mutual inductances, decreases with the addition of ground micro-bumps.

As shown in Figure 6.11c, the capacitance increases with the number of ground micro-bumps and saturates at the S6G. The increase of the capacitance is approximately 4%-14% from S2G to S4G for both pitches, which may result from additional capacitive coupling between signal and ground micro-bumps when more ground micro-bumps exist. The capacitance decreases with finer pitch, which may be due to a smaller micro-bump's lateral surface area caused by the smaller diameter.

6.4.2 Hybrid-bond

The hybrid-bonds with 10 μm pitch and 2 μm pitch are selected to study. In Figure 6.12a, the reduction of the resistance for 10 μm pitch happens when four or six ground hybrid-bonds surround one signal hybrid-bond ($\sim$3.39% reduction). For 2 μm pitch in Figure 6.12b, such reduction is around 11.84% from S2G to S4G and is around 1.48% from S4G to S6G. Similar to micro-bump, pitch scaling has a limited impact on inductance, as shown in Figure 6.12c. The inductance decreases by around 12.79%-17.36% from S2G to S4G, while such reduction is around 3%-4.11% from S4G to S6G. In Figure 6.12d, the capacitance for 2 μm pitch and 10 μm pitch is around 0.5-0.7 fF. Similar to the micro-bump, more ground I/Os increases the total capacitance and such increase saturates at the S6G.

6.5 Benchmarking of Off-Chip I/O Technologies

The resistance and the capacitance results of different I/O technologies are depicted in Figure 6.13a and Figure 6.13b. As shown in Figure 6.13a, micro-bump possesses 42.8%-44.8% lower resistance than solder bump for 30 to 50 μm pitch, while its resistance increases rapidly below 30 μm pitch and is predicted to be much higher than hybrid-bond be-

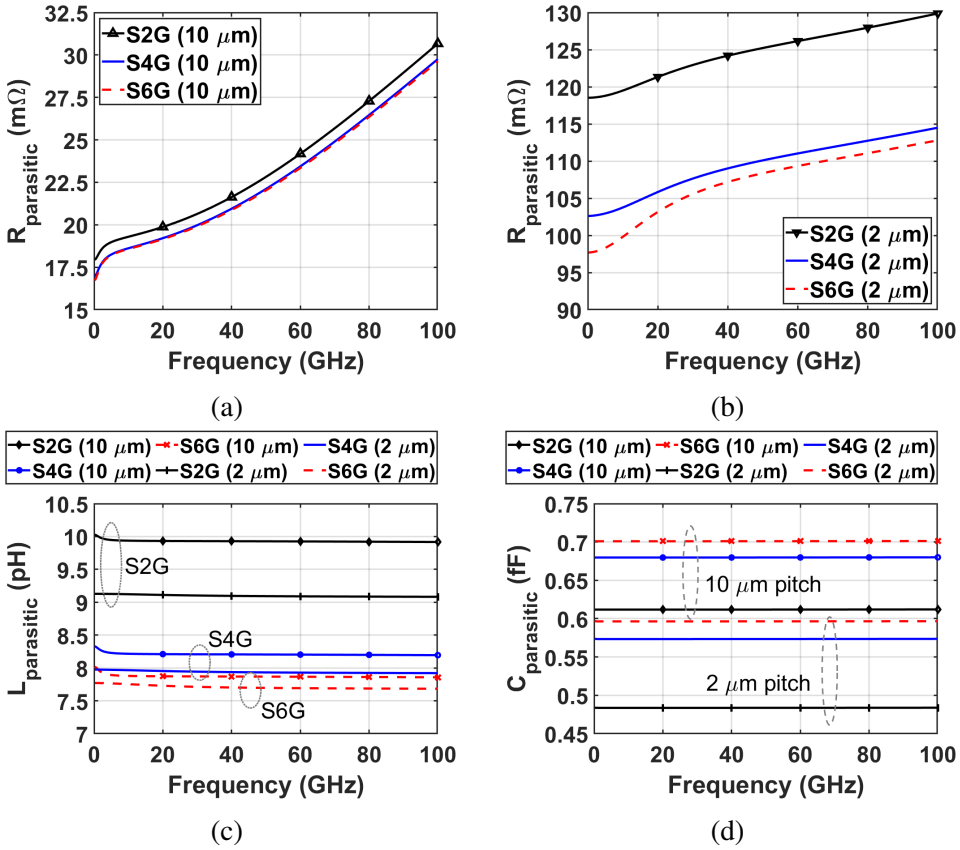
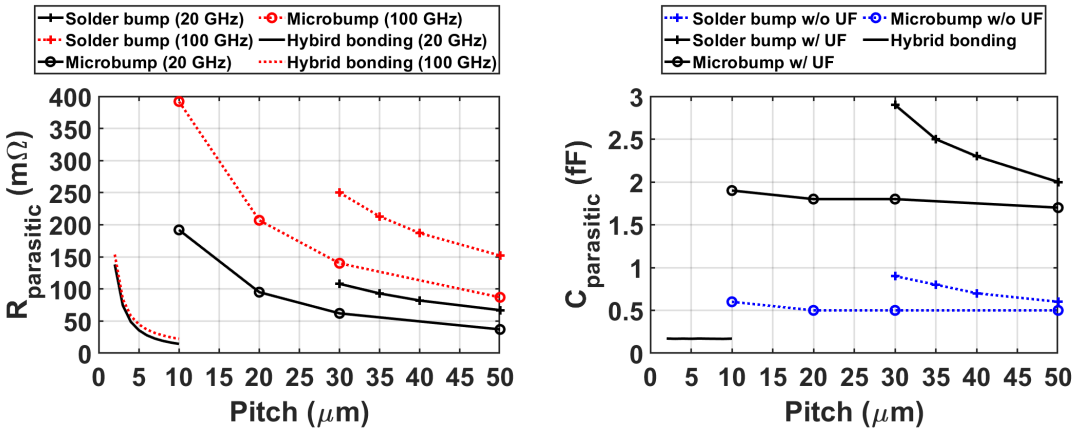


Figure 6.12: Ground-signal configurations impact on (a) resistance of 10 μm pitch hybrid-bond, (b) resistance of 2 μm pitch hybrid-bond, (c) inductance of 10 μm pitch and 2 μm pitch hybrid-bond, and (d) capacitance of 10 μm pitch and 2 μm pitch hybrid-bond

low 10 μm pitch. Hybrid-bond has extremely low resistance (14.4-22.3 mΩ at 10 μm pitch), which increases significantly at 2 μm pitch. As shown in Figure 6.13b, the UF increases the capacitance of the solder bump and micro-bump by around three times. The micro-bump shows lower capacitance than the solder bump, and such difference is expanded by the usage of UF. For pitch below 10 μm, hybrid-bond shows the lowest capacitance (0.17 fF).

Table 6.4 summarizes pitch scaling impact and ground-signal configuration impact for different I/O technologies. Solder bump's parasitics are heavily increased due to pitch scaling except for inductance, which implies its potentially high electrical parasitics that can degrade the performance of applications requiring fine-pitch I/O. Specifically, high elec-



(a) (b)

Figure 6.13: Parasitic (a) resistance and (b) capacitance benchmarking of different I/O technologies at different pitches (G-S configuration)

Table 6.4: Pitch scaling impact and ground-signal pattern impact on different I/O technologies (100 GHz frequency bandwidth).

I/O type	**Pitch (μm)**	**Pitch scaling impact**	**Ground-signal pattern impact**
Solder bump	50 to 30	R↑65.3%, L↓16.7%, C↑45%, G↑40.6%	-
Micro-bump	50 to 10	R↑4.6X, L↓4.4%, C↑11.8%, G(∼)	S2G→S4G: R↓10%, C↑4∼14%, L↓39∼43% S4G→S6G: L↓13.7∼18.1%
Hybrid-bond	10 to 2	R↑6.9X, L(∼), C(∼), G(∼)	S2G→S4G: R↓3.4% (10 μm), R↓11.8% (2 μm), L↓12.8∼17.4%, S4G→S6G: L↓3∼4.1%, C(∼)

trical parasitics (especially capacitance) of solder bumps [48], [108] can prevent the optimization of power consumption that requires both I/O resistance and capacitance reduction [87]. The micro-bump's resistance increases rapidly with pitch scaling, while other parasitics have less change. Note that the micro-bump's parasitics except resistance are less

affected by scaling than solder bumps, which shows its advantages as off-chip I/O for the pitch from 10 μm to 50 μm. For hybrid-bond, such pitch scaling only has a large impact on resistance, while other parasitics maintain similarly. Because of the lowest electrical parasitics, hybrid-bond is becoming a promising I/O technology to enable ultra-high I/O density in advanced packaging technologies, such as 3D stacking [90].

In Table 6.4, the increases in capacitance due to pitch scaling are different for solder bump, micro-bump, and hybrid-bond, which result from the geometry differences of these I/Os: (a) as shown in Figure 6.6, the solder bumps show truncated sphere shape after reflow, which increases the capacitance due to the proximity of adjacent solder. The increase may become higher than micro-bumps, especially for fine-pitch; (b) because the very short length of hybrid-bonds is a major factor affecting the capacitance, pitch scaling has a limited impact, compared to micro-bumps.

For the ground-signal pattern impact, micro-bump and hybrid-bond are selected for the study. More ground micro-bumps reduce the resistance and inductance but increase the capacitance, which shows the design trade-off for the micro-bump's ground-signal configuration. For the hybrid-bond, although more ground hybrid-bonds reduce the resistance, the ground-signal configuration shows less impact on parasitics than the micro-bump. For fine pitch (such as 2 μm pitch), the resistance reduction of the hybrid-bonds becomes significant, compared with coarse pitch (e.g. 10 μm pitch). Therefore, the design of ground-signal configuration could be a potential solution to the high resistance for fine-pitch hybrid-bonds. In addition, more ground hybrid-bonds decrease inductance and have minimal impact on capacitance.

6.6 Conclusion

In this chapter, two frequency-dependent parasitics extraction methodologies up to 100 GHz are reviewed for fine-pitch ($<$50 μm) off-chip I/O which can be potentially utilized in stitch-chip technology: indirect parasitics extraction using simulated S-parameters and nu-

merical parasitics analysis for justifying the accuracy of extractions. The indirect parasitics extraction is correlated to the numerical parasitics analysis (<8% difference).

The impacts of pitch scaling and ground-signal configuration are explored and compared for solder bump, micro-bump, and hybrid-bond. Pitch scaling from 50 μm to 30 μm increases solder bump's resistance (61.2%-65.3%), capacitance (45%-50%), conductance (34.6%-40.6%), and reduces inductance (16.7%), respectively, which implies solder bump's potentially high electrical parasitics that can degrade the performance of applications requiring fine-pitch I/O. Within the same pitch range, pitch scaling shows less impact on micro-bump except for resistance, which shows its advantages as off-chip I/O in such pitch range: from 50 μm to 10 μm pitch, the resistance and the capacitance increase by 3.1-4.6X and 11.8%-20%, respectively, while the inductance decreases 4.4% and the conductance maintains similarly. The lowest electrical parasitics of hybrid-bond can enable low-loss and fine-pitch signal routing at 2-10 μm pitch: the resistance is heavily increased by pitch scaling, while other parasitics maintain similarly.

More ground I/Os surrounding signal I/Os can be a potential solution to reduce I/O parasitics. For micro-bump, more ground I/Os bring down resistance by 10% and inductance but increase capacitance by 4%-14%. In addition, more ground I/Os reduce resistance and inductance while maintaining capacitance for hybrid-bond. Such resistance decrease using more ground I/Os becomes significant (11.8% reduction), especially for the fine-pitch hybrid-bonds case (e.g. 2 μm pitch).

For 30 to 50 μm pitch, micro-bump has lower resistance (42.8%-44.8% less) and lower capacitance than solder bump. For <10 μm pitch, hybrid-bond is envisioned to have extremely low resistance (14.4-22.3 mΩ at 10 μm pitch), which however shows a huge increase at 2 μm pitch, and the lowest capacitance (0.17 fF).

To this end, this chapter along with section 2.5.2 provides an investigation of off-chip I/Os in terms of frequency-dependent parasitics for fused-silica stitch-chip technology.

CHAPTER 7
SUMMARY AND FUTURE WORK

The chapter summarizes and emphasizes the key research contributions of this thesis and explores potential future work which can be extended from this dissertation.

7.1 Summary of the Work

In this thesis, a new polylithic integration using fused-silica stitch-chip technology is proposed, developed, and demonstrated including simulation, fabrication, assembly, and characterization for RF/mm-wave systems. The key research contributions of this thesis are emphasized as follows:

7.1.1 RF characterization methodology for fused-silica stitch-chip components

A thru-only and an L-2L de-embedding techniques are demonstrated and verified using fused-silica stitch-chips to extract loss performance and frequency-dependent parasitics of stitch-chip channels and CMIs. The fabrication process of CMIs is demonstrated on fused-silica substrate.

A 500 μm long fused-silica stitch-chip channel with 30 μm tall and 200 μm pitch CMIs are measured to have an extremely low-loss ($<$0.42 dB insertion loss up to 40 GHz) and low parasitics (4.68Ω at 28 GHz, 4.99 Ω at 39 GHz, 359 pH up to 40 GHz, and 62 fF up to 40 GHz). Such low-loss and low-parasitic features of the stitch-chip are compared with state-of-the-art, which indicates similar loss performance as glass interposer, organic substrate, and InFO wafer-level packaging and significantly lower loss than Si interposer. In addition, the CMIs' RF performance is extracted and is shown to be $<$0.2 dB insertion loss and $>$16.2 dB return loss up to 40 GHz, which is comparable or lower than solder bumps.

7.1.2 Methodology of CMI RF-mechanical co-design and stitch-chip impedance design and characterization

To minimize the impedance mismatch between the stitch-chip and the die/package substrate, a co-design methodology for the CMI is established to optimize its RF and mechanical performance. In addition, the impedance design methodology of the assembled stitch-chip is established and verified with characterization through TDR. These methodologies enable a further performance-oriented design-optimization workflow of the fused-silica stitch-chip and account pad pitch difference, package material difference, and die thickness variance. Most importantly, these methodologies are experimentally demonstrated.

A 50 μm high CMI is optimized to compensate for 30 μm non-planarity and possess $>$12.2 dB return loss, $<$0.4 dB insertion loss, $<$0.7 Ω, 25 pH, and 21 fF. The assembled fused-silica stitch-chip is optimized and measured to achieve approximately 50 Ω impedance, which indicates a significant impedance matching improvement, compared with an equivalent wire-bond. A maximum 0.2 dB insertion loss variance due to different package substrate materials is observed, which implies a good performance consistency of the fused-silica stitch-chip. The RF characterization suggests that $<$0.66 dB insertion loss and $>$11.34 dB return loss up to 50 GHz can be measured for 500 μm long fused-silica stitch-chip channels, which indicates a significant loss reduction from wire-bonding technology.

7.1.3 COTS chiplet-based module demonstration using fused-silica stitch-chip

An embedded LNA single chip module using the fused-silica stitch-chip is experimentally demonstrated including module design, assembly, and characterization. In addition, the stitch-chip design is developed further for RF/mm-wave multi-chip module.

The LNA single-chip module is measured to exhibit $<$2.5 dB package loss, while the 500 μm long stitch-chip and 5.8 mm long RF package trace are measured to have a total interconnect loss of $<$1.4 dB up to 40 GHz. There is a minimal change in the module's input

return loss, compared with the bare die. The output return loss is better than -8 dB. Using the stitch-chip instead of wire-bond reduces the package loss by$\sim$8 dB and the module performance is comparable or better than state-of-the-art. Steady-state thermal simulations are also performed to understand the module's thermal capability. Furthermore, for the RF/mm-wave multi-chip module, case studies (D2D interconnect length, the transition of stitch-chip to package, etc.) of the fused-silica stitch-chip are explored to further optimize the module performance and accommodate with power supply interconnect requirement. The assembly of the multi-chip module and its RF characterization are also discussed.

7.1.4 Investigation of pitch-scaling impact on off-chip I/Os for polylithic integration and benchmarking

Two frequency-dependent parasitics extraction methodologies up to 100 GHz are reviewed for fine-pitch ($<$50 μm) off-chip I/O, which can be potentially utilized in stitch-chip technology: indirect parasitics extraction using simulated S-parameters and numerical parasitics analysis for justifying the accuracy of extractions.

The impacts of pitch scaling and ground-signal configuration are explored and compared for solder bump, micro-bump, and hybrid-bond. When pitch scales from 50 μm to 30 μm, the solder bump shows fast-increasing electrical parasitics, which can degrade the performance of applications requiring fine-pitch I/O. However, the pitch scaling shows less impact on the micro-bump except for resistance. The hybrid-bond shows the lowest electrical parasitics that can enable low-loss and fine-pitch signal routing at 2-10 μm pitch. More ground I/Os surrounding signal I/Os can be a potential solution to reduce I/O parasitics. For micro-bump, more ground I/Os reduce resistance by 10% and inductance but increase capacitance by 4%-14%. The resistance decreases using more ground I/Os becomes significant when hybrid-bond scales to 2 μm pitch. For 30 to 50 μm pitch, the micro-bump has lower resistance (42.8%-44.8% less) and lower capacitance than the solder bump. For $<$10 μm pitch, hybrid-bond is envisioned to have extremely low resistance (14.4-22.3 mΩ at 10

μm pitch), which however shows a huge increase at 2 μm pitch, and the lowest capacitance (0.17 fF).

7.2 Future Work

The potential advancement of this thesis can be summarized into the following categories.

7.2.1 Thermal design and reliability measurement of the chiplet-based module

As discussed in Chapter 4, future integration of high-power mm-wave die may require a specific design for thermal management, given current stack-up of the package substrate of the LNA module has not been optimized from the thermal perspective.

For example, due to its low thermal conductivity, FR4 material in the stack-up may prevent the heat from spreading across the package substrate, which can be potentially improved by using higher thermal conductive stack-up material. In addition, the stack-up can be customized to reduce or balance package warpage due to CTE mismatch, such as increasing stack-up thickness or using symmetrical stack-up. The thermal performance can be further improved by optimizing die-attaching methods, such as utilizing eutectic bonding which has a higher thermal conductivity at the bonding interface, and including a backside heat sink or active air cooling design.

Characterizations, such as die temperature measurement using infrared imaging, can be performed to verify the thermal design for high-power mm-wave die (e.g. PA) integration in the module. Measurements, such as thermal cycling tests, can be utilized to understand the reliability of the designed module.

7.2.2 Passive device integration in stitch-chips

Integration of passives into the stitch-chips opens more opportunities to expand stitch-chip functions for better module performance.

One opportunity is the impedance matching network integration. As shown in Chapter

4, a slight impedance mismatching at the LNA die output degrades the linear gain performance of the module. Passive narrowband and wideband impedance matching network design can be explored and integrated into the stitch-chip design flow [43]. Therefore, the stitch-chip not only performs as RF signal interconnect but also possesses impedance matching network function to further improve the RF performance of the module.

Another opportunity is using the stitch-chip as a power supply interconnect. Unlike using the stitch-chip as the RF interconnect, the design considerations of the stitch-chip as a power supply interconnect are low DC resistance, low off-chip I/O contact resistance, and low interconnect impedance.

7.2.3 Off-chip I/O technologies mix-and-match in stitch-chips

In Chapter 6, other off-chip I/O technologies that can be utilized in the stitch-chip are discussed in terms of pitch scaling impact and ground-signal configuration impact on RF performance. These investigations open an opportunity of realizing a mix-and-match of off-chip I/O technologies in stitch-chips to take advantage of each off-chip I/O. This mix-and-match strategy of off-chip I/O rises the number of the stitch-chip applications and increases the package design flexibility.

For example, by utilizing the micro-bump and the CMI on one single stitch-chip, the stitch-chip can realize the low IR drop for power delivery and fine-pitch signal routing (enabled by the micro-bump), and mitigate thermal-induced stress and compensate for non-planarity in the package (enabled by the CMI). The design, process integration, and assembly are necessary to be investigated for the mix-and-match off-chip I/O technologies in the stitch-chip.

Appendices

APPENDIX A

PARASITICS NUMERICAL CALCULATION DETAILS

A.1 DC and AC Resistance Calculation

The calculations of the pillar's DC resistance and the middle solder's DC resistance are as follows:

$$R_{pillar}^{DC} = \frac{1}{\sigma_{cu}} \frac{h_{CuP}}{\pi(dia/2)^2} \tag{A.1}$$

$$R_{solder}^{DC} = \frac{1}{\sigma_{solder}} \frac{h_{solder}}{\pi(dia/2)^2} \tag{A.2}$$

where σ_{cu} and σ_{solder} are the conductivity of copper and solder, respectively.

The skin-effect onset frequency (ω_δ) is defined as follows [98]:

$$\omega_\delta = \frac{2}{\mu_{cond}\sigma_{cond}} \Big(\frac{4k_a}{k_p(dia)} \Big)^2 \tag{A.3}$$

where μ_{cond} and σ_{cond} are the permeability and the conductivity of the conductor, respectively. k_a is the DC resistance correction factor related to the return path [98], and k_p is a correction factor depending on the proximity effect [98]. The k_p is determined by p/dia [98].

The calculations of the pillar's AC resistance and the middle solder's AC resistance are as follows:

$$R_{pillar}^{AC} = \frac{k_p h_{CuP}\sqrt{\omega\mu_{cu}}}{\pi(dia)\sqrt{2\sigma_{cu}}} \tag{A.4}$$

$$R_{solder}^{AC} = \frac{k_p h_{solder}\sqrt{\omega\mu_{solder}}}{\pi(dia)\sqrt{2\sigma_{solder}}} \tag{A.5}$$

where ω is angular frequency, and μ_{cu}, μ_{solder} are the permeability of copper and solder, respectively. Note that return path's AC resistance is included in the calculation.

A.2 Inductance Calculation

The I/O's self-inductance and mutual-inductance are calculated as follows:

$$L_s = \frac{\mu_0(2h_{CuP} + h_{solder})}{2\pi}\Big[\ln\Big(AR + \sqrt{AR^2+1}\Big) - \sqrt{1 + \frac{1}{AR^2}} + \frac{1}{AR}\Big] \tag{A.6}$$

$$L_m = \frac{\mu_0(2h_{CuP} + h_{solder})}{2\pi}\Big[\ln\Big(AR_m + \sqrt{AR_m^2+1}\Big) - \sqrt{1 + \frac{1}{AR_m^2}} + \frac{1}{AR_m}\Big] \tag{A.7}$$

where AR and AR_m are defined as follows:

$$AR = \frac{2h_{CuP} + h_{solder}}{dia/2} \tag{A.8}$$

$$AR_m = \frac{2h_{CuP} + h_{solder}}{dia/2 + p} \tag{A.9}$$

APPENDIX B

SILICON SUBSTRATE CAPACITANCES CALCULATION

C_{diel} can be calculated based on conformal mapping method [109]:

$$C_{diel} = dia \times \varepsilon_0(\varepsilon_{r,ox} - \varepsilon_{r,air})\frac{K'(k_2)}{K(k_2)} \tag{B.1}$$

$$k_2 = \frac{\sinh(\frac{\pi(p+dia/2)}{2h_{diel}})}{\sinh(\frac{\pi(p-dia/2)}{2h_{diel}})}\sqrt{\frac{\sinh^2(\frac{\pi(p-dia/2)}{2h_{diel}}) - \sinh^2(\frac{\pi\times dia/2}{2h_{diel}})}{\sinh^2(\frac{\pi(p+dia/2)}{2h_{diel}}) - \sinh^2(\frac{\pi\times dia/2}{2h_{diel}})}} \tag{B.2}$$

where ε_0 is the vacuum permittivity, $\varepsilon_{r,ox}$ and $\varepsilon_{r,air}$ are relative permittivity of oxide layer and air, respectively, h_{diel} is oxide layer thickness, and K is complete elliptical integral of the first kind. C_{SiO_2} and C_{Si} can be calculated based on [104]:

$$C_{SiO_2} = dia \times \frac{\varepsilon_0\varepsilon_{eff}(\varepsilon_{r,ox}, h_{diel})}{F(h_{diel})} \tag{B.3}$$

$$C_{Si} = dia \times \frac{\varepsilon_0\varepsilon_{eff}(\varepsilon_{r,Si}, h_{Si})}{F(h_{Si})} \tag{B.4}$$

$$F(h) = \begin{cases} \frac{1}{2\pi}\ln(8h/dia + dia/4h), & h/dia \geq 1 \\ \frac{1}{dia/h + 2.42 - 0.44h/dia + (1-h/dia)^6}, & h/dia \leq 1 \end{cases} \tag{B.5}$$

$$\varepsilon_{eff}(\varepsilon, h) = \frac{\varepsilon+1}{2} + \frac{\varepsilon-1}{2\sqrt{1+10h/dia}} \tag{B.6}$$

where $\varepsilon_{r,Si}$ and h_{Si} are relative permittivity and thickness of Si substrate, respectively.

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