POWER DISTRIBUTION NETWORK MODELING AND MICROFLUIDIC COOLING FOR HIGH-PERFORMANCE COMPUTING SYSTEMS

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POWER DISTRIBUTION NETWORK MODELING AND MICROFLUIDIC COOLING FOR HIGH-PERFORMANCE COMPUTING SYSTEMS

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DEDICATION

To my mom and grandma

for their endless love and support

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SUMMARY

Power delivery and thermal management are two major challenges facing future high-performance computing systems. In this research, an embedded microfluidic cooling technology, which is compatible with the existing microbump and flip-chip bonding technologies, is developed and demonstrated. Microfluidic I/Os enable coolant flow between tiers (stacked dice and interpser). The microfluidic I/Os consist of fluidic microbumps and vias. Solder-based annular shaped fluidic microbumps, which can be simultaneously fabricated and assembled with fine-pitch electrical microbumps, are developed. Moreover, 3D stacking of silicon dice with electrical and fluidic I/Os is demonstrated. A silicon interposer platform utilizing the microfluidic cooling technology is proposed, which provides superior cooling performance and high-bandwidth off-chip signaling.

A numerical power distribution network simulator is developed based on distributed circuit model and the finite difference method. The distributed circuit model captures the distributed nature of the power distributed network (distributed decoupling capacitance, parasitic resistance and inductance) and improves simulation accuracy. A set of difference equations is derived based on the circuit model and iteratively solved in the time-domain for the voltage distribution across the power distribution network. The simulator is extended to 3D power distribution network simulation by including TSVs, full-chip simulation with multiple blocks of non-uniform power density, TSVs, and decoupling capacitance distribution, and die-package-board power distribution network co-simulation by including models for package and board-level power/ground planes. The simulator enables trade-off analysis and design space exploration of the die, package, and board-level power distribution network.

CHAPTER I

INTRODUCTION

1.1 Motivation

Since the inventions of the transistor in 1947 and the integrated circuit (ICs) in 1958, the world has profoundly changed due to the innovations in information technology [1]. The major driving forces are continuous cost reduction, performance improvement, and scaling of computing systems. Figure 1 shows the scaling trend of commercial products from major manufactures [2], which was predicted by Gordon E. Moore in 1965 [3]. For 50 years, the industry has followed Moore's law. However, the node-to-node scaling is reaching physical limit, which causes increased research, development, and manufacturing difficulty and cost [4]. Recently, Intel modified its tick-tock model

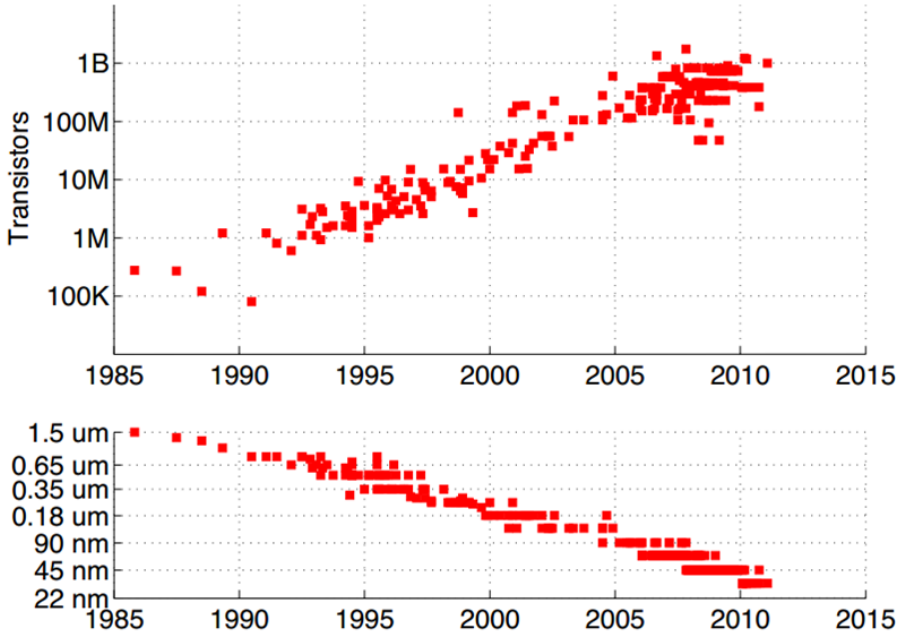


Figure 1: Transistor count and feature size vs. year.

by delaying 10 nm node product till 2017 [5].

Moreover, the performance gain from scaling is becoming saturated due to power and cooling issues [6]. Power dissipation is proportional to CV^2f, where C is switching capacitance, V is supply voltage, and f is clock frequency. Since V scaled much slower than C and f with technology node, the power density kept increasing and reached the limit of conventional air-cooling, around 100 W/cm^2 (Figure 2(a)) [2]. Moreover, the limited cooling capability of air-cooling leads to larger leakage power which has an exponential dependence on temperature [7]. The increased leakage power reduces power efficiency and system performance [8]. Due to the cooling limit and leakage current, the clock frequency scaling had to stop in early 2000s (Figure 2(b)) [2].

Silicon interposer (2.5D) and 3D integration technologies have been widely studied for their fine-pitch interconnects and high-bandwidth signaling as well as reducing form factor and heterogeneous integration [9]–[12]. With 3D integration technology, the number of the long global interconnects on a large 2D die is reduced by dividing the die into multiple smaller dice and stacking the small dice with high-density and much shorter vertical interconnects [13]. The reduced interconnect length helps reduce signaling delay and save power. Moreover, the number of interconnects can be

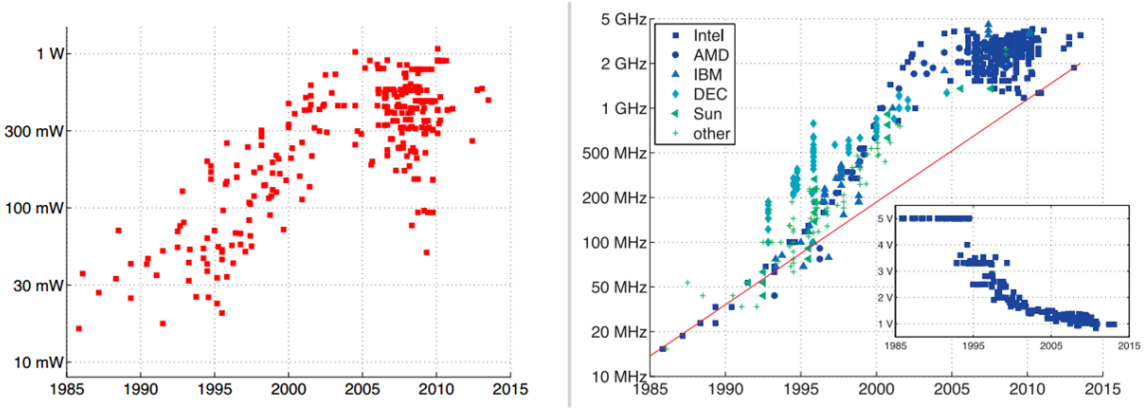


Figure 2: Power density (mW/mm^2) vs. year (left), and clock frequency vs. year (red line indicates the frequency increase due to gate speed; inserted is the Vdd vs. year).

significantly increased and routing congestion can be minimized.

Power delivery and thermal management are two major challenges facing high-performance computing systems [1], [14]. They become even more challenging for 3D integrated systems [15], [16]. Stacking multiple high-power dice drastically increases power density, which can easily exceed the capability of air cooling. Even worse, the lower dice in the stack have no direct contact to the heat sink sitting on top of the stack. A more advanced cooling technology has to be developed for high-performance 3D systems. Besides the cooling challenge, the increased power density and vertical interconnects exacerbate the power supply noise issue, which would degrade system performance or even cause failure. Thus, the impact of 3D integration on power supply noise and power distribution network design has to be investigated.

1.2 The State of the Art of Relevant Technologies

1.2.1 Microfluidic Cooling Technology

Cooling is one primary challenge facing high-power and 3-D ICs. Conventional air-cooled heat sinks have limited cooling capability [17], while the increasing power density and thermal resistance due to stacking dice make cooling even more challenging. Embedded within-tier microfluidic cooling has been explored as a promising solution [1], [18]–[20]. Compared to air-cooling, the advantages of microfluidic cooling includes: 1) water has much higher heat capacity than air, which means significant improvement in cooling performance; 2) the chip-scale embedded microfluidic heat sink, which is compatible with the CMOS fabrication technology, improves integration density and enables 3-D chip stacking by eliminating bulky air-cooled heat sinks.

In 1981, Tuckerman and Pease demonstrated cooling of 790 W/cm^2 with an embedded microfluidic heat sink for the first time [18]. In 2009, Brunschwiler et al. reported cooling of a 4-tier stack with a total power dissipation of 390 W utilizing microchannel heat sink and water as coolant [21]. More recently, Zhang et al. proposed

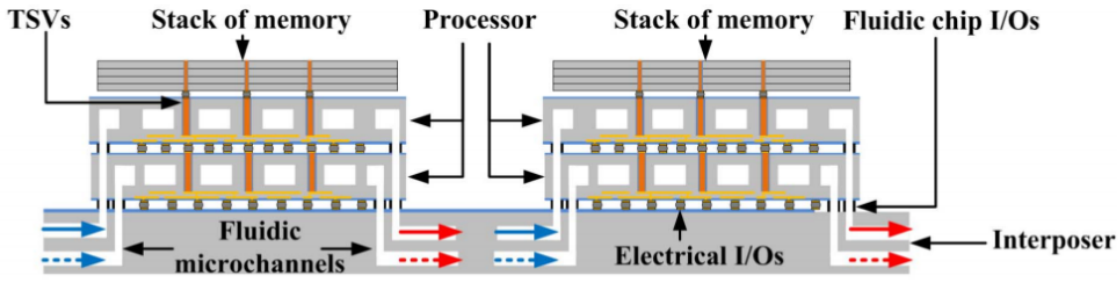
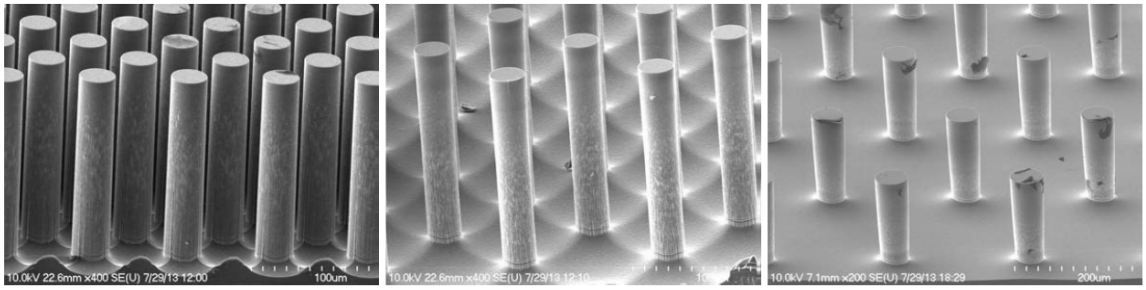


Figure 3: Tier specific microfluidic cooling for heterogeneous stacks of processor and memory dice on a silicon interposer



(a) Staggered micropin-fin of 30 um diameter and 36 um pitch

(b) Staggered micropin-fin of 30 um diameter and 60 um pitch

(c) Staggered micropin-fin of 60 um diameter and 240 um pitch

Figure 4: Micropin-fins of different diameters and pitches.

tier-specific microfluidic cooling for heterogeneous high-performance 3-D ICs [22], as illustrated in Figure 3. Heterogeneous stacks of processor and memory tiers are assembled on a silicon interposer. A microfluidic heat sink is embedded into each processor tier and connected to the coolant delivery channels in the silicon interposer through fluidic I/Os. Since each heat sink in a stack is independent, the flow rate can be adjusted for a specific tier independently. Through silicon vias (TSVs) are routed through the heat sink for electrical interconnections. Moreover, [22] compares microfluidic cooling and air cooling for a two tier stack. The junction temperature rise is 30 °C for power density of 100 W/cm^2 in each tier when the stack is cooled with micropin-fin heat sinks and de-ionized water. With air cooling, the temperature rise is larger than 54 °C while the power density in each tier is only 50 W/cm^2.

Microfluidic heat sink design has a significant impact on cooling performance.

Originally, a microfluidic channel heat sink was used by Tuckerman et. al. to demonstrate microfluidic cooling. In 2005, Peles et al. demonstrated a staggered pin-fin heat sink [23], which reduces the thermal resistance by 33% compared to the microfluidic channel design. More microfluidic heat sink designs including in-line and staggered micropin-fin, pearl chain, staggered drop-shaped pin-fin have been reported in [21]. Recently, a staggered micropin-fin design with five different pin diameters and pitches were compared to explore the design space and optimize the micropin-fin design [24]. Figure 4 shows SEM images of the micropin-fins with different diameters and pitches.

Fluidic I/Os are imperative for delivering coolant to the stacked microfluidic heat sinks. Polymer-based micropipes have been developed as fluidic I/Os [25], [26], as shown in Figure 5(a). The micropipes are aligned and inserted into polymer sockets defined on the back side of the dice and sealed with epoxy-based underfill. Another type of fluidic I/Os are solder based fluidic microbumps, as shown in Figure 5(b), which has been demonstrated by King et al. along with 80 μm diameter electrical bumps.

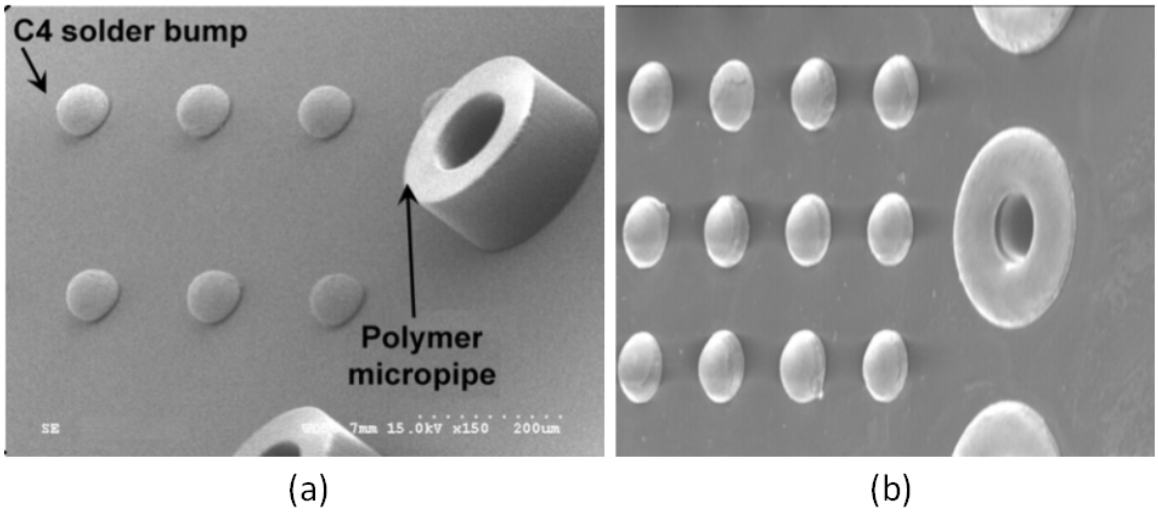


Figure 5: Fluidic I/Os: (a) polymer-based micropipe; (b) solder-based fluidic microbump

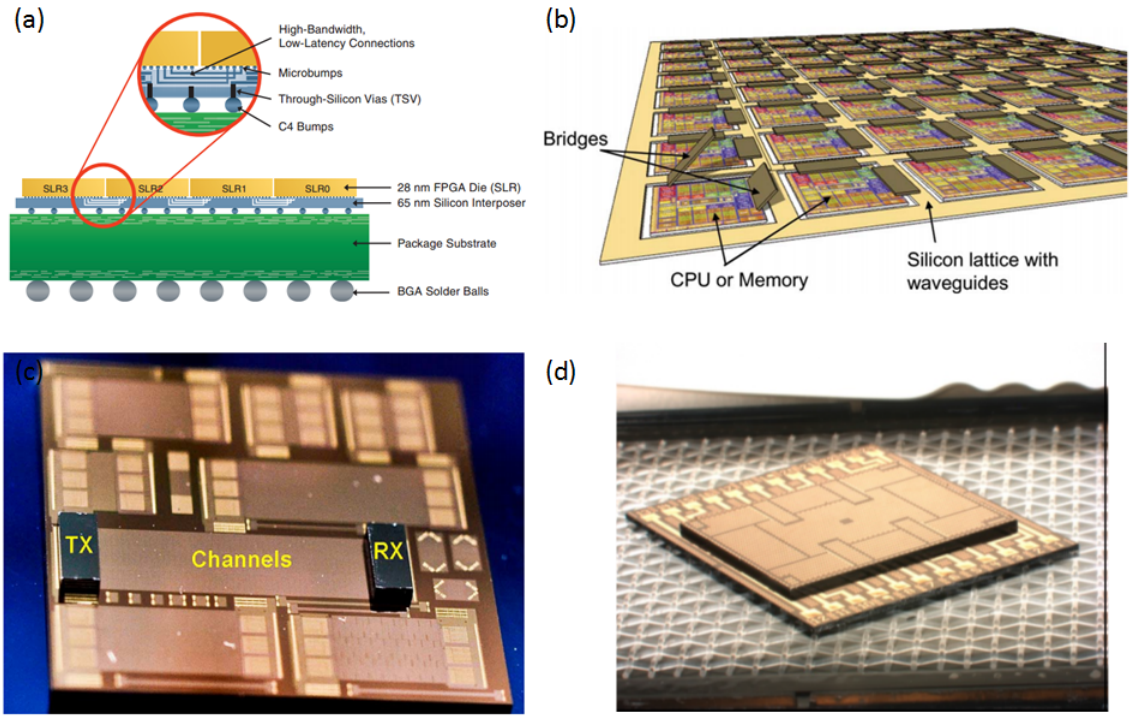


Figure 6: (a) silicon interposer-based FPGA (Xilinx); (b) silicon photonic "macrochip" (Oracle); (c) 8 × 10 Gpbs chip-to-chip signaling on a silicon interposer (IBM); and (d) silicon interposer with TSVs and flexible compliant interconnects (Oracle).

Compared to polymer-based fluidic I/Os, solder-based fluidic I/Os have the following advantages: 1) Solder-based fluidic microbumps can be simultaneously fabricated and assembled along with electrical microbumps without additional processing steps; 2) underfill is not mandatory for fluidic sealing; 3) solder fluidic microbumps are reworkable along with electrical microbumps; and 4) solder fluidic microbumps have better thermal conductivity.

1.2.2 Silicon Interposer Technology

Silicon interposers have been widely studied for their compelling advantages over conventional ceramic and organic substrates, such as very fine pitch interconnects and microbumps for high-bandwidth chip-to-chip signaling, coefficient of thermal expansion matching for improved reliability, and heterogeneous integration [12], [27]–[29].

Different architectures utilizing silicon interposers have been proposed for high-performance computing systems. Xilinx, Inc. has reported a high-end FPGA product based on silicon interposer in which four FPGA dice are assembled side-by-side, as shown in Figure 6(a). The four dice operate as one "virtually monolithic" die with the fine-pitch interconnects on interposer, which enables high-bandwidth, low-latency, and low-power signaling [30], [31]. Moreover, a silicon photonic "macrochip" system has been developed by Oracle that utilizes photonic waveguides on a silicon interposer to achieve high-bandwidth and low energy communication between dice [32], as shown in Figure 6(b). Silicon photonics are promising in chip-to-chip communication; however, electrical interconnects are still superior at shorter distances. IBM reported differential signaling of 10 Gbps per channel using high-density silicon interposer interconnects of 2 μm to 6 μm wide and up to 6 cm long [33], as shown in Figure 6(c). Another example, a silicon interposer with TSVs of 50 μm diameter and 400 μm length and MoCr flexible compliant interconnects was demonstrated for truly reworkable/rematable application [34], as in Figure 6(d).

For both silicon interposer and 3-D technologies, microbumps, as high-density electrical I/Os, are critical to implementing high-density electrical interconnections. Copper pillar bumps and solder microbumps of 30-60 μm pitch have been extensively studied [31], [32], [35], [36]. Figure 7 shows the solder microbump of 50 μm pitch from IBM [12], copper pillar bump of 45 μm reported by STATS ChipPAC Ltd [36], and squared-shaped microbumps of 45 μm pitch with "crown" on the edges for the aforementioned silicon photonic "macrochip" system from Oracle [32].

More recently, a silicon bridge concept was proposed by Yang et al., which enables high-bandwidth communication between silicon interposers, to form an even larger scale of system by integrating multiple silicon interposers [37], [38], as shown in Figure 8.

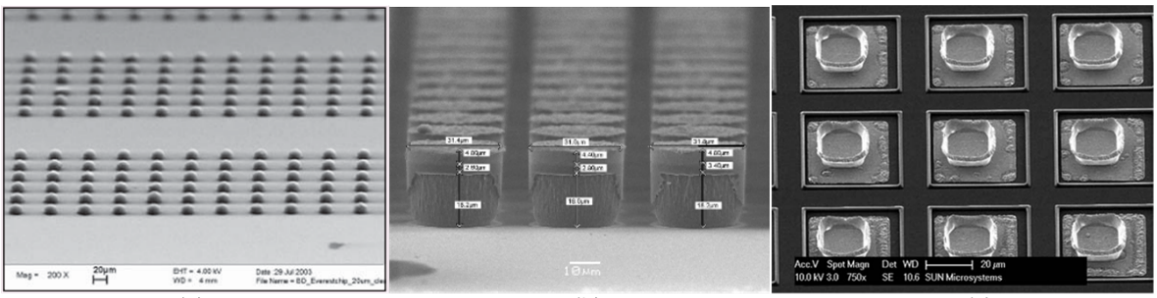


Figure 7: (a) Solder microbumps of 20 μm diameter and 50 μm pitch (IBM); (b) copper pillar bumps of 40 μm pitch (STATS ChipPAC Ltd); (c) square-shaped microbumps with "crown" over the edge for high conductivity (18 μm edge and 45 μm pitch, Oracle)

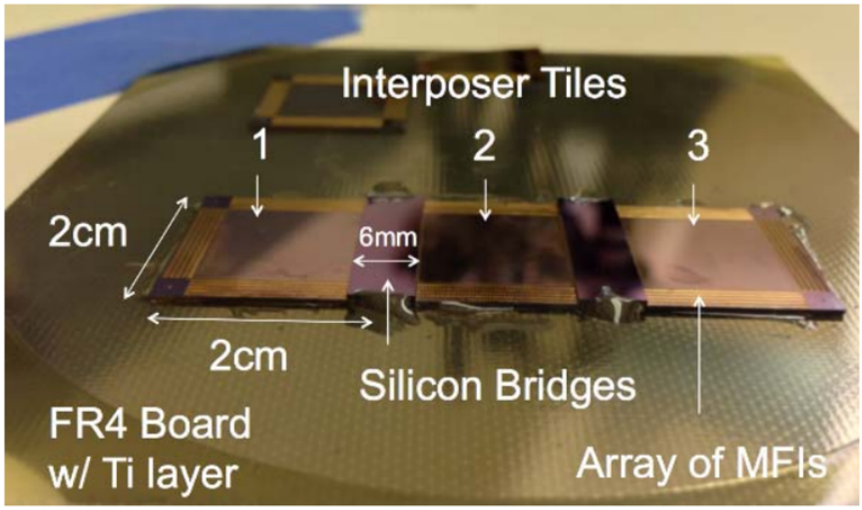


Figure 8: Silicon bridge to integrate multiple silicon interposers.

1.2.3 Power Distribution Network Modeling

Power integrity is important to electronic systems, since excessive power supply noise (PSN) drastically degrades system performance and may even cause logic failures [14]. Power supply noise consists of IR-drop and simultaneous switching noise (SSN or ΔI noise), which are due to the parasitic resistance, inductance, and decoupling capacitance (decap) of the power distribution network (PDN) [16]. The interactions of board, package, and die-level PDN cause noise of different frequency ranges, the mid-frequency noise caused by the package parasitic inductance and on-die decoupling

capacitance (decap) having the largest magnitude and would severely degrading performance when it affects critical paths [39]. Figure 9 shows the simulated noise droops for a Intel processor [39]. The first droop corresponds to the mid-frequency noise [40], [41].

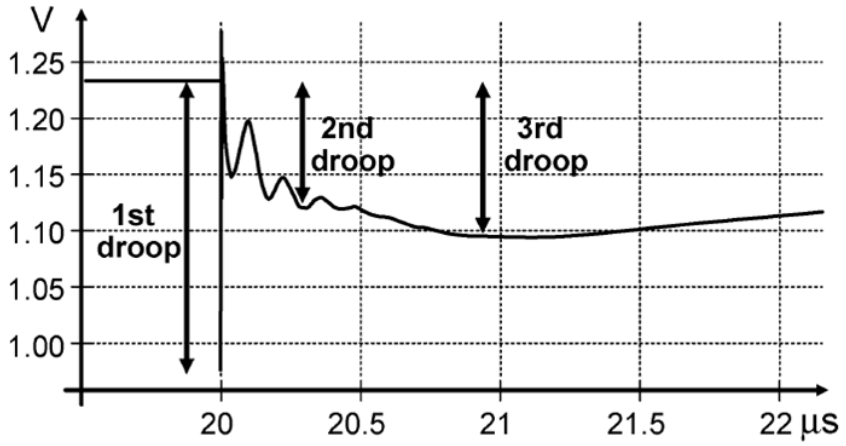


Figure 9: Simulated noise droop for Intel microprocessor.

Power delivery has been a major challenge to 3-D integration of high-performance processor dice since the amount of required current would significantly increase and the vertical interconnects, such as through silicon vias (TSVs), would add more parasitic resistance and inductance to the on-die PDN, which would lead to a significant increase in PSN [42], [43]. Thus, suppressing PSN is critical to the success of high-performance 3-D systems. Figure 10 shows the simulated power supply noise for 3D chip stacks using the compact physical model presented in [16]. Power supply noise increases drastically as the number of stacked dice increases; increasing the number of power/ground pads suppresses the power supply noise.

An efficient and accurate PDN model would help explore design space, allocate resources for PSN suppression, and avoid over- or under- design of PDN. Various methods have been developed to model PDN and explore IR-drop and ΔI noise. A compact physical model for IR-drop is developed for chip/package co-design [44].

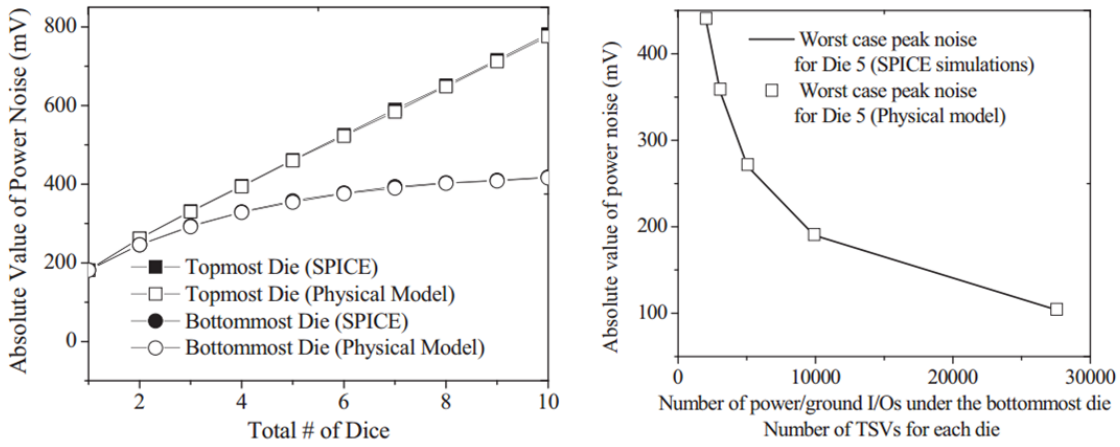


Figure 10: Power supply noise vs. number of stacked dice (left), and (b) power supply noise vs. number of power/ground I/Os (right).

In [45], IR-drop is formulated using finite volume method for electrical-thermal co-simulation. The work in [46] presents a distributed circuit model of a package and an on-die PDN for both IR-drop and ΔI noise analysis. A compact physical model for IR-drop and ΔI noise is developed based on distributed circuit model and frequency-domain formulation in [42]. A method combining electromagnetic (EM) and SPICE simulations is proposed in [47] for modeling and analyzing PDN performance. In [48], PDN impedance of TSV based 3-D ICs is extracted and analyzed based on the method developed in [47]. The work in [49] models and analyzes PDN impedance for TSV based 3-D integration using lumped circuit model and distributed circuit model. The above PDN modeling efforts either focus on steady-state IR-drop or frequency-domain impedance analysis with limited modeling of the package and board. Table 1 summarizes and compares the PDN modeling work.

1.3 Research Statement and Contribution

The research work is divided into two parts. In the first part, a silicon interposer-based platform utilizing microfluidic cooling is proposed to enable high-performance computing systems. Figure 11 illustrates our vision. A logic die stack with embedded

Table 1: Summary of PDN modeling work

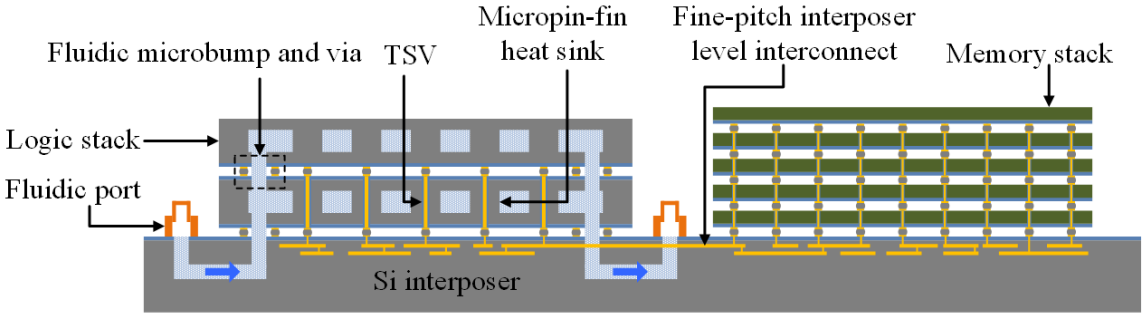
	IR-drop	Transient noise	on-die PDN	Detailed package/board model	Simulation method
K. Shakeri [44]	Yes	No	Dis	Partially	Analytical
J. Xie [45]	Yes	No	Dis	Yes	Numerical
H. Chen [46]	Yes	Yes	Dis	Partially	Commercial simulator
J. S. Pak [49]	IA*	IA*	Lmp/Dis	No	Analytical
G. Huang [42]	Yes	Yes	Dis	No	Analytical
Z. Xu [47]	Yes	Yes	Dis	No	HSPICE
This work	Yes	Yes	Dis	Yes	Numerical

*IA: impedance analysis, Dis: distributed model, Lmp: lumped model

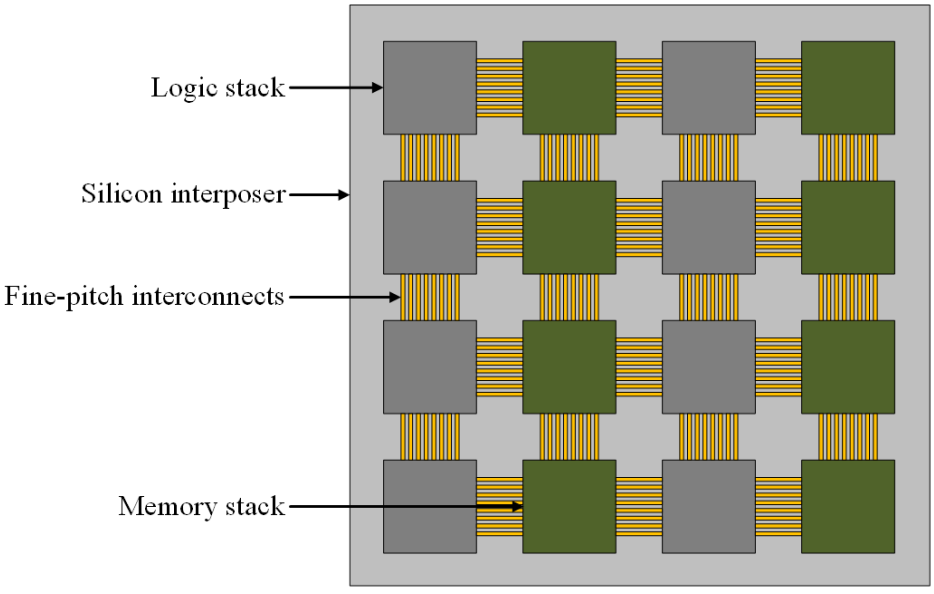
microfluidic heat sink and fluidic I/Os is assembled on a silicon interposer, as shown in Figure 11(a), adjacent to a stack of memory dice. Coolant is pumped into the fluidic channels in the silicon interposer and distributed to the stacked microfluidic heat sinks through the fluidic microbumps and vias. Logic-to-memory high-bandwidth low-energy signaling is achieved using the short fine-pitch wires on the silicon interposer. It is envisioned that a large array of such logic-memory pairs can be formed over a large 2.5D system, as shown in Figure 11(b). The critical technologies including electrical microbump compatible fluidic I/Os, flip-chip bonding of the electrical and fluidic microbumps, and 3D stacking of the electrical and fluidic I/Os have been developed and demonstrated. Moreover, the signaling and thermal benefits of the proposed silicon interposer platform are evaluated using both experiments and simulation.

The second part of the research is power distribution network modeling, simulation and analysis. The impact of integrating embedded microfluidic cooling on power supply noise is investigated using a frequency-domain compact model for the on-die power distribution network. Different methods for suppressing power supply noise, such as adding power/ground pads and decoupling capacitors, are investigated. More

importantly, a time-domain numerical power distribution network simulator for 3D ICs is developed which provides more flexible and faster simulation than the compact model. The numerical model is based on a distributed circuit model for the power distribution network and a set of difference equations derived for the circuit model. By solving the time-domain difference equations numerically and iteratively in matrix form, the voltage distribution across the power distribution network can be simulated. The simulator is further extended to 3D power distribution network by including power delivery TSVs. Moreover, the simulator is extended to full-chip



(a) Logic stack and memory stack on a silicon interposer



(b) Multiple chip-stack system on a large piece of silicon interposer

Figure 11: Simulated noise droop for Intel microprocessor.

power distribution network consisting of multiple blocks of different parameters, such power density, decoupling capacitor density, TSV density and so on. Distributed circuit models for package and board-level power/ground planes are developed and integrated to the numerical simulator to improve simulation accuracy and enable board-package-die power distribution network co-design.

The key contributions of this work include:

1. Solder-based fluidic microbumps are developed for microfluidic-cooled silicon interposer and 3-D applications. The geometry and dimensions of the fluidic microbumps are optimized in terms of pressure drop, die area consumption, and height consistency with electrical microbumps. The fabrication process of fluidic microbumps along with fine-pitch electrical microbump is developed.

2. Silicon dice with the annular-shaped fluidic microbumps and electrical microbumps (25 μm diameter and 50 μm pitch) are fabricated and flip-chip bonded to silicon interposer. Flip-chip bonding of two dice side-by-side on one silicon interposer is demonstrated. The average resistance of the electrical microbumps is 13.5 mΩ. Fluidic microbumps are tested up to 100 kPa at a flow rate of 50 mL/min.

3. The thermal benefits of the proposed silicon interposer platform are evaluated using both experiments and simulation. The measured thermal resistance is 0.24 K$\cdot$cm^2/W at a flow rate of 50 mL/min. Comparing simulation results of microfluidic-cooled and air-cooled silicon interposers, the proposed platform reduces the temperature of the silicon interposer by approximately 40.1%. Moreover, better thermal isolation between dice can be achieved.

4. The signaling performance of the silicon interposer interconnects can be improved by approximately 7.76% due to the reduced temperature. Moreover, the

better thermal isolation enables closer assembly of dice, which would significantly benefit signaling due to shorter interconnects.

5. 3D stacking of the electrical and fluidic microbumps is developed and demonstrated, which is essential to the microfluidic cooling technology for 3D ICs. Two silicon dice with electrical and fluidic microbumps are sequentially bonded to a silicon interposer. The electrical and fluidic interconnects are verified experimentally.

6. Based on a compact physical model, the power supply noise (PSN) of 3-D chip stacks is analyzed. For the 4-die stack with microfluidic heat sinks, increasing the number of power/ground I/Os to 20,000 reduces its PSN to single-die level.

7. A time-domain numerical simulator for on-die power distribution network is developed based on distributed circuit model and finite difference method. By reducing the grid fineness parameter which has a very small impact on simulation results, the simulator is extended for full-chip simulation with multiple blocks of different power densities, decoupling capacitance densities, and TSV densities.

8. Package and board-level power/ground planes are modeled and integrated to the numerical model to improve simulation accuracy and explore the co-design of board-package-die power distribution network. Different configurations of supply voltage, discrete decoupling capacitors on board and package, and the number of BGA are simulated and analyzed.

1.4 Organization of this Thesis

This thesis is organized as follows:

Chapter 2: Development of the electrical and fluidic I/Os for embedded microfluidic cooling is presented. The design considerations, fabrication process, assembly,

and electrical and fluidic testing of the electrical and fluidic I/Os are presented. Moreover, 3D stacking of the electrical and fluidic I/Os is demonstrated.

Chapter 3: The proposed silicon interposer platform is presented, and its benefits in thermal management and signaling are analyzed and discussed. The cooling performance of the proposed platform is evaluated based on both thermal measurements and simulations. Differential signaling on silicon interposer with different cooling configurations are modeled and compared.

Chapter 4: The impact of integrating microfluidic cooling on power supply noise is investigated using a compact model. Moreover, the newly developed time-domain numerical simulator for on-die power distribution network is presented. Full-chip power supply noise simulation with non-uniform power, decoupling capacitor, and TSV distribution is presented.

Chapter 5: The numerical power distribution network simulator is expanded to include board and package-level power/ground planes for more accurate simulation and board-package-die power distribution network co-simulation. Different configurations of board and package power/ground planes are explored.

Chapter 6: Conclusion of this dissertation and potential future work to continue the presented work are discussed.

CHAPTER II

ELECTRICAL AND FLUIDIC I/Os FOR MICROFLUIDIC COOLED HIGH-PERFORMANCE COMPUTING SYSTEMS

2.1 Introduction

Flip-chip bonding technology with controlled collapse chip connection (C4) microbumps has been widely used to improve I/O density for high-performance computing systems [50]. Microfluidic cooling, as a promising thermal management technology for high-performance computing systems, has to be compatible with the flip-chip bonding and C4 microbump technology.

Fluidic I/Os, which are responsible for delivering coolant from package to on-die embedded microfluidic heat sink or even between stacked dice (3D ICs) are very important components of fluidic network. However, very limited work related to fluidic I/O technology has been published. Polymer-based micropipe [51] and solder-based fluidic microbump [52] are the two possible fluidic I/O technologies that have been demonstrated and published. Compared to polymer-based micropipe, solder-based fluidic microbump technology has the following advantages: 1) Solder-based fluidic microbumps can be simultaneously fabricated along with electrical microbumps without additional processing steps; 2) it is fully compatible with flip-chip bonding technology for electrical microbumps; 3) underfill is not mandatory for fluidic sealing with fluidic microbumps; 4) fluidic microbumps are reworkable along with electrical microbumps; and 5) fluidic microbumps have better thermal conductivity. Thus, the proposed fluidic I/O work is based on the solder fluidic microbump technology. Since researchers are working on fine-pitch microbumps for higher electrical I/Os density,

this research adopted electrical microbumps of 25 μm diameter and 50 μm pitch in the electrical and fluidic I/O design. Both electrical and fluidic microbumps can be further scaled for higher I/O density.

2.2 Design of Solder-Based Fluidic I/Os

Fluidic I/Os, which consist of through silicon vias (TSVs) and fluidic microbumps, enables vertical fluidic interconnects between layers, as shown in Figure 12. A row of several fluidic I/Os is placed at two opposite edges of the silicon die. Coolant is pumped into the microfluidic channels in the silicon interposer and distributed to the microfluidic heat sink through the fluidic I/Os. A fluidic microbump is used to seal a fluidic via to avoid coolant leakage which would impact electrical devices and circuits.

The design concerns for the fluidic I/Os are: 1) the complexity and cost of fabrication and assembly; 2) the compatibility with electrical IOs/microbumps; 3) the die area consumption; and 4) the reliability and fluidic sealing quality. Solder based fluidic microbumps are chosen since they can be simultaneously fabricated and assembled along with electrical microbumps and are fully compatible with the conventional

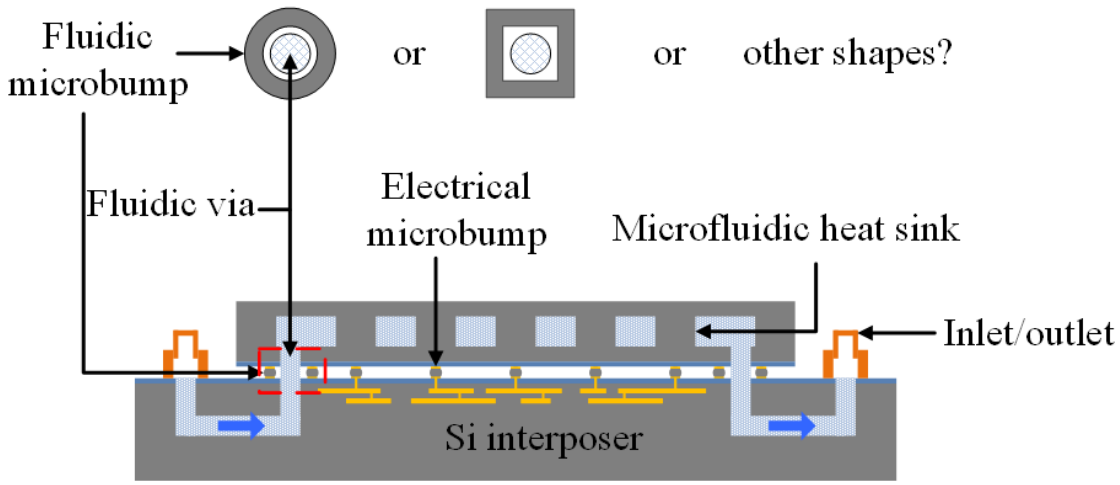


Figure 12: Fluidic I/O consisting of fluidic via and fluidic microbump for embedded microfluidic cooling.

bumping and flip-chip bonding processes. Thus, minimal extra fabrication and assembly complexity and cost are required. However, there are still challenges due to the significant size difference between the fluidic and electrical microbumps. The geometry and dimensions of the fluidic microbump are critical to its success.

2.2.1 Geometry Design of Fluidic I/Os

The fabrication process of fluidic microbumps involves solder reflow which impacts the surface and geometry of fluidic microbumps. The solder reflow impact is investigated using the simulator "Surface Evolver", which can be used to simulate the solder reflow

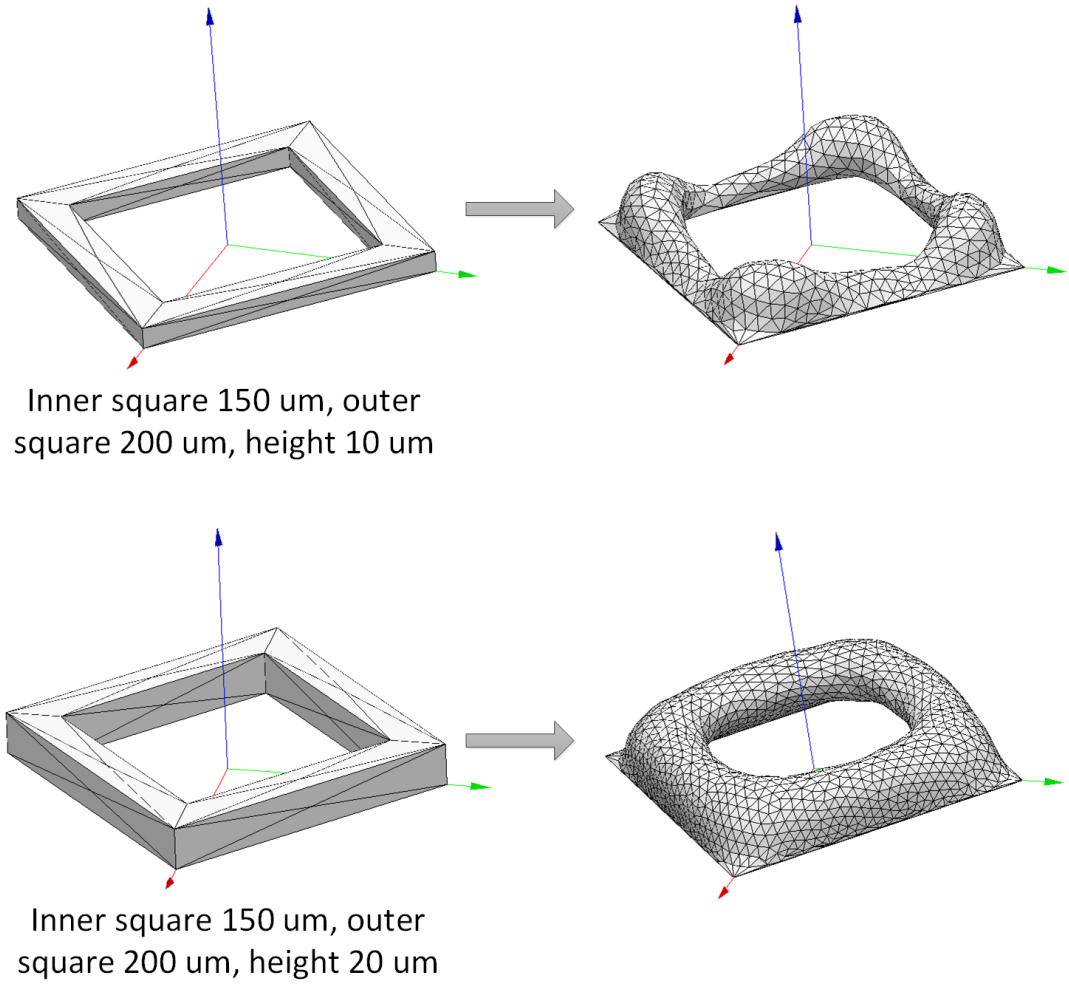


Figure 13: Reflow of square-shaped fluidic microbump.

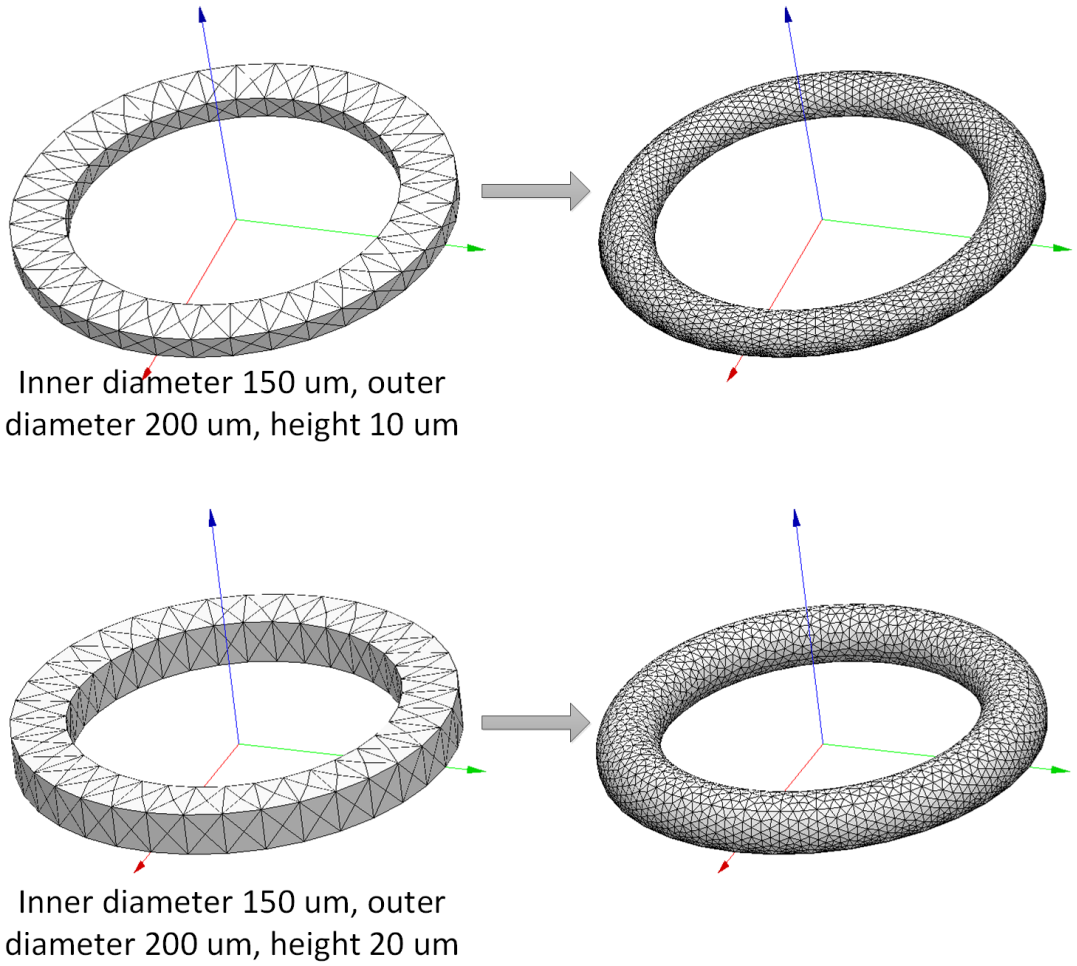


Figure 14: Reflow of annular-shaped fluidic microbump.

process by minimizing energy including surface tension, gravity, etc. [53].

Two different geometries including squared-shaped and annular-shaped fluidic microbumps are simulated. For the square-shaped fluidic microbump, the surface is not flat after solder reflow, as shown in Figure 13. The solder aggregates at the four corners in the case where solder thickness is 10 μm, which is similar to the "balling" effect reported in [54]; when increasing the solder thickness to 20 μm , the "balling" effect no longer exists, but there is still surface fluctuation, especially at corners. Moreover, increasing the thickness makes the photoresist mold patterning more difficult due to larger aspect ratio (thickness to width). With annular-shaped fluidic microbumps,

as shown in Figure 14, we can get a perfect surface for different solder thicknesses. In addition, with circular fluidic vias, annular-shaped fluidic microbumps reduce chip area requirement. Thus annular-shaped fluidic microbumps are adopted in this work.

2.2.2 Height Uniformity of Electrical and Fluidic Microbumps

Electrical and fluidic microbumps are simultaneously assembled to achieve electrical and fluidic interconnections, respectively. Thus, the height uniformity of electrical and fluidic microbumps is critical to the success of assembly. A large height difference will cause either fluidic leakage or electrical opening, as shown in Figure 15.

Fluidic microbumps of different inner diameter and outer diameter were electroplated along with the electrical microbumps of 25 μm . The different combinations of inner and outer diameter lead to different microbump heights. The measured heights of the fluidic and electrical microbumps are listed in Table 1. The observations are: 1) The height increases along with the width (outer radius minus inner radius) of the fluidic microbump; and 2) the height of the fluidic microbump is close to the height of the electrical microbump when its width is close to the diameter of the electrical microbumps. Based on the measurement results, one constraint for the fluidic microbumps is that the width has to be close to the diameter of electrical microbumps to achieve height uniformity.

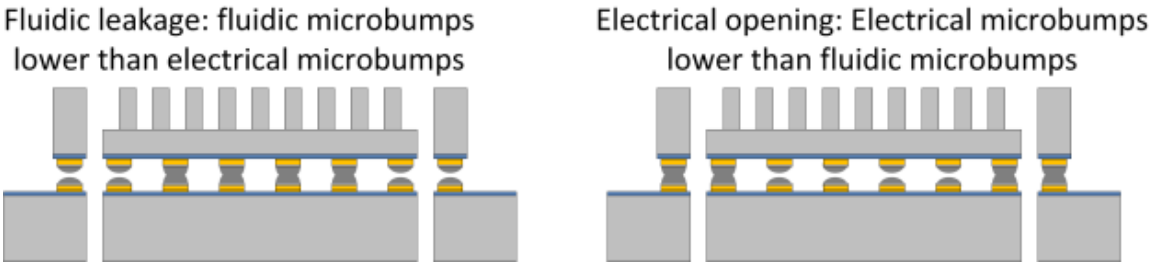


Figure 15: Height non-uniformity causing fluidic leakage or electrical opening.

Table 2: Measured height of the electrical and fluidic microbumps (Unit: μm)

Microbump	Inner diameter	Outer diameter	Width	Height
Fluidic #1	140	180	20	10.8
Fluidic #2	150	200	25	11.0
Fluidic #3	150	210	30	11.5
Fluidic #4	160	230	35	12.2
Fluidic #5	160	340	90	13.5
Fluidic #6	140	340	100	14.6
Electrical	0	25	25	12.2

2.2.3 Pressure Drop and Die Area Consumption of Fluidic Microbump and Via

The number and diameter of the fluidic vias determine the pressure drop within the vias and the die area consumption of the vias. Larger fluidic via helps reduce pressure drop but increases die area consumption, and vice versa. Thus, there is a trade-off between pressure drop and die area consumption when choosing fluidic via diameter. Pressure drop within a fluidic via is calculated using the following formulas [55].

$$\Delta p = \frac{V^2 \cdot f \cdot L \cdot \rho}{2D} \tag{1}$$

where Δp is pressure drop in Pascals, v is velocity in m/s, L is length of fluidic via in m, ρ is density of coolant in kg/m^3, D is diameter of fluidic via in m, and f is friction factor. If the fluidic flow is laminar, the friction factor is calculated by

$$f = \frac{64}{R_e} \tag{2}$$

where R_e is Reynolds Number, which can be calculated by

$$R_e = \frac{1000 \cdot v \cdot D}{\nu} \tag{3}$$

where ν is kinematic viscosity in centistokes.

Die area consumption of fluidic vias can be simply calculated by

$$P = \frac{A_{via} \cdot N}{A_{chip}} = \frac{\pi \cdot (\frac{D}{2})^2 \cdot N}{A_{chip}} \times 100\% \tag{4}$$

where P is percentage of fluidic via area,A_{via} is area of a fluidic via, N is number of fluidic vias, and A_{chip} is total die area.

For a fixed silicon die of 7.5 mm by 7.5 mm, fluidic microbump width of 25 μm, fluidic microbump spacing of 150 μm, fluidic via length of 200 μm, and coolant (de-ionized water) flow rate of 70 mL/min, the pressure drop and area consumption of the fluidic vias are calculated, as shown in Figure 16.

For a given flow rate, a smaller pressure drop is preferred. It not only improves reliability, but also saves pumping power. For the microfluidic heat sink of interest, it was reported that the pressure drop is approximately 40 kPa to 80 kPa for a flow rate between 45 mL/min and 70 mL/min [56]. Here, the pressure drop threshold of

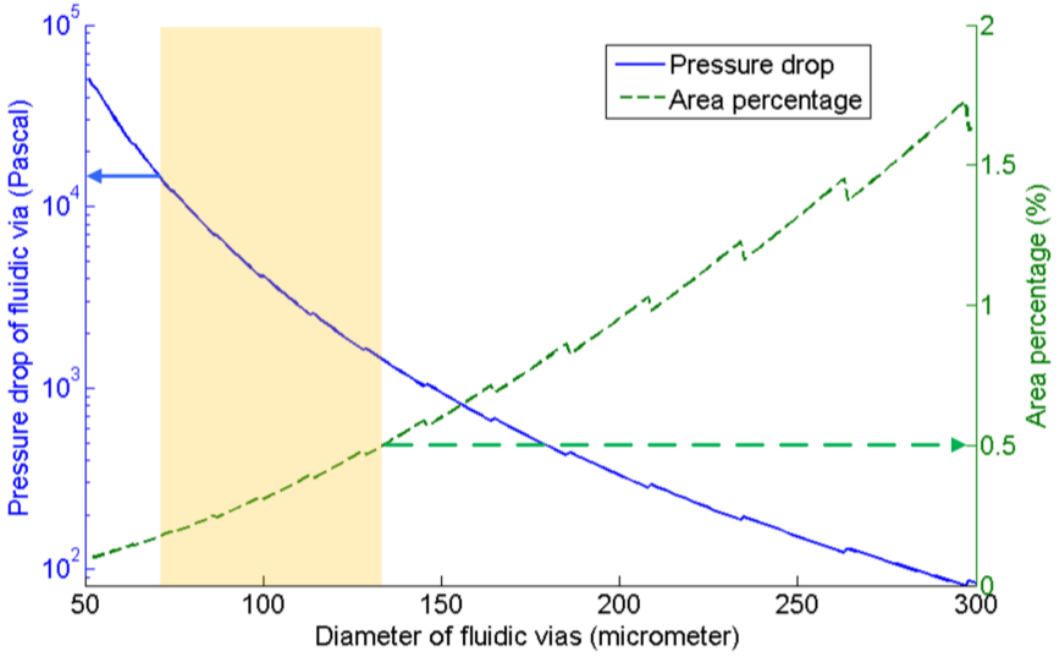


Figure 16: Pressure drop within fluidic vias and percentage die area of fluidic vias as a function of fluidic via diameter.

fluidic via is set to 15 kPa. Thus, the total pressure drop can be kept under 120 kPa. Regarding die area consumption, the threshold is set to 0.5% of total die area. With the pressure drop and die area consumption thresholds, we find the feasible fluidic via diameter range to be ∼70 and ∼130 μm , as shown by the shaded region in Figure 16.

The final diameter of the fluidic vias is 100 μm . The inner diameter of fluidic microbumps should be equal to or larger than the diameter of fluidic vias. Moreover, in order to avoid solder clogging and compensate for flip-chip assembly alignment errors, 25 μm spacing is kept between the fluidic microbump and the fluidic via. Thus, the final inner diameter and outer diameter of the fluidic microbumps are 150 μm and 210 μm, respectively. Figure 17 compares the size of the electrical and fluidic microbumps and fluidic via. Table 2 lists the final dimensions of the electrical microbump, fluidic microbump, and fluidic via.

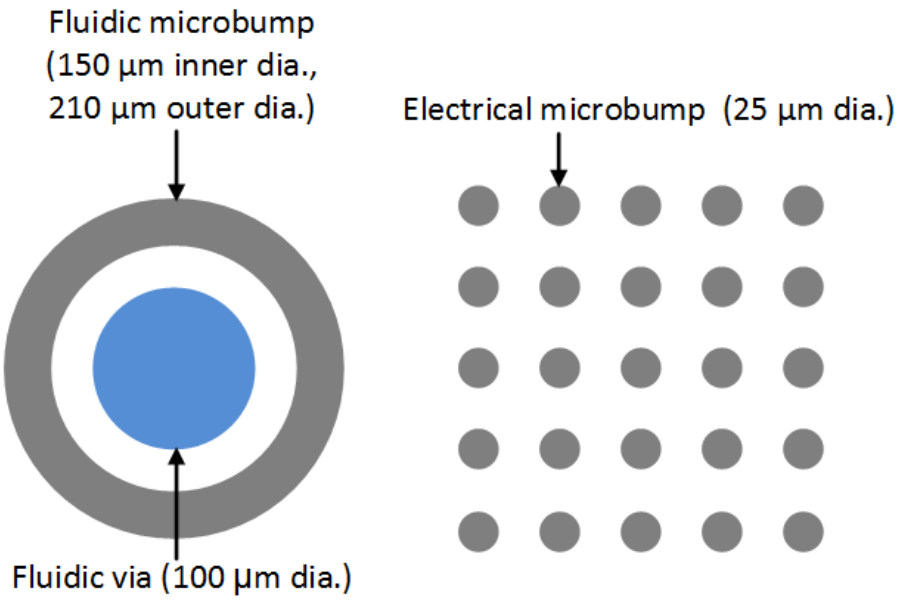


Figure 17: Size comparison of the electrical and fluidic microbumps.

Table 3: Final dimensions of electrical microbump, fluidic microbump and fluidic via (Unit: μm)

	Electrical microbump	Fluidic microbump	Fluidic via
Diameter	25	150 (inner dia.) 210 (outer dia.)	100
Pitch	50	372.5	372.5

2.3 Fabrication of Silicon Die with Electrical and Fluidic I/Os and Microfluidic Heat Sink

Silicon dice and interposers with the electrical and fluidic microbumps were fabricated. Moreover, staggered micropin-fin heat sink was integrated into the silicon dice [57]. The fabrication process is described in this section.

2.3.1 Fabrication of Electrical and Fluidic Microbumps

Wafer-level simultaneous fabrication of electrical and fluidic microbumps is illustrated in Figure 18. The fabrication process for silicon die starts with a double-side polished 4-inch wafer. First, a 3 μm SiO_2 film is deposited. Next, a seed layer is sputtered on the SiO_2 film. The seed layer consists of a titanium (300 Å) film and a copper (2000 Å) film. The Ti film improves the adhesion of the copper film to the SiO_2 layer. The next step is to pattern the fine pitch wires (8 μm width) and copper pads for the electrical and fluidic microbumps. Circular- and annular-shaped pads are patterned for the electrical and fluidic microbumps, respectively. Wires and pads are electroplated in a copper plating solution. After copper electroplating, a thick resist mold is patterned for the copper pads, to electroplate Ni on the copper pads as under bump metalization (UBM). Eutectic solder (60%/40% tin-lead) is plated on the Ni layer. Following electroplating, seed layer is removed. The last step is to reflow the solder with flux. The same process is used for silicon substrate/interposer fabrication.

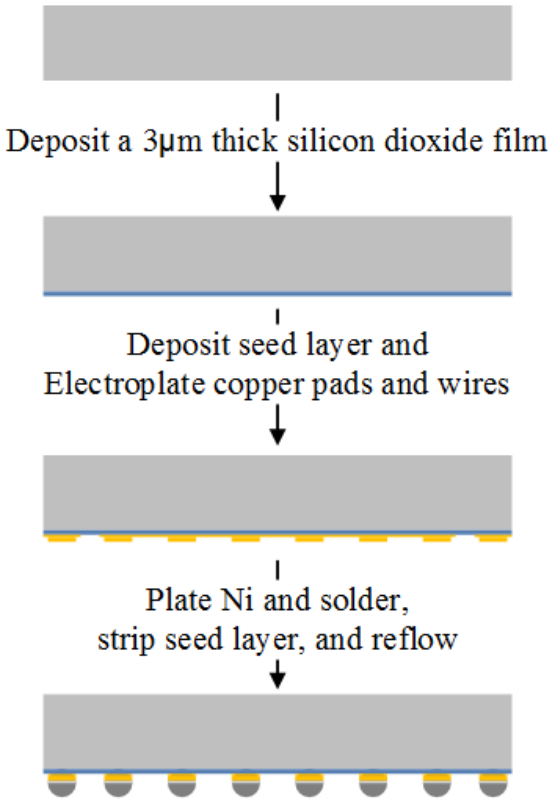


Figure 18: Fabrication process of electrical and fluidic microbumps.

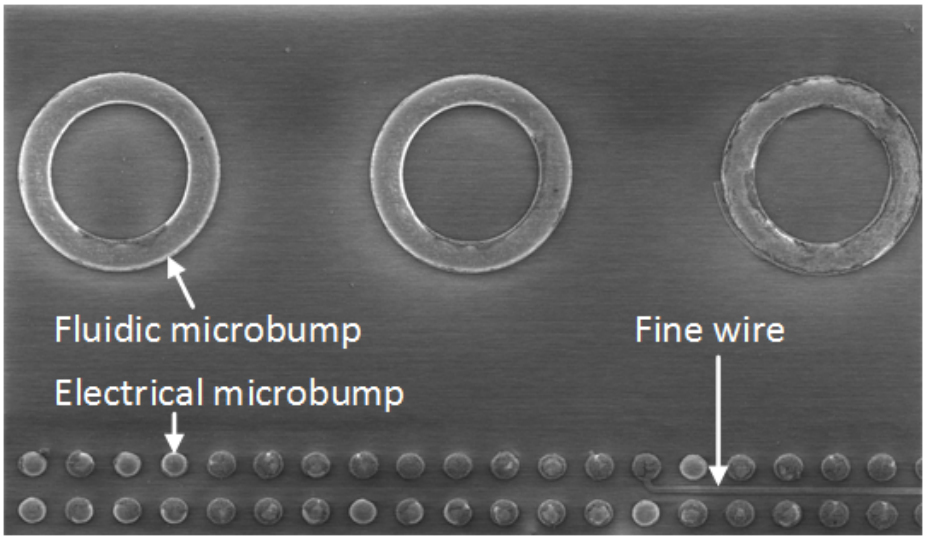


Figure 19: SEM image of fabricated electrical and fluidic microbumps.

Figure 19 shows the SEM image of the fabricated electrical and fluidic microbumps. Some flux residual was left around the microbumps. Fine-pitch wires are routed in the electrical microbump array to connect microbumps for electrical testing, which will be discussed later.

2.3.2 Integration of Microfluidic Heat Sink with Fluidic I/Os

Microfluidic heat sink is embedded into the back side of a silicon die for cooling purpose. Figure 20 shows the SEM image of the embedded micropin-fin heat sink. The micropin-fins of 150 μm diameter, 225 μm pitch, and 200 μm height are directly etched on the back side of a silicon die. The placement and dimensions of the staggered micropin-fins are based on a previous study [58]. We have previously demonstrated

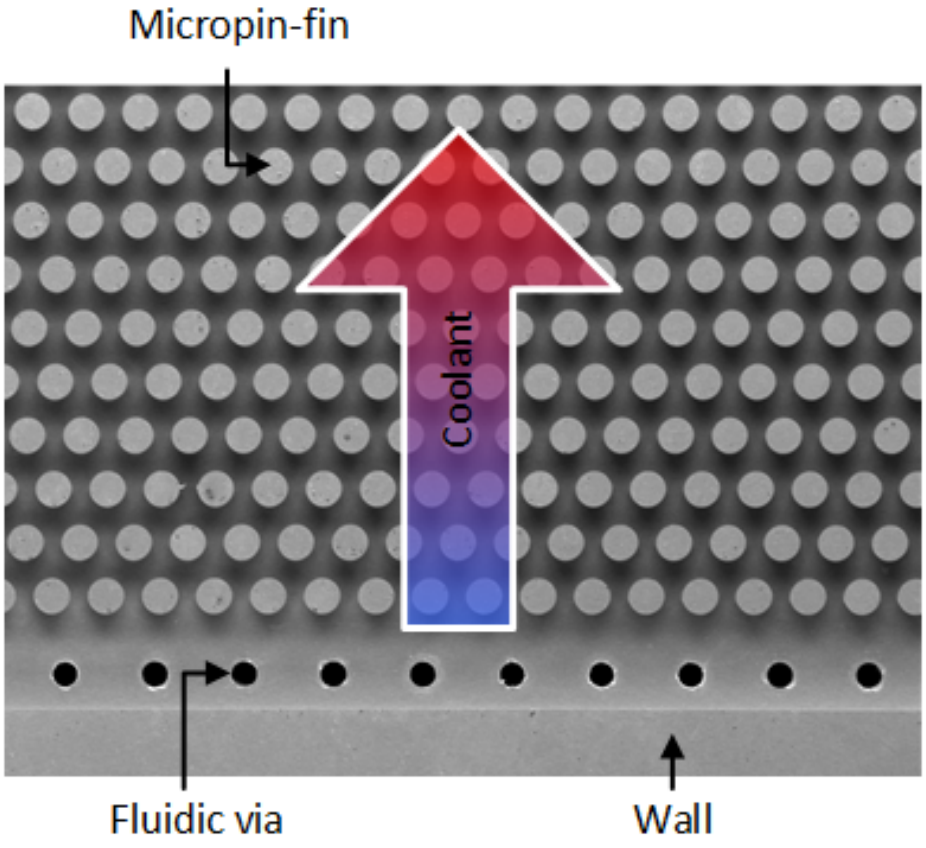


Figure 20: SEM image of staggered micropin-fin heat sink.

this silicon micropin-fin heat sink dissipating 103.4 W/cm^2 at a junction temperature of 47.9 °C using a flow rate of 70 mL/min [59].

Following the development of a fabrication process for electrical and fluidic microbumps, the fabrication process for fluidic via and staggered pin-fin heat sink is developed and integrated with the microbump process, as shown in Figure 21.

The fabrication process is briefly described as follows: A layer of SiO_2 is deposited on the front side of a 300 μm thick 4-inch wafer as a dielectric layer. Following this process step, the micropin-fin heat sink and fluidic vias are etched on the back side of the wafer using two BOSCH etch steps. In the first etching step, the fluidic vias are half way etched to approximately 100 μm depth; the fluidic vias are etched through and the micropin-fin heat sink is etched simultaneously in the second etching step. Next, a seed layer (Ti/Cu) is deposited on the front side for the electroplating of fine-pitch wires (8 m width, 2 m thick) and the copper pads for the electrical and fluidic microbumps. Next, Ni and solder are electroplated on the copper pads to form the electrical and fluidic microbumps. Following the electroplating step, the seed layer is stripped, the SiO_2 film hanging over the fluidic vias is opened using ultrasonic bath, and the microbumps are reflowed. The silicon interposers are fabricated using a similar process except that only fluidic vias are required with one BOSCH etch step.

The fabricated silicon die and interposer were inspected using both an optical microscope and a scanning electron microscope (SEM). Figure 22 displays the optical images of the whole silicon die and interposer with high-density electrical microbump array (150 150 = 22,500 microbumps), two rows of fluidic microbumps (21 fluidic microbumps per row), and fine-pitch wires (8 μm width). The size of the silicon die is 1 cm $\times$ 1 cm. Figure 23 displays the SEM images of the fabricated structures. Figure 23(a) shows the fluidic vias and micropin-fins on the back side of the silicon die. Figure 23(b) shows the the electrical microbumps, fluidic microbumps, fluidic vias and fine-pitch wires on the front side. Figure 23(c) shows the close-up of electrical microbumps

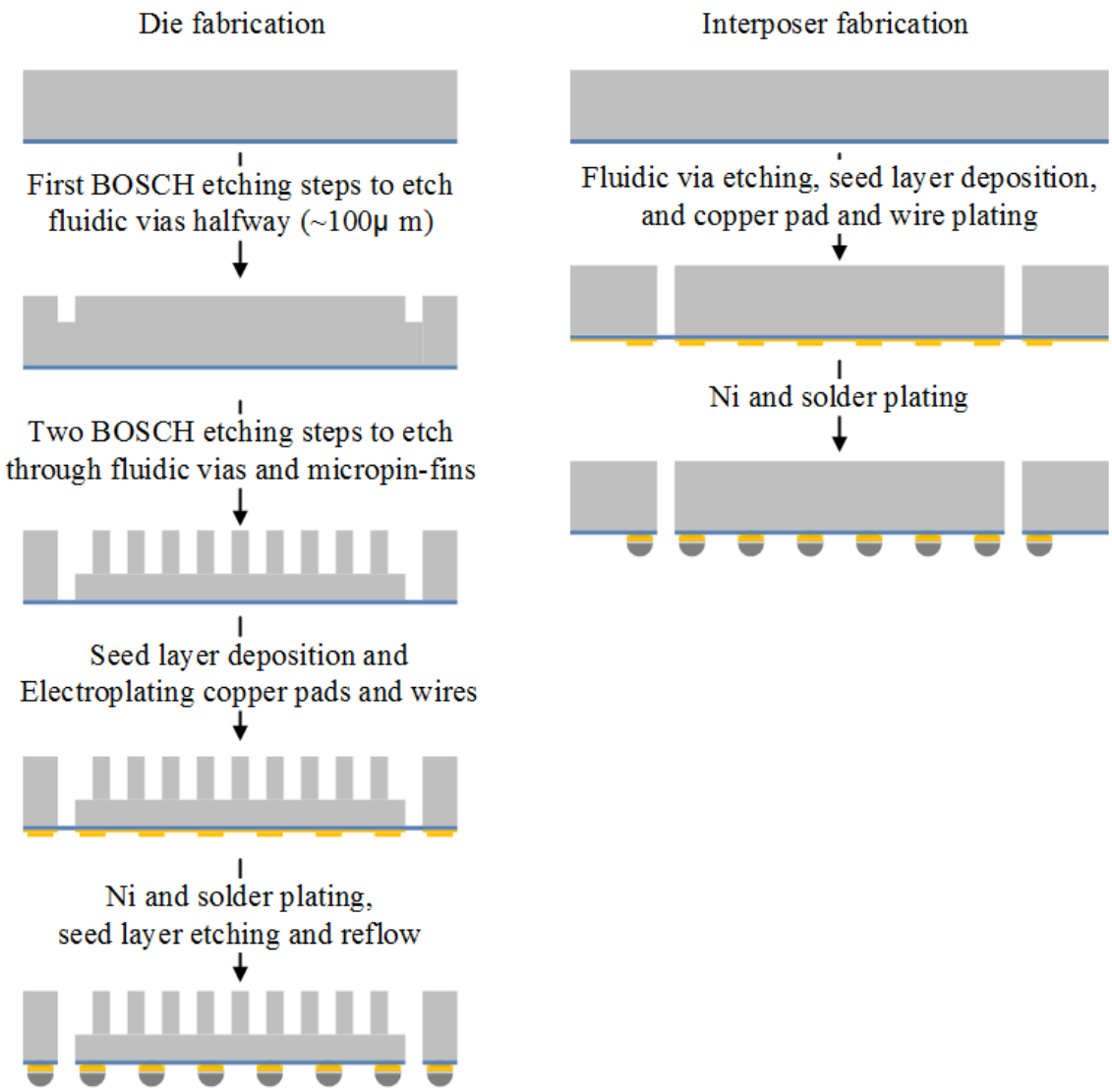


Figure 21: Fabrication process for silicon die and interposer with electrical and fluidic I/Os and microfluidic heat sink.

and fine-pitch wires. Figure 23(d) is the close-up of the fluidic microbump and via. Figure 24 shows the optical images of the electrical microbumps, fluidic microbumps and vias, fine-pitch wires, and micropin-fins.

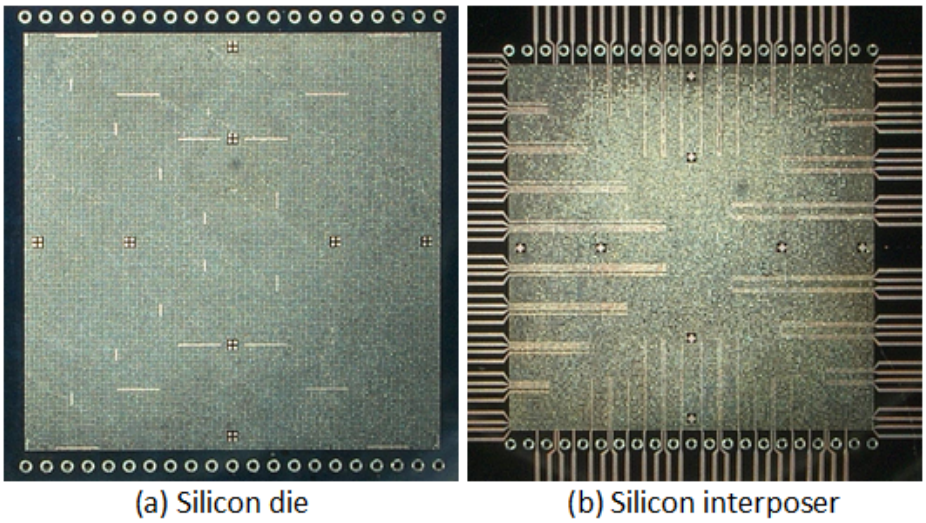


Figure 22: Optical images of (a) the fabricated silicon die and (b) silicon interposer.

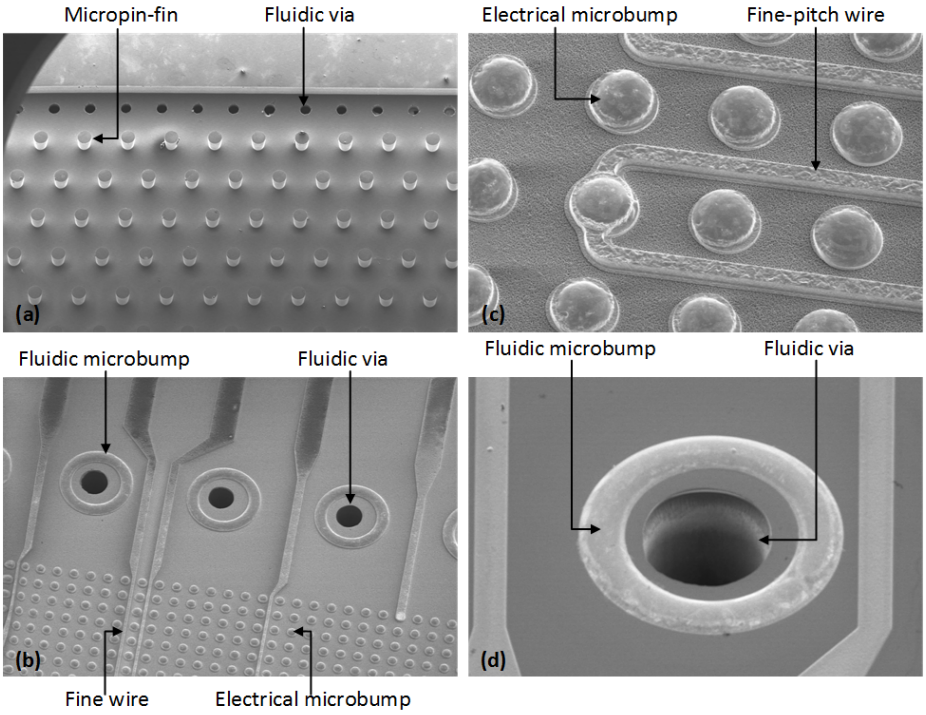
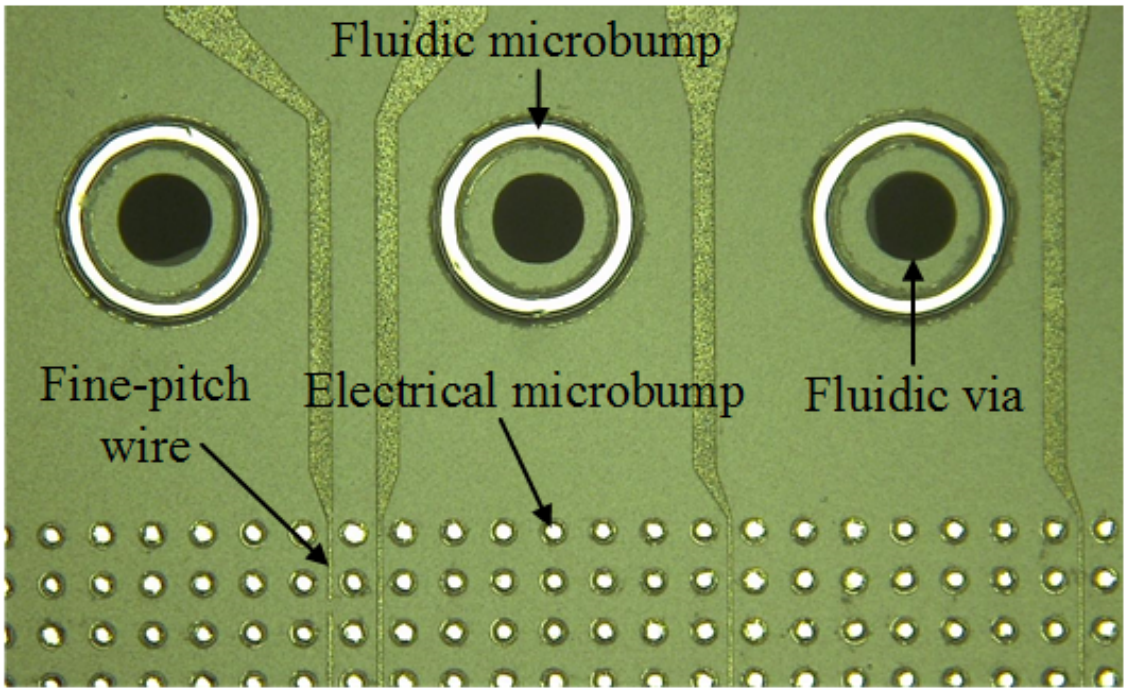
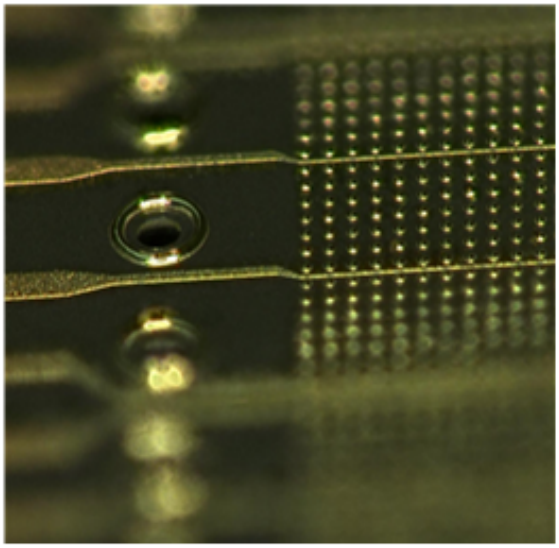


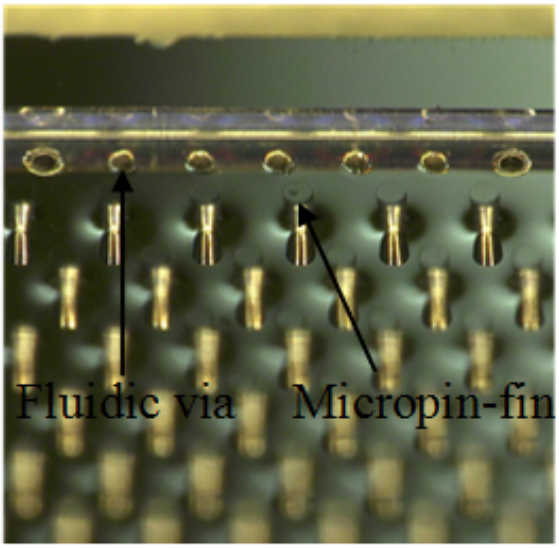
Figure 23: SEM images of (a) micropin-fins and fluidic vias on the back side of the die; (b) Electrical and fluidic microbumps, fluidic vias and fine-pitch wires; (c) close-up of electrical microbumps and fine-pitch wires; (d) close-up of a fluidic microbump and a fluidic via.



(a) Electrical and fluidic microbumps, fluidic via and fine-pitch wires



(b) Fluidic microbump and via



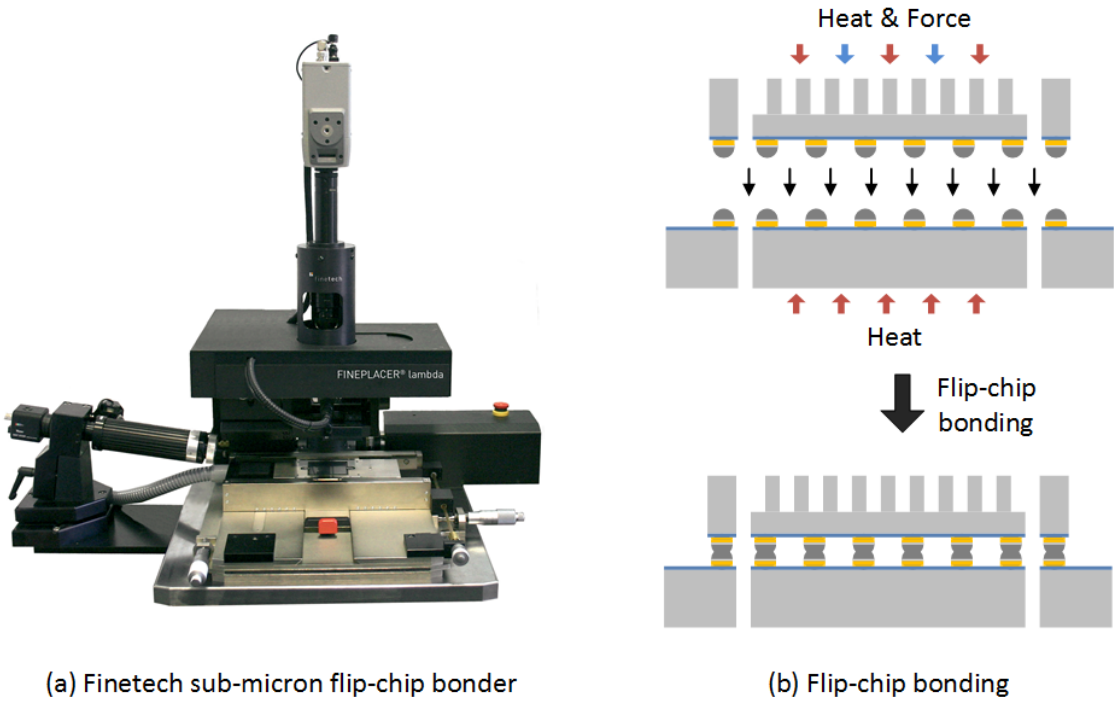
(c) Fluidic via and micropin-fin

Figure 24: (a) Close-up of the electrical microbumps, fluidic microbumps, fluidic vias and fine-pitch wires; (b) angled view of fluidic microbump and via; (c) angled view of fluidic via and micropin-fins on the back side of the die.

2.4 Assembly of Silicon Die with Electrical and Fluidic Microbumps and Micropin-fin Heat Sink

Following fabrication, the silicon die is assembled on the silicon interposer using a Finetech flip-chip bonder which provides sub-micron alignment accuracy, temperature profiles for both die and substrate, and bonding force during the process. Figure 25(a) shows the flip-chip bonder, and Figure 25(b) illustrates the flip-chip bonding process.

In the flip-chip bonding process, the chip holder of the bonder picks up the silicon die by applying vacuum on the back side of the die, as shown in Figure 26(a)(b).The silicon die is aligned to the interposer by using the overlay vision alignment system (VAS) with fixed beam splitter and adjusting the position and angle of the silicon interposer. After aligning the silicon die and interposer and applying flux on the interposer, the silicon die is brought down into contact with the silicon interposer, as shown in Figure 26(c)(d). When the bonding process begins, heat is applied to both



(a) Finetech sub-micron flip-chip bonder (b) Flip-chip bonding

Figure 25: (a) Flip-chip bonder; (b) flip-chip bonding of the silicon die with electrical and fluidic microbumps on a silicon inteposer.

the silicon die and interposer and bonding force is applied on the die.

Figure 27 shows the images captured using the overlay vision alignment system with fixed beam splitter on the flip-chip bonder. Figure 27(a) and (b) are the images of the silicon die and interposer, respectively. Figure 27(c) is the overlay image of the aligned silicon die and interposer from which we can see the copper wires on both

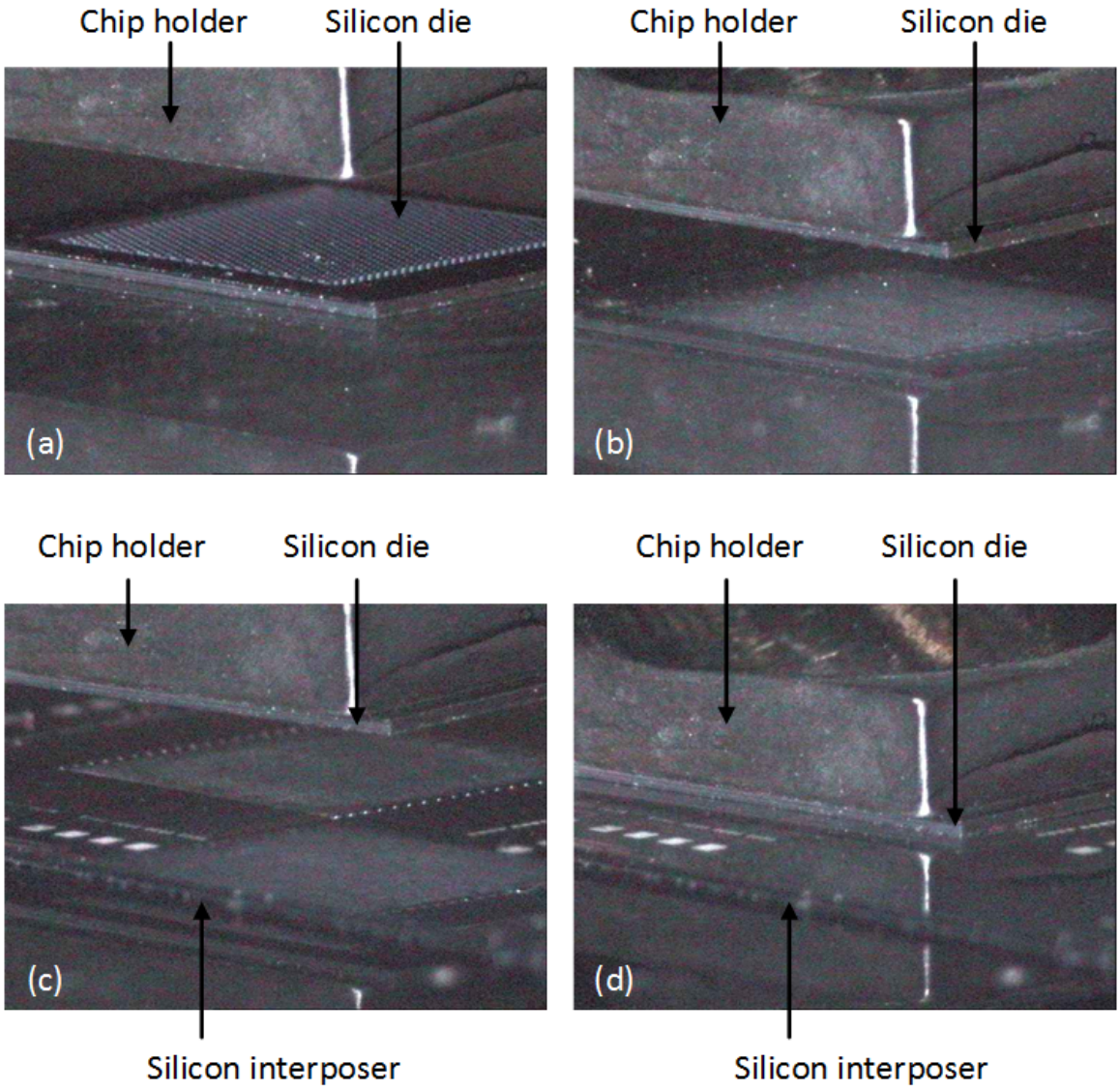


Figure 26: (a) chip holder and silicon die; (b) chip holder picking up the silicon die; (c) aligning the silicon interposer to the silicon die; (d) bringing silicon die in contact with silicon interposer.

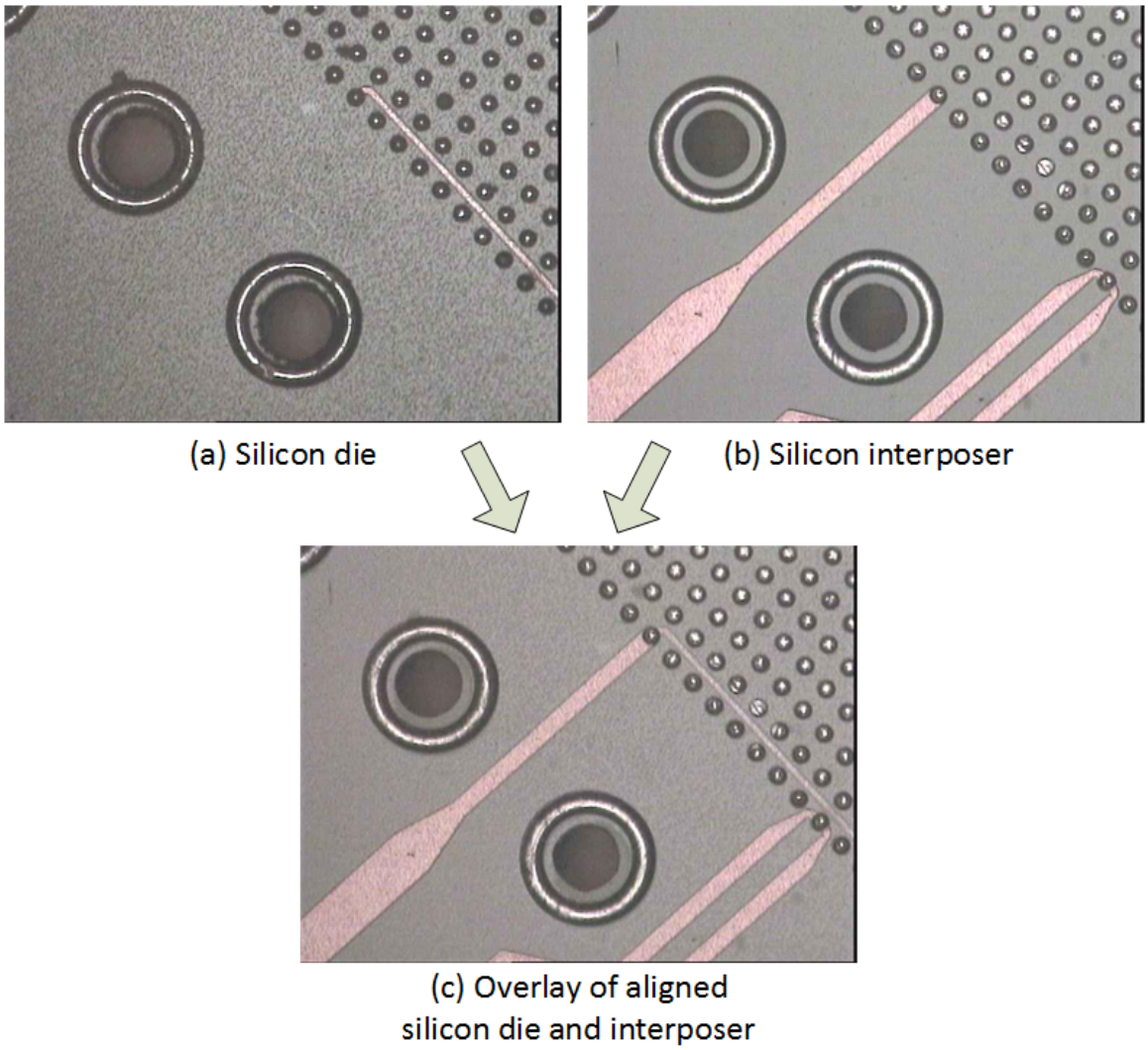


Figure 27: (a) silicon die image; (b) silicon interposer image; (c) over-lay of silicon die and interposer.

silicon die and interposer. Table 3 lists the die and bonding parameters. The peak temperature of 230 °C lasts for 15 s, and the bonding force is 7 N.

Following flip-chip bonding, an X-ray imager was used to inspect the bonded sample, as shown in Figure 28. From the X-ray image, we can clearly see the bonded electrical and fluidic microbumps, fluidic vias, fine-pitch wires, and micropin-fins. More importantly, the electrical and fluidic microbumps are well aligned.

Table 4: Silicon die and bonding parameters

Parameter	Value
Die size	1 cm × 1 cm
Number of fluidic microbumps	42 (21 each row)
Number of electrical microbumps	22,500 (150 ×) 150
Temperature ramp rate	2 °C/s
Peak temperature	230 °C
Peak temperature duration	15 s
Bonding force	7 N

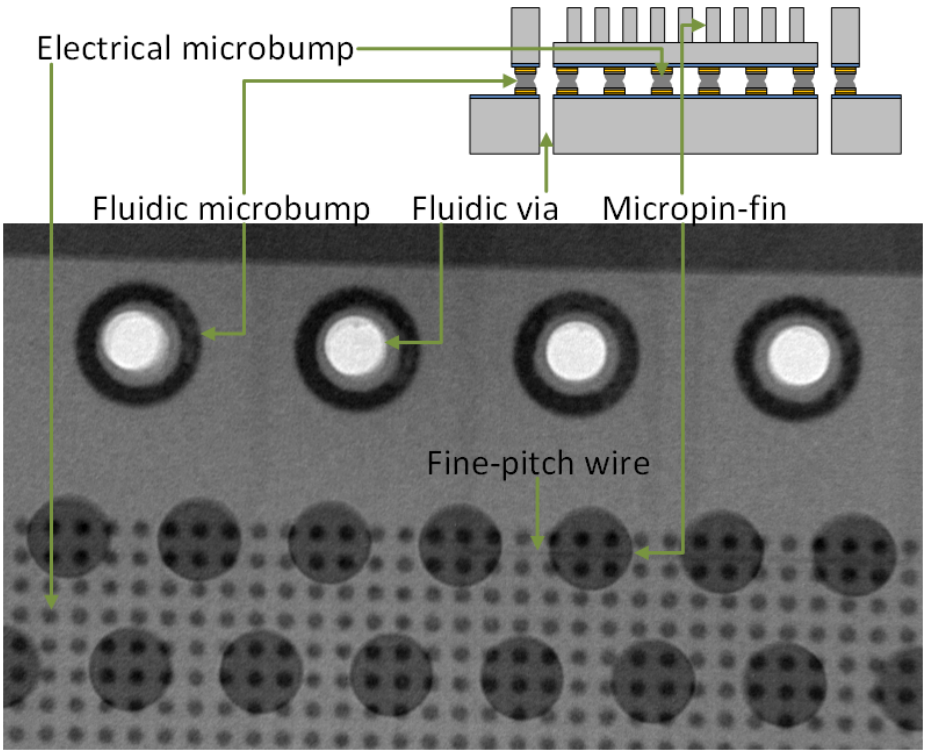


Figure 28: X-ray image of the bonded silicon die and interposer (top view).

2.5 Testing of Electrical and Fluidic Microbumps

Electrical and fluidic testing were conducted to verify the bonding of the electrical and fluidic microbumps, respectively. The testing details and results are described in this section.

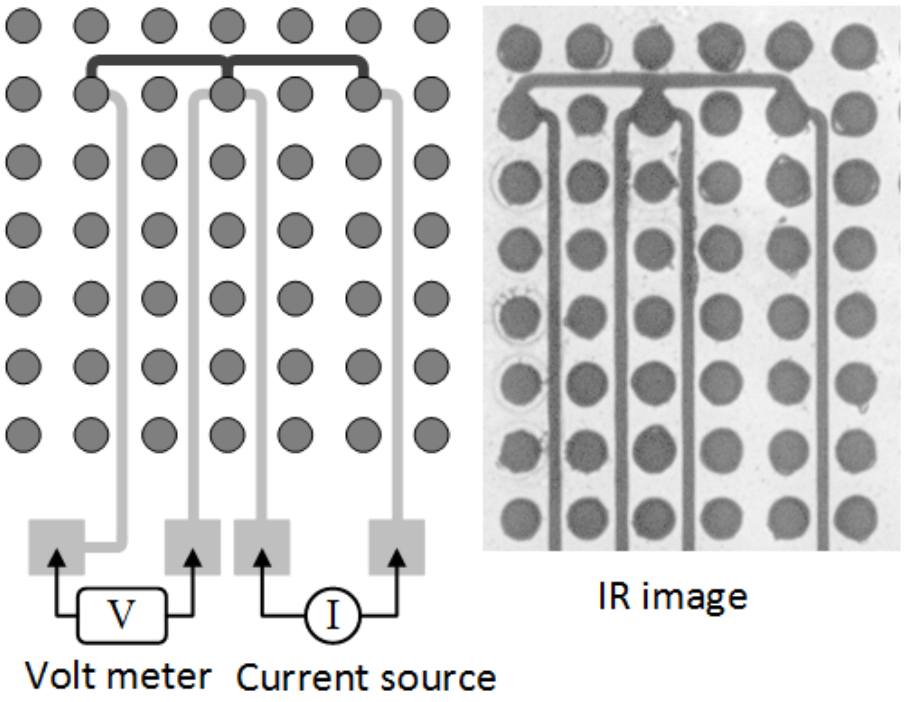


Figure 29: Four point resistance measurement structure: (a) illustration, and (b) IR image of the measurement structure.

2.5.1 Electrical Testing

Following assembly, the resistance of the electrical solder joints were measured using the 4-point resistance measurement technique. The fine-pitch wires on the die and interposer are used to form the 4-point measurement structure, as shown in Figure 29. Three electrical microbumps were connected using the wires. The middle one is the target microbump and the other two are used to form the connections. In Figure 29(a), the light-colored wires are on the interposer, and the dark-colored wires are on the die. While the current is injected to the target microbump, the voltage drop across the microbump is measured to determine the resistance. Figure 29(b) is the IR image of the 4-point measurement structure on the sample.

Measurements were conducted on three bonded samples. Figure 30 illustrates the measurement results. The average resistance of eight measured microbumps is 13.5

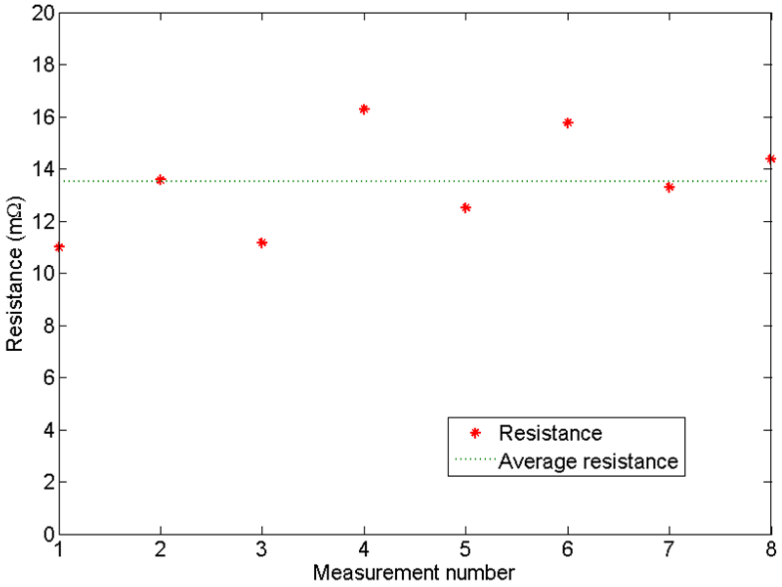


Figure 30: Resistance of a single electrical microbump.

mΩ ± 1.82 mΩ. This result is consistent with the results reported in [35] demonstrating proper bonding.

2.5.2 Fluidic Testing

Upon completion of the resistance measurement, a glass slide was used to seal the micropin-fin heat sink, and inlet/outlet ports and tubes were attached to the back

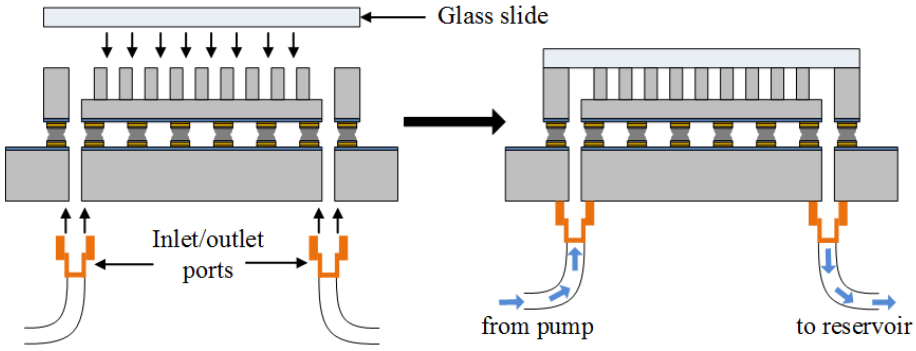


Figure 31: Capping the micropin-fin heat sink and attaching inlet/outlet ports and tubes.

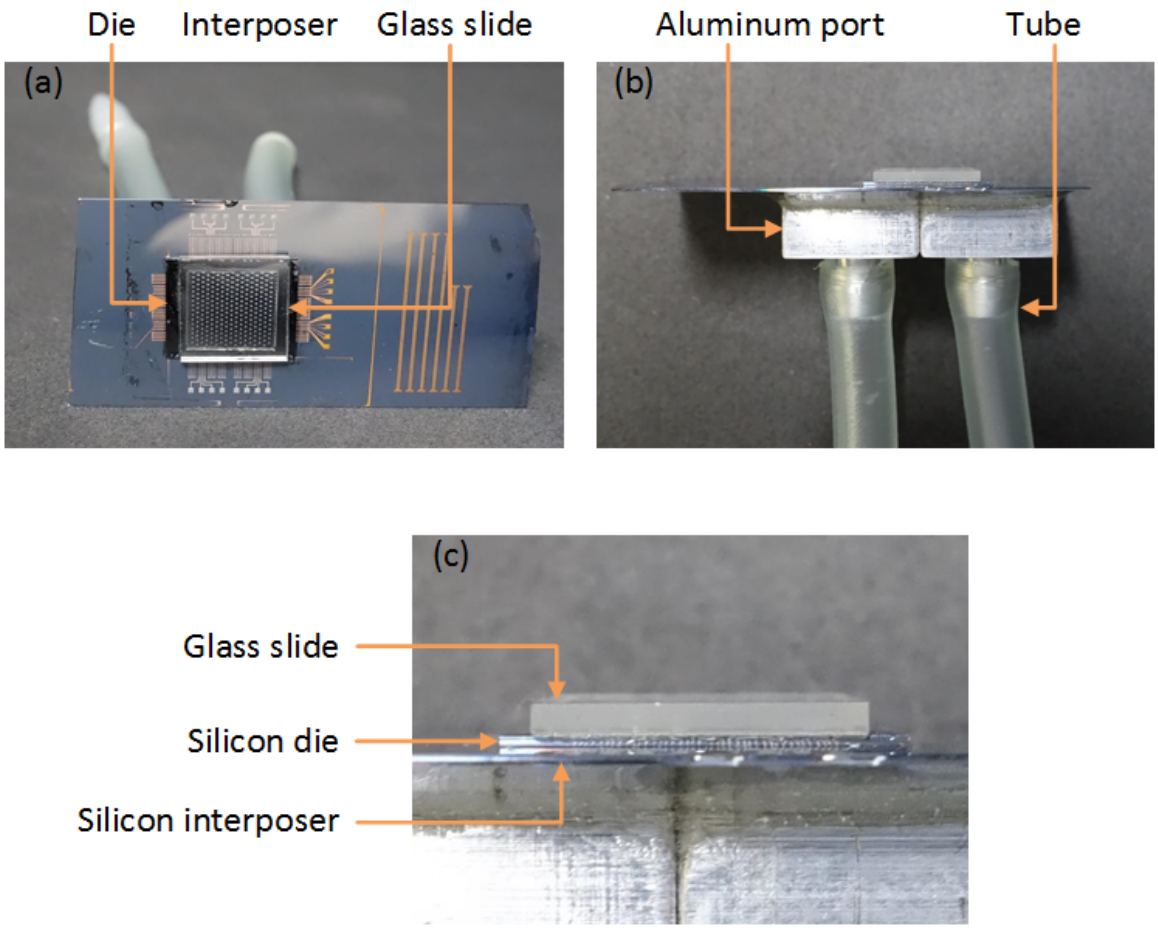


Figure 32: Assembled sample for fluidic testing: (a) top view of the glass slide, silicon die, and interposer, (b) side view of the assembled sample, and (c) zoomed in view of glass slide, silicon die, and interposer.

side of the interposer to facilitate fluidic testing, as shown in Figure 31. Figure 32(a) shows the the top view of the assembled sample for fluidic testing. Figure 32(b) is the side view of the sample with input/output ports and tubes attached to the back side of the interposer. Figure 32(c) shows the zoomed in view of the glass slide, silicon die, and silicon interposer.

During fluidic testing, DI water was pumped into the die, and the flow rate and pressure drop between the inlet and outlet ports (atmospheric pressure at outlet port) were recorded in real time. As expected, the pressure drop increases as flow rate increases, as shown in Figure 33.

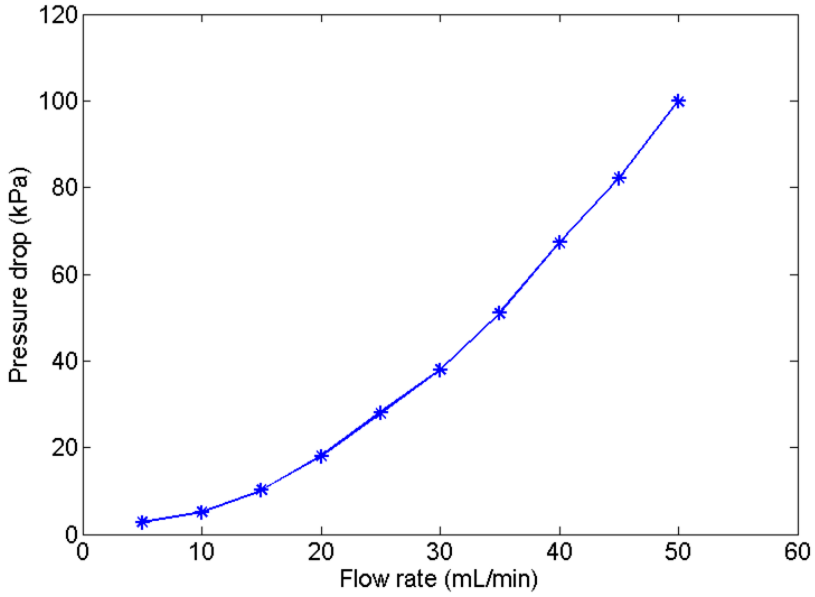


Figure 33: Measured pressure drop as a function of flow rate.

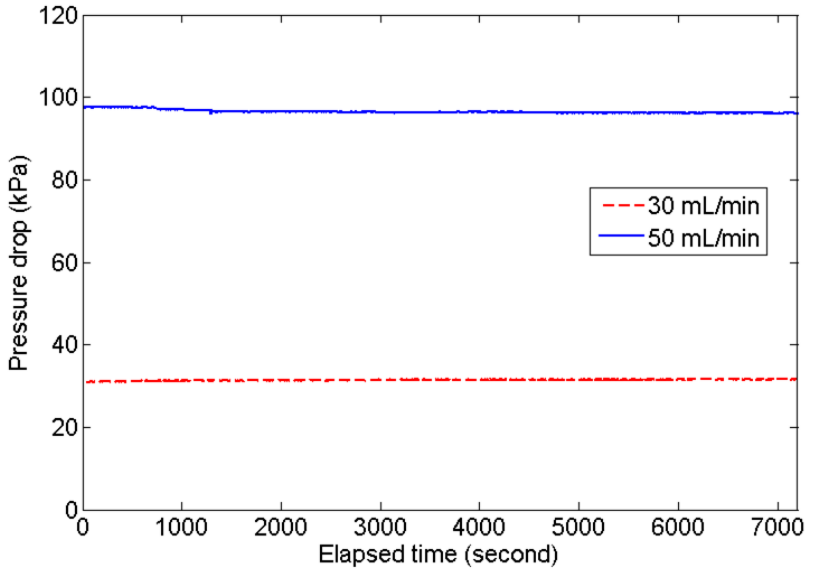


Figure 34: Fluidic testing (continuous pumping DI water for four hours, at flow rates of 30mL/min and 50ml/min).

To test the preliminary reliability and sealing quality of the fluidic microbumps, DI water was pumped into the die continuously for four hours at flow rates of 30 mL/min and 50 mL/min. No leakage was observed during testing. Figure 34 illustrates the real-time pressure drop during the four-hour fluidic testing. The pressure drop is quite stable indicating no leakage occurred during the test, which was also consistent with visual inspection.

2.6 3-D Stacking of Electrical and Fluidic I/Os

3-D integration is critical to future high-performance computing systems. In this section, the 3-D integrated microfluidic cooled silicon dice with electrical and fluidic I/Os are presented.

2.6.1 3-D Testbed Design

In this effort, two silicon dice with fine-pitch electrical and fluidic I/Os are stacked on a silicon interposer, as illustrated in Figure 35. The micropin-fin heat sink and electrical through silicon vias (TSVs) are not included in the lower die (Die #2) in order to simply the fabrication of the 3-D testbed. The micropin-fin heat sink with integrated TSVs has been demonstrated in [60], [61], as shown in Figure 36.

Figure 37 shows the layout of the lower die (Die #1), upper die (#2), and silicon

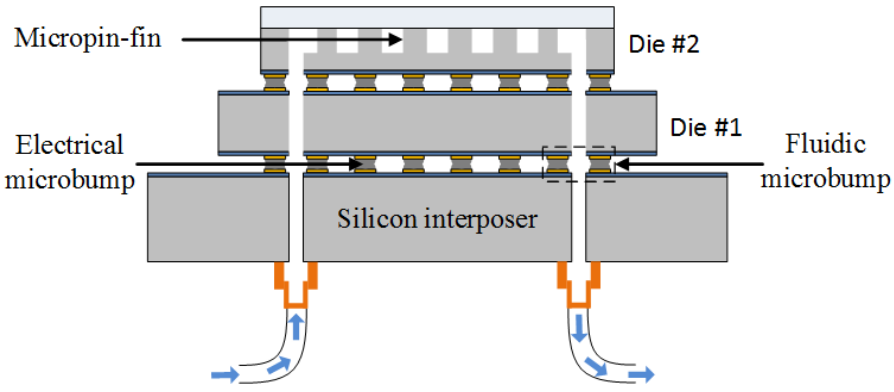


Figure 35: 3-D stack with electrical and fluidic I/Os.

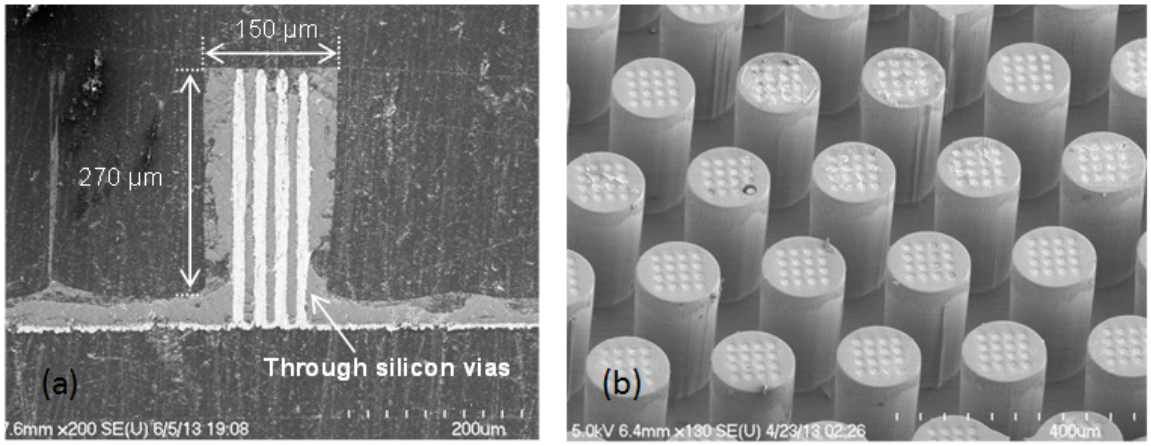


Figure 36: (a) Cross-section of the TSV array in a micropin-fin, and (b) array of micropin-fins with integrated TSVs.

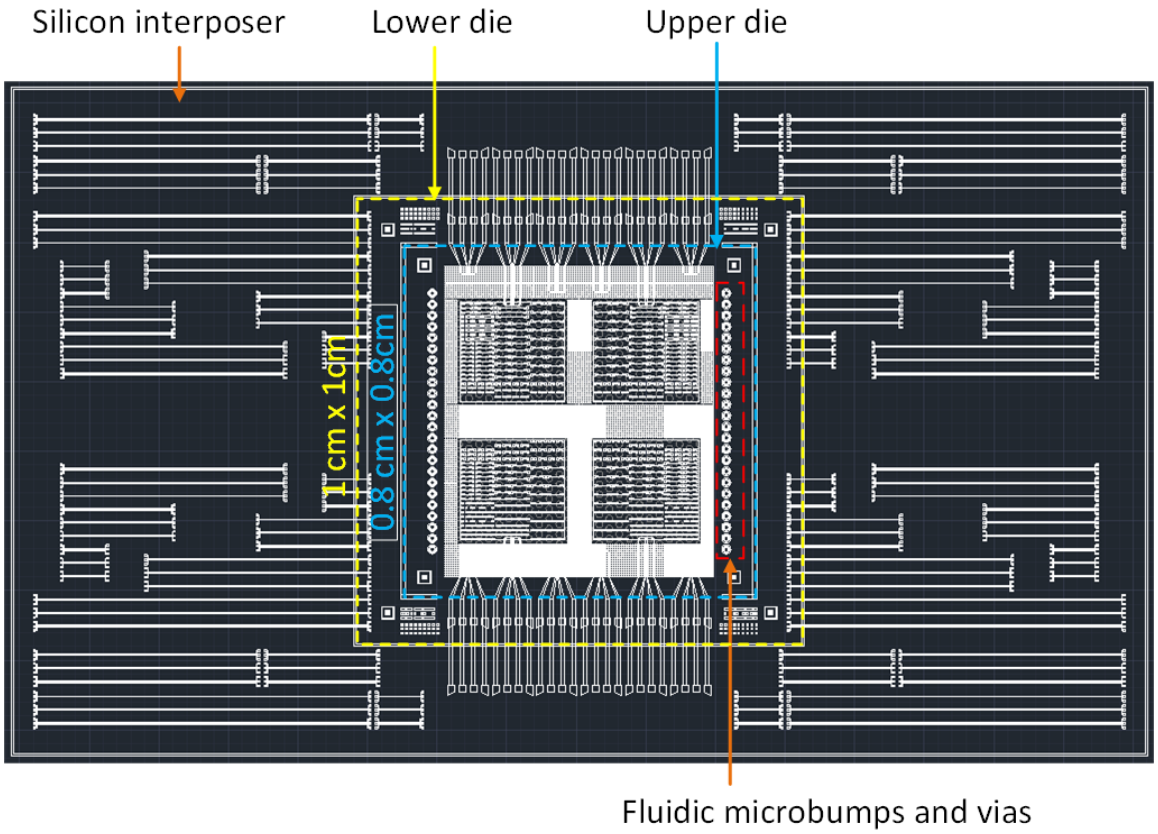


Figure 37: Layout of the two stacked silicon dice and interposer.

interposer. The size of Die #1 and Die #2 is approximately 1 cm × 1 cm and 0.8 cm × 0.8 cm, respectively. The lower die is slightly larger to allow for probing pads at the edges for electrical testing. Table 4 lists the design parameters of Die #1, Die #2, and the silicon interposer.

2.6.2 Fabrication and Assembly

The fabrication processes for Die #2 and the silicon interposer are the same as described in Section 2.3.2. The major challenge is the fabrication of Die #1 which requires processes on both sides of the die. Figure 38 illustrates the fabrication process for Die #1. The process begins with a 300 μm thick 4-inch wafer with a thin layer of SiO_2 deposited on the front side. Fluidic vias are etched through from the back side using the BOSCH process followed by an SiO_2 deposition step. Next, a thin layer of Ti/Cu/Au is evaporated on both sides of the wafer to form the wires and pads using the lift-off process. The Au layer is used to prevent oxidation which would affect bonding process. The last step is to remove the SiO_2 membrane hanging over the fluidic vias in an ultrasonic bath. The silicon die and interposer parameters are listed in Table 4.

Following fabrication, the two silicon dice are stacked on the silicon interposer sequentially in two bonding steps, as shown in Figure 39. The same Finetech flip-chip bonder presented in Section 2.4 was used for the 3-D stack assembly. The bonding

Table 5: Silicon die and interposer parameters

Parameter	Value
Die #1 size	∼1 cm × 1 cm
Die #1 size	∼0.8 cm × 0.8 cm
Interposer size	∼1.5 cm × 2.5 cm
Number of fluidic microbumps	48 (24 each row)
Number of electrical microbumps	∼7600

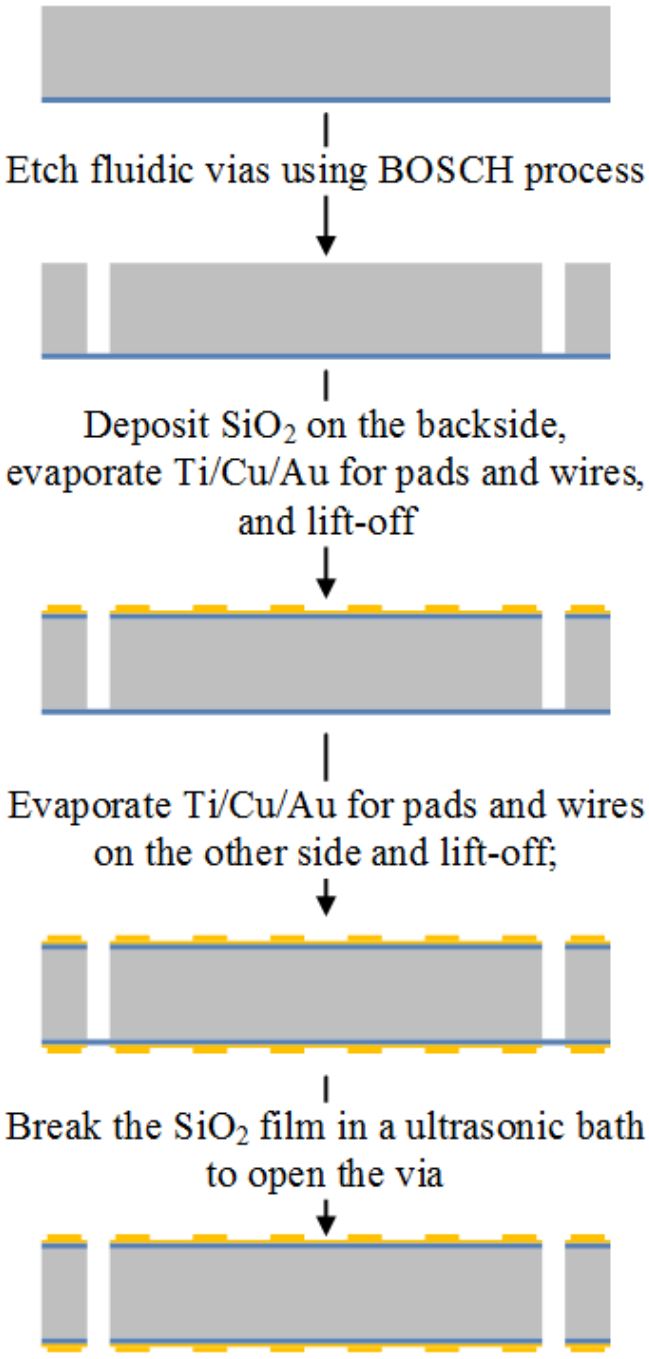


Figure 38: Fabrication process of the middle die in the stack (Die #1).

parameters are listed in Table 5.

Figure 40 shows the optical image of the assembled 3-D stack. The assembled 3-D stack was also inspected using an X-ray imager. Figure 41(a) and (b) show the top and angled view of the 3-D stack from which the two silicon dice and interposer can

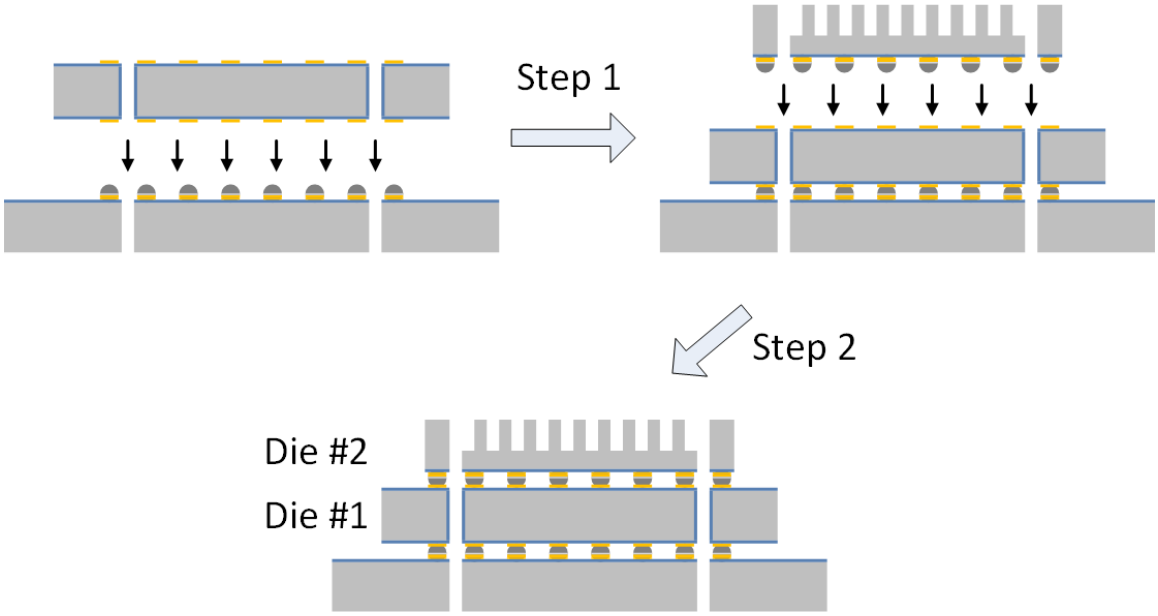


Figure 39: Flip-chip bonding process of the 3D stack.

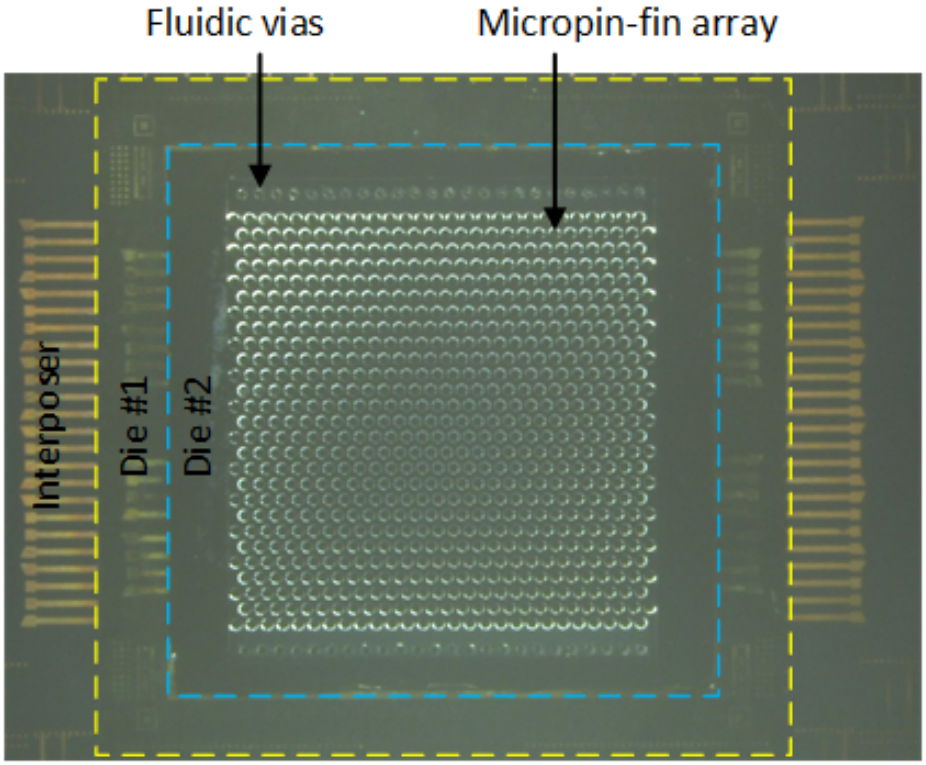


Figure 40: Optical image of the assembled 3-D stack .

Table 6: Flip-chip bonding parameters

Parameter	Step 1 (Die #1)	Step 2 (Die #2)
Temperature ramp rate	2 °C/s	2 °C/s
Peak temperature	230 °C	230 °C
Peak temperature time	15 s	15 s
Bonding force	3.5 N	4 N

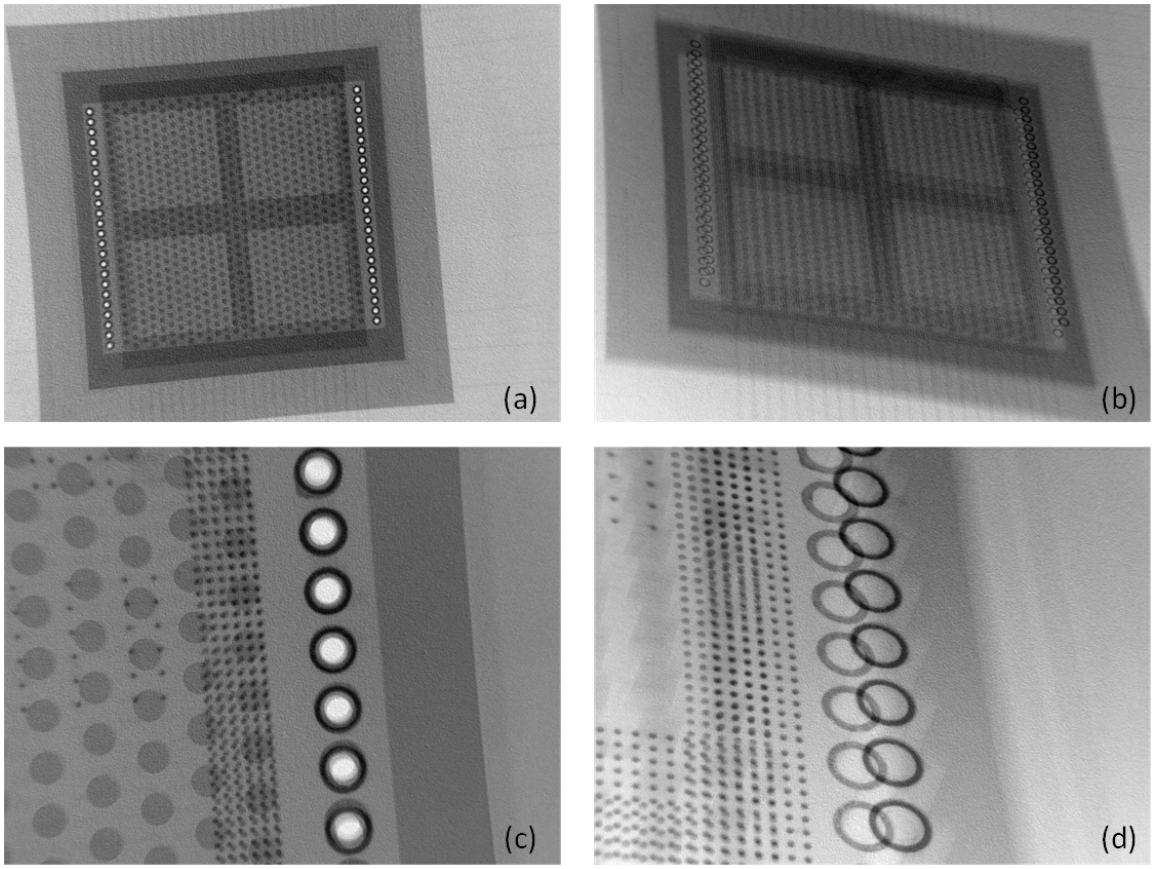


Figure 41: X-ray images of the 3-D stack with electrical and fluidic I/Os: (a) top view of the stack; (b) angled view of the stack; (c) top view of the fluidic I/Os; and (d) angled view of the fluidic I/Os on both tiers.

be clearly seen. Figure 41(c) shows the close-up of a column of fluidic I/Os. The small dots and large circles to the left of the fluidic I/Os are the electrical microbumps and micropin-fins, respectively. Figure 41(d) is the angled close-up in which we observe the fluidic I/Os on both silicon dice.

2.6.3 Electrical and Fluidic Testing

The resistance of the electrical microbumps on the two stacked dice was measured using the 4-point measurement technique. On each die, three microbumps were measured. Figure 42 shows the measurement results. The average resistance of the microbumps is 8.85 mΩ.

Next, the micropin-fin heat sink on Die #2 was capped with a glass slide and inlet and outlet ports were attached to the back side of the interposer for fluidic testing. Figure 43 shows the assembled testbed with glass side and input/output ports. During the fluidic testing, DI water was pumped into the testbed continuously and the pressure drop between inlet and outlet was recorded using the Omega transient pressure data logger (OM-CP-PRTRANS-1-30G) with a sampling frequency of 1 Hz.

During a 1.5 hour continuous testing, three different flow rates (10, 20, and 25 mL/min) were applied. The recorded pressure drop is shown in Figure 44. The testing started with the low flow rate and increased to higher flow rate in half an hour, the

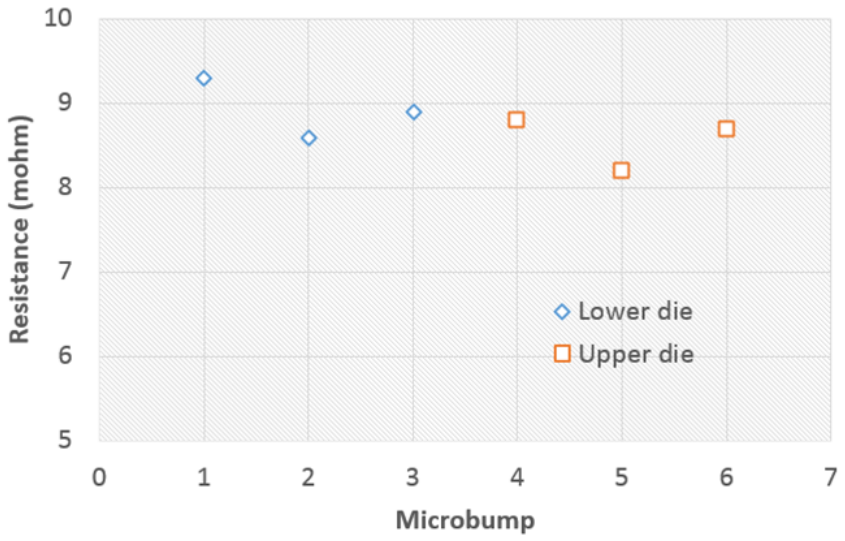


Figure 42: Measured resistance of the electrical microbumps on the two stacked dice.

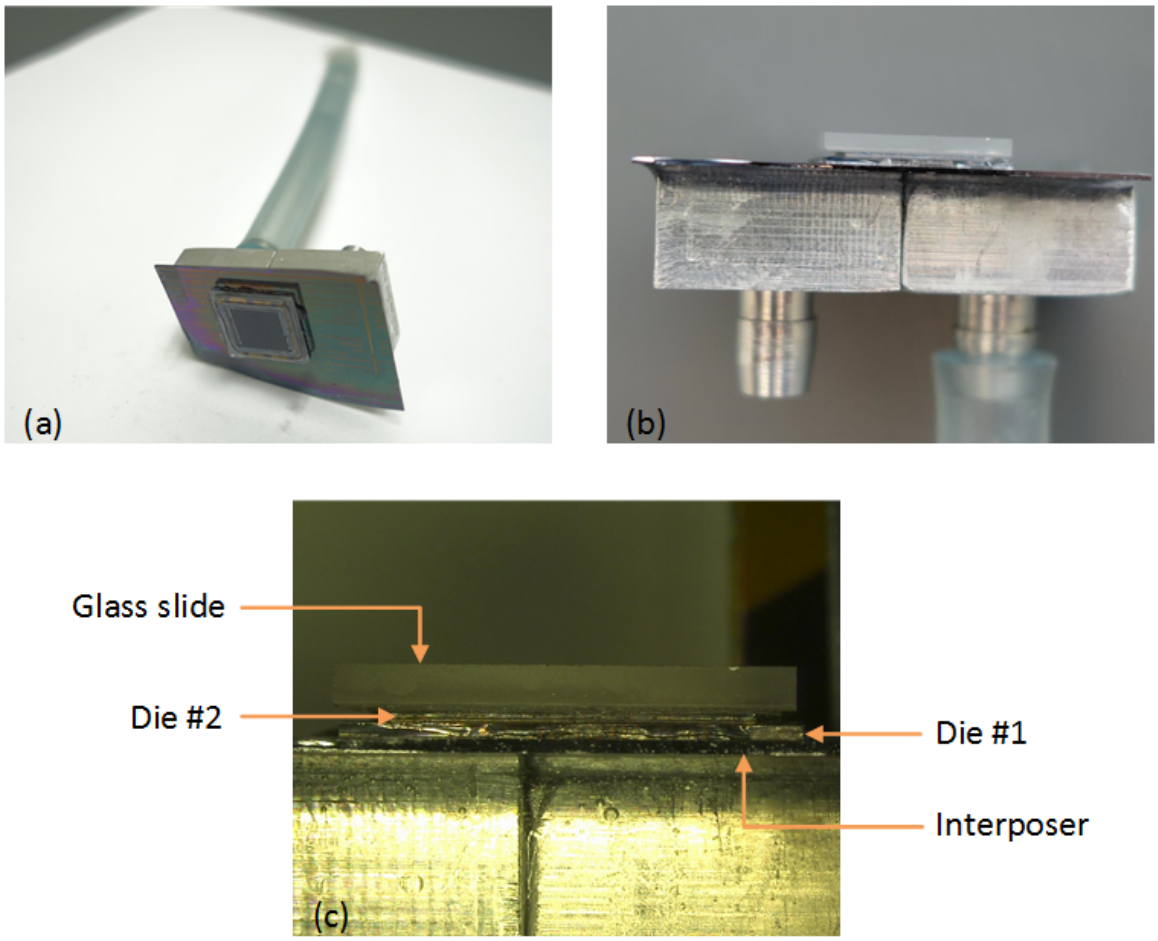


Figure 43: 3-D testbed for fluidic testing: (a) 3-D die stack with glass slide and input/output ports assembled; (b) side view of the assembled testbed; and (c) zoomed-in view of the stack.

transition was also recorded. At 25 mL/min the pressure drop reaches 100 kPa, the measured pressure drop was stable and no leakage was observed. Figure 45 shows the pressure drop as a function of flow rate. More work is needed in optimizing the pressure drop.

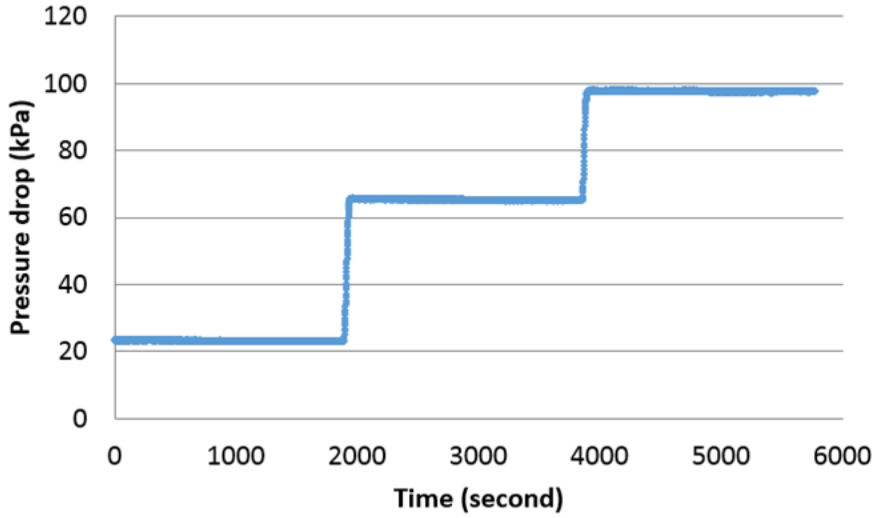


Figure 44: 1.5 hour fluidic testing with three flow rates (10 mL/min, 20 mL/min, and 25 mL/min, each for half an hour).

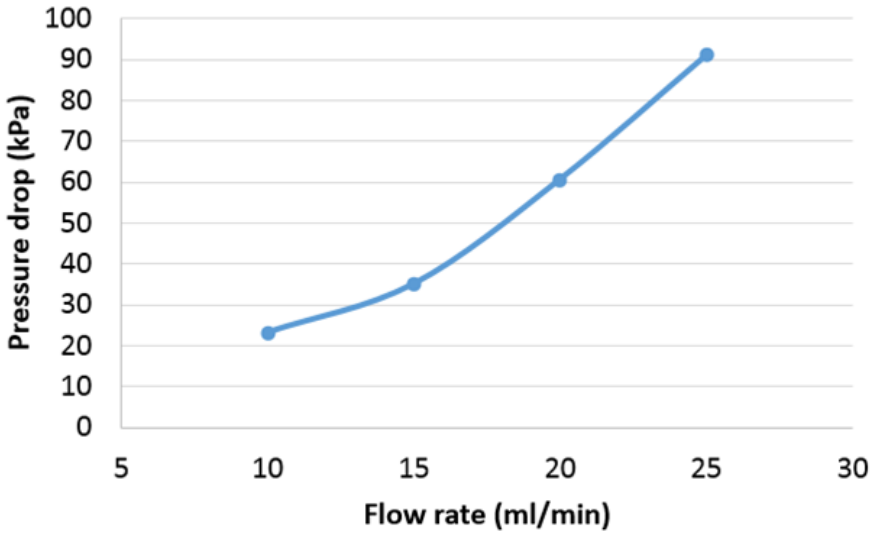


Figure 45: Measured pressure drop as a function of flow rate for the 3D stack.

2.7 Conclusions

This chapter presents the design, fabrication, assembly, and testing of electrical and fluidic I/Os. Annular-shaped fluidic microbumps and circular fluidic vias are designed considering geometry impact on solder reflow, height uniformity between electrical and fluidic microbumps, die area consumption, and pressure drop within the fluidic vias. Fabrication processes for silicon dice with electrical and fluidic microbumps and micropin-fin heat sink were developed. Flip-chip bonding technology is utilized to assemble the silicon die to the interposer. Following assembly, the electrical and fluidic interconnections are verified with electrical and fluidic testing. The measured resistance of electrical microbumps is 13.5 mΩ $\pm$ 1.82 mΩ. No leakage occurred during the fluidic testing with pressure drop reaching 100 kPa. Lastly, 3D stacking of electrical and fluidic microbumps was demonstrated. A 3D die stack with electrical and fluidic microbumps was designed, fabricated, assembled and tested.

CHAPTER III

SILICON INTERPOSER PLATFORM UTILIZING MICROFLUIDIC COOLING FOR HIGH-PERFORMANCE COMPUTING SYSTEMS

3.1 Introduction

Silicon interposer technology has been widely studied recently due to its ultra-fine pitch wiring density. Having multiple chips assembled closely on a silicon interposer, high-bandwidth chip-to-chip signaling between the chips can be achieved with the fine-pitch silicon interposer interconnects. Different silicon interposer platforms have been proposed for high-performance computing systems [30]–[34]. Based on the fluidic I/O technology presented in Chapter II, a silicon interposer platform with microfluidic cooling is presented in this chapter.

Figure 46 illustrates the proposed microfluidic-cooled silicon interposer platform. Multiple chips are closely assembled on a silicon interposer. Coolant is pumped into the fluidic channels in the silicon interposer, then distributed to the on-die microfluidic heat sinks through solder-based fluidic I/Os. Besides microfluidic cooling, a large number of signaling channels can be achieved using the fine-pitch silicon interposer

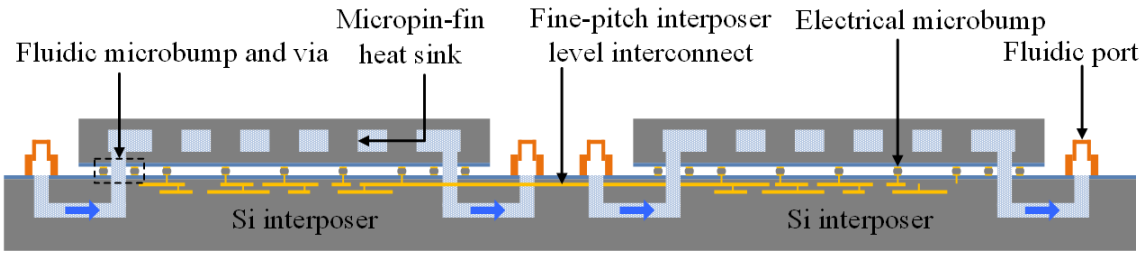


Figure 46: Silicon interposer platform with microfluidic cooling.

interconnects. Thus, combining silicon interposer and microfluidic cooling technology can help address the two major challenges facing high-performance computing system, which are signaling bandwidth and thermal management.

3.2 Test Vehicle for the Proposed Silicon Interposer Platform

3.2.1 Two Microfluidic Cooled Dice on A Silicon Interposer

Based on the electrical and fluidic I/O technology presented in Chapter II, a silicon interposer with two microfluidic cooled-silicon dice assembled side-by-side is demonstrated in this section. The fabrication process of the silicon dice and interposer is the same as the one presented in Section 2.3.2.

Two silicon dice are sequentially bonded to the interposer, as illustrated in Figure 47. Figure 48(a) shows the fabricated silicon interposer with two bonding sites. Two silicon dice with microfludic cooling were flip-chip bonded on the silicon interposer in two bonding steps, as shown in Figure 48(b)(c). The bonding temperature and force

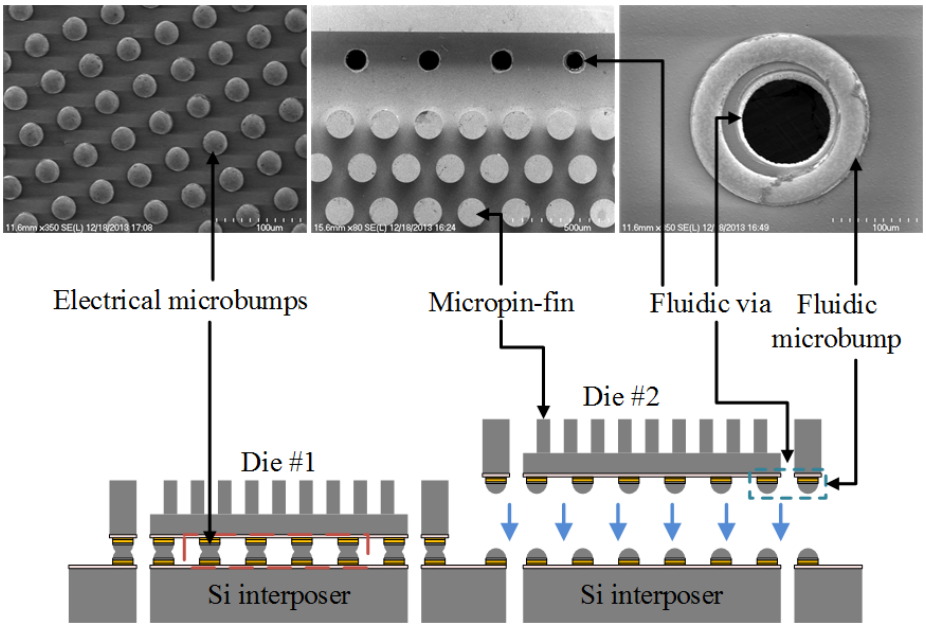


Figure 47: two silicon dice sequentially bonded to a silicon interposer.

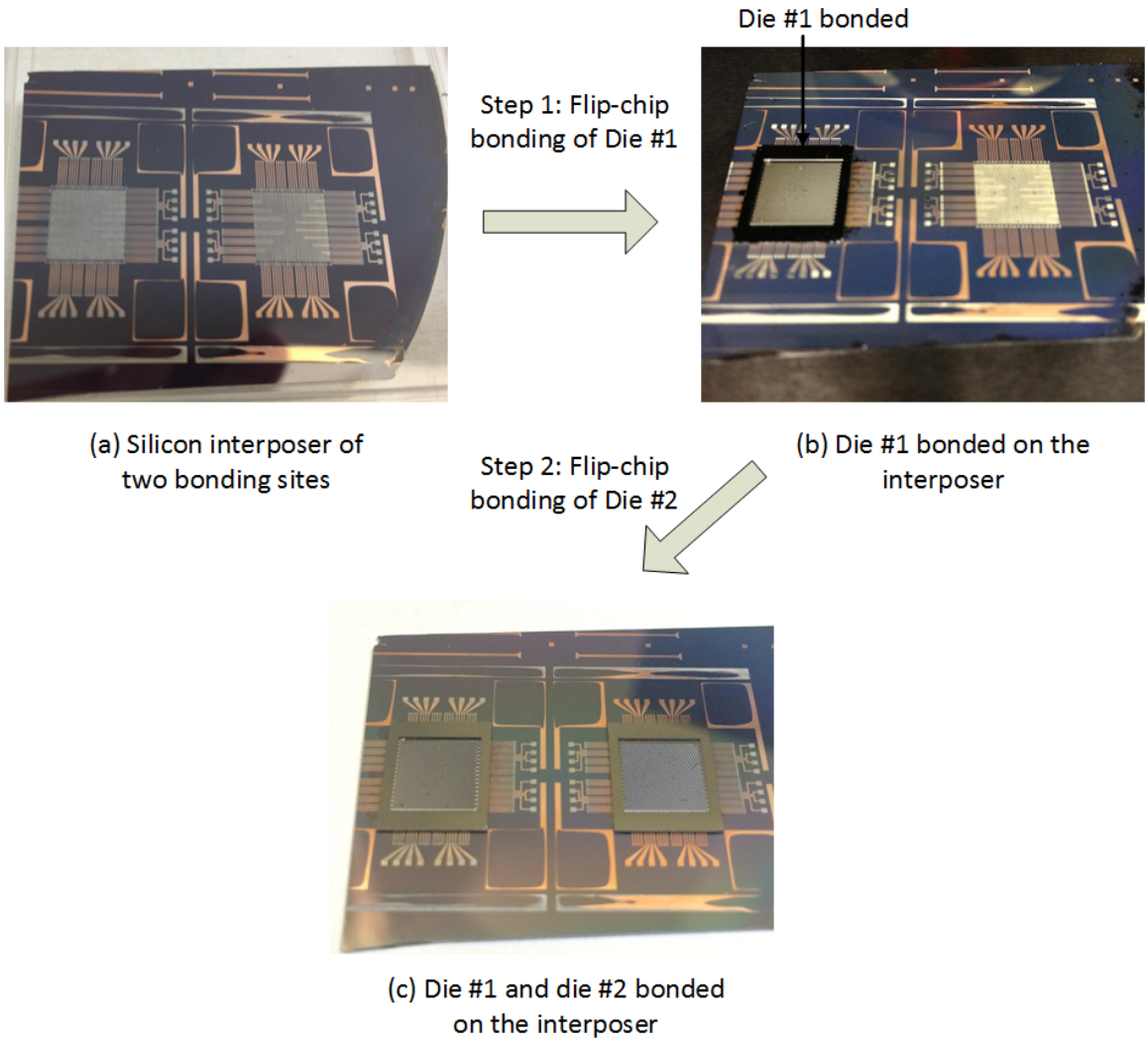


Figure 48: Sequential flip-chip bonding of two silicon dice on one interposer.

for the two dice are the same as listed in Table 3. Following flip-chip bonding, the bonded sample was inspected using an X-ray imager, as shown in Figure 49. We can see from the close-up image that the microbumps are well aligned.

Following assembly of two silicon die on the interposer, the resistance of some of the electrical micrubmps on the two dice was measured using the 4-point resistance measurement. On each die, three microbumps were measured. Table 6 lists the measured resistance of the electrical microbumps on the two silicon dice and the average resistance.

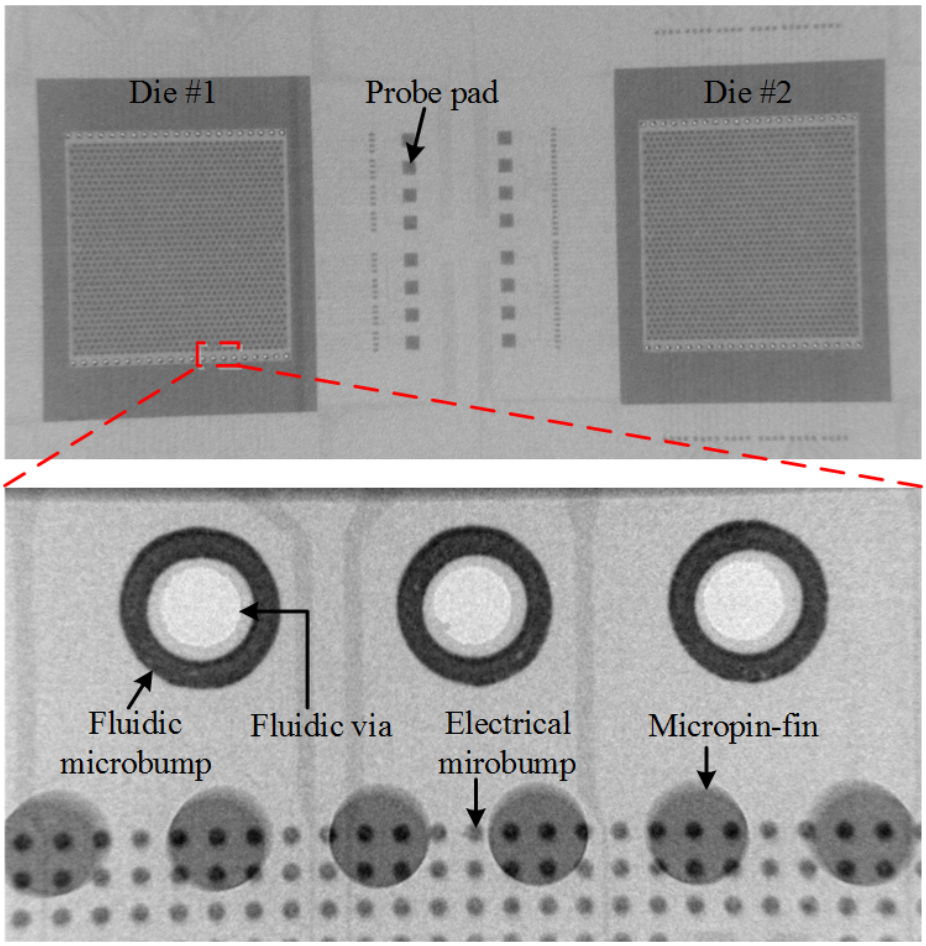


Figure 49: (a) X-ray image of two bonded silicon dice on a silicon interposer; (b) close-up of bonded fluidic and electrical microbumps.

Table 7: Resistance of the electrical microbumps (Unit: mΩ)

Microbump	Die #1	Die #2
#1	11.6	12.8
#2	10.6	11.3
#3	12.9	13.2
Average	11.7	12.4

3.2.2 Test Vehicle for Thermal Measurement

To experimentally evaluate the cooling performance of the proposed silicon interposer platform utilizing microfluidic cooling, a test vehicle was fabricated. The test vehicle

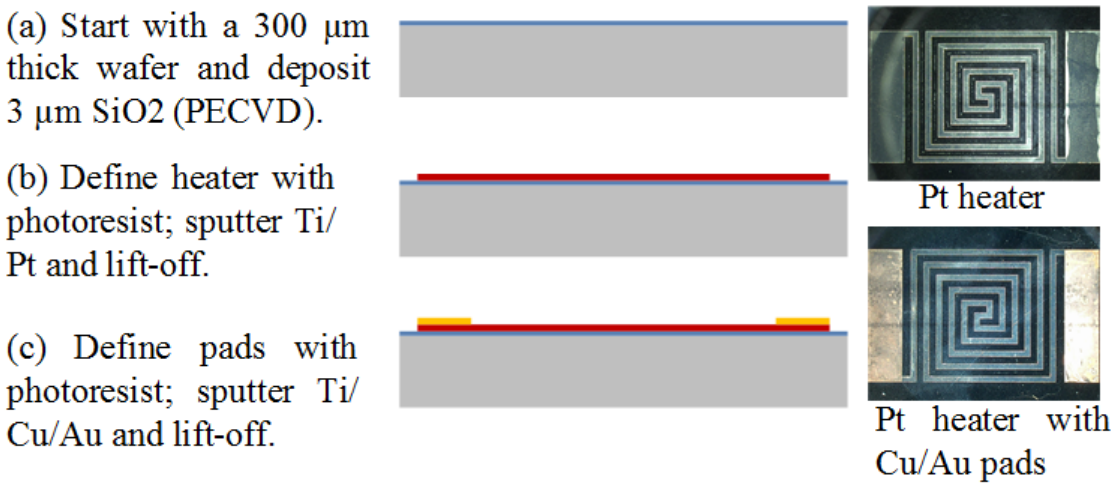


Figure 50: Fabrication process for the Pt heater/RTD.

consists of a silicon die with electrical fluidic microbumps, fluidic vias, and staggered micropin-fin heat sink and a silicon interposer. In order to facilitate thermal measurements, a thin-film platinum heater/resistance temperature detector (RTD) is integrated on the back-side of the assembled dice.

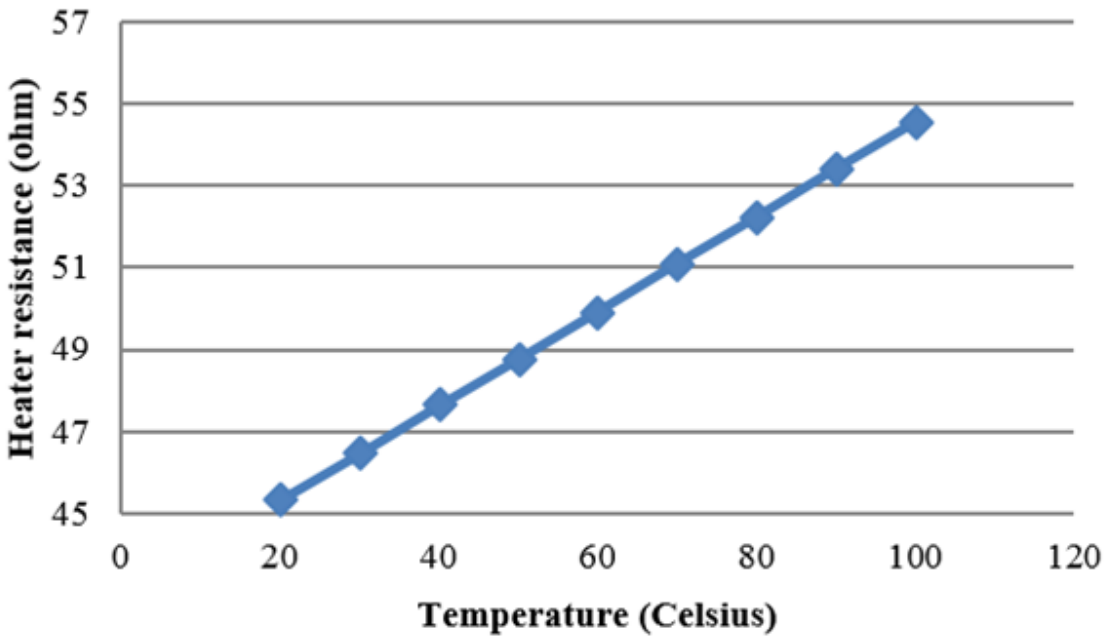


Figure 51: Heater calibration results.

The fabrication process of the platinum heater is illustrated in Figure 50. The process begins with depositing a 3 μm SiO_2 film on one side of a silicon wafer using plasma-enhanced chemical vapor deposition (PECVD). Next, a Ti/Pt (25 nm/1 μm) film is sputtered on the SiO_2 layer followed by a lift-off process to form the heater. The last step is to sputter Ti/Cu/Au on the pads to enable electrical wire soldering to the electrical test equipment (power supply and data acquisition system). The area of the square heater is 0.5 cm^2.

Following fabrication, the heater is calibrated in an oven up to 100 °C. The calibration result indicates a good linear relationship between the temperature and heater resistance, as shown in Figure 51. Using the calibration result, measured heater resistance can be converted to temperature.

The fabricated heater/RTD die was used to cap the micropin-fin heat sink instead

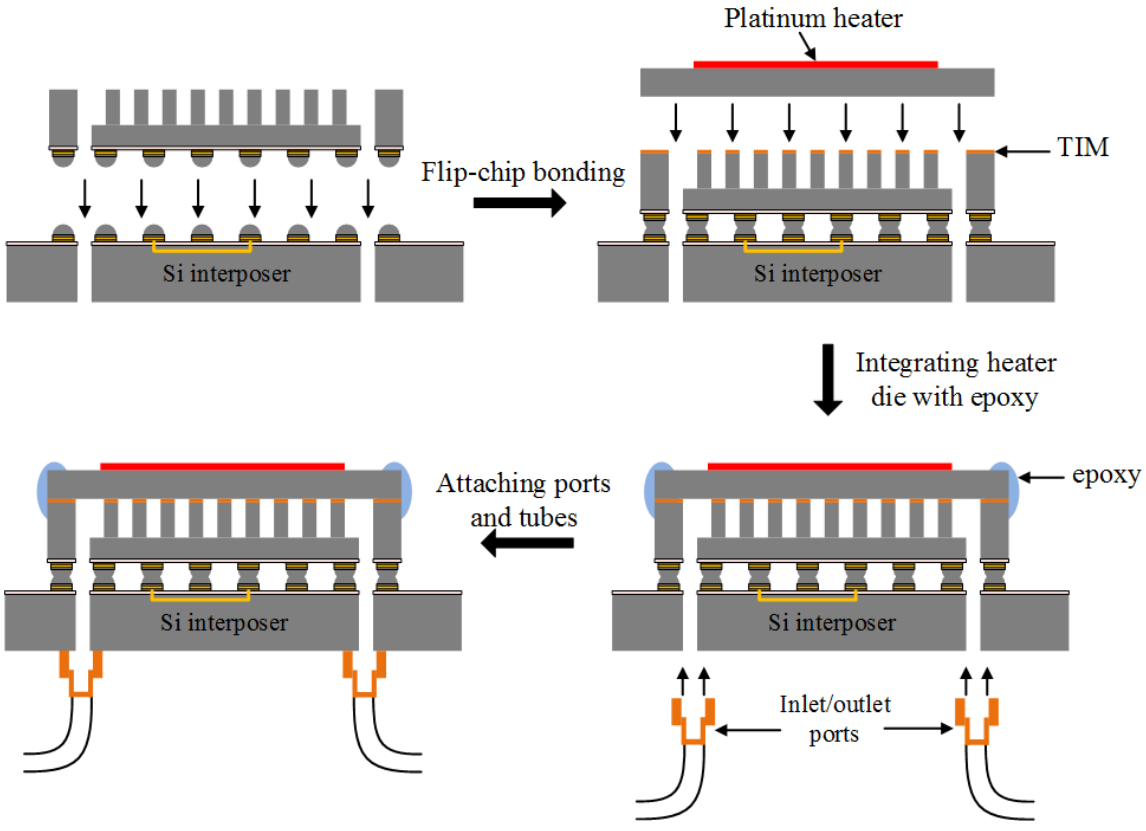


Figure 52: Assembly process of the test vehicle for thermal measurement.

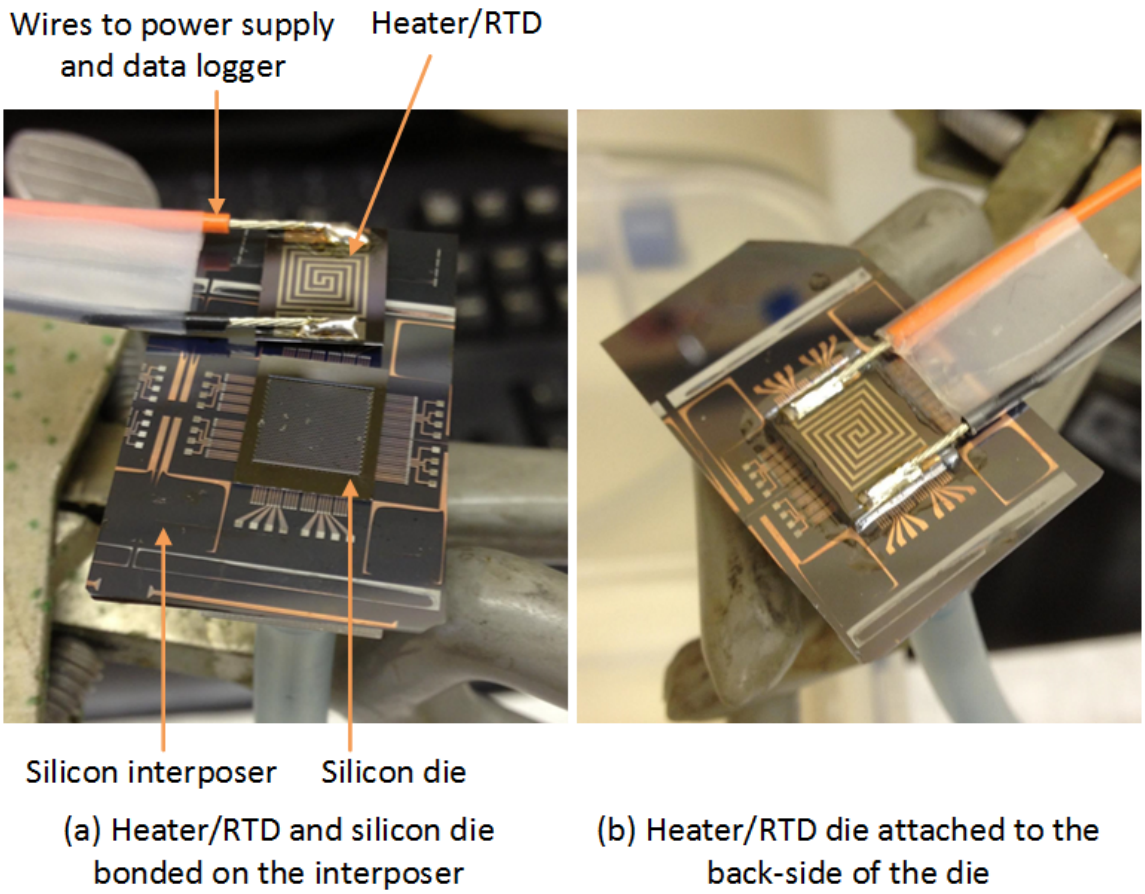


Figure 53: Integration of the heater/RTD to the back-side of the silicon die.

the glass slide. The full assembly process is illustrated in Figure 52. A thin thermal interface material (TIM) layer was applied between the interfacing surfaces to enhance thermal contact. An epoxy film was applied to the edges for sealing. The last step is to attach the inlet/outlet ports to the back side of the silicon interposer. Figure 53 shows the heater/RTD attached to the back side of the silicon die. Wires are soldered to the heater pads for connecting power supply and data logger.

3.3 Thermal Measurements and Thermal Resistance Analysis

3.3.1 Experiment Setup

Following assembly, microfluidic cooling experiments were conducted with the test vehicle. De-ionized (DI) water at room temperature (20 °C) was used as the coolant. The experimental setup is illustrated in Figure 54. During the experiment, an adjustable digital gear pump drew the DI water from a reservoir. The DI water flowed through a mass flow meter and a polyester-based filter to remove particles ($>$ 20 μm) that could possibly clog the fluidic vias and micropin-fin heat sink. A differential pressure gauge was used to measure the pressure at the input port. After flowing across the micropin-fin heat sink, the DI water exits the chip into another reservoir. The temperature of the DI water was measured at both the inlet and output ports.

Once coolant flow commenced, the thin film Pt heater was powered by an Agilent N6705B power analyzer to mimic the power dissipation of a functional die. The electrical resistance of the temperature sensor was recorded with an Agilent 34970A

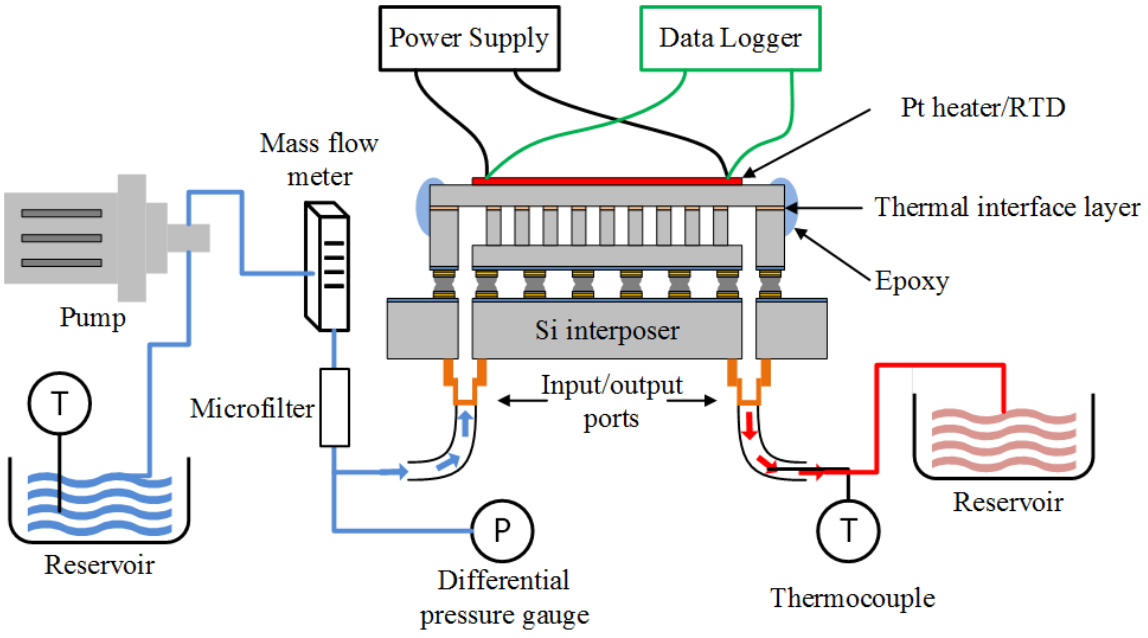


Figure 54: Microfluidic cooling experiment setup.

data logger. The electrical resistance values are used to calculate the heater/RTD temperature according to the calibration results shown in Figure 51.

3.3.2 Measurement Results

Flow rate is an important factor that affects the cooling performance of the micropin-fin heat sink. Different flow rates, from 10 mL/min to 50 mL/min, were applied during the experiment. A power density of up to 100 W/cm^2 was applied to the heater.

The results of the experiments are shown in Figure 55. As expected, the temperature of the heater increases linearly with increased power density, and the temperature decreases as the flow rate increases for a given power density. The measured junction temperature is 55.9 °C at a power density of 97.0 W/cm^2 with a flow rate of 50 mL/min. Note that these results include the thermal resistance of the TIM layer between the capping layer and the micropin-fins; the TIM was used to simplify the fabrication of the testbed.

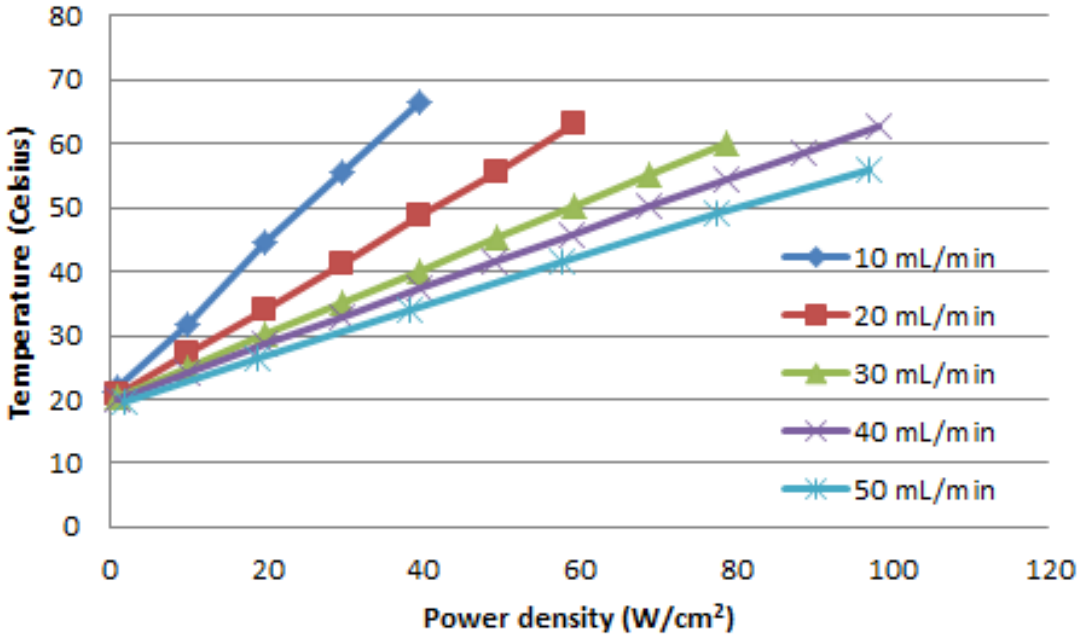


Figure 55: Heater/RTD temperature vs. power density for different flow rates (DI water at room temperature ~20 °C).

3.3.3 Thermal Resistance Analysis

The thermal resistances of the test vehicle are calculated and analyzed to a first order using the measured temperatures. Equation (5) is used to calculate the total thermal resistance [18].

$$R_{total} = \frac{T_{heater} - T_{inlet}}{P} \tag{5}$$

where R_{total} is the total thermal resistance of the sample; T_{inlet} is the inlet DI water temperature (room temperature); T_{heater} is the heater temperature; P is the power applied to the heater.

Based on the measured temperature, the summation of the conductive and convective thermal resistances can be calculated using equation (6) [20]:

$$R_{cond} + R_{conv} = \frac{(T_{heater} - \frac{T_{inlet} + T_{outlet}}{2})}{P} \tag{6}$$

where T_{outlet} is the DI water temperature at the outlet port; R_{cond} is the conductive thermal resistance; R_{conv} is the convective thermal resistance.

Equations (7-9) are used to calculate the convective thermal resistance [22]:

$$R_{conv} = \frac{1}{h \cdot A_t} \tag{7}$$

$$A_t = A_b + \eta \cdot A_{fin} \tag{8}$$

$$\eta = \frac{tanh(2H_{fin}\sqrt{\frac{h}{k_{si}D}})}{2H_{fin}\sqrt{\frac{h}{k_{si}D}}} \tag{9}$$

where h is the heat transfer coefficient, which is determined by the dimensions and placement of the micropin-fins and coolant velocity; A_t is the total effective heat transfer area; A_b is the base area exposed to coolant; η is the fin efficieny; A_{fin} is

the total surface area of the micropin-fins exposed to coolant; H_{fin} is the height of the micropin-fins; D is the diameter of the micropin-fins; and k_{si} is the thermal conductivity of silicon. Given that the dimensions and layout of the micropin-fins heat sink and the DI water velocity are the same as in [22], the heat transfer coefficient h is approximated as the reported value (18,235 W/m^{2}K for a flow rate 40 mL/min in this experiment) from [22].

After obtaining R_{conv}, R_{cond} is simply calculated with equation (6). R_{cond} has three components: R_{cond_TIM}, R_{cond_Si}, and $R_{cond\_SiO_2}$, which are related to the TIM layer, the bulk silicon (300 μm thick), and the silicon dioxide film (3 μm thick) beneath the Pt heater, respectively. R_{cond_Si}, and $R_{cond\_SiO_2}$ are calculated using equation (10) and (11), respectively:

$$R_{cond\_Si} = \frac{T_{Si}}{k_{Si} \cdot A} \tag{10}$$

$$R_{cond\_SiO_2} = \frac{T_{SiO_2}}{k_{SiO_2} \cdot A} \tag{11}$$

where T_{Si} is the thickness of the bulk silicon; T_{SiO_2} is the thickness of the silicon dioxide film; A is the total heating area; and k_{SiO_2} is the thermal conductivity of silicon dioxide. After calculating R_{cond_Si} and $R_{cond\_SiO_2}$, R_{cond_TIM} can be obtained.

Table 7 lists the normalized thermal resistances for 1 cm^2 heating area, where R_{total} and $R_{cond} + R_{conv}$ are calculated from the measured temperature using Equation (5) and (6). The remaining thermal resistances are derived.

In a functional die, the generated heat would be directly beneath the heat sink without a TIM layer. Thus, we adjust the thermal resistance by subtracting the thermal resistance of the TIM layer. Since the thermal resistance of the TIM layer is part of R_{cond}, which is not a function of flow rate, it can be subtracted from the total thermal resistance for the different flow rates. Figure 56 shows the approximated thermal resistance (without TIM) for various flow rates. The adjusted thermal resistance is

Table 8: Thermal resistances (K·cm^2/W) at 40 mL/min

Resistance	Value	Derivation
R_{total}	0.43	Measured temperature, equation (5)
$R_{cond} + R_{conv}$	0.34	Measured temperature, equation (6)
R_{conv}	0.165	Heat transfer coefficient, equation (7)
R_{cond}	0.175	$(R_{cond} + R_{conv}) - R_{conv}$
R_{cond_Si}	0.02	Equation (10)
$R_{cond\_SiO_2}$	0.02	Equation (11)
R_{cond_TIM}	0.135	$R_{cond} - R_{cond\_Si} - R_{cond\_SiO_2}$
$R_{total} - R_{cond\_TIM}$	0.0295	

0.24 K·cm^2/W at a flow rate of 50 mL/min.

Figure 57 shows the measured pressure drop across the assembled die. As expected, the pressure drop increases with increasing flow rate. At 50 mL/min, it reaches 98.3 kPa. One reason for this high pressure drop is the large opening area difference between the input port (1.25 cm × 1.25 cm) and fluidic vias. Optimizing

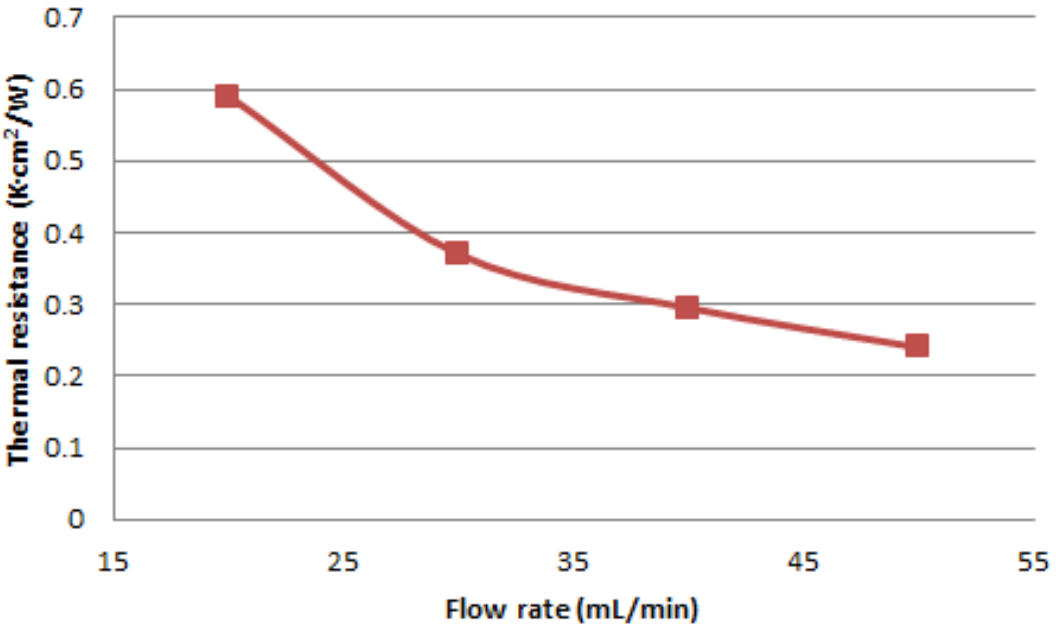


Figure 56: Adjusted thermal resistance vs. flow rate.

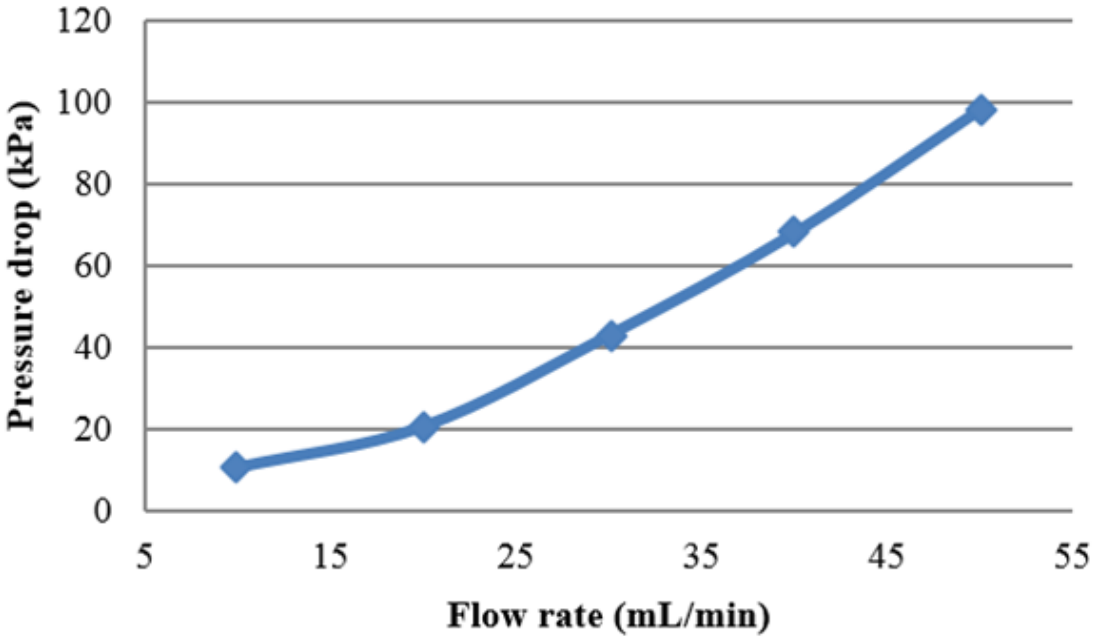


Figure 57: Pressure drop vs. flow rate.

the transition between the input port and fluidic vias would help reduce the pressure drop.

3.4 Thermal Benefits of the Proposed Silicon Interposer Platform

In this section, thermal modeling based on the finite volume method [62], [63] is used to compare different air and microfluidic cooled silicon interposer-based systems. The thermal models, to which a convective boundary is applied, have been validated using ANSYS with an error of less than 3% [64].

3.4.1 Silicon Interposer with Different Cooling Configurations

For the silicon interposer-based system, we assume two silicon dice (1 cm $\times$ 1 cm each) assembled side-by-side on a silicon interposer with a 1 mm gap between the dice. The power maps of the two logic dice are based on the Intel i7 microprocessor [65], [66], as shown in Figure 58. There are multiple functional blocks with different power

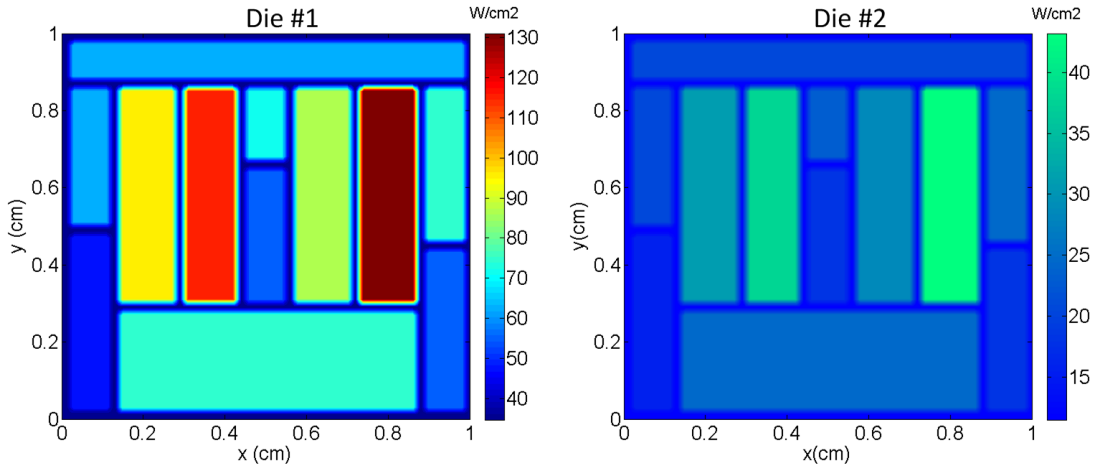


Figure 58: Power maps of the two dice (74.63 W for die #1 and 24.88 W for die #2).

densities on a die. We further assume that the left die (Die #1) is operating at a maximum power of 74.63 W, and the right die (Die #2) is operating at one third of the maximum power. For Die #1, the largest power density reaches 130 W/cm^2. The size of the silicon interposer is 2 cm x 3 cm.

For the above silicon interposer-based system, we consider four different cooling scenarios, as shown in Figure 59. Figure 59(a) shows an air cooling solution with a heat spreader and a bulky air-cooled heat sink placed on top of the two dice; Figure 59(b) is the microfluidic cooling scenario in which a microfluidic heat sink is embedded in each of the two dice; in Figure 59(c), a microfluidic heat sink is embedded in the silicon interposer. This configuration would reduce the system complexity by avoiding microfluidic heat sinks in the active dice and fluidic interconnections between the dice and interposer; The configuration in Figure 59(d) combines die-level and interposer-level microfluidic cooling.

For the microfluidic cooling scenarios, a thermal resistance of 0.24 Kcm^2/W (from the reported experiments in Section 3.3.3) was used in the thermal models. The air-cooled heat sink design and attributes are similar to that used for the Intel i7 microprocessor; the heat spreader is 5 cm $\times$ 4.5 cm and the total thermal resistance

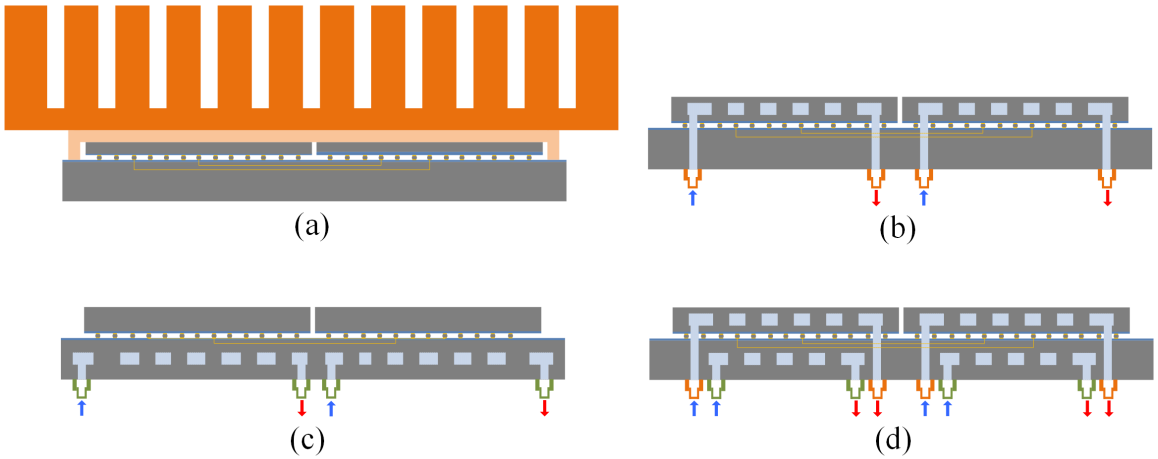


Figure 59: Different cooling scenarios for a silicon interposer based system assuming two dice: (a) air cooling; (b) microfluidic cooling in silicon dice; (c) microfluidic cooling in silicon interposer; (d) microfluidic cooling in both silicon die and interposer.

from the heat spreader to the ambient is 0.218 K/W [67], which can be converted to a resistance of 0.8918 Kcm^2/W from the die surface to the ambient according to the spreading resistance model in [68].

3.4.2 Thermal Simulation and Analysis

The temperature distributions across the high-power die, low-power die, and silicon interposer are simulated for the four cooling scenarios using a thermal simulator based on finite-difference method.

Figure 60 shows the simulated power maps of the two silicon dice and the interposer for the air cooling scenario. The maximum temperature of Die #1 (high-power die) is 102.4 °C, which appears in the high-power-density block as expected. The maximum temperature of Die #2 (low-power die) is 86.0 °C, which appears at the left edge of the die. This severe thermal coupling from Die #1 is mainly caused by the sharing of the heat spreader and air-cooled heat sink. The temperature difference of the two silicon dice is also reflected by the temperature map of the silicon interposer. The Die #1 region on the silicon interposer has much higher temperature than that of the Die #2 region. The thermal coupling effect can also be clearly seen on the

interposer temperature map. The average temperature of the region (1 mm wide) between Die #1 and Die #2 is 83.5 °C.

The simulated power maps of the two silicon dice and the interposer for Scenario (b) microfluidic cooling in silicon die are shown in Figure 61. The maximum temperature of Die #1 (high-power die) is 63.6 °C, which appears in the high-power-density block as expected. The maximum temperature of Die #2 (low-power die) is 46.5 °C, which also appears in its high-power-density block. Compared to air cooling, the thermal coupling between two dice is significantly reduced with die-level microfluidic cooling. This coupling reduction can also be observed on the temperature map of the silicon interposer. The average temperature of the silicon interposer region (1 mm wide) between Die #1 and Die #2 is 49.8 °C.

Figure 62 shows the simulated power maps of the two silicon dice and the interposer for the Scenario (c) microfluidic cooling in silicon interposer. The maximum temperature of Die #1 (high-power die) is 86.2 °C, while the maximum temperature of Die #2 (low-power die) is 53.8 °C. Thermal coupling between the two dice is significantly reduced. The average temperature of the silicon interposer region (1 mm wide) between Die #1 and Die #2 is 49.0 °C.

Figure 63 shows the simulated power maps of the two silicon dice and the interposer for the Scenario (d) microfluidic cooling in both silicon die and interposer. The maximum temperature of Die #1 (high-power die) is 56.7 °C, while the maximum temperature of Die #2 (low-power die) is 44.1 °C. Thermal coupling between the two dice is significantly reduced. The average temperature of the silicon interposer region (1 mm wide) between Die #1 and Die #2 is 41.6 °C.

Having the four cooling scenarios simulated, the cooling performances are compared in Figure 64. Air cooling is used as the baseline case for comparison. The maximum temperature of Die #1 is reduced from 102.4 °C to 63.6 °C (37.89% reduction) and 56.7 °C (44.63% reduction) with die-level and composite (die and interposer-level)

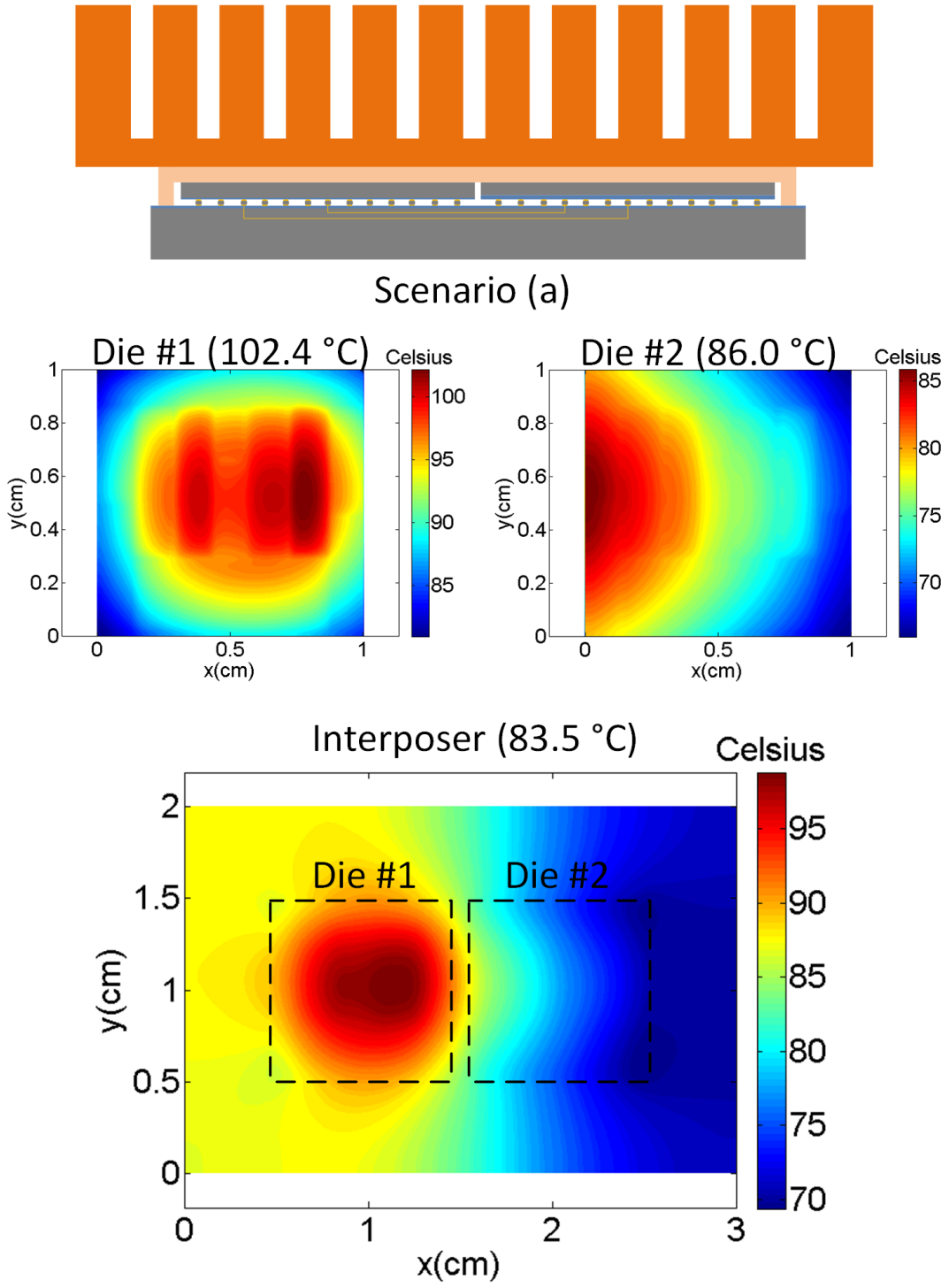


Figure 60: Simulated temperature maps for the two silicon dice and silicon interposer of Scenario (a) air cooling: maximum temperature of Die #1 is 102.4 °C; maximum temperature Die #2 is 86.0 °C; average temperature of the silicon interposer region (1mm wide) between Die #1 and Die #2 is 83.5 °C.

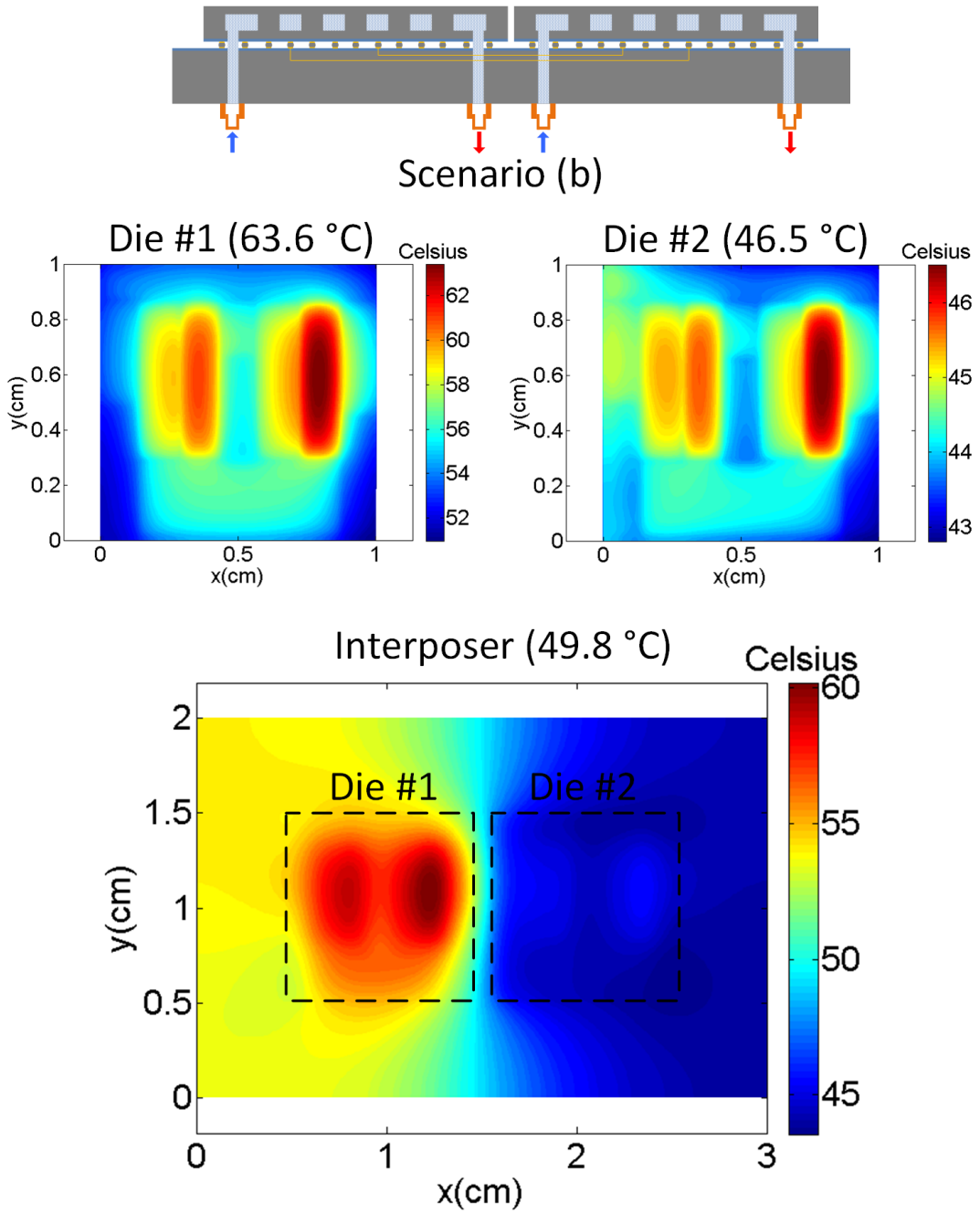


Figure 61: Simulated temperature maps for the two silicon dice and silicon interposer of scenario (b) microfluidic cooling in silicon die: maximum temperature of Die #1 is 63.6 °C; maximum temperature Die #2 is 46.5 °C; average temperature of the silicon interposer region (1mm wide) between Die #1 and Die #2 is 49.8 °C.

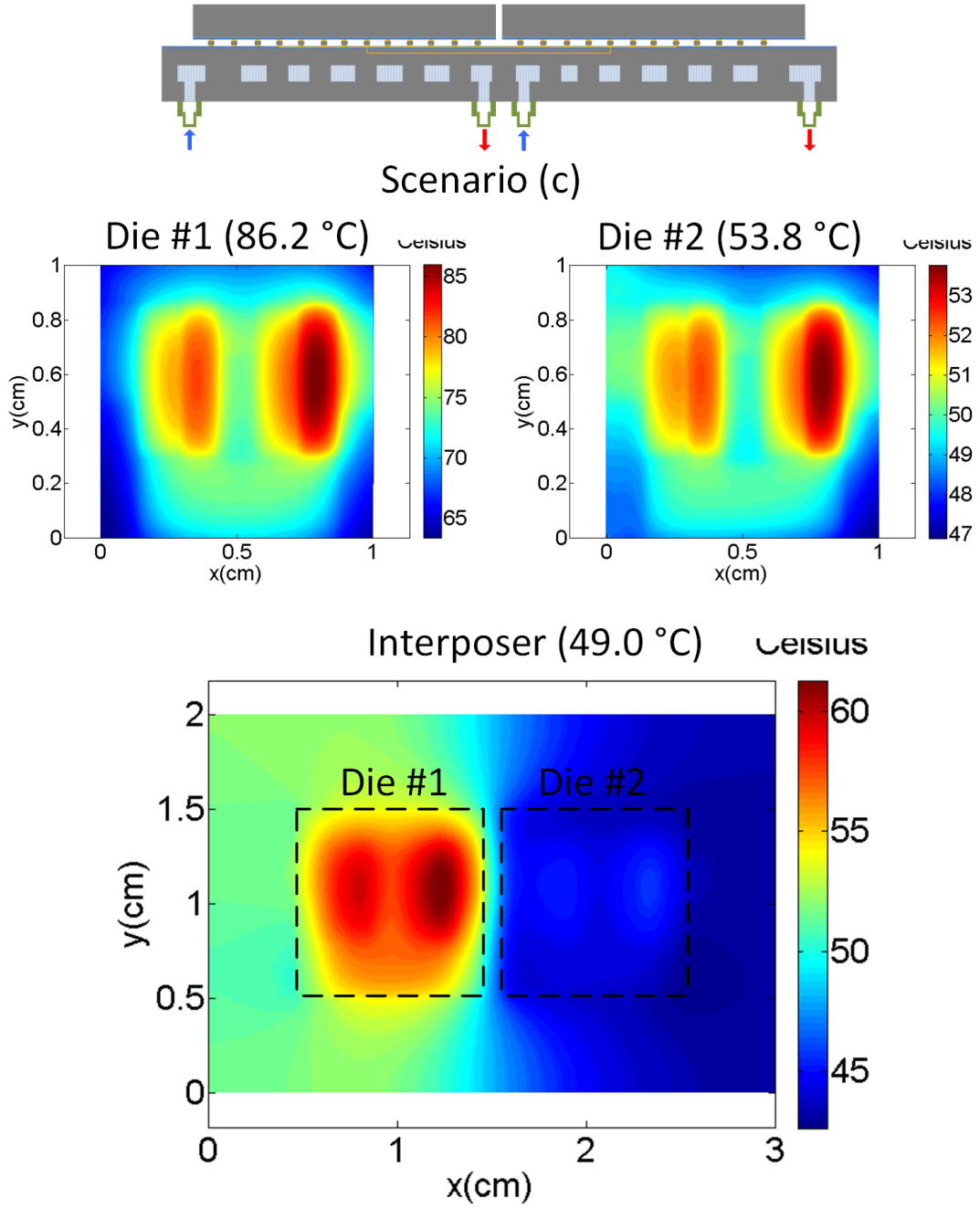


Figure 62: Simulated temperature maps for the two silicon dice and silicon interposer of scenario (c) microfluidic cooling in silicon interposer: maximum temperature of Die #1 is 86.2 °C; maximum temperature Die #2 is 53.8 °C; average temperature of the silicon interposer region (1mm wide) between Die #1 and Die #2 is 49.0 °C.

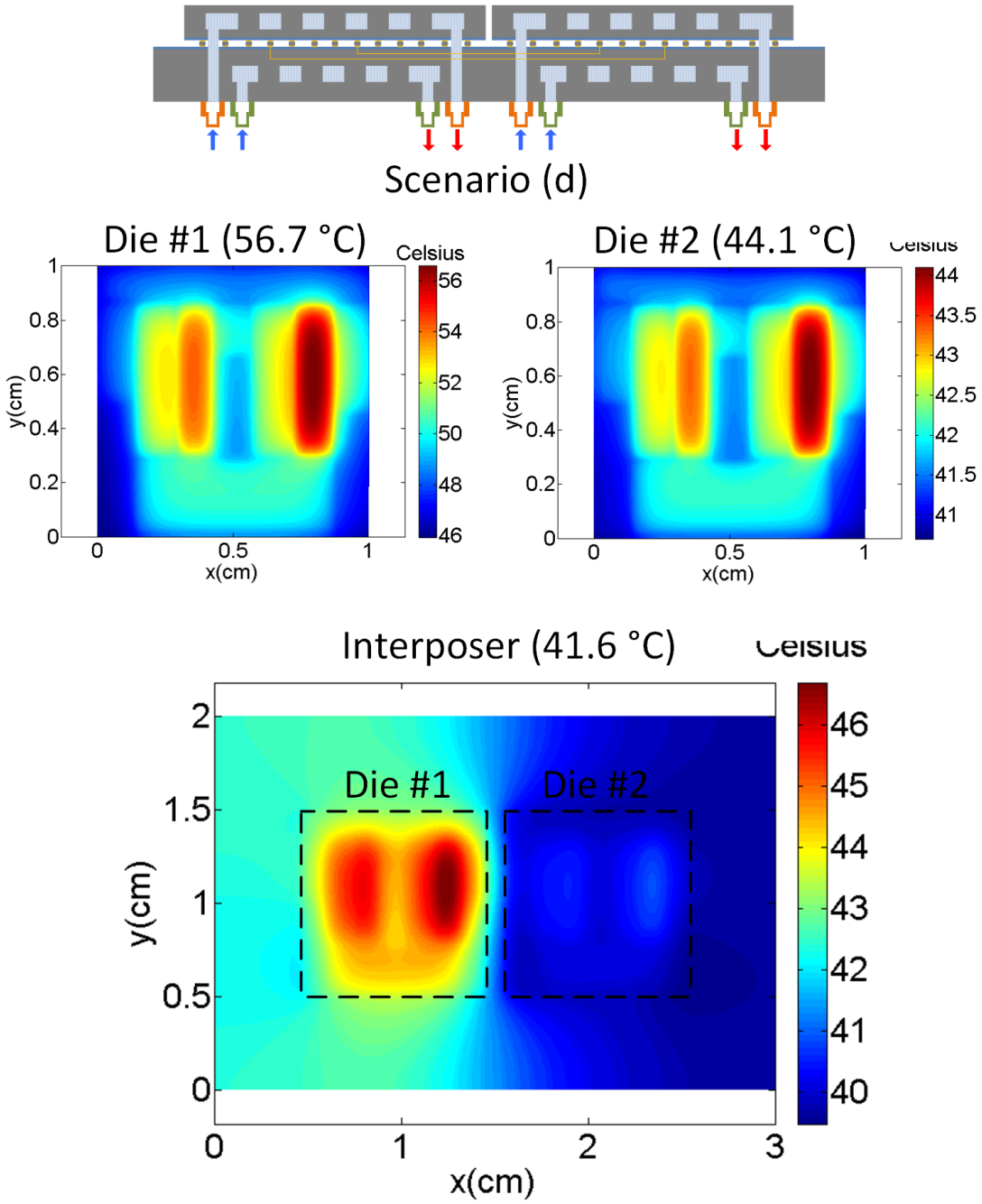


Figure 63: Simulated temperature maps for the two silicon dice and silicon interposer of scenario (d) microfluidic cooling in both silicon die and interposer: maximum temperature of Die #1 is 56.7 °C; maximum temperature Die #2 is 44.1 °C; average temperature of the silicon interposer region (1mm wide) between Die #1 and Die #2 is 41.6 °C.

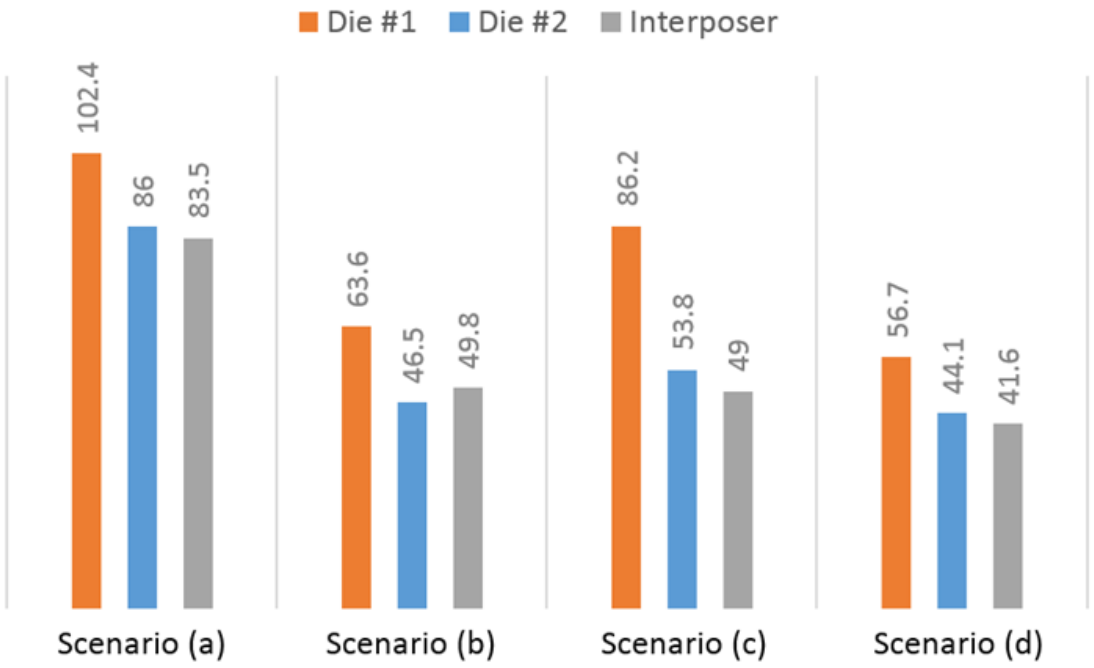


Figure 64: Comparison of the temperatures (Celsius) of the silicon dice and interposer in the four scenarios: (a) air cooling; (b) microfluidic cooling in silicon dice; (c) microfluidic cooling in silicon interposer; (d) microfluidic cooling in both silicon dice and interposer.

microfluidic cooling, respectively. With interposer-level microfluidic cooling, due to the lack of direct contact with the silicon die, the temperature of Die #1 is reduced to 86.2 °C (15.8% reduction). For Die #2, die-level microfluidic cooling reduces its maximum temperature from 86.0 °C to 46.5 °C (45.93% reduction); interposer-level microfluidic cooling reduces the maximum temperature to 53.8 °C (37.44% reduction); and composite microfluidic cooling reduces the maximum temperature to 44.1 °C (48.72% reduction). Regarding the silicon interposer, die-level microfluidic cooling reduces its average temperature from 83.5.0 °C to 49.8 °C (40.36% reduction); interposer-level microfluidic cooling reduces the temperature to 49.0 °C (41.32% reduction); and composite microfluidic cooling reduces the temperature to 41.6 °C (50.18% reduction).

Based on the above observations, we can conclude that microfluidic cooling can

Table 9: Simulated temperature of the silicon dice and interposer for the four cooling scenarios (Unit: °C)

	Scenario #1	Scenario #2	Scenario #3	Scenario #4
Die #1	102.4	63.6 ↓37.89%	86.2 ↓15.82%	56.7 ↓44.63%
Die #2	86	46.5 ↓45.93%	53.8 ↓37.44%	44.1 ↓48.72%
Interposer	83.5	49.8 ↓40.36%	49 ↓41.32%	41.6 ↓50.18%

significantly reduce silicon die and interposer temperature as well as thermal coupling between silicon dice, compared to air cooling. Different microfluidic cooling configurations have different properties. Interposer-level cooling can achieve low interposer temperature but has limited cooling capability for high-power die. Composite microfluidic cooling achieves the lowest temperatures for both high- and low- power dice and the silicon interposer among the four scenarios, but it requires embedding microfluidic heat sinks in both silicon die and interposer, which increases system complexity. The performance of die-level microfluidic cooling is comparable to that of the composite microfluidic cooling. Thus, die-level microfluidic cooling is probably the best choice in terms of cooling performance and system complexity. Table 8 summarizes the simulated temperatures and percentage reductions.

3.4.3 Thermal Coupling Analysis

In the previous thermal simulation, we see severe thermal coupling with air cooling. In order to reduce the coupling, one can increase the space between the high power and low power dice (albeit at the cost of reduced system integration and increased interconnect lengths, which will be discussed later). Figure 65 shows the temperatures of the two dice (maximum temperature) and silicon interposer (average temperature of the space between the two dice) as a function of spacing between the two dice.

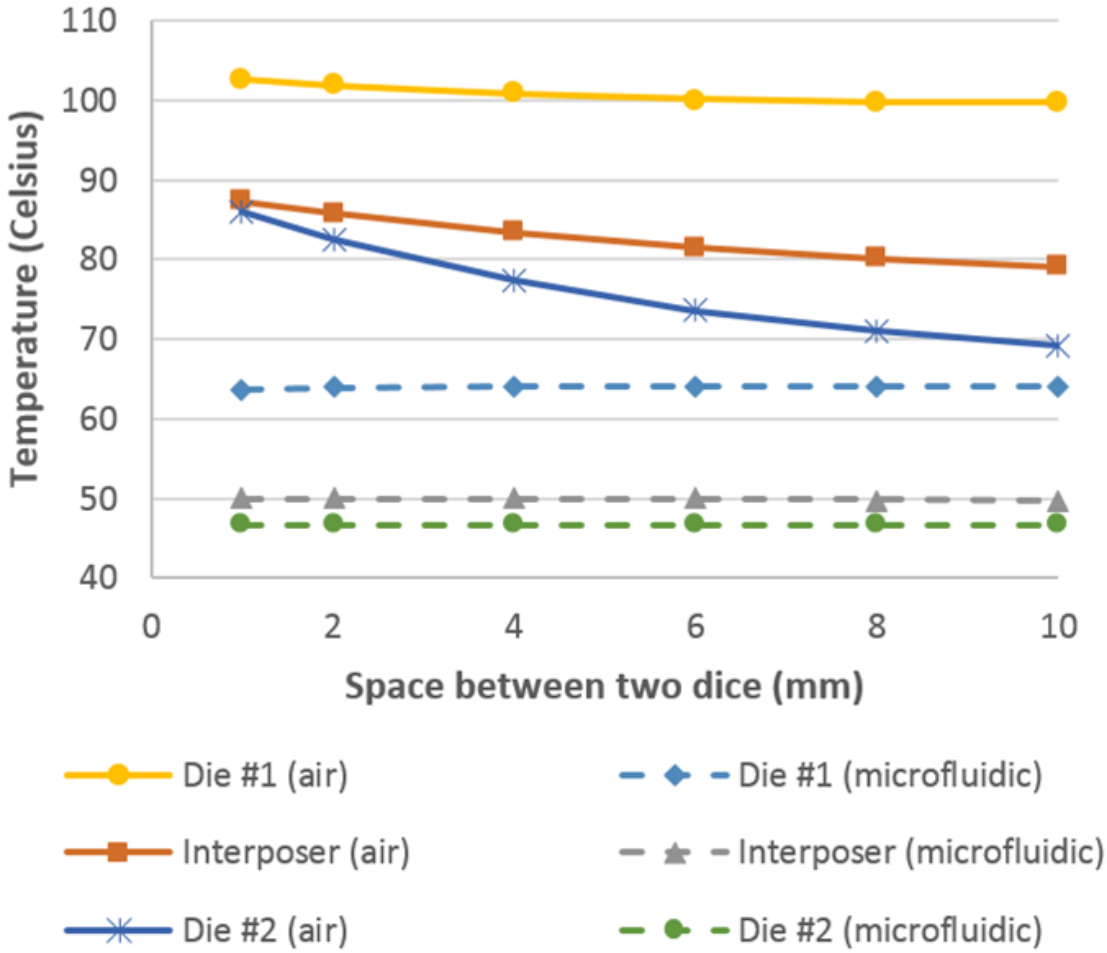


Figure 65: Temperature of silicon dice and interposers as a function of the space between the two dice.

Since the die size and interposer size are assumed to be 1 cm × 1 cm and 2 × 3 cm, respectively, the maximum space between the two dice is 10 mm. Although 10 mm space is not practical and opposes the purpose of high-density integration on silicon interposer, we swept the spacing distance from 1 mm to 10 mm for wide range exploration. As shown in Figure 65, for air cooling, the maximum temperature of Die #1 is relatively stable, reducing from 102.6 °C to 99.8 °C (2.7% reduction) when the space increases from 1 mm to 10 mm. This is because Die #1 is the major heat source of the system. However, the maximum temperature of Die #2 is significantly

reduced from 86.0 °C to 69.3 °C (19.4% reduction) because of the increased distance from Die #1. For silicon interposer, its temperature is reduced from 87.2 °C to 79.1 °C (9.4% reduction) when the space between the two dice increases from 1 mm to 10 mm. For microfluidic cooling, separating the dice does not impact the temperature, as shown in the figure. Again, although increasing the space helps reduce temperature coupling in the air cooling configuration, it significantly reduces integration density (less number of dice on an interposer) and signaling performance (discussed in Section 3.5).

3.5 Signaling Benefits of The Proposed Silicon Interposer Platform

In this section, the fine-pitch interconnects on the proposed silicon interposer are modeled, and the signaling benefits of the proposed platform are analyzed.

3.5.1 Analytical Frequency Dependent Resistance Model for Silicon Interposer Interconnects

Multiple analytical models have been previously developed for the frequency dependent resistance of transmission lines [69], [70]. However, for the fine-pitch interconnects on a silicon interposer, the cross-sectional dimensions are so small that the previously developed models have significant errors at the frequencies of interest. The new analytical model as developed, combines the asymptotic models for resistance in the low and the high-frequency regions [71], with a fitting parameter k to ensure continuity at the transition frequency f_0.

The low frequency region resistance are calculated using equation (12).

$$R_{low} = \sqrt{R_{dc}^2 + R_{ac}^2} \tag{12}$$

where R_{dc} and R_{ac} are calculated using equation (13) and equation (14), respectively.

$$R_{dc} = \frac{\rho}{wt} \tag{13}$$

$$R_{ac} = \frac{\rho}{2\delta(w+t)} \tag{14}$$

where ρ is the resistivity of copper, w is the width, t is the thickness, δ is the skin depth (equation (16)).

The high frequency region resistance are calculated using equation (15).

$$R_{high} = k\frac{\rho}{2\delta(w+t-2\delta)} \tag{15}$$

$$\delta = \sqrt{\frac{\rho}{\pi\mu f}} \tag{16}$$

where μ is the permeability, and f is the frequency. The high and low frequency models given above are combined to from

$$R = \begin{cases} R_{low}, f \leq f_0 \\ R_{high}, f \geq f_0 \end{cases} \tag{17}$$

$$f_0 = \frac{4\rho}{\pi\mu t^2} \tag{18}$$

where the frequency f_0 is defined as the transition frequency at which the skin depth is equal to half of the conductor thickness t.

The analytical models developed are validated with Synopsys Raphael [72] utilizing the differential stripline structure. The error in the new model is less than 15% for the dimensions and frequency range of interest.

3.5.2 Differential Signaling Modeling

In this work, a low-swing current mode, bipolar, and unidirectional differential signaling scheme is chosen for high bandwidth and good noise immunity signaling. We follow the modeling methodology presented in [73] and [74]. The stripline structure illustrated in Figure 66 is utilized.

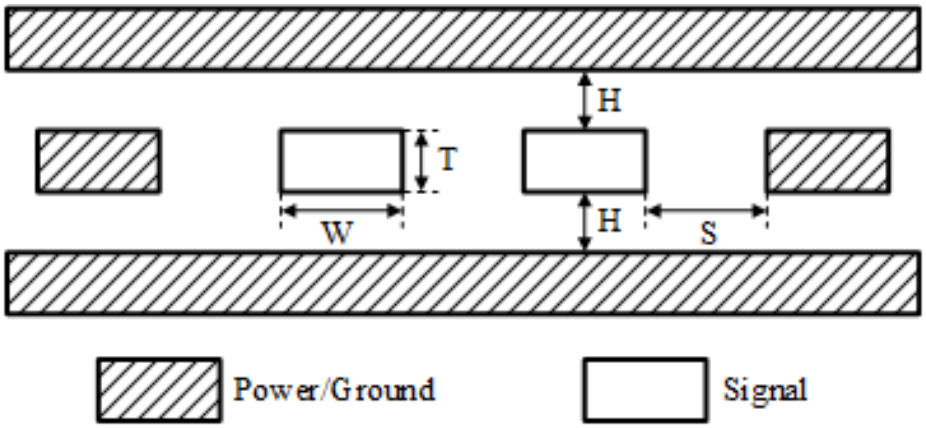


Figure 66: Stripline differential signaling on silicon interposer.

To model the power or energy-per-bit (EPB) of the differential signaling channel, the two major parameters are channel attenuation and noise, as shown in the following equation:

$$I_{min} \geq \frac{V_{margin}}{A \cdot Z_{in}} \tag{19}$$

where I_{min} si the minimum required current swing, V_{margin} is the noise margin, A is the channel attenuation, and Z_{in} is the interconnect impedance. Basically, it requires that the signal magnitude after attenuation to dominate the noise.

Resistance, inductance, capacitance, and conductance (RLCG) of the interposer interconnects are extracted to calculate the attenuation at a given data rate (or frequency) [75]. Resistance is calculated using the new frequency-dependent model developed for interposer interconnects in Section 3.5.1 [29]. Capacitance and conductance are calculated using the models from [76]. Inductance is derived from its relationship with propagation velocity and capacitance.

The noise margin is the sum of noise margin required at a given bit error rate (BER) and other fixed noise sources, such as receiver offset and sensitivity [73]. Channel crosstalk is neglected because the signaling channels are well shielded by ground wires and planes, as in Figure 66.

After determining I_{min}, the power consumption of the signaling channel is calculated as follows:

$$P = V_{dd} \cdot I_{min} \tag{20}$$

where P is the signaling channel power, I_{min} is the power supply voltage [74].

3.5.3 Silicon Interposer Interconnect Analysis

Fine-pitch wiring is a key advantage of silicon interposer technology. Using a larger number of interconnects, very large signaling bandwidth can be achieved. However, reducing the pitch of the interconnects (and thus, interconnect width and height) increases interconnect resistance, which leads to higher energy-per-bit (EPB). Thus, there is a trade-off between signaling bandwidth and energy-per-bit. To capture this trade-off, we use a composite metric BWD/EPB. Bandwidth density (BWD) is defined as the aggregate bandwidth within a unit width.

We assume interconnect thickness, T, and dielectric layer thickness, H, are constant ($T = H = 2\mu m$), space S is two thirds of interconnect width W, as shown in Figure 66. We also assume a signaling frequency of 5 GHz (or data rate 10 Gbps). The impact of interconnect width, length, and operating temperature, which impacts interconnect resistance, on BWD/EPB are investigated.

The interconnect temperature is assumed to be the average temperature of the space between the two dice (shaded region in Figure 67), as shown in Figure 67. The temperature impacts signaling through resistivity, as indicated by the following equation:

$$\rho(T) = \rho_0[1 + \alpha(T - T_0)] \tag{21}$$

where ρ is resistivity, ρ_0 is resistivity at temperature T_0, T_0 is reference temperature, and α is temperature coefficient of resistivity.

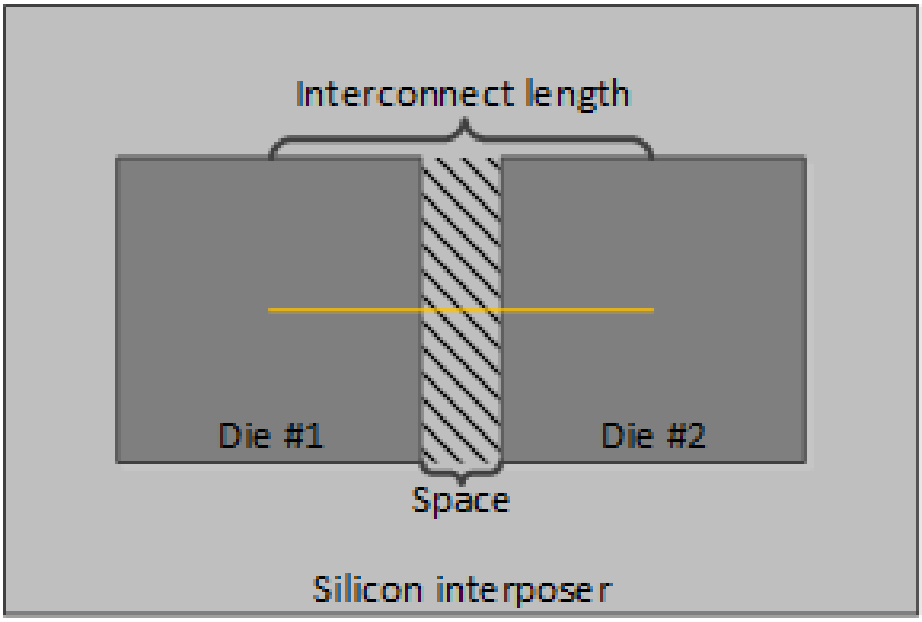


Figure 67: Center-to-center distance for interconnect length.

Table 10: Three scenarios for signaling analysis

	Scenario #1	Scenario #2	Scenario #3
Interconnect length (cm)	1.1	1.1	2.0
Spacing (mm)	1	1	10
Temperature (Celsius)	49.9	86.0	79.1
Cooling	microfluidic	air	air
Copper resistivity	$1.88 \times 10^{-8}\Omega \cdot m$	$2.11 \times 10^{-8}\Omega \cdot m$	$2.07 \times 10^{-8}\Omega \cdot m$

For a given interconnect length and temperature, there is an optimal width that maximizes BWD/EPB since increasing width improves EPB but reduces BWD, and vice versa. In the following analysis, we use the die center-to-center distance as interconnect length, as shown in Figure 67. Table 9 lists the three scenarios with air cooling and die-level microfluidic cooling for analysis.

Figure 68 shows the normalized BWD/EPB for the three scenarios. For scenario

#1 and scenario #2, BWD/EPB is maximized with an optimal interconnect width of 2.0 μm and 2.1 μm, respectively. There is approximately a modest 7.76 % improvement in BWD/EPB for microfluidic cooling (scenario #1) compared to air cooling (scenario #2). In scenario #3, the interconnect length is increased to 2 cm for temperature and thermal coupling reduction. As noted in Section 3.4, a 10 mm space is not practical and does not enable the high-density integration on silicon interposer. We use this scenario for comparison and exploration of the impact of interconnect length on signaling performance. As shown in Figure 68, the optimal width for the 2 cm long interconnect increases to 2.9 μm; however, the BWD/EPB (at optimal width) becomes less than half of that of scenario #1 and scenario #2.

Figure 69 shows the normalized BWD/EPB for interconnects of 1.1 cm, 2 cm, and 5 cm length as a function of temperature; the results are normalized to each

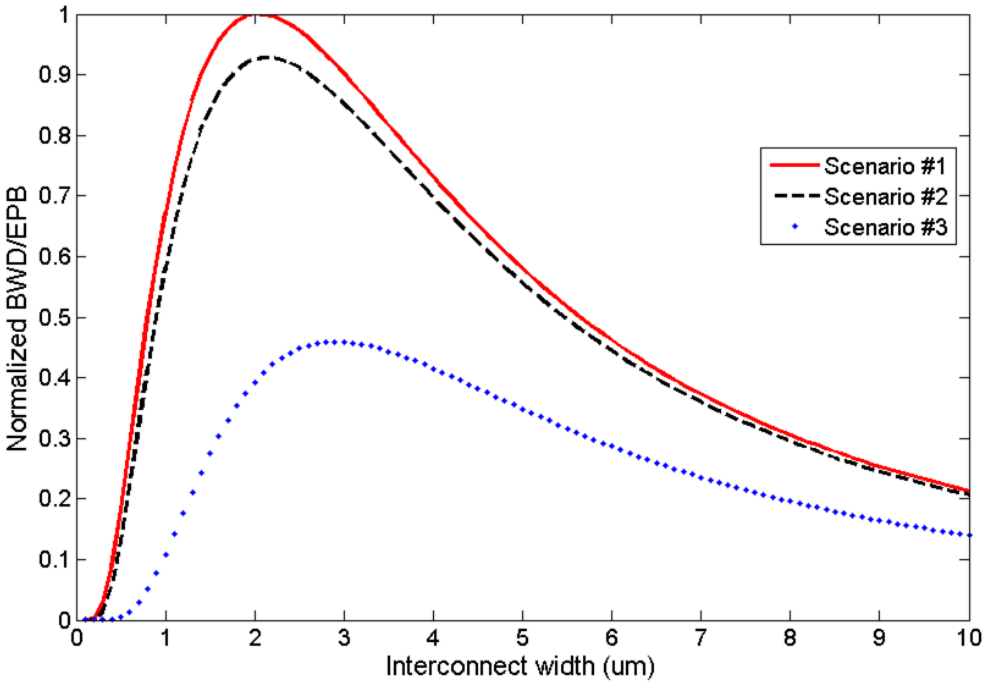


Figure 68: Normalized BWD/EPB as a function of interconnect width for the three scenarios.

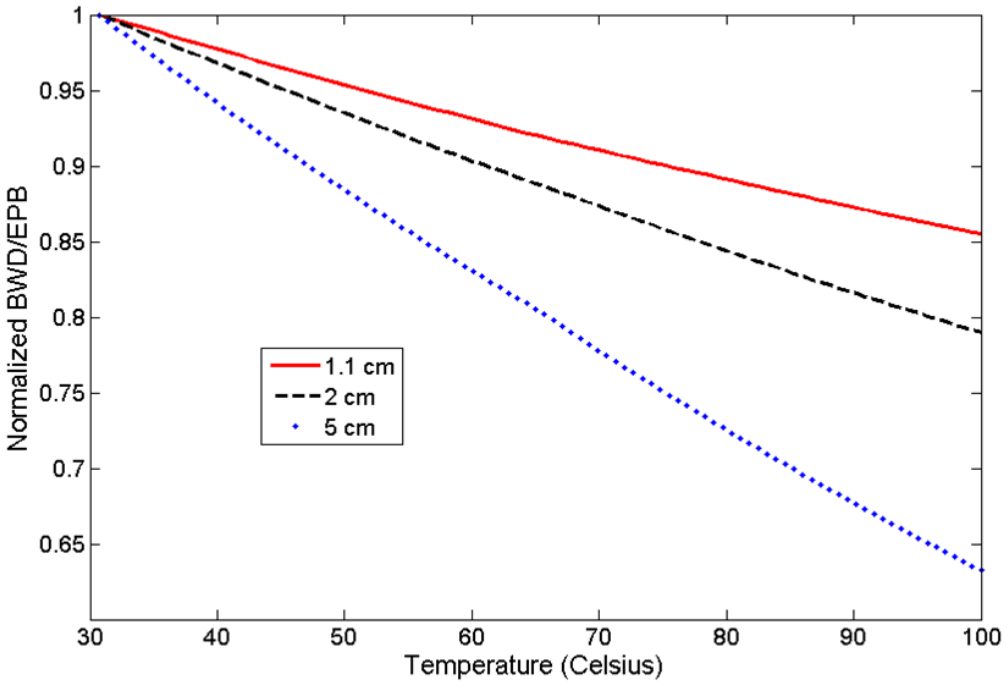


Figure 69: Normalized BWD/EPB as a function of temperature for three interconnects of different lengths.

interconnects BWD/EPB at 30 °C. We can see that the BWD/EPB decreases rapidly for longer interconnects. When interposer temperature increases from 30 °C to 80 °C, there is approximately a 11.7%, 16.33%, and 28.5% reduction in BWD/EPB for interconnects of 1.1 cm, 2 cm, and 5 cm length, respectively. Thus, for large silicon interposers with long interconnect length, microfluidic cooling could potentially provide some benefits for chip-to-chip singling.

3.6 Conclusion

In this chapter, a silicon interposer platform utilizing microfluidic cooling is proposed for high-performance computing systems. The key advantage of the silicon interposer is its very fine-pitch wiring, which enables high-bandwidth off-chip signaling for chips assembled on the silicon interposer. Compared to conventional air-cooling, embedded microfluidic cooling is utilized for better cooling and thermal isolation of chips on the

silicon interposer. A test vehicle consisting of a silicon interposer and silicon dice with microfluidic I/Os and embedded microfluidic heat sink is fabricated and assembled for thermal measurements. At a flow rate of 50 mL/min, the measured temperature is 55.9 C for a power density of 97.0 W/cm^2, which represents a normalized thermal resistance of 0.24 K·cm^2/W. The thermal simulations based on the measured thermal resistance show that a 40.1% reduction in silicon interposer temperature is achieved with microfluidic cooling compared to air cooling. Moreover, thermal coupling between the dice on the silicon interposer is significantly reduced with microfluidic cooling, which significantly benefits integration density and signaling performance by integrating chips more closely and reducing interconnect length.

CHAPTER IV

ON-DIE POWER DISTRIBUTION NETWORK MODELING, SIMULATION, AND ANALYSIS

4.1 Introduction

Power delivery is another major challenge facing high-performance computing systems besides cooling and signaling. High-performance chips drain a large amount of current which causes large power supply noise (PSN) and reliability challenges for power delivery network (PDN). The scaling of frequency and supply voltage for high-performance chips leaves less noise margin and thus further exacerbates the power integrity issue. Power noise margin is becoming tight even for a single chip; when multiple chips are stacked, the power/ground TSVs introduce more parasitics into PDN and the amount of current required is multiplied. Thus, power integrity becomes more challenging for 3D systems [77], [78]. The microfluidic cooling technology, which requires integrating microfluidic heat sinks to silicon dice, could make it even more challenging due to longer TSVs.

Therefore, it is important to understand the impact of 3D stacking and microfluidic cooling on power delivery. In this chapter, a compact physical model for on-die power distribution network is used to investigate the impact of 3D stacking and integrating microfluidic heat sink on power supply noise. Conventionally, increasing the number of power/ground I/Os and decoupling capacitors are used to suppress PSN. However, both of them are precious resources that have to be carefully allocated for effective use. Moreover, a numerical PDN simulator, which is more flexible and faster than the compact model, is developed for design space exploration and avoiding over-design and under-design of power distribution networks.

4.2 Power Delivery Analysis for Microfluidic Cooled 3-D ICs

Integrating an embedded microfluidic heat sink increases silicon die thickness and TSV length. The increased resistive and inductive parasitics due to longer TSVs in turn lead to an increase in power supply noise. Thus, microfluidic cooling introduces a new power delivery challenge, as shown in Figure 70. It is important to understand the impact of an embedded microfluidic heat sink on power delivery and to investigate effective ways to suppress power supply noise (PSN). In this section, power supply noise of a 3D chip stack with microfluidic cooling is simulated and analyzed using a frequency-domain compact physical model [16].

4.2.1 Frequency Domain Compact Physical Model for On-Die Power Distribution Network

The model considers both IR-drop and simultaneous switching noise (SSN) and focuses on the first noise droop (mid-frequency noise) [79], which results from the

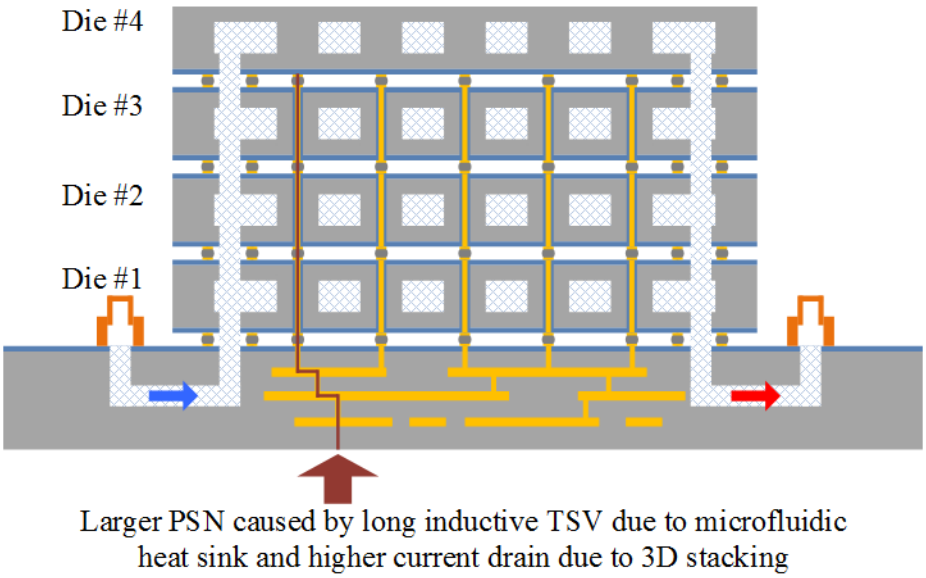


Figure 70: Larger power supply noise due to longer TSVs and higher current drain for microfluidic-cooled 3D stack.

interaction of on-die decoupling capacitors and package inductance. On-die global power distribution grids consist of power/ground pads and orthogonal interleaved power/ground interconnects on the top two metal layers, as shown in Figure 71. Under the assumptions that the current density and the on-die decoupling capacitors are uniformly distributed, the grids can be divided into identical unit cells. Within each unit cell, two adjacent power/ground nodes and the area in-between can be modeled by the circuit model shown in Figure 71, where R_s is the resistance of an interconnect segment connected to the node, Δ is the length of the segment, $J(s)$ is on-die current density in the frequency-domain, and C_d is the on-die decoupling capacitance density.

Based on this circuit model, partial differential equation (22) is derived to represent the voltage distribution within a unit cell (the derivation details in [16]).

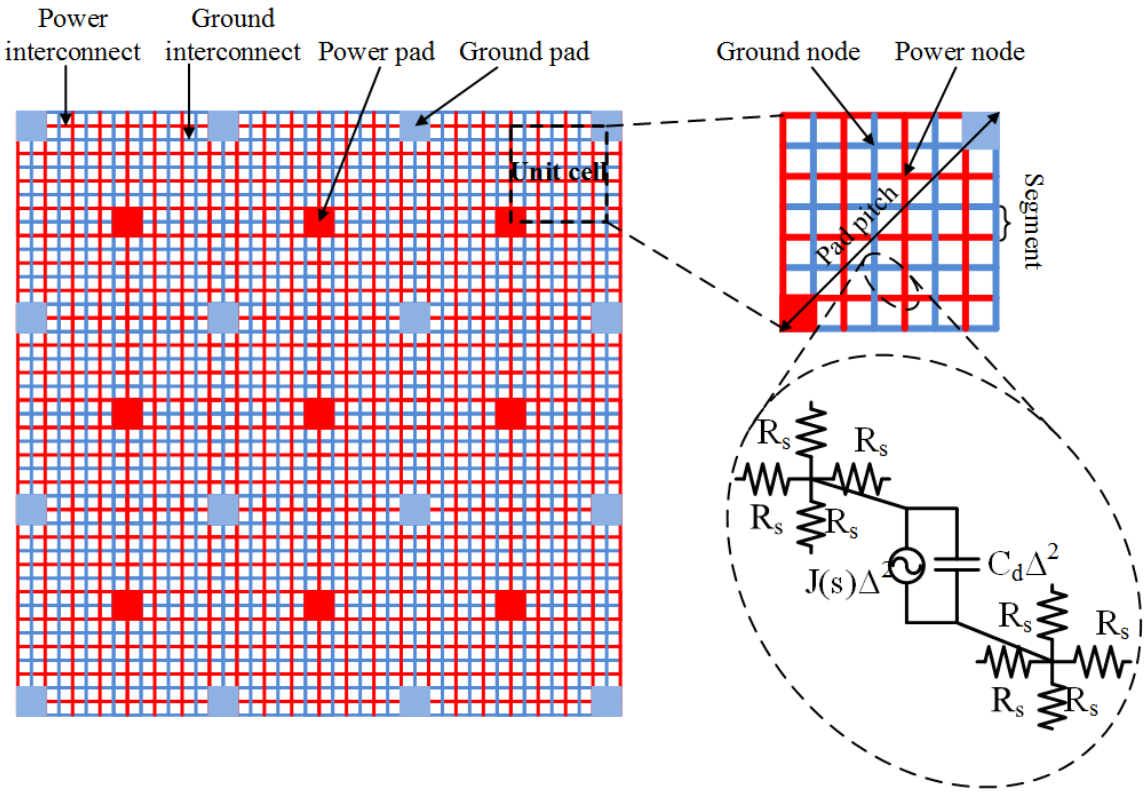


Figure 71: On-die global power distribution grid is divided into unit cells which are modeled by the simplified circuit.

$$\bigtriangledown^2 V(x,y,s) = R_s J(s) + R_s V(x,y,s) 2sC_d + \Phi(x,y,s) \tag{22}$$

where $V(x,y,s)$ denotes the voltage level at location (x,y) in a unit cell, $\Phi(x,y,s)$ is the source function of the partial differential equation (PDE) representing the voltage applied to the pad and can be expressed as

$$\Phi(x,y,s) = -R_s \frac{V(\alpha D_{pad}, 0, s)}{4(sL_p + R_p)} \delta(x)\delta(y) \tag{23}$$

where $V(\alpha D_{pad}, 0, s)$ is the equivalent voltage at location $(\alpha D_{pad}, 0, s)$, assuming lower-left corner of the unit cell is the origin; α is a coefficient for pad shape [44], and D_{pad} is the side length of a quarter pad; L_p and R_p are the package inductance and resistance; $\delta(x)\delta(y)$ is the product of two delta functions, indicating the source is only applied to the origin.

Since it is assumed that current is uniformly distributed, no current flows across the four boundaries of the unit cell. Thus, the following boundary conditions are derived:

$$\frac{\partial V(x,y,s)}{\partial x} \mid_{x=0} = 0, \frac{\partial V(x,y,s)}{\partial x} \mid_{x=a} = 0, \frac{\partial V(x,y,s)}{\partial y} \mid_{y=0} = 0, \frac{\partial V(x,y,s)}{\partial y} \mid_{y=a} = 0 \tag{24}$$

where a is the edge length of the unit cell.

Next, the model was expanded to 3D grids by incorporating the TSVs. The following PDEs for 3D grids were derived [16]:

$$\bigtriangledown^2 V_i(x,y,s) = R_{si} J_i(s) + R_{si} V_i(x,y,s) 2sC_{di} + \Phi_i(x,y,s) \tag{25}$$

where i indicates the i_{th} die in a stack.

The source function for die #1 (bottom die) is as follows:

$$\Phi_1(x,y,s) = -R_{s1}[\frac{V_1(\alpha D_{pad},0,s)}{4(sL_p+R_p)} + \frac{V_2(\alpha D_{pad},0,s)-V_1(\alpha D_{pad},0,s)}{4(sL_{TSV}+R_{TSV})}]\delta(x)\delta(y) \quad (26)$$

where L_{TSV} and R_{TSV} are the inductance and resistance of the TSV, respectively. The source function for die #i is given by equation (27).

$$\begin{aligned}\Phi_i(x,y,s) = &- R_{si}[\frac{V_i(\alpha D_{pad},0,s)-V_{i-1}(\alpha D_{pad},0,s)}{4(sL_p+R_p)} \\ &+ \frac{V_{i+1}(\alpha D_{pad},0,s)-V_i(\alpha D_{pad},0,s)}{4(sL_{TSV}+R_{TSV})}]\delta(x)\delta(y)\end{aligned} \quad (27)$$

The boundary conditions for each die in the stack remain the same as in the 2D case. The set of frequency-domain PDEs can be solved analytically [16], which enables a quick assessment of PSN for 3D ICs.

4.2.2 Power Supply Noise Simulation and Analysis for 3D Stack

Based on the model described in the previous section, PSN of a 3D stack consisting of four dice was simulated. Table 10 lists the parameters of the die stack. We

Table 11: Parameters of the 3D die stack

Parameters	Value
Number of stacked dice	4
Die thickness (TSV length)	50 μm
TSV diameter	10 μm
Die area	100 mm^2
On-die current density	1 A/mm^2
On-die decap percentage	10% of die area
Number of pad/TSV	2500
Pad/TSV pitch	202 μm
Pad shape parameter	0.2
Package inductance	0.5 nH
Wire segment length	28.3 μm
Wire width	2 μm
Wire thickness	1 μm

assume homogeneous integrated dice in the stack and every die in the stack switching simultaneously for worst case PSN simulation.

Figure 72 illustrates the PSN of each die in the stack (solid line with cross marks). As expected, the PSN increases gradually from die #1 to die #4, with die #4 having the maximum PSN (240.4 mV). Compared to the PSN of a single die (118.8 mV), PSN of the stack (die #4) increases by 102.4%. Next, the impact of die thickness on PSN was investigated, which is very relevant for dice with embedded microfluidic cooling. The die thickness increases from 50 μm to 250 μm due to the integration of the micropin-fin heat sink (all other parameters of the stack are unchanged). The PSN increases from die #1 to die #4 with a maximum PSN of 377.3 mV, a 217.6% increase compared to the single die case, as shown in Figure 72. Therefore, PSN

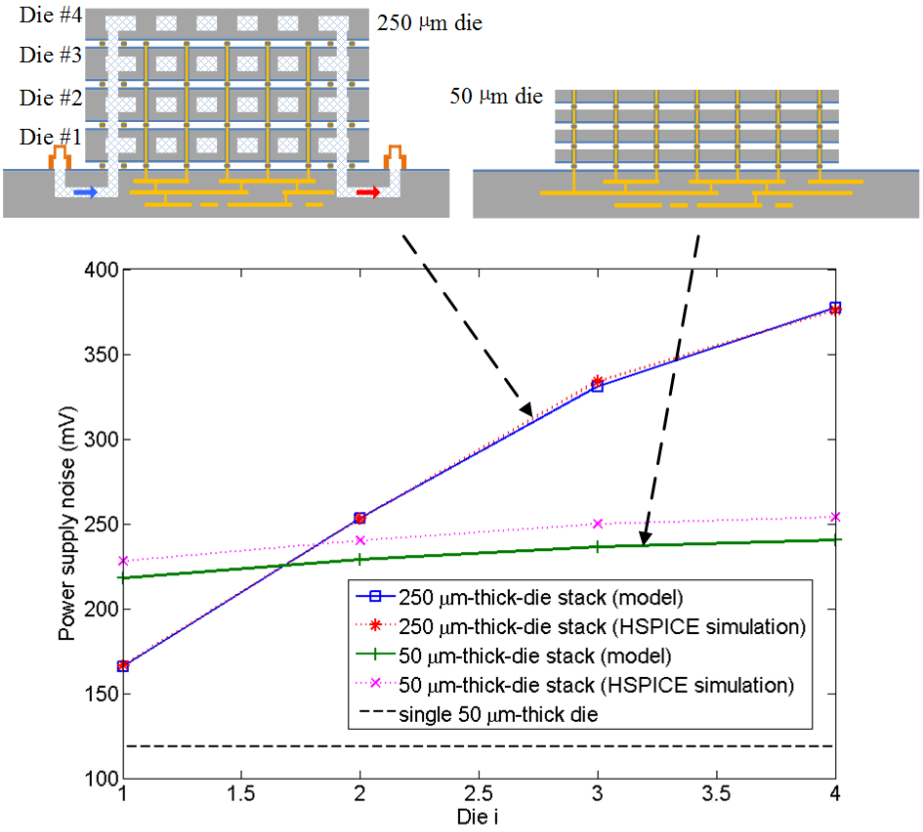


Figure 72: PSN of two 4-die stacks consisting of 50 μm thick dice and 250 μm thick dice, respectively.

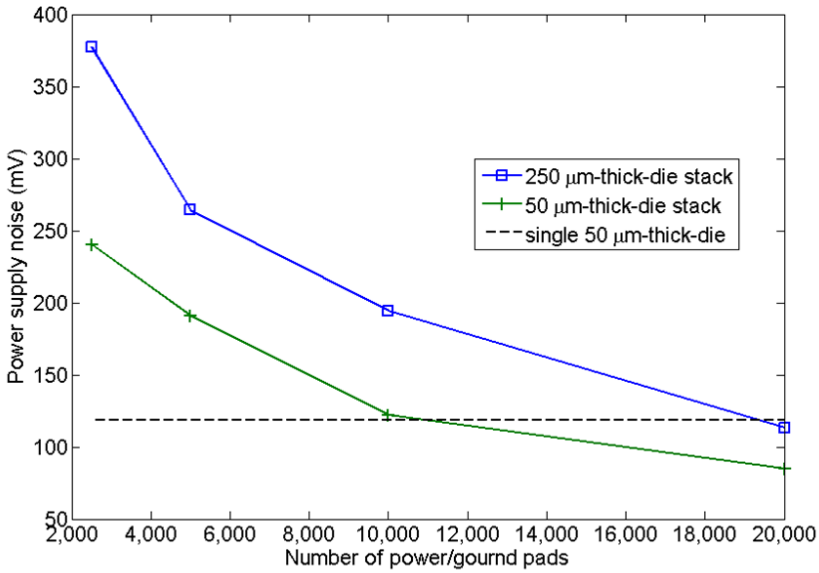


Figure 73: PSN of two 4-die stacks as a function of the number of power/ground pads.

suppression is critical for 3D ICs. PSN of the two stacks are also simulated using HSPICE, as shown by the two dotted lines in Figure 72. The difference between the compact model and HSPICE [80] simulation is about 5%.

Increasing the number of power/ground pads is one of the effective ways of suppressing PSN. Figure 73 illustrates the PSN of the two stacks (50 μm thick die and 250 μm thick die) as a function of the number of power/ground pads. The PSN is significantly reduced with increasing number of power/ground pads. For the 50-μm-thick-die stack, PSN of the stack drops to the single die level when the number of pads increases from approximately 2,500 to approximately 10,000. For the 250 μm-thick-die stack, approximately 20,000 power/ground pads are needed, as shown in Figure 73.

Next, the impact of the number of dice in a stack was investigated. The PSN of a 2-die stack (all other parameters unchanged from Table 3) and a 4-die stack are plotted in Figure 74. Obviously, PSN of the 2-die stack (top most die) is less

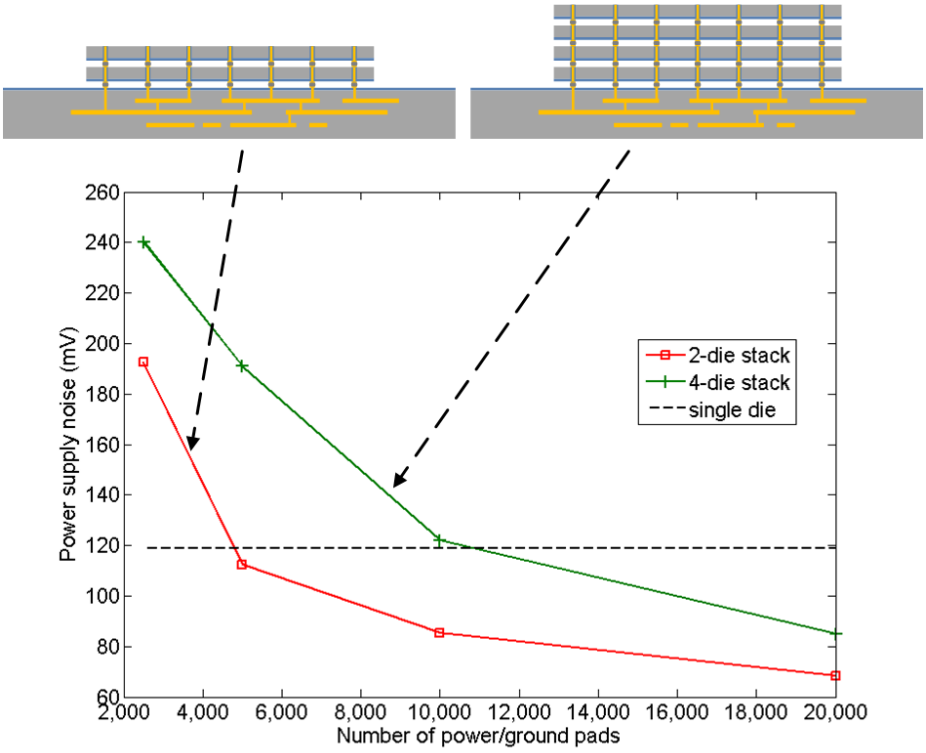


Figure 74: PSN of a 2-die stack and a 4-die stack as a function of the number of power/ground pads.

than that of the 4-die stack. To achieve single die level PSN, the 2-die stack requires approximately 5,000 power/ground pads, while the 4-die stack requires approximately 10,000 power/ground pads, as shown in Figure 74.

Conventionally, PSN can be suppressed by increasing the amount of on-die decoupling capacitors, although this is costly. Figure 75 compares the PSN of the 4-die stack when the area allocated to the decoupling capacitors in each die is increased from 10% to 20%. With 20% area allocation, the PSN is fairly well suppressed but still not close to the PSN of a single die. Potentially larger area for the decoupling capacitors might be needed, but of course this is cost prohibitive.

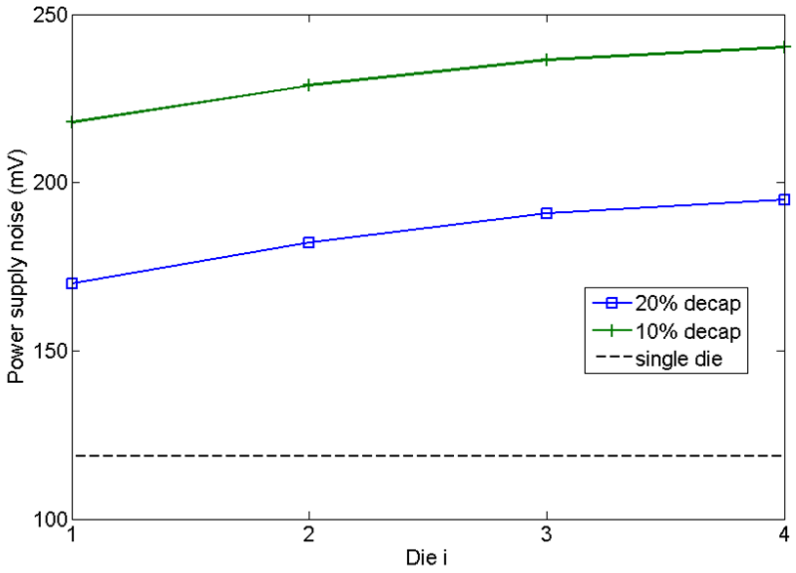


Figure 75: PSN of two 4-die stacks with 10% and 20% on-die decaps, respectively.

4.3 Numerical Modeling of Uniform On-Die Power Distribution Network

A time-domain numerical power distribution network simulator based on finite difference method and distributed circuit model for on-die power distribution network is developed. Compared to the frequency-domain PDN model presented in the previous section, the time-domain model enables power supply noise simulation across the die, solves power supply noise directly in the time domain, and provides much more simulation flexibility, such as different grid structures, power/ground pad distributions, decoupling capacitor allocations, and power density distributions.

4.3.1 Numerical Modeling of On-Die Power Distribution Network

The on-die power distribution network consists of global and local networks. The global network distributes supply current across the die, and the local network delivers the supply current from the global network to the active devices. In this work, the global network is modeled since it contributes most of the parasitics.

The distributed circuit model is similar to the one in Section 4.2. Figure 76(a) illustrates the global PDN on the top two metal layers of a die, which consists of power/ground grids with pads. The orthogonal power/ground grids are interleaved as shown in Figure 76(b). Under the uniform PDN assumption, which assumes that 1) the power/ground pads are uniformly distributed, 2) the power density is uniformly distributed, 3) the on-die decoupling capacitance is uniformly distributed, and 4) the grid segments are uniform, the on-die PDN can be divided into many identical unit cells, as shown in Figure 76(c). A unit cell is comprised of a quarter of the power pad, a quarter of the ground pad, and the grid segments in-between.

With the uniform PDN assumption, we can model the unit cell since it fully represents the on-die PDN. Figure 77 illustrates the modeling approach and circuit models for the nodes within the unit cell. First, the power/ground grids in a unit

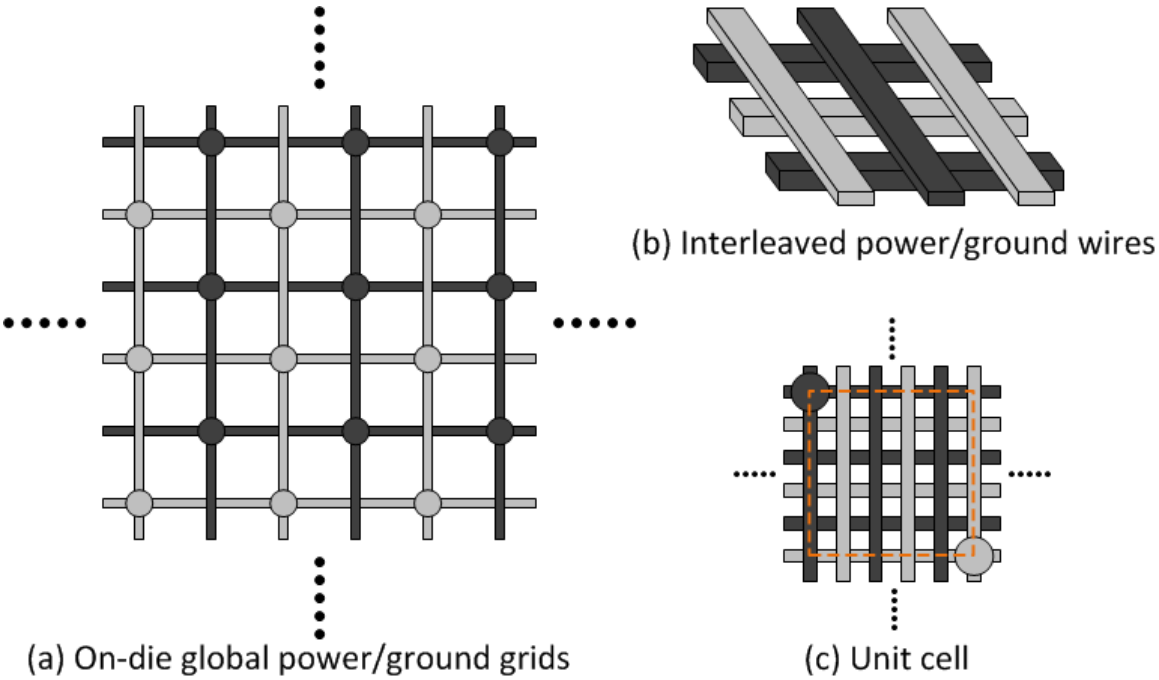


Figure 76: (a) On-die global power/ground grids: power pads and grid segments (dark colored), ground pads and grid segments (light colored); (b) Interleaved structure of power/ground segments; (c) Unit cell (confined by a pair of power and ground pads).

cell are separated into two isolated grids following the approach in [42], as shown in Figure 77(a-c). Since the power and ground grids are identical, the same circuit model can be applied.

There are two types of nodes in the grid, which are intersections of the grid segments. A pad node is a node at the corner of the grid and covered by a power/ground pad, while the remainder nodes represent the intersection of two orthogonal wires. Each node has neighboring nodes and an associated region with distributed decoupling capacitance and current drain (to represent gate activity), as shown in Figure 77(b)(c). Figure 77(d) illustrates the circuit model for the pad node, which is connected to its two neighboring nodes with segment resistance R_x and R_y. C and J

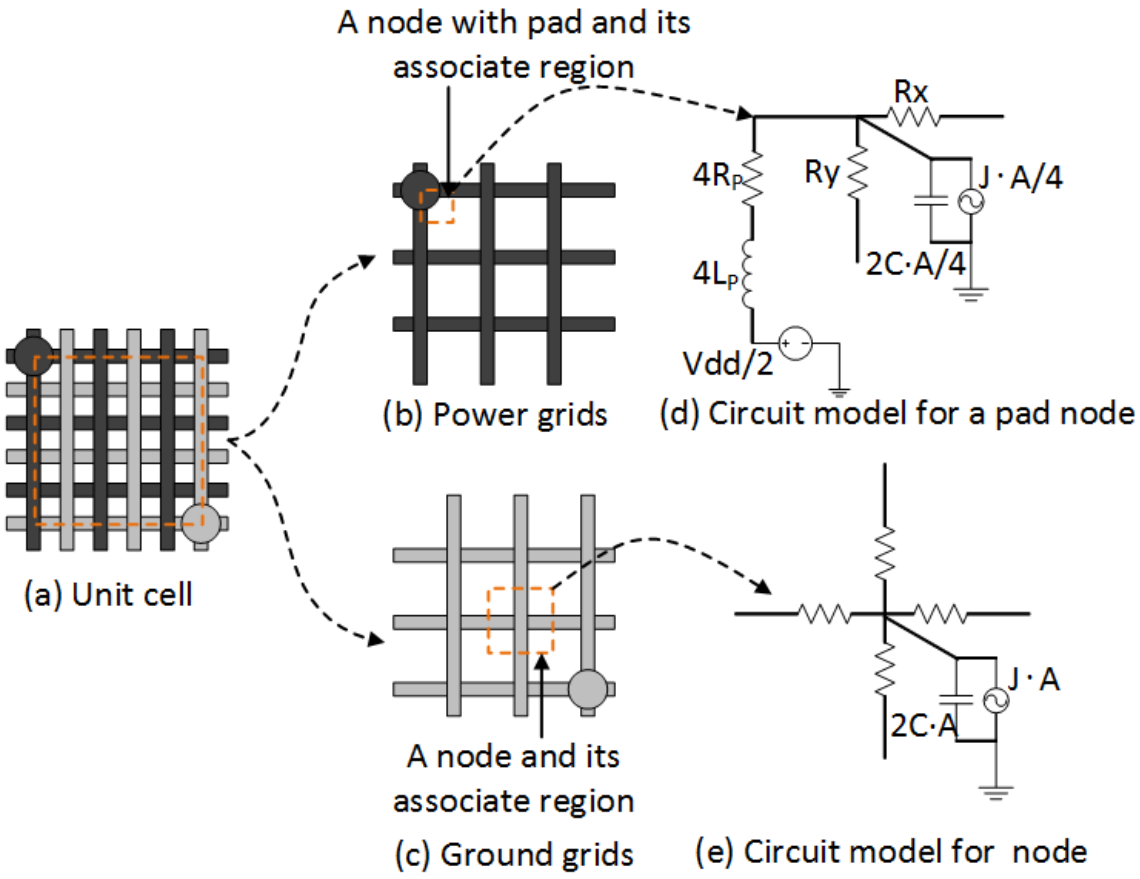


Figure 77: Split the power/ground grids of a unit cell to separate identical power grids and ground grids; circuit models the nodes in the grids.

are the on-die decoupling capacitance density and current density, respectively. A is the area of the associated region of a node, which has four neighbors. Therefore, the associated decoupling capacitance and current of the pad node is $2 \cdot C \cdot A/4$ and $J \cdot A/4$, respectively. The decoupling capacitance density is multiplied by two because the decoupling capacitance in two grids is split. R_p and L_p are the resistance and inductance of the package-level PDN associated with each pad, respectively. Since only a quarter of the pad is included in a unit cell, it should be multiplied by 4. The supply voltage is divided by two because the power/ground grids are split into two identical grids.

Based on the above circuit models and Kirchhoffs circuit law, difference equations are derived to describe the voltage distribution over the grids. Equation (28) and (29) are for the circuit model in Figure 77(d).

$$\begin{aligned} &\frac{V(0,0,t) - V(\Delta x,0,t)}{R_x} + \frac{V(0,0,t) - V(0,\Delta y,t)}{R_y} \\ &= -J(t) \cdot \frac{\Delta x \cdot \Delta y}{4} - 2C \cdot \frac{\Delta x \cdot \Delta y}{4} \cdot \frac{V(0,0,t) - V(0,0,t-\Delta t)}{\Delta t} - I_P(0,0,t) \end{aligned} \tag{28}$$

$$V(0,0,t) + 4R_P \cdot I_P(0,0,t) + 4L_P \cdot \frac{I_P(0,0,t) - I_P(0,0,t-\Delta t)}{\Delta t} = \frac{Vdd}{2} \tag{29}$$

where is $V(0,0,t)$ is the unknown voltage of the pad node at time t assuming the pad node is at the origin; Δx and Δy are the segment lengths in x and y axes, respectively; $V(\Delta x,0,t)$ and $V(0,\Delta y,t)$ are the unknown voltages of the two neighbor nodes at time t; $J(t)$ is the current density at time t; C is the decoupling capacitance density; $\frac{\Delta x \cdot \Delta y}{4}$ is the associated region area of the pad node; $I_P(0,0,t)$ is the unknown current from the package to the pad node at time t; R_P is the package PDN resistance; L_P is the package PDN inductance; Vdd is the system supply voltage.

Similarly, difference equation (30) is derived using the circuit model for a regular node, as in Figure 77(e).

$$\frac{V(x,y,t)-V(x+\Delta x,y,t)}{R_x}+\frac{V(x,y,t)-V(x,y+\Delta y,t)}{R_y}+\frac{V(x,y,t)-V(x-\Delta x,y,t)}{R_x}$$
$$+\frac{V(x,y,t)-V(x,y-\Delta y,t)}{R_y}$$
$$=-J(t)\cdot\Delta x\cdot\Delta y-2C\cdot\Delta x\cdot\Delta y\cdot\frac{V(x,y,t)-V(x,y,t-\Delta t)}{\Delta t} \tag{30}$$

Using the circuit models and the difference equations above, a distributed circuit model, as shown in Figure 78(a), and a set of difference equations are derived for all nodes in the unit cell grid. The difference equations are numerically solved for the voltage distribution using the trapezoid scheme [81]. Since the voltage distribution is a function of time, it is iteratively solved as time advances with an initial current source excitation. In this work, a simple step function of predefined rise time is used, as in Figure 78(a).

4.3.2 Modeling of 3D Power Distribution Network

In this section, the 2D distributed circuit model is extended to grids in 3-D ICs. Figure 78(b) shows the distributed circuit model for a 2-tier die-stack with TSV resistance and inductance. After integrating the TSV branch into the grids, the circuit models for the pad nodes on different tiers are derived. Difference equations (31-33) are derived for pad node on different tiers based on the new circuit models. The circuit model for the regular nodes (intersection of orthogonal wires) remains the same. Figure 79 shows the circuit models for pad nodes on different tiers in a 3D stack.

$$\frac{V_1(0,0,t)-V_1(\Delta x,0,t)}{R_x}+\frac{V_1(0,0,t)-V_1(0,\Delta y,t)}{R_y}$$
$$=-J_1(t)\cdot\frac{\Delta x\cdot\Delta y}{4}-2C\cdot\frac{\Delta x\cdot\Delta y}{4}\cdot\frac{V_1(0,0,t)-V_1(0,0,t-\Delta t)}{\Delta t} \tag{31}$$
$$-I_P(0,0,t)-I_{TSV\_1}(0,0,t)$$

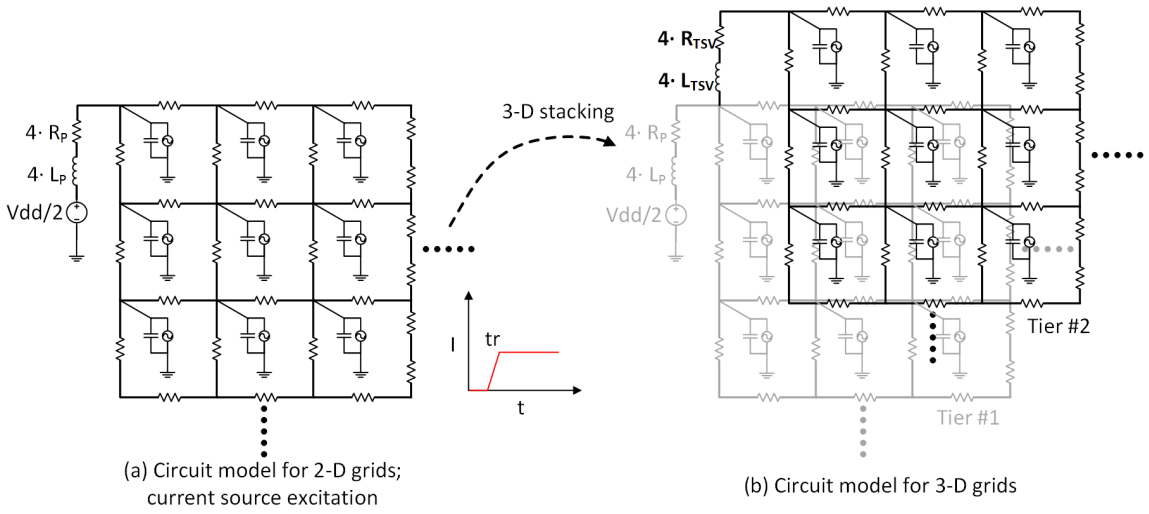


Figure 78: (a) Distributed circuit model for 2-D grids; (b) Extend the circuit model for 2-D grids to 3-D grids by integrating resistance and inductance of TSVs.

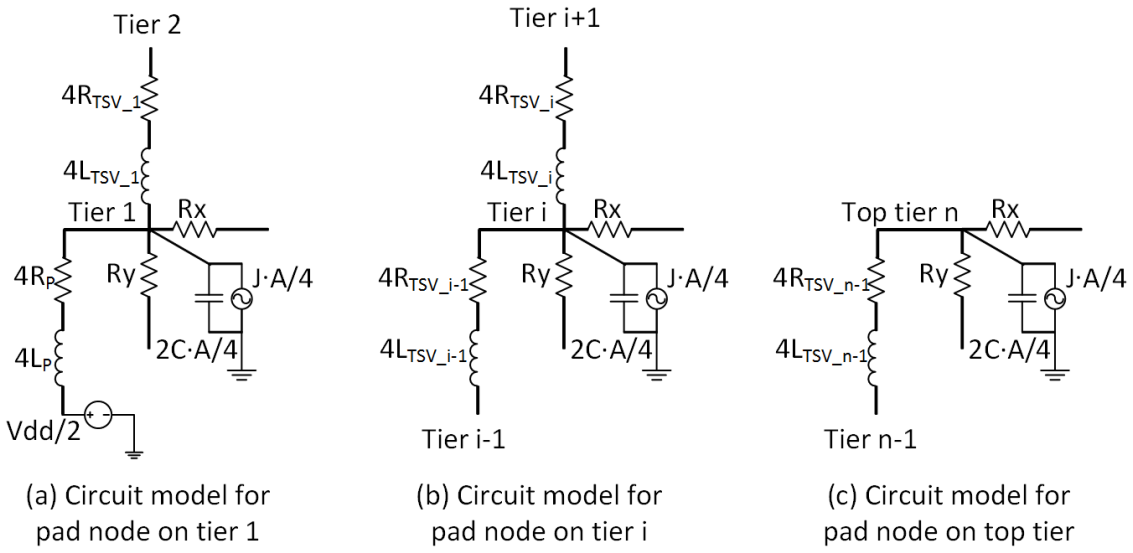


Figure 79: Circuit model for the pad nodes in 3-D grids.

$$\begin{aligned}
&\frac{V_i(0,0,t)-V_i(\Delta x,0,t)}{R_x}+\frac{V_i(0,0,t)-V_i(0,\Delta y,t)}{R_y}\\
&=-J_i(t)\cdot\frac{\Delta x\cdot\Delta y}{4}-2C\cdot\frac{\Delta x\cdot\Delta y}{4}\cdot\frac{V_i(0,0,t)-V_i(0,0,t-\Delta t)}{\Delta t}\\
&-I_{TSV_i}(0,0,t)-I_{TSV_i-1}(0,0,t)
\end{aligned}\tag{32}$$

$$V_i(0,0,t) - V_{i-1}(0,0,t) = 4R_{TSV} \cdot I_{TSV\_i-1}(0,0,t) + 4L_{TSV} \cdot \frac{I_{TSV\_i-1}(0,0,t) - I_{TSV\_i-1}(0,0,t-\Delta t)}{\Delta t} \quad (33)$$

where $V_i(0,0,t)$ is the unknown voltage of the pad node on tier $i(>1)$ at time t; $I_{TSV_i}(0,0,t)$ is the unknown current of the TSV branch on tier i at time t; R_{TSV} and L_{TSV} are the TSV resistance and inductance. Since a unit cell only possesses a quarter of TSV, R_{TSV} and L_{TSV} should be multiplied by four in the unit cell model.

4.4 Power Supply Noise Analysis Based on The Numerical Unit Cell Modeling and Simulation

Using the numerical PDN model for unit cell developed in the previous section, PSN of a 4-die stack is simulated and analyzed in this section. The simulation parameters used for the die stack are listed in Table 11. We assume a homogeneous 3-D integration in which all dice in the stack are the same.

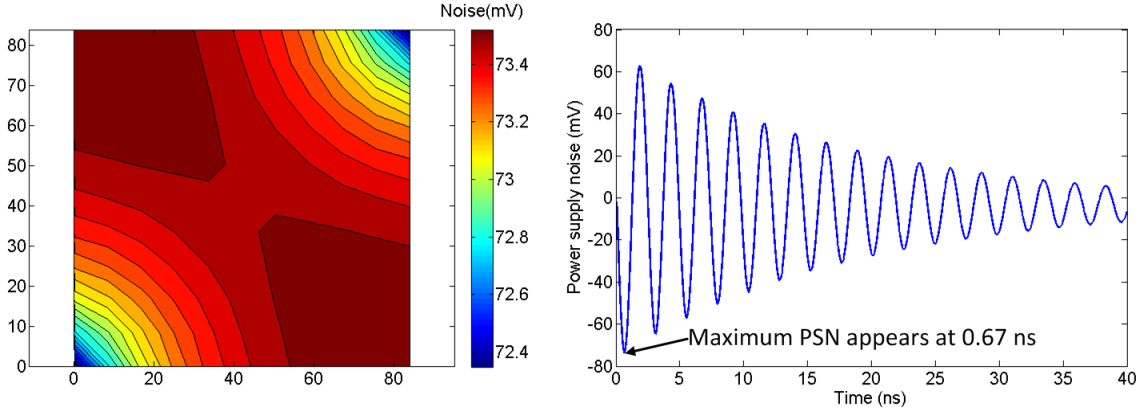
The size of the unit cell is 84 × 84 μm^2 with a pad/TSV pitch of 118.8 μm (distance between a pair of power and ground pads at two opposite corners of a unit cell). The grid fineness is defined as the number of intercrossing wires in the grids, which determines the number of nodes in the grids. The maximum on-die current density is 1 A/mm^2. In the simulation, we assume the current drain rises from 0 to 1 A/mm^2 linearly in 0.01 ns and all dice in the stack start switching at the same time. This would emulate the worst case PSN.

First, PSN of a single 2-D unit cell is simulated. Figure 80(a) shows the simulated PSN map of the unit cell, which is symmetric along the two diagonals. The lower-left and upper-right corners have the smallest PSN because they are covered by the power and ground pads, which are connected to package directly. PSN increases away from the power and ground pads due to additional parasitics of the on-die grids. Therefore, the upper-left and lower-right corners have the largest PSN. Figure 80(b) shows the

Table 12: Simulation parameters of the 3D die stack

Parameters	Value
Number of stacked dice	4
Die thickness (TSV length)	50 μm
TSV diameter	7 μm
Unit cell size	84 $\times$ 84 μm^2
Pad/TSV pitch	118.8 μm
On-die current density	1 A/mm^2
On-die decap density	5.3 nF/mm^2
Grid fineness	11 $\times$ 11
Wire segment length	28.3 μm
Wire width	2 μm
Wire thickness	1 μm
Package inductance	0.5 nH
Package resistance	0.01 nΩ
current rise time	0.1 ns
Δt	0.01 ns
Vdd	1 V

PSN waveform at the upper-left and lower-right corners. The fluctuation is caused by the interaction of the on-die decoupling capacitance and package inductance, and the damping magnitude is due to the resistive parasitics. The largest PSN magnitude



(a) Simulated Power supply noise map (b) Power supply noise wave

Figure 80: (a) Simulated power supply noise map of a 2-D unit cell at 0.67 ns. (b) Power supply noise wave at no-pad corners (upper left and lower right); the maximum PSN is 73.6 mV at 0.67 ns.

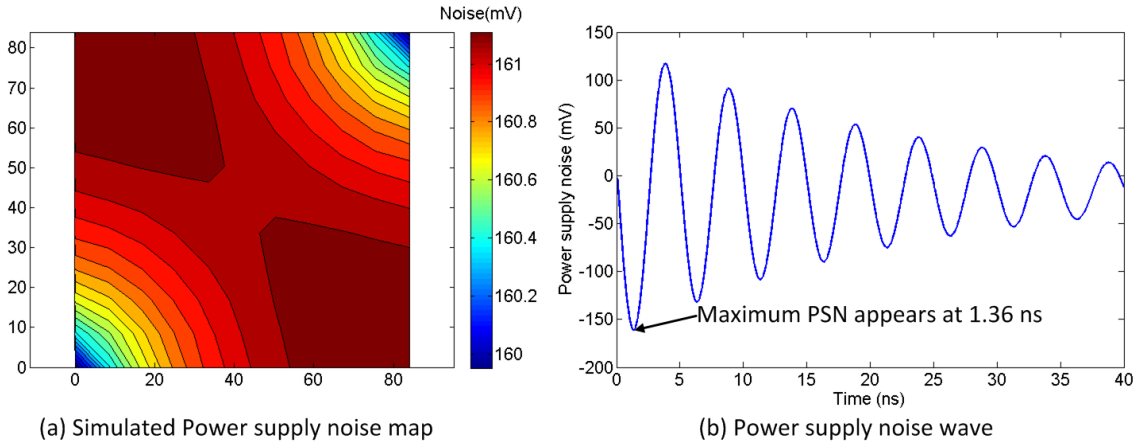


Figure 81: (a) Simulated power supply noise map of the upper unit cell in a 4-tier stack at 1.36 ns. (b) Power supply noise wave at no-TSV corners (upper left and lower right); the maximum PSN is 161.2 mV at 1.36 ns.

of 73.6 mV appears at 0.67 ns assuming that the current begins to rise at 0 s.

In the 4-die stack, the top die has the largest PSN because of the longest TSVs. Figure 81 shows the PSN map of the top die and PSN waveform at the upper-left and lower-right corners with no pad/TSV. The PSN distribution pattern is the same as that of 2-D case. The largest PSN magnitude is 161.2 mV, an approximately 120% increase due to 3-D stacking. The largest PSN appears at 1.36 ns.

The simulation results of the 4-die stack are verified with HSPICE, as shown in Figure 82. The difference is less than 1% between our time-domain finite difference method based simulation and HSPICE simulation.

Next, the impact of the grid fineness on PSN simulation is investigated. Figure 83 shows the PSN of each tier in the 4-die stack with different grid fineness. All other parameters are the same as listed in Table 11. There is a relatively small difference in PSN when the grid fineness decreases from 11 $\times$ 11 to 6 $\times$ 6, as shown in Figure 83. The difference is less than 1% when the grid fineness is further reduced to 2 $\times$ 2, which only considers the segments at the edges of the unit cell. This indicates that we can significantly reduce the number of nodes for a unit cell with a small accuracy loss, which would enable full die simulation, to be discussed in the next section.

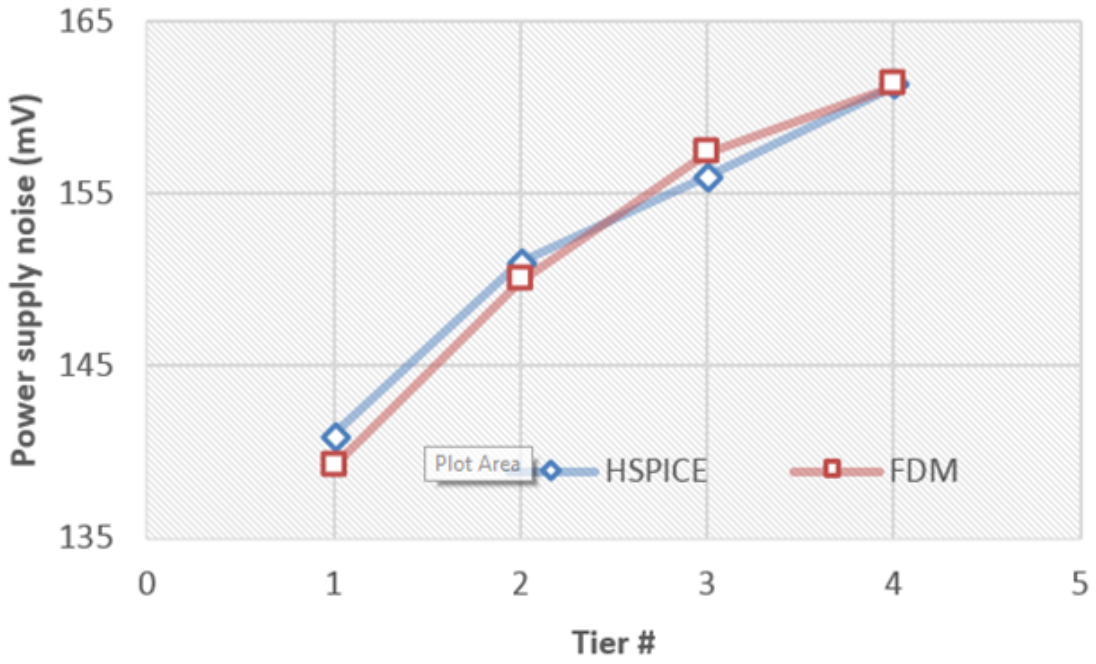


Figure 82: Power supply noise simulation for the 4-tier stack using FDM and HSPICE.

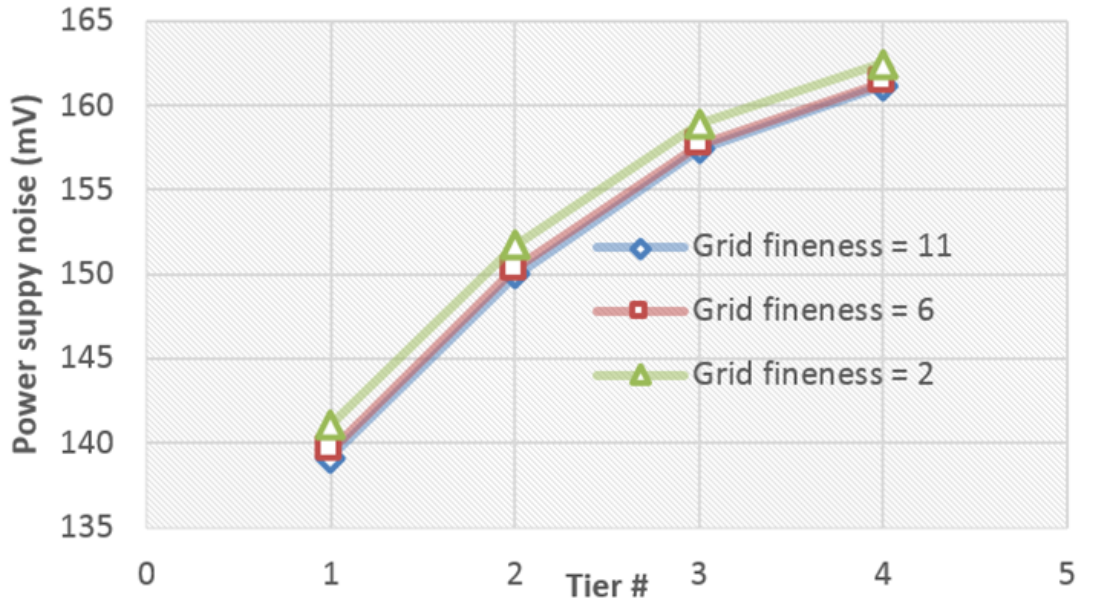


Figure 83: Power supply noise of each tier in the 4-tier stack with different grid fineness.

4.5 Full Chip Non-uniform Power Distribution Network Numerical Modeling, Simulation, and Analysis

In this section, the distributed circuit model and difference equations are derived for a full die with multiple blocks of different decoupling capacitance and power densities based on the method described in the previous sections. PSN of a 2-die stack is simulated and the impact of adding decoupling capacitance and power/ground pads is analyzed.

4.5.1 Numerical Modeling of Full Chip Power Distribution Network

Figure 84 illustrates the distributed circuit model for a 2-die stack. Different from the unit cell circuit model, each node in this circuit model is connected to a pad/TSV. Different values of decoupling capacitance and current can be assigned to each node to account for non-uniform distribution of decoupling capacitance and current.

Based on the circuit model, difference equations for the nodes on tier i are derived as follows.

$$\begin{aligned}
&\frac{V_{i,k}(x,y,t)-V_{i,k}(x+\Delta x,y,t)}{R_x}+\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y+\Delta y,t)}{R_y}\\
&+\frac{V_{i,k}(x,y,t)-V_{i,k}(x-\Delta x,y,t)}{R_x}+\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y-\Delta y,t)}{R_y}\\
&=-J_{i,k}(t)\cdot\Delta x\cdot\Delta y-2C_{i,k}\cdot\Delta x\cdot\Delta y\cdot\frac{V_{i,k}(x,y,t)-V_{i,k}(x,y,t-\Delta t)}{\Delta t}\\
&+I_{TSV_i-1,k}(x,y,t)-I_{TSV_i,k}(x,y,t)
\end{aligned} \tag{34}$$

$$\begin{aligned}
V_{i,k}(x,y,t)-V_{i-1,k}(x,y,t)&=4R_{TSV}\cdot I_{TSV_i-1,k}(x,y,t)\\
&+4L_{TSV}\cdot\frac{I_{TSV_i-1,k}(x,y,t)-I_{TSV_i-1}(0,0,t-\Delta t)}{\Delta t}
\end{aligned} \tag{35}$$

where $V_{i,k}(x,y,t)$ is voltage of node in block k on tier i since a die has multiple blocks; $I_{TSV_i-1,k}(x,y,t)$ is the current flowing from tier $i-1$ to tier i through the TSV and $I_{TSV_i,k}(x,y,t)$ the current flowing from tier i to tier $i+1$.

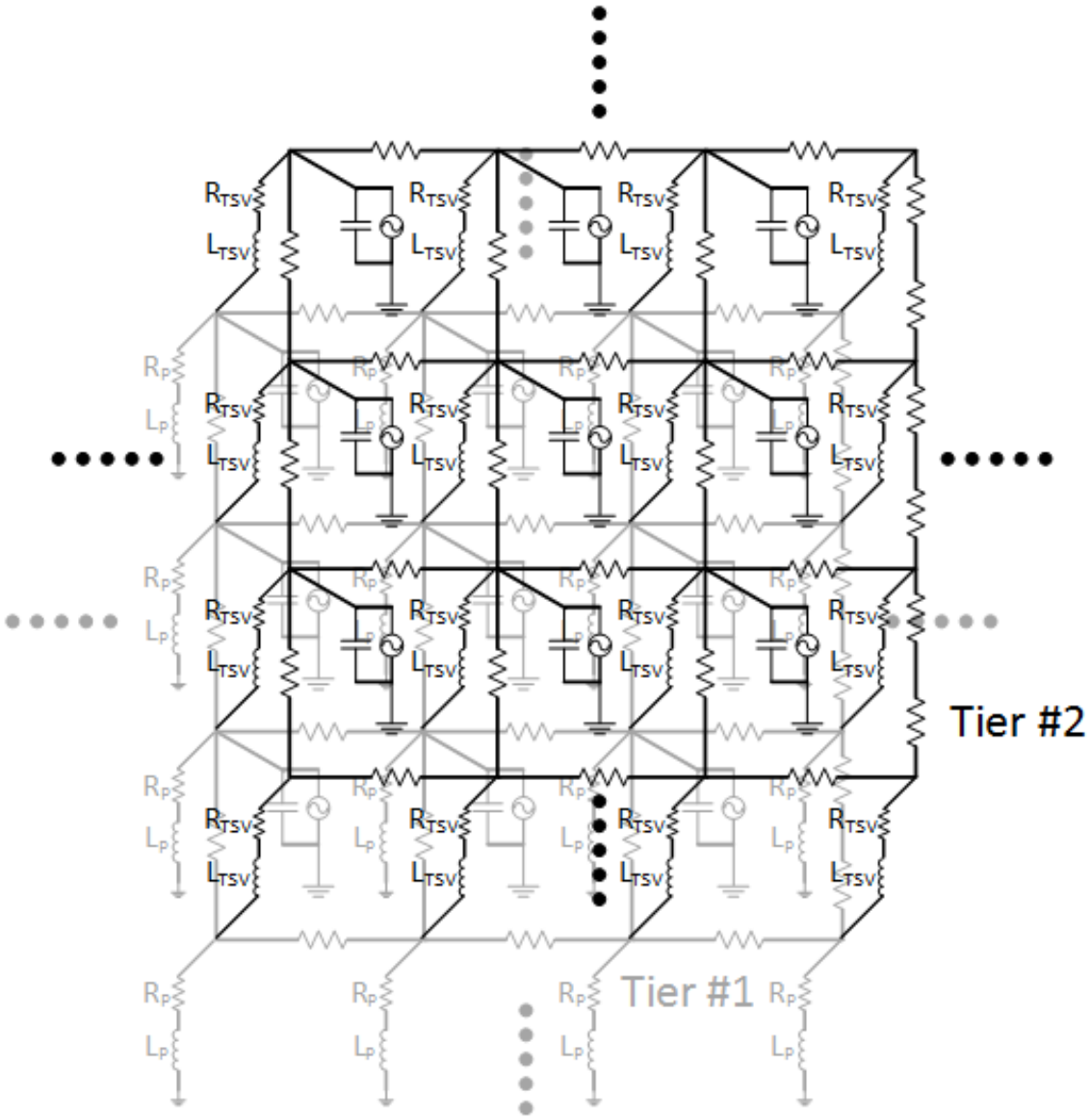


Figure 84: Distributed 3-D Circuit model for full die stack.

4.5.2 Full Chip Power Supply Noise Simulation and Analysis

The PSN of a processor die with multiple blocks is simulated using the full-die model described in the previous section. The block layout and power map are based on an Intel i7 processor [67]. The die size is 1 cm × 1 cm and the total power is 74.49 W. Figure 85(a) shows the current density distribution assuming a supply voltage of 1 V. Blocks I, II, II, and IV, which have relative large current/power density, are labeled.

Block IV has the largest current density, which is greater than 1.2 A/mm^2. Except for the current/power distribution, other parameters of the power grid are the same as those listed in Table 11.

Figure 85(b) shows the simulated PSN map for a single processor die. As expected, large current density leads to large PSN. The maximum PSN is 169.9 mV at 1.9 ns in Block IV.

Next, two processor dice are stacked using TSVs. The parameters in Table 11 are used as the baseline case. Since the two stacked dice are identical, their PSN pattern is the same. Figure 86(b) shows the simulated PSN map of the upper die, which has larger PSN than the lower die. The largest PSN increases to 242.8 mV, a 43% increase compared to the single-die case.

Besides the non-uniform distribution of power/current density, we can apply non-uniform decoupling capacitance and power/ground pad distributions using the full-die model. Increasing on-die decoupling capacitance and number of power I/Os are two effective ways of suppressing PSN. The impact of doubling decoupling capacitance density and the number of power/ground pads for the high-power blocks in the 2-die

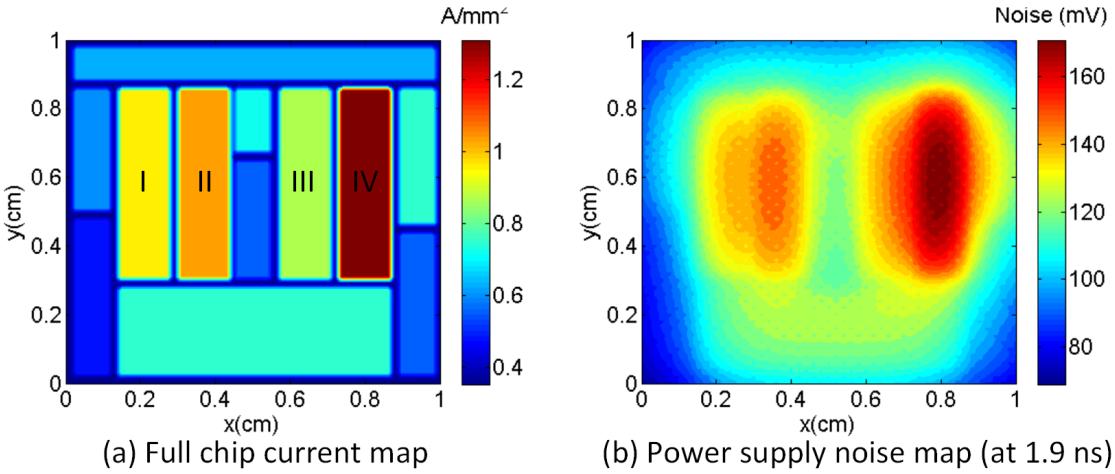


Figure 85: (a) Current map of the processor die; (b) power supply noise map of the processor die at (maximum power supply noise 169.9 mV at 1.9 ns).

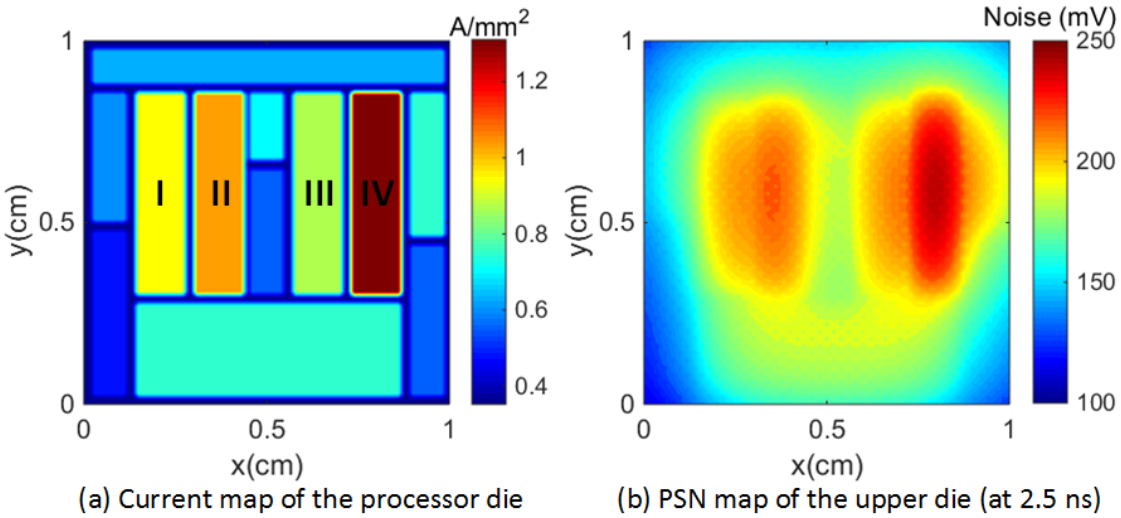


Figure 86: (a) Current map of the logic die (with four high current blocks labeled); (b) Power supply noise map of the upper die (maximum power supply noise 249.1 mV at 2.5 ns).

stack is investigated.

First, the decoupling capacitance density of Block IV is doubled for both dice in the stack while keeping all other parameters unchanged. Figure 87(a) shows the PSN map of the upper die. PSN of Block IV is suppressed and the maximum PSN occurs in Block II now, which has the second largest current density. Compared to the baseline case, the maximum PSN is suppressed to 218.1 mV, an approximately 10.2% reduction. Next, we double the decoupling capacitance density for all four labeled blocks. In this case, the PSN is suppressed to 201.0 mV, an approximately 17.2% reduction, as in Figure 87(b).

Figure 88(a) shows the PSN map of the upper die with doubled number of TSVs (power/ground pads) in Block IV. The PSN of Block IV is well suppressed and the maximum PSN now occurs in Block II. The maximum PSN of the die decreases to 209.4 mV, an approximately 13.8% reduction compared to the baseline case. Next, the number of TSVs is doubled in all four blocks. The PSN is suppressed and the maximum PSN is no longer in the four high power density Blocks I, II, III, and IV, as

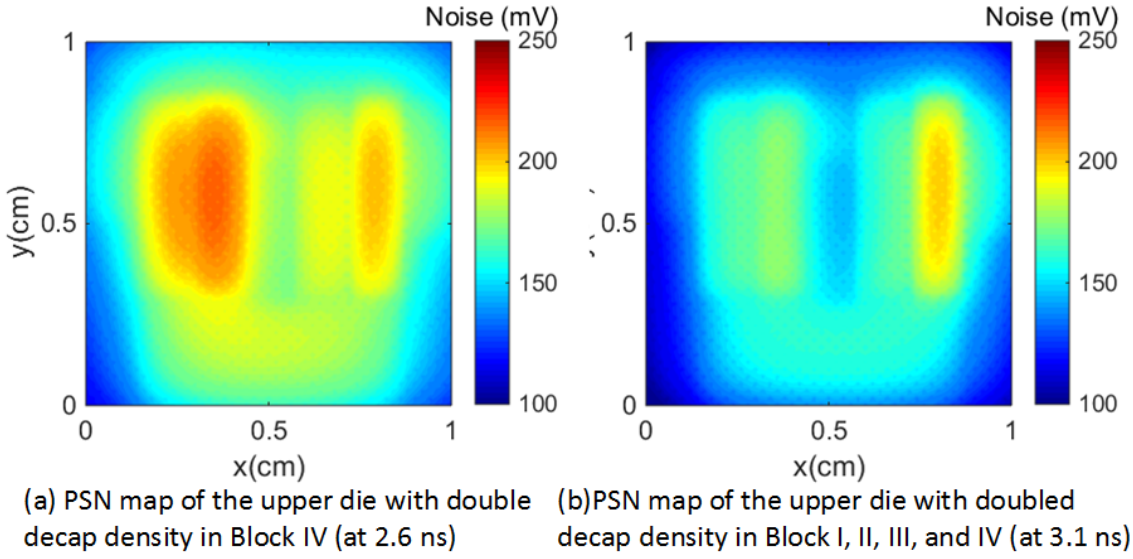
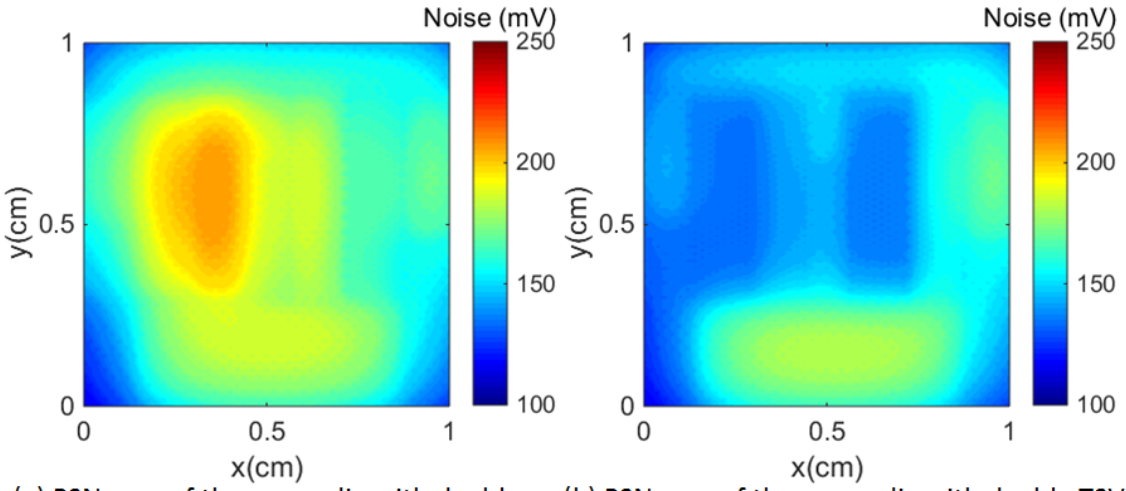


Figure 87: (a) Power supply noise map of the upper die with doubled decoupling capacitance density for block IV (maximum power supply noise 219.0 mV at 3.2 ns); (b) Power supply noise map of the upper die with doubled decoupling capacitance density for block I, II, III, and IV (maximum power supply noise 207.0 mV at 3.2 ns).

shown in Figure 88(b). The maximum PSN is reduced to 183.1 mV, an approximately 24.6% reduction.

In the above analysis, the maximum PSN of the stack is compared for five different scenarios (A: baseline case, B: doubling decoupling capacitance in Block IV, C: doubling decoupling capacitance in all four blocks, D: doubling the TSVs in Block IV, and E: doubling the TSV in all four blocks). Figure 89 compares the PSN of the center point of the four blocks for the five different scenarios. Comparing scenario B and D to A, doubling decoupling capacitance and TSV in Block IV suppresses PSN of Block IV (16.3% reduction in PSN) and the adjacent Block III (8.1% reduction) but has limited impact on Blocks I and II. Comparing scenario B and C, further doubling decoupling capacitance in Blocks I, II, and III significantly suppresses the PSN of the corresponding blocks but has minimal impact on Block IV, achieving 17% to 20% reduction in PSN for the four blocks. Doubling the TSVs in all four blocks achieves approximately 35% reduction in PSN for the four blocks, as in scenario E.



(a) PSN map of the upper die with double TSV density in Block IV (at 2.6 ns)

(b) PSN map of the upper die with double TSV density in Block I, II, III, and IV (at 2.5 ns)

Figure 88: (a) Power supply noise map of the upper die with doubled TSV density for block IV (maximum power supply noise 210.2 mV at 2.6 ns); (b) Power supply noise map of the upper die with doubled TSV density for block I, II, III, and IV (maximum power supply noise 183.0 mV at 2.6 ns).

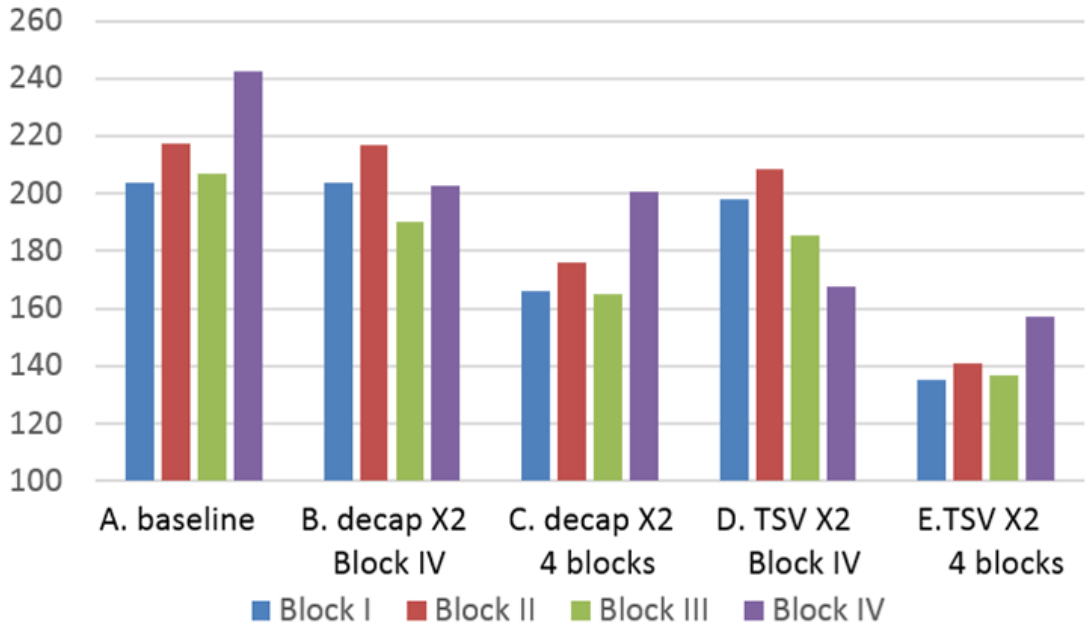


Figure 89: PSN at the center point of the four blocks for the five scenarios.

4.6 Conclusion

The impact of 3D stacking and integrating a micropin-fin heat sink on power supply noise is investigated based on a frequency-domain compact physical model for on-die power distribution network. Compared to a single 2D chip, the power supply noise of a 4-chip stack with microfluidic heat sink increases by 217.6 %, which is not acceptable. Increasing the number of power pads/TSVs and on-die decoupling capacitance are two effective methods for suppressing noise. Moreover, a time-domain numerical PDN simulator is developed based on the distributed circuit model for on-die PDN and finite difference method. Compared to the frequency-domain PDN model, the time-domain numerical model provides more simulation flexibility. A full chip stack with multiple function blocks of different power density, decoupling capacitance density, and power pad/TSV density is simulated and analyzed using the time-domain numerical model.

CHAPTER V

DIE, PACKAGE, AND BOARD-LEVEL POWER DISTRIBUTION NETWORK CO-MODELING, SIMULATION AND ANALYSIS

5.1 Introduction

In this chapter, the time-domain numerical simulator presented in the previous chapter is extended to include the package and board-level power distribution network for comprehensive co-simulation and analysis. Figure 90 is an overview of the conventional power delivery system. The supply current comes from the voltage regulator module (VRM) at the board and is fed into the package through the board-level power planes and a ball grid array (BGA). The current then flows through package-level power planes and enters the die through a C4 (Controlled Collapse Chip Connection) bump array, and is finally distributed to the on-die circuitry by on-die power

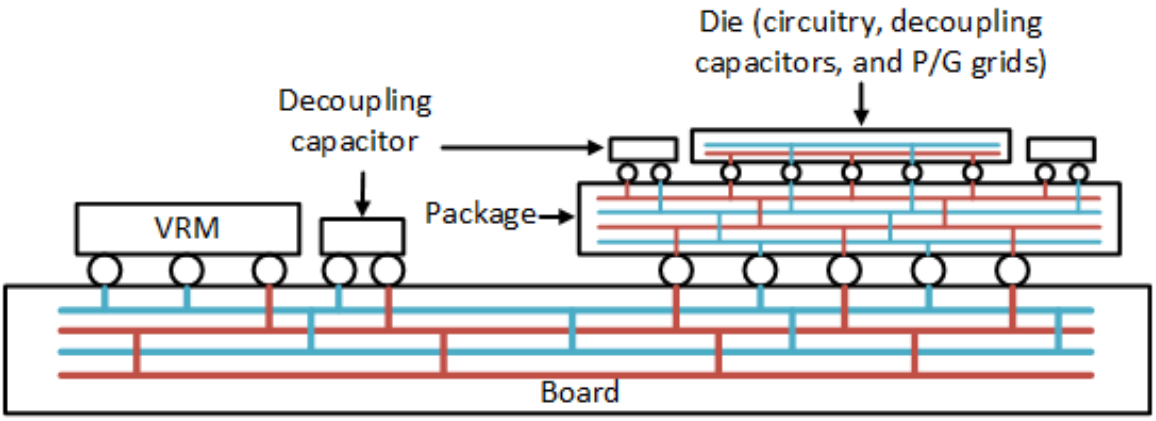


Figure 90: Power delivery system of a high-performance computing system.

grids. The current returns through the opposite path. Board and package-level discrete capacitors and on-die decoupling capacitors are used to help supply current and suppress noise. Careful design of the power distribution network and allocation of the decoupling capacitors and power I/Os are critical to suppress power supply noise and assure the performance and reliability of the system with minimum amount of resources.

5.2 Numerical Modeling of Die, Package and Board-Level Power Distribution Network

5.2.1 Modeling of Board-Level Power Distribution Network

For a high-performance computing system, the board-level power distribution network usually consists of multiple power and ground planes in order to provide an impedance controlled environment and decouple signal wires at different levels [82]. To simplify the modeling work, the power and ground planes are snapped into a pair of planes [41]. We further assume that the power and ground planes are symmetric. The power/ground plane pair is divided into small unit cells and modeled with distributed circuit models, as shown in Figure 91, where L_B, R_B, and C_B are the inductance, resistance, and capacitance associated with the unit cell. Since the circuit model for the power and ground planes are identical, we split the power and ground models for simplicity.

The power/ground planes are meshed, and the intersection points of the mesh lines are "nodes". Each node is associated with a unit cell and it is the center of the unit cell. In the board power/ground plane meshes, there are two types of nodes, as shown in Figure 92. A regular node is connected to 2-4 neighboring nodes depending on its location. The regular nodes at the four corners of the plane are connected to two neighboring nodes, while the regular nodes at the four edges of the plane are connected to three neighboring nodes. The other regular nodes are connected to four neighboring nodes. The second type is the "BGA" node. The board-level power/ground planes

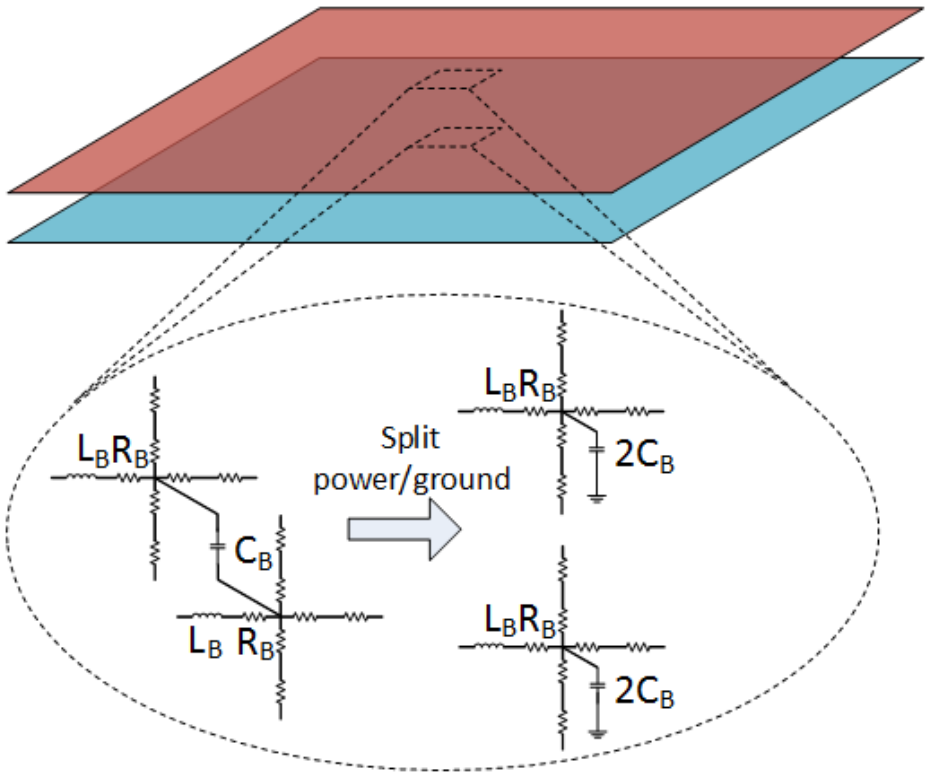


Figure 91: Distributed circuit model of board-level power/ground planes.

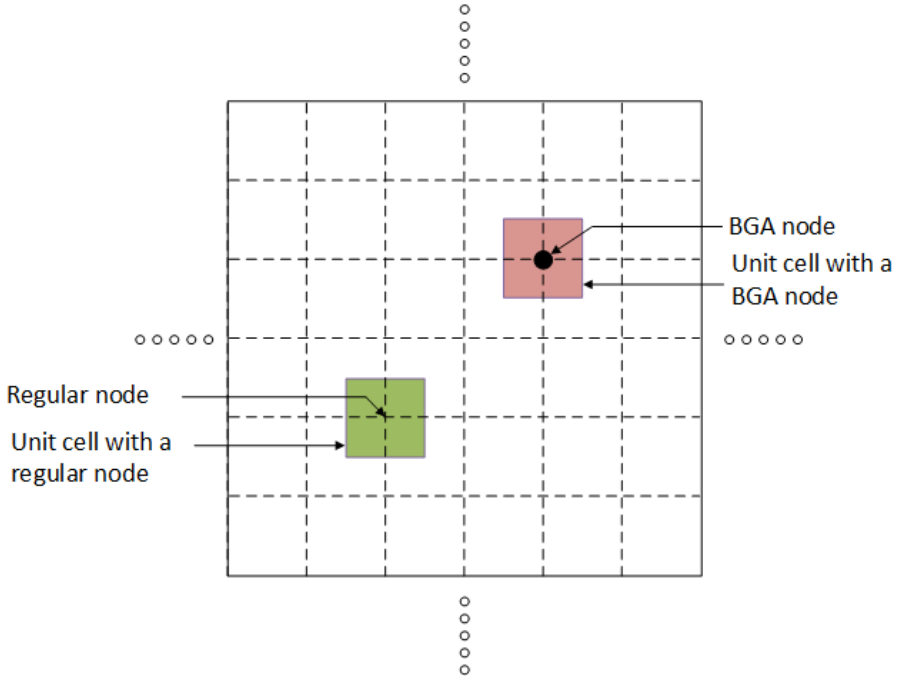


Figure 92: Meshed board power/ground planes with two types of nodes.

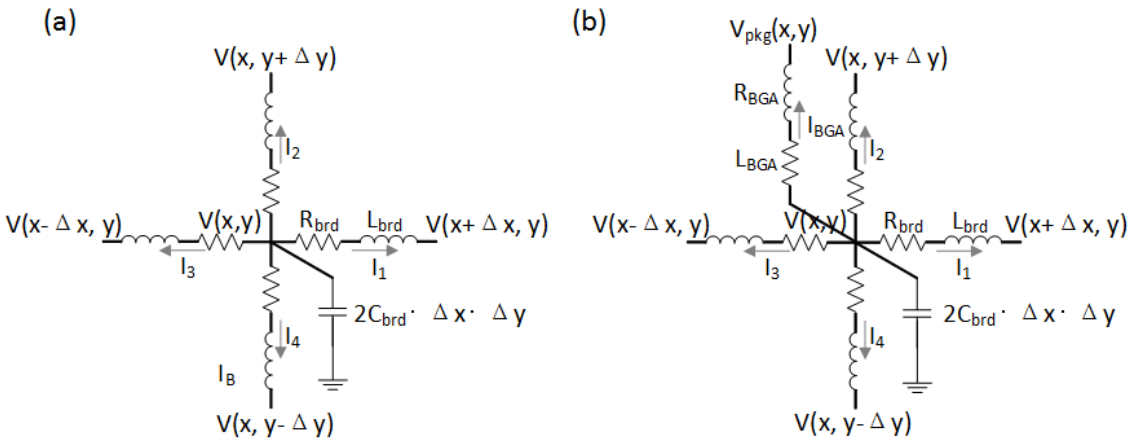


Figure 93: Circuit model for (a) a regular node connected with four neighboring nodes, and (b) a BGA node.

are interconnected with package-level power/ground planes using BGA, which enable current delivery from board to package. A node where a BGA is assigned is called "BGA" node. A circuit branch representing the BGA has to be added for the circuit model of a BGA node.

Figure 93 shows the circuit models for the regular node and the BGA node. The circuit models look somewhat similar to the models for the on-die power/ground grid node, with the major difference that the distributed inductance of the board power/ground planes has to be integrated into the model. Based on the circuit model for the regular node in Figure 93(a), the following difference equations are derived.

$$V(x,y,t) - R_{brd} \cdot I_1(t) - L_{brd} \cdot \frac{I_1(t) - I_1(t-\Delta t)}{\Delta t} = V(x+\Delta x, y, t) \qquad (36)$$

$$V(x,y,t) - R_{brd} \cdot I_2(t) - L_{brd} \cdot \frac{I_2(t) - I_2(t-\Delta t)}{\Delta t} = V(x, y+\Delta y, t) \qquad (37)$$

$$V(x,y,t) - R_{brd} \cdot I_3(t) - L_{brd} \cdot \frac{I_3(t) - I_3(t-\Delta t)}{\Delta t} = V(x-\Delta x, y, t) \qquad (38)$$

$$V(x,y,t) - R_{brd} \cdot I_4(t) - L_{brd} \cdot \frac{I_4(t) - I_4(t-\Delta t)}{\Delta t} = V(x, y-\Delta y, t) \qquad (39)$$

$$\sum_{i=1}^{4} I_i(t) + 2C_{brd}\Delta x \Delta y \frac{V(x,y,t) - V(x,y,t-\Delta t)}{\Delta t} = 0 \qquad (40)$$

where $V(x,y,t)$ is the voltage of the node at location (x,y) at time t; $I_i(t)$ is current between two adjacent nodes at time t; Δx and Δy are the distance between two adjacent nodes (or unit cell length) in two axes; R_{brd} and L_{brd} are the distributed parasitic resistance and inductance of the board power/ground plane per unit area, respectively; and C_{brd} is the distributed parallel plate capacitance per unit area. Equation (36-39) are voltage equations and Equation (40) is a current equation.

The difference equations for the BGA node are very similar to that of the regular node except that we need to add one more voltage equation for the BGA branch and add the BGA current term in the current equation. Equation (41) is the additional voltage equation and Equation (42) is the modified current equation for the BGA node.

$$V(x,y,t) - R_{BGA} \cdot I_{BGA}(t) - L_{BGA} \cdot \frac{I_{BGA}(t) - I_{BGA}(t-\Delta t)}{\Delta t} = V_{pkg}(x,y,t) \qquad (41)$$

$$\sum_{i=1}^{4} I_i(t) + 2C_{brd}\Delta x \Delta y \frac{V(x,y,t) - V(x,y,t-\Delta t)}{\Delta t} + I_{BGA}(t) = 0 \qquad (42)$$

where $V_{pkg}(x,y,t)$ is the voltage of the node at location (x,y) on package-level power/ground plane at time t; $I_{BGA}(t)$ is the current flowing across the BGA at time t.

By integrating the circuit models for the regular node and BGA node, we have a distributed circuit model for the board-level power/ground plane, as shown in Figure 94. There are some nodes needing special treatment. In this work, we assume ideal VRM with constant output voltage. Thus, the node connected to the VRM should have a constant Vdd and supply all the currents required by the on-die devices. For

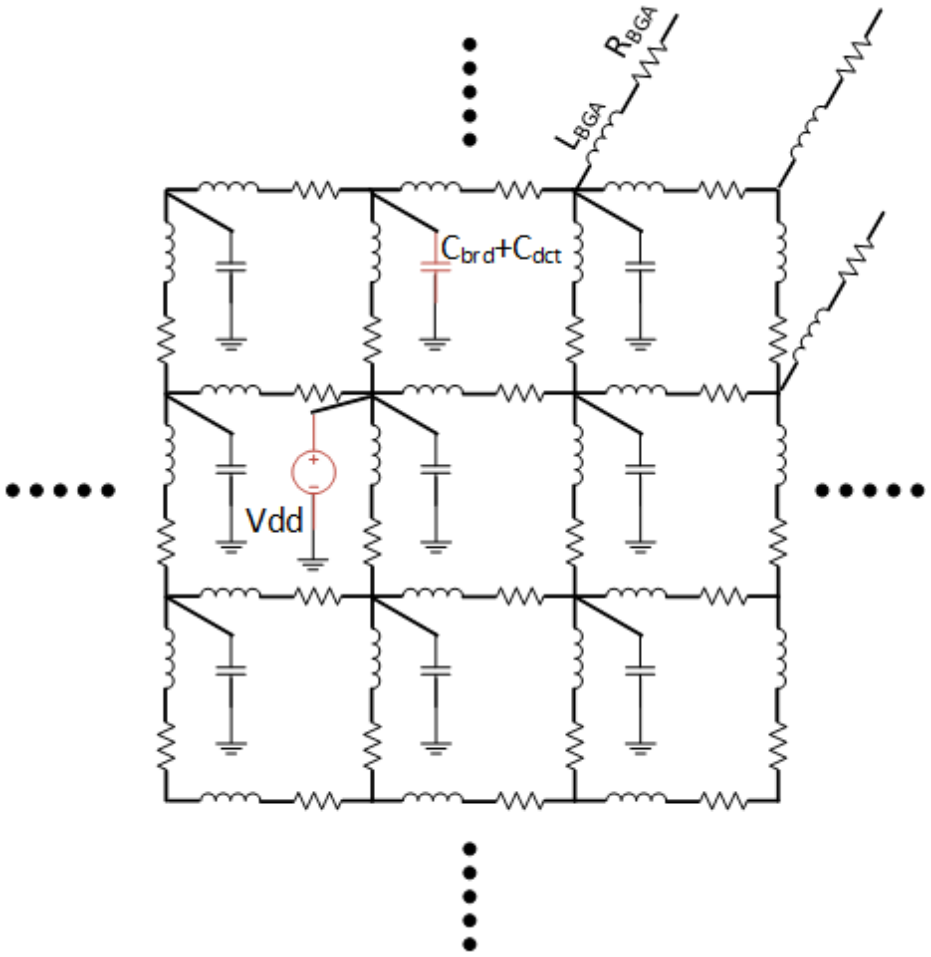


Figure 94: Distributed circuit model for board-level power/ground plane.

the Vdd node, we assign its voltage as Vdd and remove the current equation for this node. Discrete capacitors are placed on board for noise decoupling. For the regular nodes connecting with discrete capacitors, the extra capacitance has to be added to its capacitance term in the current equation, as shown in Figure 94.

5.2.2 Modeling of Package-Level Power Distribution Network

Modeling for the package-level power/ground planes are very similar to board-level modeling. Multiple power/ground planes are snapped to a pair of power and ground planes. The power/ground planes are meshed and the nodes in the mesh are modeled with simplified circuit models. There are four kinds of nodes on the package

power/ground planes: 1) regular node is the same as defined for board power/ground planes; 2) BGA node is a node where package is connected to board through a BGA. It is also exactly the same as BGA node on board power/ground plane; 3) C4 node is the node with a C4 bump which connects the package power/ground planes to on-die power/ground grids; and 4) C4+BGA node is the node where a C4 bump and a BGA overlap. Figure 95 illustrates the four kinds of nodes on the package power/ground plane.

The simplified circuit models for the four kinds of nodes are shown in Figure 96. Difference equations for the node voltage and current are derived based on the circuit models and voltage and current law. The equations for the regular node are as follows, which are the same as that of the regular node on board.

$$V(x,y,t) - R_{pkg} \cdot I_1(t) - L_{pkg} \cdot \frac{I_1(t) - I_1(t-\Delta t)}{\Delta t} = V(x+\Delta x, y, t) \qquad (43)$$

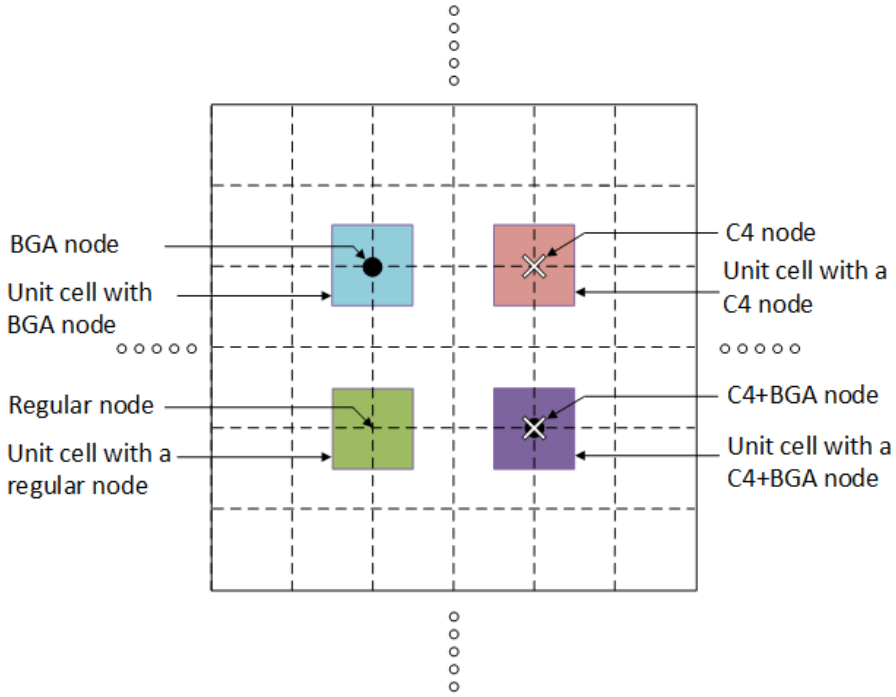


Figure 95: Meshed package power/ground planes with four types of nodes.

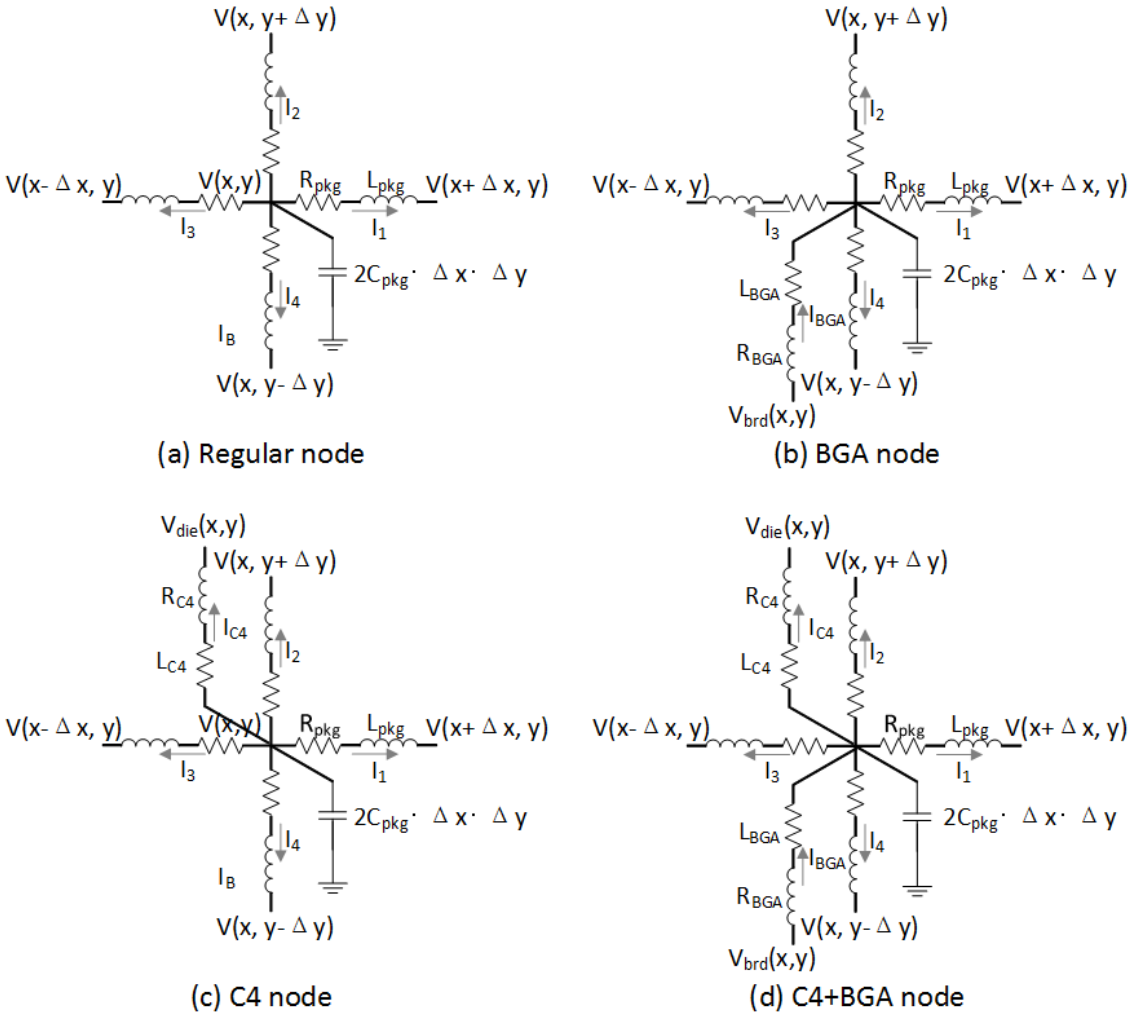


Figure 96: Circuit models for (a) a regular node connected with four neighboring nodes, (b) a BGA node, (c) a C4 node, and (d) a C4+BGA node on package power/ground plane.

$$V(x,y,t) - R_{pkg} \cdot I_2(t) - L_{pkg} \cdot \frac{I_2(t) - I_2(t-\Delta t)}{\Delta t} = V(x, y+\Delta y, t) \qquad (44)$$

$$V(x,y,t) - R_{pkg} \cdot I_3(t) - L_{pkg} \cdot \frac{I_3(t) - I_3(t-\Delta t)}{\Delta t} = V(x-\Delta x, y, t) \qquad (45)$$

$$V(x,y,t) - R_{pkg} \cdot I_4(t) - L_{pkg} \cdot \frac{I_4(t) - I_4(t-\Delta t)}{\Delta t} = V(x, y-\Delta y, t) \qquad (46)$$

$$\sum_{i=1}^{4} I_i(t) + 2C_{pkg}\Delta x\Delta y\frac{V(x,y,t) - V(x,y,t-\Delta t)}{\Delta t} = 0 \tag{47}$$

where $V(x, y, t)$ is the voltage of the node at location (x, y) at time t on package; $I_i(t)$ is current between two adjacent nodes at time t; Δx and Δy are the distance between two adjacent nodes (or unit cell length) in two axes; R_{pkg} and L_{pkg} are the distributed parasitic resistance and inductance of the package power/ground plane per unit area, respectively; and C_{pkg} is the distributed parallel plate capacitance per unit area. Equation (43-46) are voltage equations and Equation (47) is a current equation.

For the BGA node on package, one additional voltage equation is added for the BGA branch and its current equation should include the BGA current term.

$$V(x,y,t) - R_{BGA}\cdot I_{BGA}(t) - L_{BGA}\cdot\frac{I_{BGA}(t) - I_{BGA}(t-\Delta t)}{\Delta t} = V_{brd}(x,y,t) \tag{48}$$

$$\sum_{i=1}^{4} I_i(t) + 2C_{pkg}\Delta x\Delta y\frac{V(x,y,t) - V(x,y,t-\Delta t)}{\Delta t} - I_{BGA}(t) = 0 \tag{49}$$

where $V_{brd}(x, y, t)$ is the voltage of the node at location (x, y) on board power/ground plane at time t. One thing needing special attention here is the direction of the BGA current, thus the sign of the current term.

The voltage equations for the C4 node and its neighboring nodes are the same as that of the regular node. Due to integrating the C4 bump, an additional voltage equation has to be added accounting for the C4 branch, and the current flowing through the C4 bumps has to be added to the current equation for the node.

$$V(x,y,t) - R_{C4}\cdot I_{C4}(t) - L_{C4}\cdot\frac{I_{C4}(t) - I_{C4}(t-\Delta t)}{\Delta t} = V_{die}(x,y,t) \tag{50}$$

$$\sum_{i=1}^{4} I_i(t) + 2C_{pkg}\Delta x\Delta y\frac{V(x,y,t) - V(x,y,t-\Delta t)}{\Delta t} + I_{C4}(t) = 0 \tag{51}$$

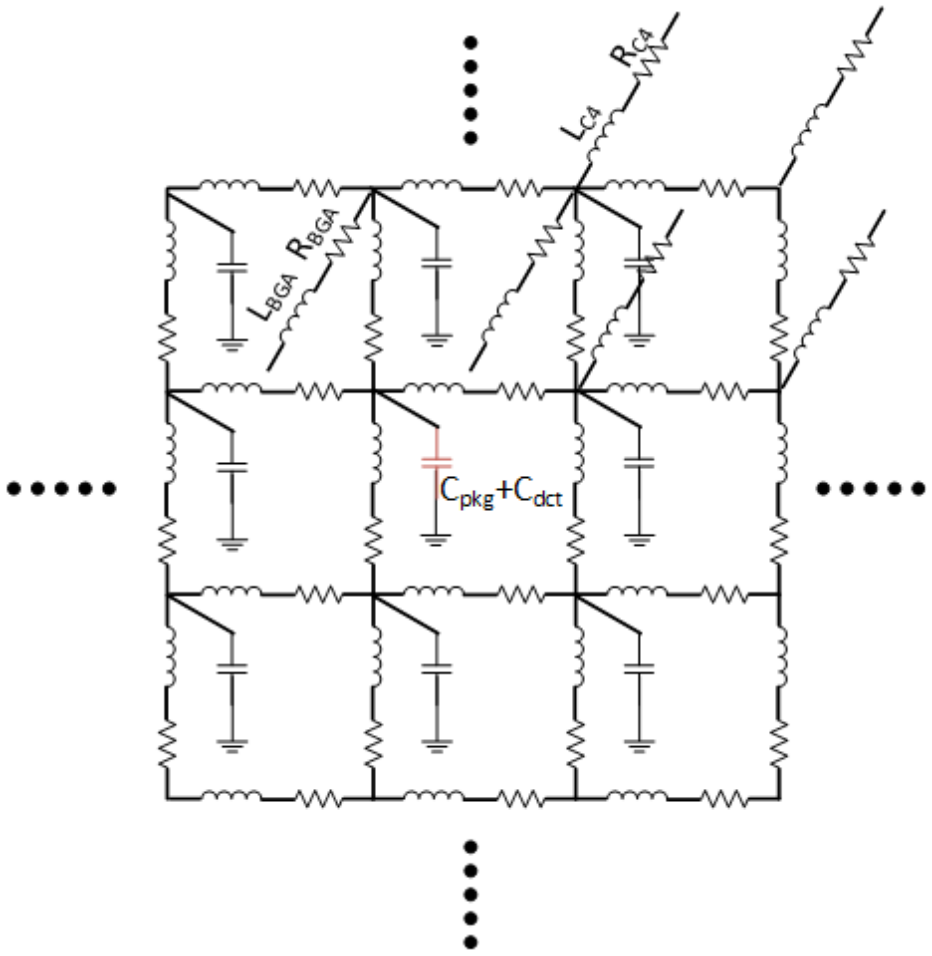


Figure 97: Distributed circuit model for package power/ground plane.

where $V_{die}(x, y, t)$ is the voltage of the node at position (x, y) on die-level power/ground grid at time t; $I_{BGA}(t)$ is the current flowing across the C4 bump at time t.

For the C4+BGA node, we combine all the voltage equations for the C4 node and BGA node including the voltage equations for C4 and BGA branch. The current equation has to account for the currents in both C4 and BGA branches. It becomes:

$$\sum_{i=1}^{4} I_i(t) + 2C_{pkg}\Delta x\Delta y\frac{V(x, y, t) - V(x, y, t - \Delta t)}{\Delta t} + I_{C4}(t) - I_{BGA}(t) = 0 \qquad (52)$$

Figure 97 illustrates the distributed circuit model for the package power/ground

planes with the four kinds of nodes. Similar to the board power/ground plane modeling, we also have discrete capacitors on package for noise decoupling. The current equation for the nodes connected with the discrete capacitors have to include the extra capacitance.

5.2.3 Integration of Models for Board, Package, and Die-Level Power Distribution Network

The modeling work for the board and package-level power/ground planes has to be combined with the numerical model for on-die power/ground grids, which is presented earlier in Chapter 4, to enable the modeling and simulation of the complete power delivery path. There are a few issues to be addressed when combining the models.

Figure 98 shows the meshed board, package, and die-level power/ground planes. Different mesh finenesses are applied to board, package and die due to their size difference. Applying coarser mesh to board and package reduces the number of nodes and improves simulation speed. BGAs and C4 bumps are used to connect board, package, and die-level power/ground planes. It's possible to have BGA and C4 overlapping on the meshed plane, which means the BGA is directly connected to the C4 bump. It is acceptable to have a power BGA connected to a power C4 or a ground BGA connected to a ground C4, which have already been considered by the circuit model in Figure 96(d). However, a power BGA cannot be connected to a ground C4 and vice versa. When this situation happens, there are two solutions. Since the density of C4 bumps is usually larger than that of BGA, one way is to move the C4 bump to an adjacent node. The other method is just to remove the C4 bump. Since this power-ground overlapping is rare and the number of C4 bumps is larger, the impact of removing a few C4 bumps is small.

For each node on the meshed plane, a set of difference equations based on a circuit model has been developed. By sorting all the equations for all the nodes in the mesh and re-writing them in matrix form, the following matrix equation can be derived, as

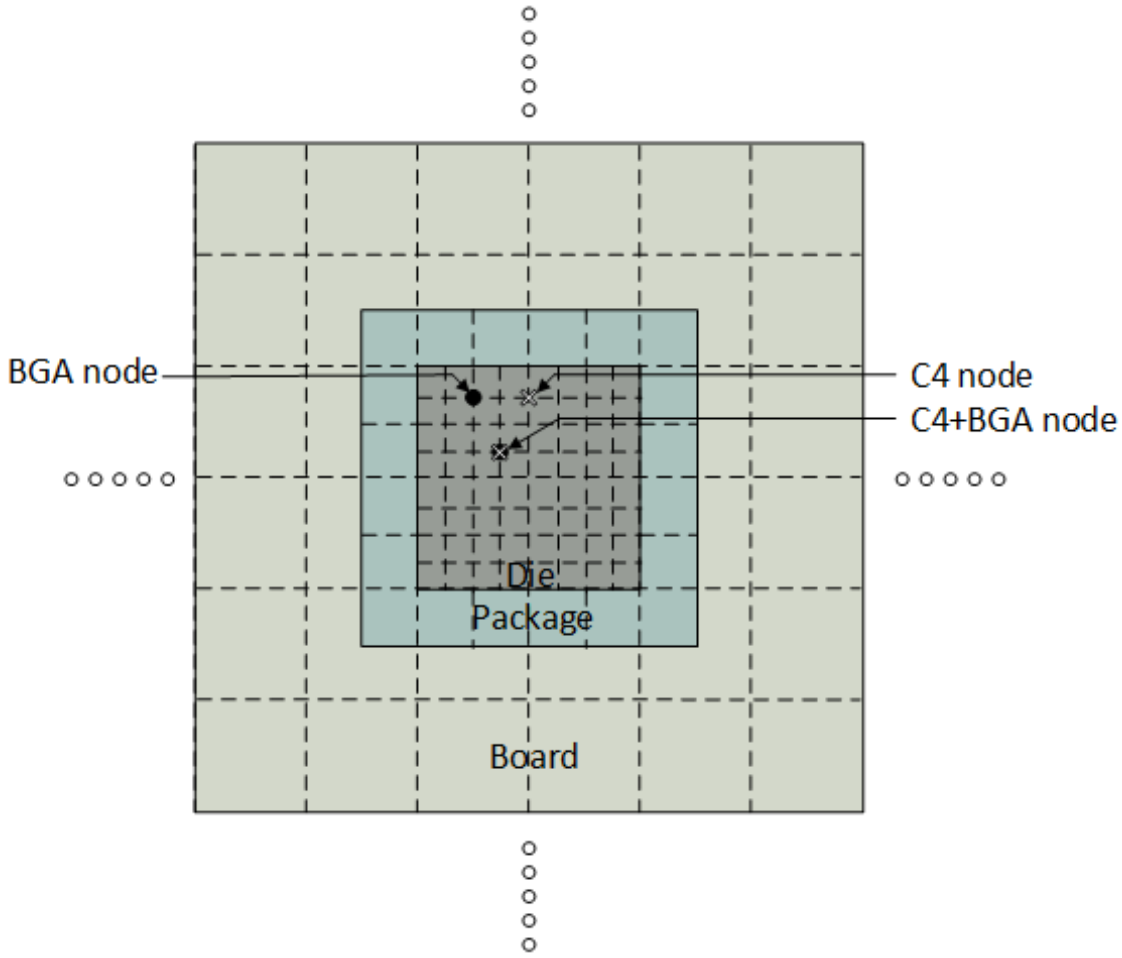


Figure 98: Meshed board, package, and die-level power/ground planes.

in Figure 99. All the unknown variables including voltages of the nodes on the board, package, and die, the currents between two node on the board, package and die, and the currents flowing across the TSVs, C4 bump and BGA form an unknown vector. The sparse matrix consists of the parasitic resistance, inductance, and capacitance of the board, package, die-level power/ground planes and the discrete decoupling capacitors. By discretizing the time, the unknown vector at time n can be calculated using the its previous state at time $n-1$. Thus, the voltage and current distribution across the board, package and die-level power/ground planes can be iteratively solved in the time domain. The last vector in the matrix equation is the current drain of on-die devices and the supply voltage.

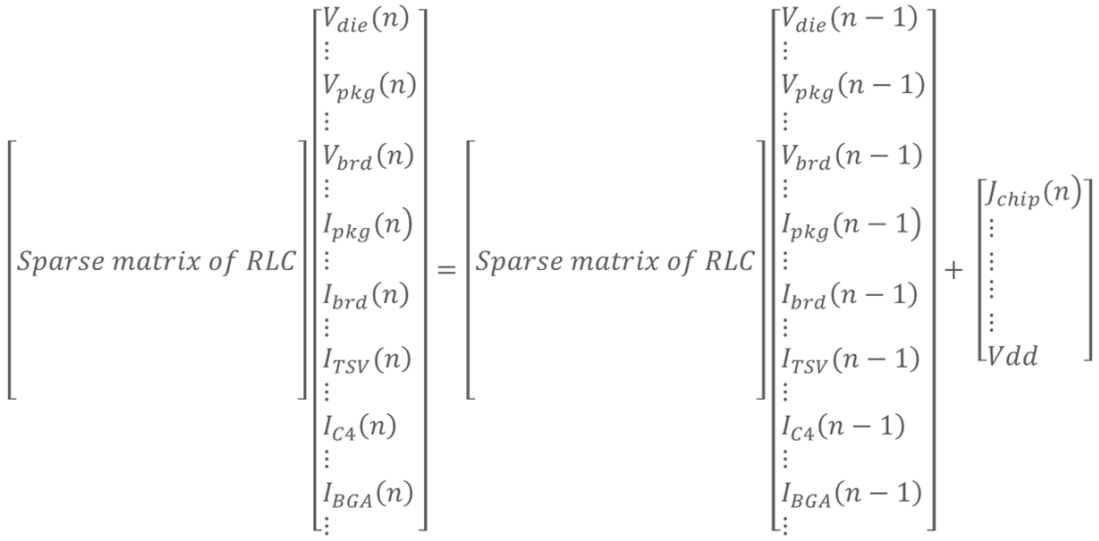


Figure 99: Matrix form of the difference equation for board, package, and die nodes.

5.3 Co-Simulation and Analysis of Board, Package, and Die-Level Power Distribution Network

5.3.1 IR-drop of the Die, Package, and Board-Level Power Distribution Network

Based on the numerical modeling for the die, package and board-level power distribution network presented in the previous sections, power supply noise is simulated. The parameters of the on-die power distribution network and die power map are the same as that of the on-die power distribution network modeling and simulation in Chapter 3 (Table 10 and Figure 85). The parameters for the package and board-level power distribution network are listed in Table 12 [83], [84].

The size of board, package, and die are 4×4 cm^2, 2×2 cm^2, and 1×1 cm^2, respectively. It is further assumed that the package and die are centered on the board. Figure 100 shows the meshed board and package planes with assigned power/ground BGA and microbumps. In the board layout, the red cross nodes are power BGAs; the black circle nodes are ground BGAs; and the green dots are common nodes on the board planes. The BGA nodes are uniformly distributed within the region covered by

Table 13: Simulation parameters for the package and board power distribution network

Parameters	Value
Board size	4×4 cm^2
Package size	2×2 cm^2
Board power/ground plane	3 oz copper
Package power/ground plane	1 oz copper
Board parasitic inductance	0.2 nH/cm^2
Board parasitic capacitance	1 nF/cm^2
Package parasitic inductance	0.2 nH/cm^2
Package parasitic capacitance	2 nF/cm^2
BGA inductance	6.62 pH
BGA resistance	39.5 mΩ
microbump inductance	4.73 pH
microbump resistance	6.16 mΩ
current rise time	1 ns
Δt	0.1 ns
Vdd	0.9 V

the package. In the package layout, we have the power/ground BGA nodes (red cross nodes and black circle nodes). Moreover, we have the red and blue dots clustered in

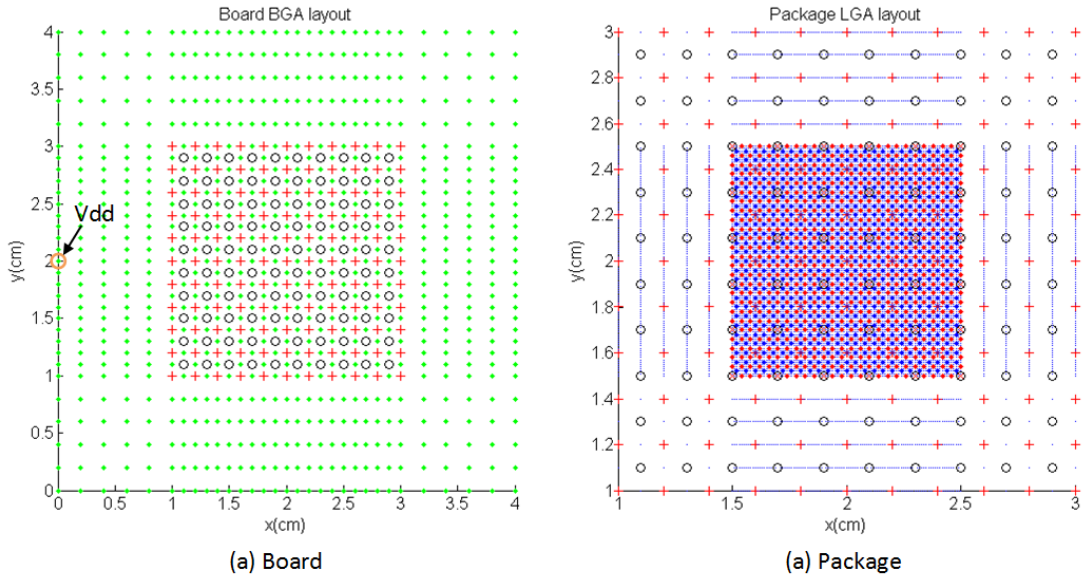


Figure 100: (a) Board BGA layout, and (b) package BGA and microbump layout.

the center region, which are microbumps connected to the die. The supply voltage Vdd is placed at the middle point of the left edge on the board.

The simulated IR-drop on die, package, and board power/ground planes are shown in Figure 101. The on-die IR-drop distribution is positively correlated to the power density distribution, as shown in Figure 101(a). Due to the concentration of current from package to die, larger IR-drops appear at the BGA locations. The maximum IR-drop on die is 32.3 mV. The IR-drop distribution on package is shown in 101(b). There is a high IR-drop region in the center due to the current drain of the die. The IR-drop at he left edge is slightly lower than the right edge because of the different distances to Vdd. The maximum IR-drop on package is 9.1 mV. Figure 101(c) is the

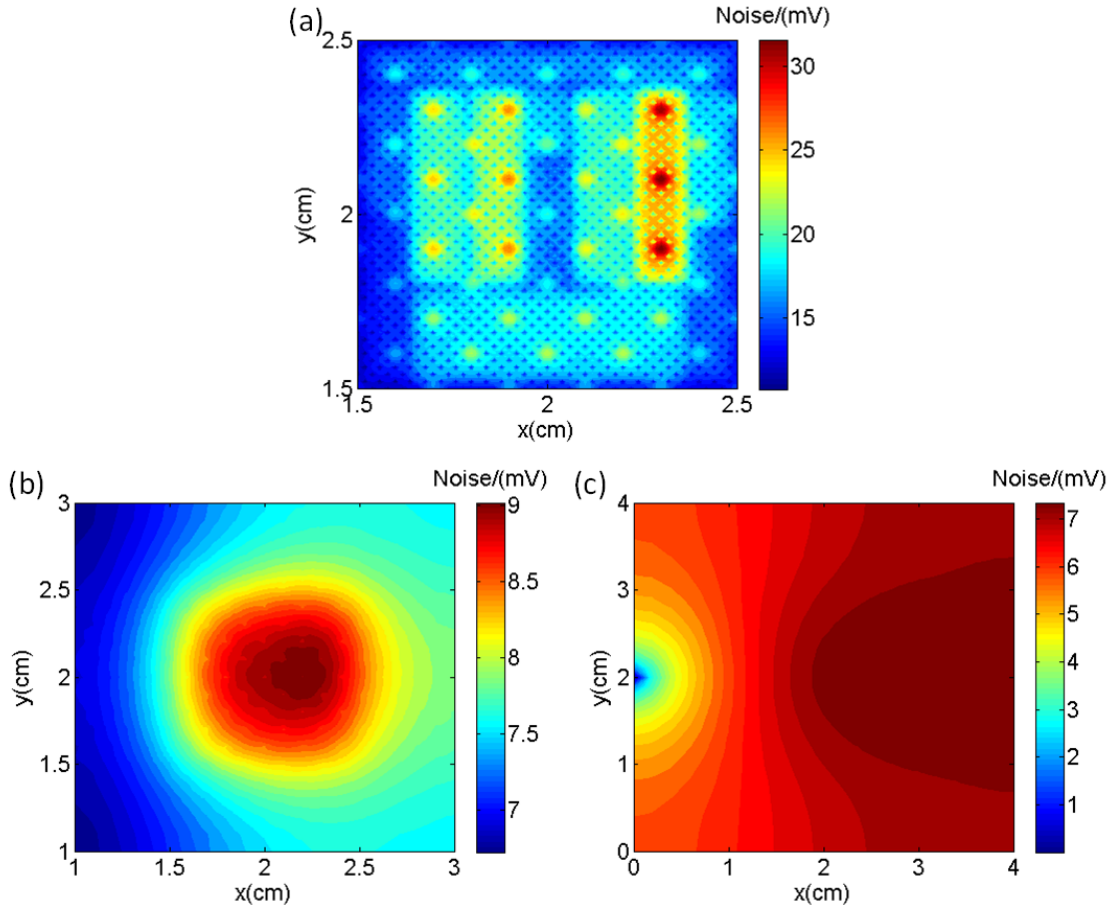


Figure 101: (a) on-die IR-drop, (b) package IR-drop, and (c) board IR-drop.

IR-drop distribution across the board power/ground planes. The IR-drop increases as it gets further away from Vdd. The maximum IR-drop is 7.6 mV.

5.3.2 Simultaneous Switching Noise of the Die, Package, and Board-Level Power Distribution Network

In this section, the transient power supply noise of the die, package, and board power distribution network is simulated, which includes both IR-drop and simultaneous switching noise. To decouple the power supply noise, discrete capacitors are added on package and board. Four discrete capacitors of 0.5 μF are placed on four sides of the package, as shown in Figure 102(a), and one large capacitor of 300 μF is placed on board close to Vdd. Figure 102 (b-d) are the simulated power supply noise

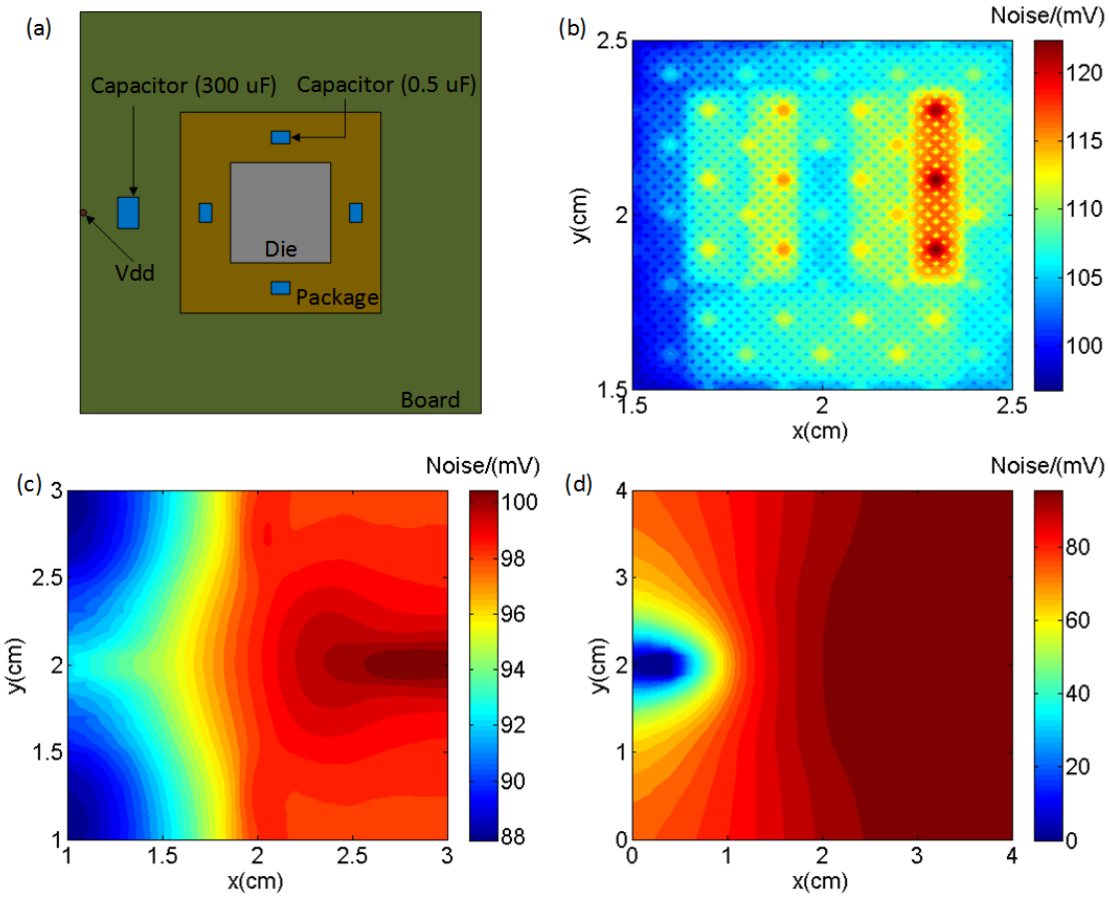


Figure 102: (a) Discrete capacitor configuration, (b) power supply noise on die, (c) power supply noise on package, (d) power supply noise on board.

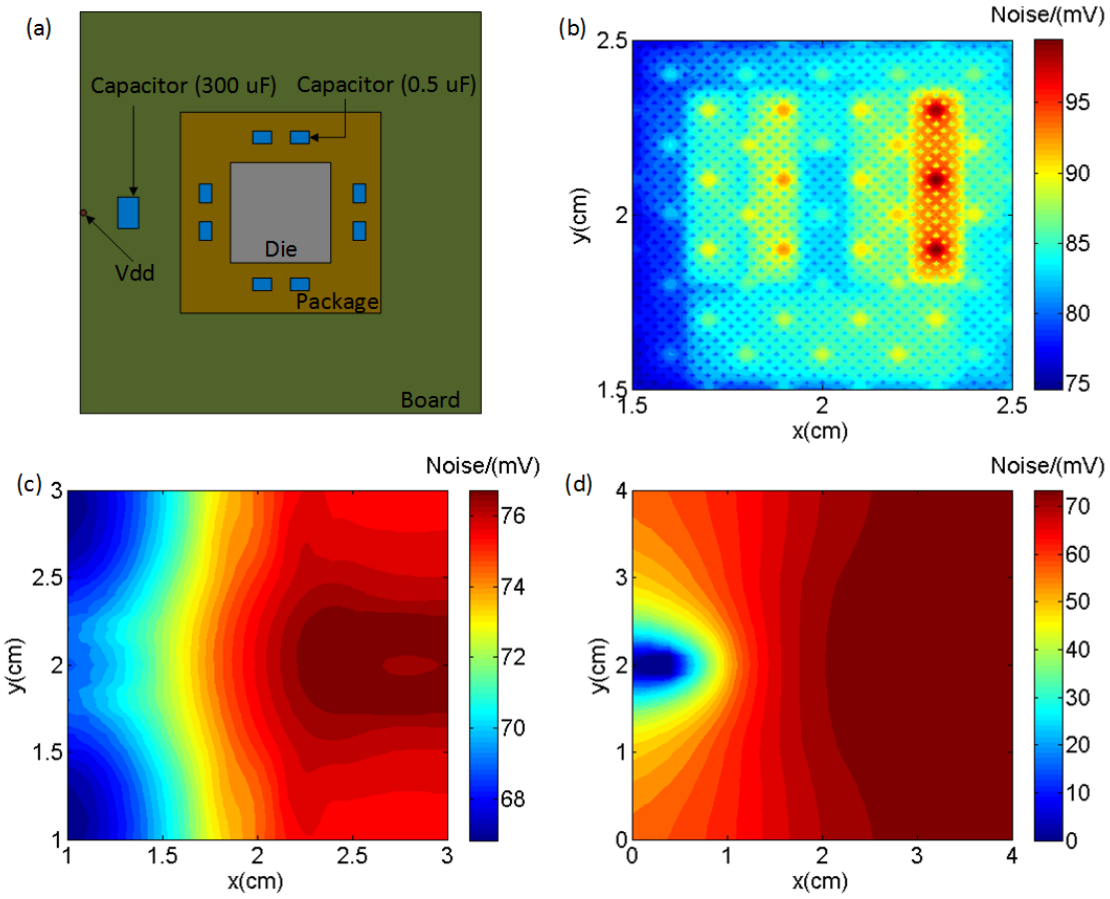


Figure 103: (a) Discrete capacitor configuration, (b) power supply noise on die, (c) power supply noise on package, (d) power supply noise on board.

distribution on die, package, and board, respectively. The on-die power supply noise is positive related to the die power map. The maximum power supply noise is 123.3 mV and appears at the region with the largest power density. The left edge of the die has smaller power supply noise than that of the right edge because it's closer to Vdd and the large on-board decoupling capacitor. The maximum power supply noise is 100.9 mV and 98.9 mV, respectively, for package and board.

Next, the number of discrete decoupling capacitors on package is doubled, as shown in Figure 103(a). Figure 103 (b-d) are the simulated power supply noise distributions for the die, package and board, which are similar to the first case. Noise reduction is achieved by adding decoupling capacitors on package. The maximum

power supply noise on die is reduced to 100.3 mV from 123.3 mV, an approximately 18.7% reduction. For the package, power supply noise is reduced to 77.1 mV from 100.9 mV, an approximately 23.6% reduction. The board-level power supply noise decreases from 98.9 mV to 75.8 mV, an approximately 23.4% reduction.

5.4 Conclusion

In this chapter, the numerical modeling and finite difference method are applied to the package and board-level power distribution network. Different from the modeling of the on-die power/ground grid, the distributed inductance has to be considered in package and board modeling. Distributed circuit models and difference equations for the nodes on package and board power/ground planes are derived and integrated with the die-level equations. The difference equations are rewritten in matrix form and iteratively solved in the time domain. Using the extended numerical simulator including package and board-level power distribution network, IR-drop and simultaneous switching noise of the die, package, and board are simulated for different configurations. Adding more discrete decoupling capacitors on package reduces power supply noise.

CHAPTER VI

SUMMARY AND FUTURE WORK

The presented research work is summarized and potential future work is discussed.

6.1 Summary

6.1.1 Microfluidic Cooling for Silicon Interposer and 3-D Integration

Thermal management is one of the major challenges facing future high-performance computing systems, especially for 3D integrated systems, where conventional air cooling may not be sufficient or even not applicable. Embedded microfluidic cooling has been proposed and demonstrated as a promising solution. In this work, microfluidic cooling is demonstrated for silicon interposer-based 2.5D and 3D systems. The key enabling technologies include the novel electrical and fluidic I/O, micropin-fin heat sink, and flip-chip bonding for simultaneous assembly of electrical and fluidic microbumps. Fluidic I/Os consisting of fluidic vias and microbumps are designed to enable coolant flow between vertical tiers (including interposer and dice). The solder based fluidic microbumps are fully compatible with the fabrication and assembly process of fine-pitch electrical microbumps. Silicon dice with electrical and fluidic I/Os and micropin-fin heat sink were fabricated and assembled for a microfluidic cooling demonstration. The flip-chip bonding parameters including temperature profile and bonding force were tuned for good bonding results. Following assembly, the bonded electrical and fluidic microbumps were experimentally tested. Moreover, 3D stacking of electrical and fluidic I/Os, which is essential for integrating microfluidic cooling into 3D systems, is demonstrated. Figure 104 shows the key components for embedded microfluidic cooling and X-ray images of bonded 2D chip and 3D chip stack with electrical and fluidic I/Os and micropin-fin heat sink.

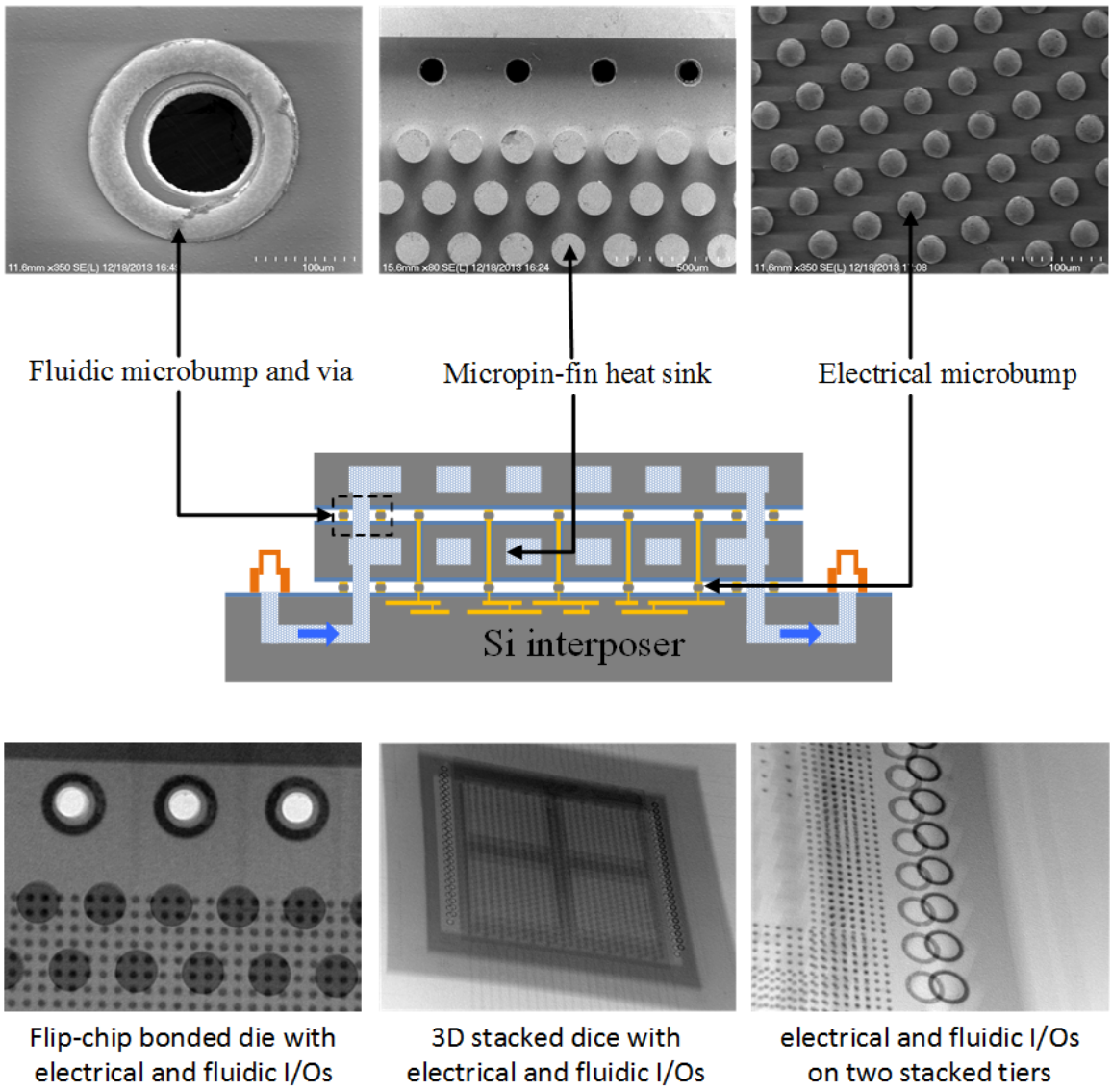


Figure 104: Key components of microfluidic cooling for 3D chip stack.

Besides technology development, the thermal and signaling benefits of the proposed microfluidic cooled silicon interposer platform were evaluated. Microfluidic-cooled test vehicle equipped with platinum heater/RTD was built for thermal measurements. The measured temperatures under different power densities up to 100 W/cm^2 and flow rates up to 50 mL/min were converted to thermal resistances of the test vehicle. The thermal resistances are decomposed and analyzed. Flow rate is

an important factor affecting thermal resistance; at 50 mL/min, the adjusted thermal resistance is 0.24 K·cm^2/W. Using a thermal simulator, silicon interposer based systems with different cooling configurations including air cooling and three different microfluidic cooling configurations are simulated and analyzed. As expected, all the microfluidic cooling scenarios significantly reduce the system temperature compared to air cooling. The three microfluidic cooling configurations have their own pros and cons. Considering cooling performance, implementation difficulty and system complexity, the proposed silicon interposer platform with die-level microfluidic cooling is the most effective and efficient. Besides reducing system temperature, microfluidic cooling provides better thermal isolation between high-power and low-power dice compared to air cooling. The major advantage of silicon interposer is very high signaling bandwidth enabled by the fine-pitch silicon interposer interconnects. However, one issue with the fine-pitch interconnect is high resistance due to small cross-section and relative long length, which would cause larger power loss on the interconnects. Microfluidic cooling helps reduce system temperature which in turn benefits signaling, especially for long narrow interconnects.

6.1.2 Time Domain Numerical Power Distribution Network Simulator

A time-domain numerical simulator is developed for a power distribution network based on distributed circuit model and the finite difference equations. The numerical modeling and finite difference method was first applied to a unit cell of on-die power distribution network with assumptions of uniform power and decoupling capacitance distribution. By integrating TSV into the circuit model, 3D power distribution network is also numerically modeled. Next, the simulator was extended to full chip simulation with multiple blocks of different power density, TSV, and decoupling capacitance distributions. Based on simulation results, adding power I/Os and decoupling capacitance to high power density regions can significantly reduce power supply

noise. The numerical simulator is further extended by including package and board-level power/ground planes. The major difference from the on-die power/ground grid modeling is that the distributed inductance of the package and board power/ground planes has to be considered. Distributed circuit models and difference equations for the nodes on package and board power/ground planes are derived and integrated with the die-level equations. The difference equations are rewritten in matrix form and iteratively solved in the time domain. Using the extended numerical simulator including package and board-level power distribution network, IR-drop and simultaneous switching noise of the die, package, and board are simulated for different configurations. Adding more discrete decoupling capacitors on package reduces power supply noise.

6.2 Future Work

6.2.1 Reliability of the Fluidic Microbump

Reliability of the fluidic I/Os is extremely important to the success of the embedded microfluidic cooling technology in real-world applications. No leakage can be tolerated. Moreover, high-power systems would require a larger a flow rate to improve cooling performance, which would increase the pressure drop as indicated by the measurement results. Thus, good fluidic sealing under high pressure drop is critical. The solder-based flip-chip bonded fluidic microbumps have been preliminarily tested up to 100 KPa with deionized water as the coolant. However, a larger pressure drop is possibly required by high-power systems. A more comprehensive reliability study with higher flow rate and pressure drop must be done for the fluidic microbumps. A stress measurement and simulation under different temperatures and pressure drops would be helpful to understand the weak points and improve the fluidic microbumps design and assembly process. Moreover, different coolants may be used in single- or two- phase cooling. Understanding the erosion of the solder-based fluidic microbumps

is also important.

6.2.2 Pressure Drop Optimization

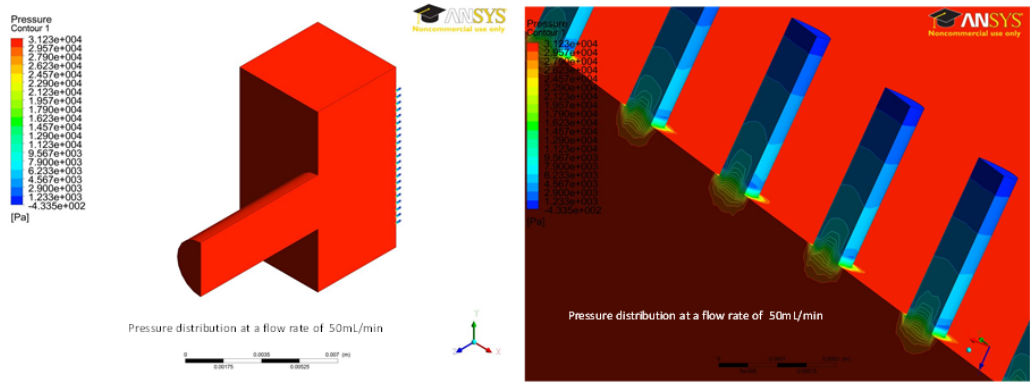
As mentioned previously, there are trade-offs between cooling performance and pressure drop. Increasing flow rate improves cooling capability but induces a larger pressure drop, which would affect reliability and longevity of the system. Optimizing the design and dimensions of the flow path including fluidic distribution channels, fluidic microbumps and vias, and microfluidic heat sink certainly helps reduce pressure drop at the same time meeting the cooling requirement. Figure 105 shows the simulated pressure drop and velocity distribution in the manifold and fluidic vias. We can see there is a big change in pressure drop at the transition between the manifold and fluidic vias. Optimizing the transitions in the flow path would be helpful in reducing pressure drop.

6.2.3 Integrating Fluidic I/Os, Fluidic Heat Sink, and TSVs

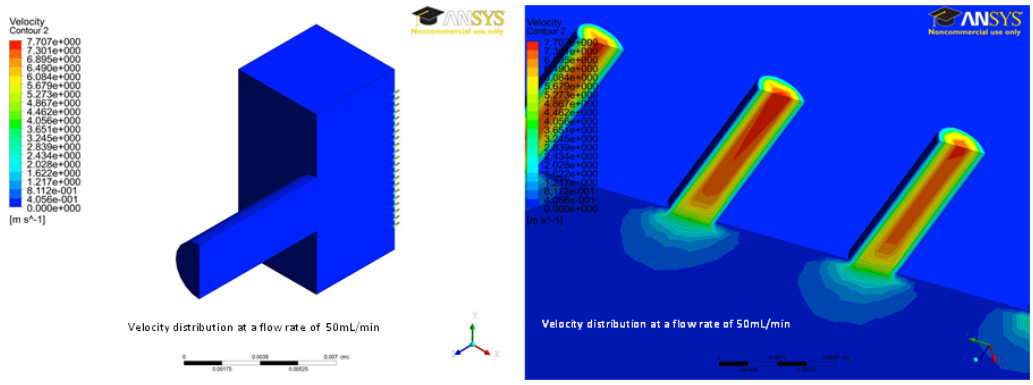
In real 3D integrated systems with microfluidic cooling, both vertical fluidic and electrical interconnects are required. The integration of fluidic I/Os with embedded microfluidic heat sinks have been demonstrated in this work, while the integration of TSVs in microfludic heat sink have been demonstrated in [60], [61], as shown in Figure 106. A full integration of fluidic I/Os, microfluidic heat sinks, and TSVs would be imperative for microfluidic-cooled 3D integration.

6.2.4 Integrating Microfluidic Cooling to Real High-Power Die

In this work, a platinum heater is integrated to a silicon die to mimic the power dissipation of real devices. Applying microfluidic cooling to a real high-power die would be very different and much more challenging than the platinum heater case. The most recently progress is in integrating the micropin-fin heat sink into the back side of a FPGA die for cooling (Figure 107), which is a significant step. In the future,



(a) Pressure drop distribution in manifold and fluidic vias



(b) Velocity distribution in manifold and fluidic vias

Figure 105: Simulated pressure drop and velocity distribution in manifold and fluidic vias.

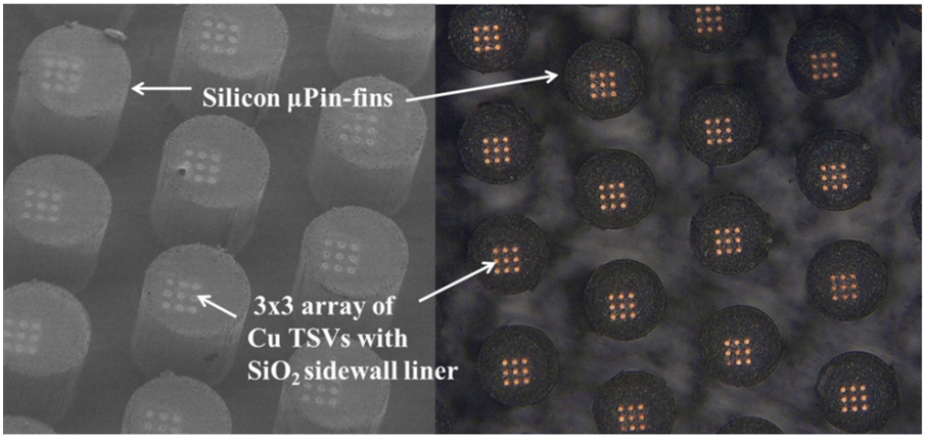


Figure 106: TSV array in micropin-fins.

full integration of fluidic I/Os, microfluidic heat sink, and TSVs into a real chip stack would be a very powerful demonstration.

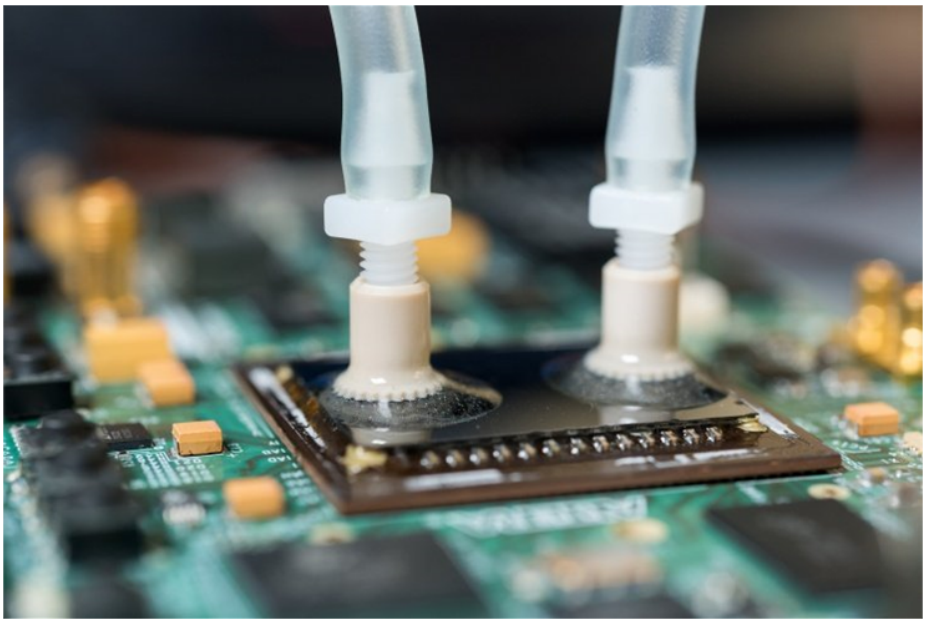


Figure 107: Real FPGA die with microfluidic cooling.

6.2.5 Irregular Power Distribution Network Modeling

In the power distribution network modeling work, we assume regular/rectangular power and ground grid/plane. This assumption is appropriate for on-die and package power distribution network. However, it is not always the case for board-level power/ground planes. The power and ground planes on board can be irregular. In that case, we have to adopt and implement a more complex meshing scheme for the irregular power/ground planes. The numerical simulator is very flexible in that a different meshing scheme can be integrated.

6.2.6 In-Package and On-Die Voltage Regulator Simulation

A number of researchers are working on integrated voltage regulators to save power and improve system performance [85]. Compared to the conventional on-board voltage regulator, the in-package and on-die integrated voltage regulator has many benefits: 1) improved response time, the switching frequency increases to 100 MHz from a few Hz, 2) fine-grain power management by having many voltage regulators, 3) reducing the board size and routing complexity, 4) reducing the decoupling capacitor requirement due to the faster switching frequency, and 5) reducing power loss and cost. The numerical power distribution network simulator can be extended to include a voltage regulator model, which would enable investigating the trade-offs of the integrated voltage regulator and co-design of voltage regulator and power distribution network.

REFERENCES

[1] M. S. Bakir and J. D. Meindl, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*. Boston: Artech House, 2008.

[2] M. Horowitz, "Computing's energy problem (and what we can do about it)," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International*, Feb 2014, pp. 10–14.

[3] G. E. MOORE, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, April 1965.

[4] S. Jones, "Cashing in with chips: Improving efficiency in semiconductor r&d," March 2014, http://www.alixpartners.com/.

[5] R. S. Brett Howse, "Tick tock on the rocks: Intel delays 10nm, adds 3rd gen 14nm core product "kaby lake"," July 2015, http://www.anandtech.com/.

[6] R. Nagarajan, "Multicore technologies and software challenges," January 2010, http://www.embedded.com/.

[7] K. Shakeri and J. Meindl, "Temperature variable supply voltage for power reduction," in *VLSI, 2002. Proceedings. IEEE Computer Society Annual Symposium on*, 2002, pp. 64–67.

[8] L. He, W. Liao, and M. Stan, "System level leakage reduction considering the interdependence of temperature and leakage," in *Design Automation Conference, 2004. Proceedings. 41st*, July 2004, pp. 12–17.

[9] W. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. Sule, M. Steer, and P. Franzon, "Demystifying 3d ics: the pros and cons of going vertical," *Design Test of Computers, IEEE*, vol. 22, no. 6, pp. 498–510, Nov 2005.

[10] P. Emma and E. Kursun, "Is 3d chip technology the next growth engine for performance improvement?" *IBM Journal of Research and Development*, vol. 52, no. 6, pp. 541–552, Nov 2008.

[11] L. Li, P. Su, J. Xue, M. Brillhart, J. Lau, P. Tzeng, C. Lee, C. Zhan, M. Dai, H. Chien, and S. Wu, "Addressing bandwidth challenges in next generation high performance network systems with 3d ic integration," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, May 2012, pp. 1040–1046.

[12] J. Knickerbocker, P. Andry, L. P. Buchwalter, A. Deutsch, R. Horton, K. Jenkins, Y. Kwark, G. McVicker, C. Patel, R. Polastre, C. Schuster, A. Sharma, S. Sri-Jayantha, C. Surovic, C. K. Tsang, B. Webb, S. Wright, S. R. McKnight,

E. Sprogis, and B. Dang, "Development of next-generation system-on-package (sop) technology based on silicon carriers with fine-pitch chip interconnection," *IBM Journal of Research and Development*, vol. 49, no. 4.5, pp. 725–753, July 2005.

[13] W. Wahby, A. Dembla, and M. Bakir, "Evaluation of 3dics and fabrication of monolithic interlayer vias," in *3D Systems Integration Conference (3DIC), 2013 IEEE International*, Oct 2013, pp. 1–6.

[14] M. Swaminathan and E. Engin, *Power Integrity: Modeling and Design for Semiconductor and Systems*. Boston: Prentice Hall PTR, 2007.

[15] S. Sri-Jayantha, G. McVicker, K. Bernstein, and J. Knickerbocker, "Thermomechanical modeling of 3d electronic packages," *IBM Journal of Research and Development*, vol. 52, no. 6, pp. 623–634, Nov 2008.

[16] G. Huang, M. Bakir, A. Naeemi, and J. Meindl, "Power delivery for 3-d chip stacks: Physical modeling and design implication," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 5, pp. 852–859, May 2012.

[17] S.-C. Lin and K. Banerjee, "Cool chips: Opportunities and implications for power and thermal management," *Electron Devices, IEEE Transactions on*, vol. 55, no. 1, pp. 245–255, Jan 2008.

[18] D. Tuckerman and R. Pease, "High-performance heat sinking for vlsi," *Electron Device Letters, IEEE*, vol. 2, no. 5, pp. 126–129, May 1981.

[19] J.-M. Koo, S. Im, L. Jiang, and K. E. Goodson, "Integrated microchannel cooling for three-dimensional electronic circuit architectures," *J. Heat Transfer*, vol. 127, no. 1, pp. 49–58, 2005.

[20] T. Brunschwiler, B. Michel, H. Rothuizen, U. Kloter, B. Wunderle, H. Oppermann, and H. Reichl, "Interlayer cooling potential in vertically integrated packages," *Microsystem Technologies*, vol. 15, no. 1, pp. 57–74, Jan. 2009.

[21] T. Brunschwiler, S. Paredes, U. Drechsler, B. Michel, W. Cesar, G. Toral, Y. Temiz, and Y. Leblebici, "Validation of the porous-medium approach to model interlayer-cooled 3d-chip stacks," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, Sept 2009, pp. 1–10.

[22] Y. Zhang, L. Zheng, and M. Bakir, "3-d stacked tier-specific microfluidic cooling for heterogeneous 3-d ics," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 11, pp. 1811–1819, Nov 2013.

[23] Y. Peles, A. Kosar, C. Mishra, C. Kuo, and B. Schneider, "Forced convective heat transfer across a pin fin micro heat sink," *International J. Heat Mass Transfer*, vol. 48, p. 3615C3627, Aug 2005.

[24] T. Sarvey, Y. Zhang, Y. Zhang, H. Oh, and M. Bakir, "Thermal and electrical effects of staggered micropin-fin dimensions for cooling of 3d microsystems," in *Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2014 IEEE Intersociety Conference on*, May 2014, pp. 205–212.

[25] B. Dang, M. Bakir, D. Sekar, C. King, and J. Meindl, "Integrated microfluidic cooling and interconnects for 2d and 3d chips," *Advanced Packaging, IEEE Transactions on*, vol. 33, no. 1, pp. 79–87, Feb 2010.

[26] C. King, D. Sekar, M. Bakir, B. Dang, J. Pikarsky, and J. Meindl, "3d stacking of chips with electrical and microfluidic i/o interconnects," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, May 2008, pp. 1–7.

[27] M. Matsuo, N. Hayasaka, K. Okumura, E. Hosomi, and C. Takubo, "Silicon interposer technology for high-density package," in *Electronic Components amp; Technology Conference, 2000. 2000 Proceedings. 50th*, 2000, pp. 1455–1459.

[28] M. Sunohara, T. Tokunaga, T. Kurihara, and M. Higashi, "Silicon interposer with tsvs (through silicon vias) and fine multilayer wiring," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, May 2008, pp. 847–852.

[29] V. Kumar, L. Zheng, M. Bakir, and A. Naeemi, "Compact modeling and optimization of fine-pitch interconnects for silicon interposers," in *Interconnect Technology Conference (IITC), 2013 IEEE International*, June 2013, pp. 1–3.

[30] N. Kim, D. Wu, D. Kim, A. Rahman, and P. Wu, "Interposer design optimization for high frequency signal transmission in passive and active interposer using through silicon via (tsv)," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, May 2011, pp. 1160–1167.

[31] R. Chaware, K. Nagarajan, K. Ng, and S. Y. Pai, "Assembly process integration challenges and reliability assessment of multiple 28nm fpgas assembled on a large 65nm passive interposer," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*, April 2012, pp. 2B.2.1–2B.2.5.

[32] J. Cunningham, A. Krishnamoorthy, R. Ho, I. Shubin, H. Thacker, J. Lexau, D. Lee, D. Feng, E. Chow, Y. Luo, X. Zheng, G. Li, J. Yao, T. Pinguet, K. Raj, M. Asghari, and J. Mitchell, "Integration and packaging of a macrochip with silicon nanophotonic links," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, no. 3, pp. 546–558, May 2011.

[33] T. Dickson, Y. Liu, S. Rylov, B. Dang, C. Tsang, P. Andry, J. Bulzacchelli, H. Ainspan, X. Gu, L. Turlapati, M. Beakes, B. Parker, J. Knickerbocker, and D. Friedman, "An 8x 10-gb/s source-synchronous i/o system based on high-density silicon carrier interconnects," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 4, pp. 884–896, April 2012.

[34] I. Shubin, E. Chow, A. Chow, D. De Bruyker, H. Thacker, K. Fujimoto, K. Raj, A. Krishnamoorthy, J. Mitchell, and J. Cunningham, "Package demonstration of an interposer with integrated tsvs and flexible compliant interconnects," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, May 2013, pp. 329–333.

[35] S. Wright, R. Polastre, H. Gan, L. P. Buchwalter, R. Horton, P. Andry, E. Sprogis, C. Patel, C. Tsang, J. Knickerbocker, J. R. Lloyd, A. Sharma, and M. S. Sri-Jayantha, "Characterization of micro-bump c4 interconnects for si-carrier sop applications," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, 2006, pp. 8 pp.–.

[36] S. W. Yoon, J. H. Ku, N. Suthiwongsunthorn, P. Marimuthu, and F. Carson, "Fabrication and packaging of microbump interconnections for 3d tsv," in *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on*, Sept 2009, pp. 1–5.

[37] H. Yang, C. Zhang, and M. Bakir, "Self-aligning silicon interposer tiles and silicon bridges for large nanophotonics enabled systems," *Electronics Letters*, vol. 50, no. 20, pp. 1475–1477, September 2014.

[38] H. S. Yang, C. Zhang, M. Zia, L. Zheng, and M. Bakir, "Interposer-to-interposer electrical and silicon photonic interconnection platform using silicon bridge," in *Optical Interconnects Conference, 2014 IEEE*, May 2014, pp. 71–72.

[39] K. Wong, T. Rahal-Arabi, M. Ma, and G. Taylor, "Enhancing microprocessor immunity to power supply noise with clock-data compensation," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 4, pp. 749–758, April 2006.

[40] W. Becker, J. Eckhardt, R. Frech, G. Katopis, E. Klink, M. McAllister, T. McNamara, P. Muench, S. Richter, and H. Smith, "Modeling, simulation, and measurement of mid-frequency simultaneous switching noise in computer systems," *Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on*, vol. 21, no. 2, pp. 157–163, May 1998.

[41] B. Garben, M. McAllister, W. Becker, and R. Frech, "Mid-frequency delta-i noise analysis of complex computer system boards with multiprocessor modules and verification by measurements," *Advanced Packaging, IEEE Transactions on*, vol. 24, no. 3, pp. 294–303, Aug 2001.

[42] G. Huang, M. Bakir, A. Naeemi, H. Chen, and J. Meindl, "Power delivery for 3d chip stacks: Physical modeling and design implication," in *Electrical Performance of Electronic Packaging, 2007 IEEE*, Oct 2007, pp. 205–208.

[43] N. Khan, S. Alam, and S. Hassoun, "Power delivery design for 3-d ics using different through-silicon via (tsv) technologies," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 19, no. 4, pp. 647–658, April 2011.

[44] K. Shakeri and J. Meindl, "Compact physical ir-drop models for chip/package co-design of gigascale integration (gsi)," *Electron Devices, IEEE Transactions on*, vol. 52, no. 6, pp. 1087–1096, June 2005.

[45] J. Xie and M. Swaminathan, "Electrical-thermal co-simulation of 3d integrated systems with micro-fluidic cooling and joule heating effects," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 234–246, Feb 2011.

[46] H. Chen and J. Neely, "Interconnect and circuit modeling techniques for full-chip power supply noise analysis," *Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on*, vol. 21, no. 3, pp. 209–215, Aug 1998.

[47] Z. Xu, Q. Wu, H. He, and J.-Q. Lu, "Electromagnetic-simulation program with integrated circuit emphasis modeling, analysis, and design of 3-d power delivery," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 4, pp. 641–652, April 2013.

[48] H. He and J.-Q. Lu, "Modeling and analysis of pdn impedance and switching noise in tsv-based 3-d integration," *Electron Devices, IEEE Transactions on*, vol. 62, no. 4, pp. 1241–1247, April 2015.

[49] J. S. Pak, J. Kim, J. Cho, K. Kim, T. Song, S. Ahn, J. Lee, H. Lee, K. Park, and J. Kim, "Pdn impedance modeling and analysis of 3d tsv ic by using proposed p/g tsv array model based on separated p/g tsv and chip-pdn models," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 208–219, Feb 2011.

[50] R. Tummala, Ed., *Fundamentals of Microsystems Packaging*. McGraw Hill, 2001.

[51] B. Dang, M. Bakir, and J. Meindl, "Integrated thermal-fluidic i/o interconnects for an on-chip microchannel heat sink," *Electron Device Letters, IEEE*, vol. 27, no. 2, pp. 117–119, Feb 2006.

[52] C. King, J. Zaveri, M. Bakir, and J. Meindl, "Electrical and fluidic c4 interconnections for inter-layer liquid cooling of 3d ics," in *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th*, June 2010, pp. 1674–1681.

[53] K. A. Brakke, "The surface evolver," *Experimental Mathematics*, vol. 1, no. 2, pp. 141–165, 1992.

[54] T. Brunschwiler, Y. Madhour, T. Tick, G. Schlottig, and S. Oggioni, "Investigation of novel solder patterns for power delivery and heat removal support," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, May 2013, pp. 417–424.

[55] M. Massoud, Ed., *Engineering Thermofluids: Thermodynamics, Fluid Mechanics, and Heat Transfer*. Springer US, 2005.

[56] Y. Zhang, L. Zheng, and M. Bakir, "Tier-independent microfluidic cooling for heterogeneous 3d ics with nonuniform power dissipation," in *Interconnect Technology Conference (IITC), 2013 IEEE International*, June 2013, pp. 1–3.

[57] L. Zheng, Y. Zhang, G. Huang, and M. Bakir, "Novel electrical and fluidic microbumps for silicon interposer and 3-d ics," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, no. 5, pp. 777–785, May 2014.

[58] Y. Zhang, A. Dembla, and M. Bakir, "Silicon micropin-fin heat sink with integrated tsvs for 3-d ics: Tradeoff analysis and experimental testing," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 11, pp. 1842–1850, Nov 2013.

[59] Y. Zhang, C. King, J. Zaveri, Y. J. Kim, V. Sahu, Y. Joshi, and M. Bakir, "Coupled electrical and thermal 3d ic centric microfluidic heat sink design and technology," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, May 2011, pp. 2037–2044.

[60] A. Dembla, Y. Zhang, and M. Bakir, "High aspect ratio tsvs in micropin-fin heat sinks for 3d ics," in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*, Aug 2012, pp. 1–6.

[61] H. Oh, Y. Zhang, L. Zheng, and M. Bakir, "Electrical interconnect and microfluidic cooling within 3d ics and silicon interposer," in *Proc. ASME 4th Joint US-European Fluids Engineering Division Summer Meeting and 12th International Conf. Nanochannels, Microchannels, and Minichannels*, Chicago, IL, USA, 2014.

[62] J. Xie and M. Swaminathan, "Fast electrical-thermal co-simulation using multigrid method for 3d integration," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, May 2012, pp. 651–657.

[63] Y. Zhang, Y. Zhang, and M. Bakir, "Thermal design and constraints for heterogeneous integrated chip stacks and isolation technology using air gap and thermal bridge," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, no. 12, pp. 1914–1924, Dec 2014.

[64] Y. Zhang, T. Sarvey, and M. Bakir, "Thermal challenges for heterogeneous 3d ics and opportunities for air gap thermal isolation," in *3D Systems Integration Conference (3DIC), 2014 International*, Dec 2014, pp. 1–5.

[65] Intel. (2010) New 2010 intel coretmi7 processor extreme edition. Http://newsroom.intel.com, [Available Online].

[66] S. Li, J. H. Ahn, R. Strong, J. Brockman, D. Tullsen, and N. Jouppi, "Mcpat: An integrated power, area, and timing modeling framework for multicore and manycore architectures," in *Microarchitecture, 2009. MICRO-42. 42nd Annual IEEE/ACM International Symposium on*, Dec 2009, pp. 469–480.

[67] Intel. (2013) Core i7 processor families for the lga2011-0 socket: Thermal mechanical specification and design guide. Http://www.intel.com/.

[68] S. Lee, S. Song, V. Au, and K. Moran, "Constricting/spreading re- sistance model for electronics packaging," in *Proc. American-Japan Thermal Eng. Conf.*, Mar. 1995, pp. 199–206.

[69] B. Krauter and S. Mehrotra, "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," in *Design Automation Conference, 1998. Proceedings*, June 1998, pp. 303–308.

[70] A. Djordjevic and T. Sarkar, "Closed-form formulas for frequency-dependent resistance and inductance per unit length of microstrip and strip transmission lines," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 42, no. 2, pp. 241–248, Feb 1994.

[71] S. H. Hall and H. L. Heck, *Advanced Signal Integrity for High-Speed Digital Designs*. Wiley-IEEE Press, 2009.

[72] Synopsys. (2015) Hspice. Www.synopsys.com.

[73] H. Cho, P. Kapur, and K. Saraswat, "Power comparison between high-speed electrical and optical interconnects for interchip communication," *Lightwave Technology, Journal of*, vol. 22, no. 9, pp. 2021–2033, Sept 2004.

[74] V. Kumar, R. Sharma, E. Uzunlar, L. Zheng, R. Bashirullah, P. Kohl, M. Bakir, and A. Naeemi, "Airgap interconnects: Modeling, optimization, and benchmarking for backplane, pcb, and interposer applications," *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 4, no. 8, pp. 1335–1346, Aug 2014.

[75] D. M. Pozar, *Microwave Engineering*. John Wiley & Sons, Inc., 2011.

[76] R. Venkatesan, "Multilevel interconnect architectures for gigascale integration (gsi)," Ph.D. dissertation, Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 2003.

[77] Y.-J. Lee, Y. J. Kim, G. Huang, M. Bakir, Y. Joshi, A. Fedorov, and S. K. Lim, "Co-design of signal, power, and thermal distribution networks for 3d ics," in *Design, Automation Test in Europe Conference Exhibition, 2009. DATE '09.*, April 2009, pp. 610–615.

[78] M. Bakir, C. King, D. Sekar, H. Thacker, B. Dang, G. Huang, A. Naeemi, and J. Meindl, "3d heterogeneous integrated systems: Liquid cooling, power delivery, and implementation," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, Sept 2008, pp. 663–670.

[79] T. Zhou, T. Strach, and W. Becker, "On chip circuit model for accurate mid-frequency simultaneous switching noise prediction," in *Electrical Performance of Electronic Packaging, 2005. IEEE 14th Topical Meeting on*, Oct 2005, pp. 275–278.

[80] Synopsys. (2015) Raphael. Http://www.synopsys.com.

[81] H. Zhuang, S.-H. Weng, J.-H. Lin, and C. kuan Cheng, "Matex: A distributed framework for transient simulation of power distribution networks," in *Design Automation Conference (DAC), 2014 51st ACM/EDAC/IEEE*, June 2014, pp. 1–6.

[82] G. Huang, A. Naeemi, T. Zhou, D. O'Connor, A. Muszynski, B. Singh, D. Becker, J. Venuto, and J. Meindl, "Compact physical models for chip and package power and ground distribution networks for gigascale integration (gsi)," in *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th*, May 2008, pp. 646–651.

[83] G. Huang, "Compact physical models for power supply noise and chip/package co-design in gigascale integration (gsi) and three-dimensional (3-d) integration systems," Ph.D. dissertation, Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 2008.

[84] J.-H. Kim and M. Swaminathan, "Modeling of irregular shaped power distribution planes using transmission matrix method," *Advanced Packaging, IEEE Transactions on*, vol. 24, no. 3, pp. 334–346, Aug 2001.

[85] E. Burton, G. Schrom, F. Paillet, J. Douglas, W. Lambert, K. Radhakrishnan, and M. Hill, "Fivr - fully integrated voltage regulators on 4th generation intel core socs," in *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, March 2014, pp. 432–439.