3D AND 2.5D HETEROGENEOUS INTEGRATION PLATFORMS WITH INTERCONNECT STITCHING AND MICROFLUIDIC COOLING

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3D AND 2.5D HETEROGENEOUS INTEGRATION PLATFORMS WITH INTERCONNECT STITCHING AND MICROFLUIDIC COOLING

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DEDICATION

Dedicated to my wife Hong Cui

And my parents Xinhui Wang and Changan Zhang

for their endless love and support.

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SUMMARY

Signal integrity and thermal management are two major challenges in heterogeneous integration technologies. In this research, the impact of through silicon vias (TSVs) on electrical performance of 3D/2.5D IC was experimentally investigated. It was found the delay of a 3D IC link can be improved by up 17.4% by decreasing the distance between the driver and the TSV. To address the thermal challenges, embedded microfluidic cooling was proposed and two testbeds were fabricated and characterized. The first testbed investigated boiling of water in large micropin-fin arrays at sub-atmospheric pressures for the first time. The maximum heat transfer coefficient was up to 60 kW/m^2K. The second testbed was to emulate chip hotspots with ultra-high heat flux of up to 4.75 kW/cm^2.

A heterogeneous interconnect stitching technology (HIST) platform was proposed to avoid the shortcomings of conventional heterogeneous integration technologies. HIST achieves a similar signal bandwidth density as a silicon interposer, but is not reticle-size limited; HIST is based on Si-Si face-to-face bonding, thus enables high I/O pitch; HIST eliminates the need for TSVs and is agnostic to packaging substrate. The signal performance was investigated for both digital and analog/RF applications. Through modeling, the bandwidth density of HIST platform can reach up to 9.3 Tbps/cm with a power efficiency of 0.24 pJ/bit. The insertion loss of a HIST channel was 0.85 dB/mm at 50 GHz. The measured inductance and capacitance values of the compressible microinterconnects (CMIs), which core of the HIST platform, are approximately 50 pH and 80 fF and can be decreased via scaling.

CHAPTER 1

INTRODUCTION

1.1 Current Trend of Heterogeneous Integration

In the era of big data, cloud computing and Internet-of-Things (IoT), the massive amount of digital data produced today is unprecedented in human history. The volume of data created, replicated, and consumed in 2020 is predicted to be more than 44 exabytes (ZB), which is 300 times greater than in 2005 [1], as shown in Fig. 1.

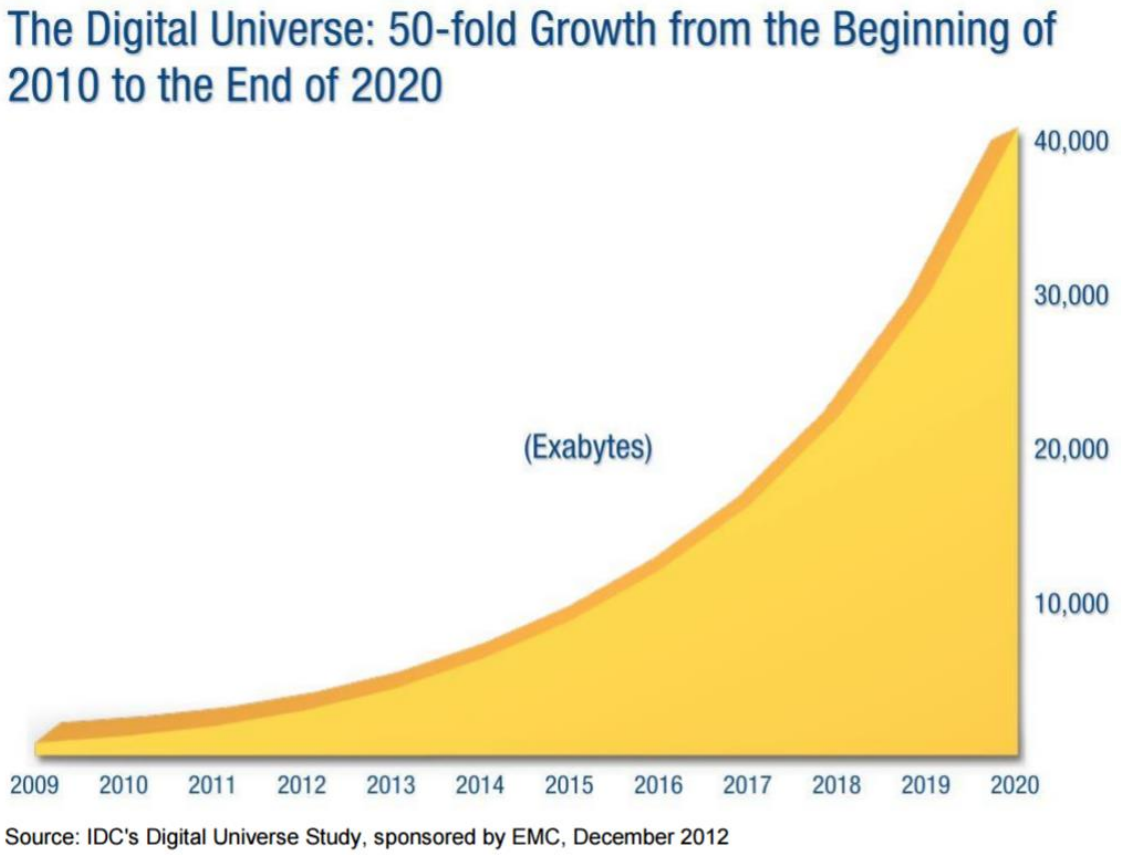


Fig. 1. The amount of digital data per year.

This explosion of data has spurred significant research in high performance computing. Figure 2 shows the trend of microprocessors in the past 40 years. By scaling

CMOS technology, the single-thread performance and number of transistors in microprocessors have improved logarithmically over time. The industry has followed Moore's Law until recent technology nodes [2], where the typical power, operating frequency and single-thread performance became saturated, as shown in Fig 2. The continued aggressive scaling of transistors has reached a point where off-chip interconnect performance and power dissipation become limiting factors for high-performance integrated circuits [3]. As shown in Fig. 3 [4], increasing the off-chip memory bandwidth by 2X can improve the performance of a multi-core processor by approximately 30%.

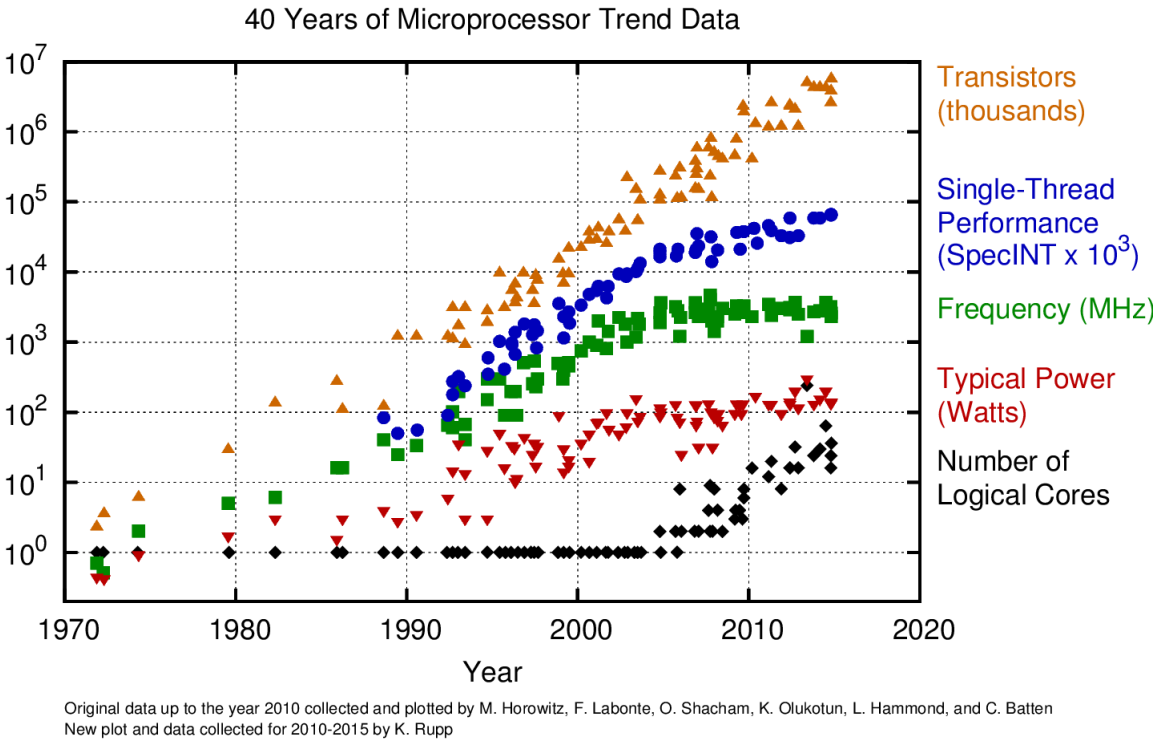


Fig. 2. 40 years of microprocessor trend data.

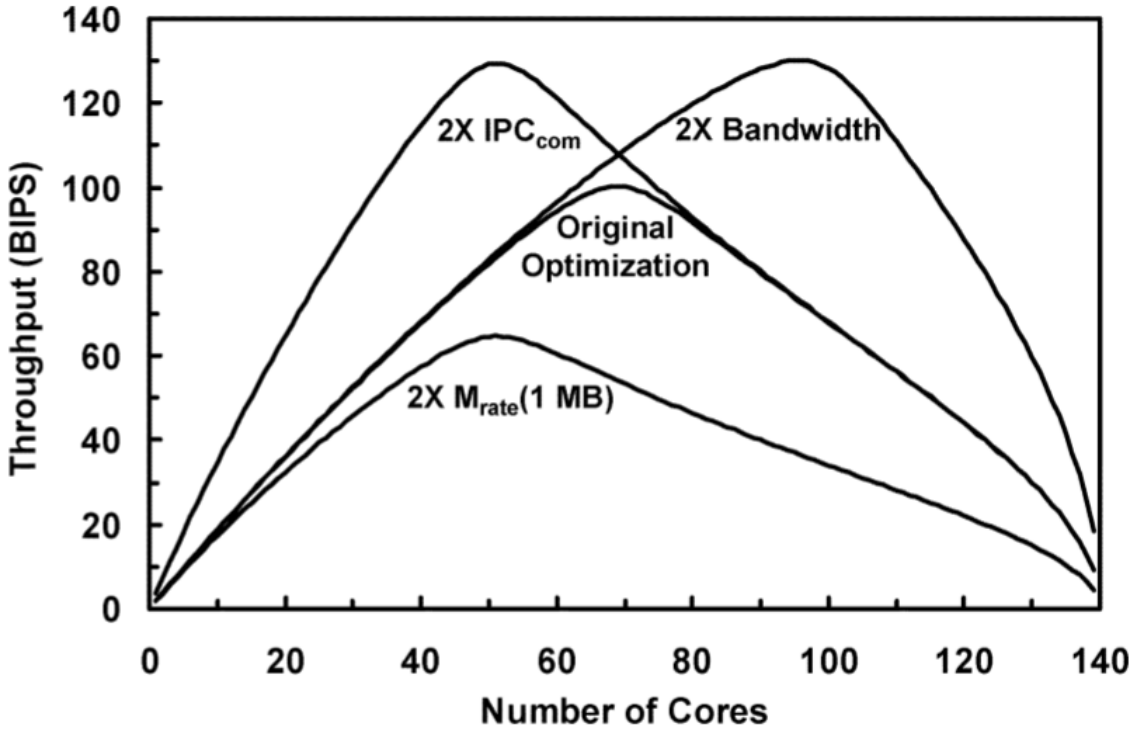


Fig. 3. Performance of a multi-core processor with doubling memory bandwidth.

To improve the signal bandwidth, decrease latency and energy-per-bit (EPB) of the interconnects, advanced integration technologies including three-dimensional (3D) integrated circuits (IC) and silicon interposers (2.5D IC) have been proposed. Compared to a conventional packaging on the motherboard, a heterogeneous 3D IC or 2.5D IC can significantly increase the number of signal channels while decreasing the average length of the interconnects. Figure 4 illustrates the schematics of a typical 3D IC and a typical 2.5D IC.

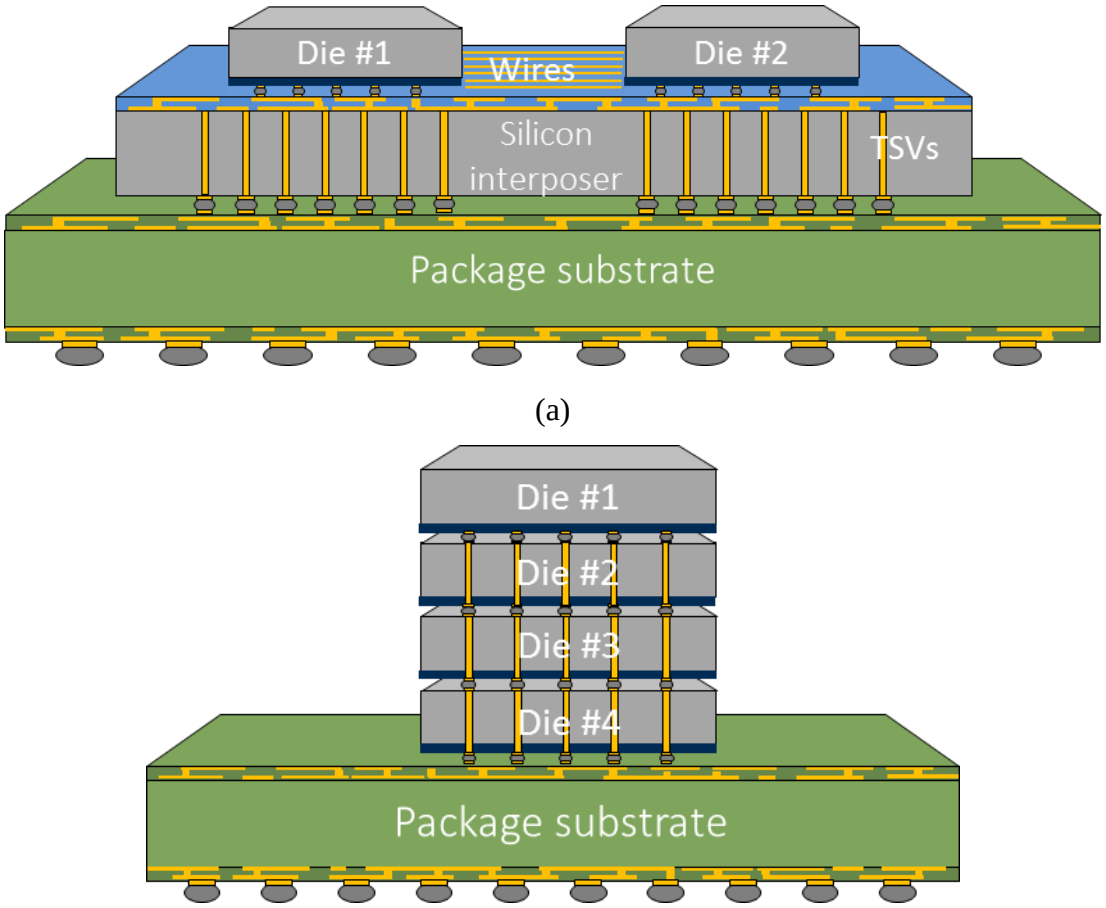


Fig. 4 Schematics of typical 2.5D IC (a) and 3D IC (b).

Interconnect performance and power dissipation are two major challenges facing high-performance computing systems [5]. They become even more challenging for 3D/2.5D integrated systems [6], [7]. From an electrical aspect, the combination of high resistance on-chip wires and high capacitance TSVs may lead to a significant signal delay and loss. From a thermal aspect, as the increasing integration levels push the power density higher, the heat dissipation in 3D ICs may exceed the capability of conventional air-cooled heat sinks. A switch from air cooling to microfluidic cooling is believed to be a promising

solution. In addition to the electrical and thermal challenges, 3D/2.5D integration technologies have other TSV-related undesired characteristics.

Therefore, the research reported in this dissertation will focus on investigating the electrical and thermal challenges in 3D/2.5D IC, and a heterogeneous interconnect stitching technology (HIST) platform that mimics monolithic-like performance and eliminates the use of TSVs.

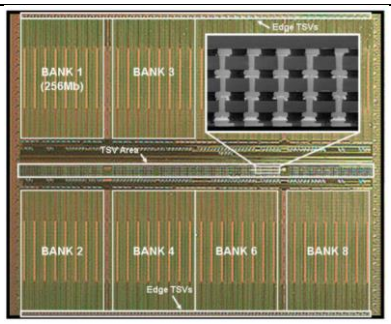
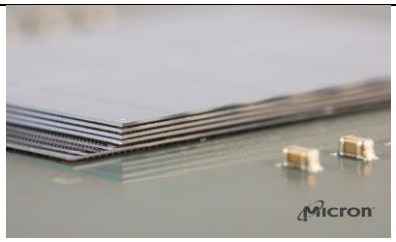
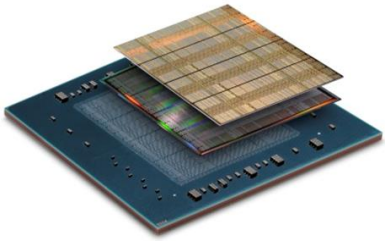
1.2 Current State of the Art Relevant Research

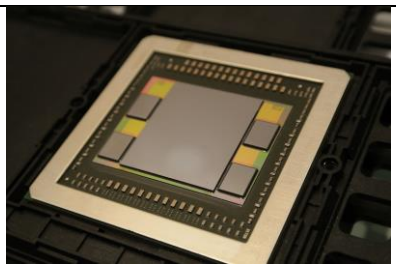
1.2.1 3D/2.5D IC products and electrical characteristics of TSVs

Table 1 summarizes recent 3D/2.5D IC products. In 2009, Samsung announced the first 8 Gb volume 3D DRAM with 300 TSVs on a minimal pitch down to 40 μm [8]. Compared to conventional quad-die package (QDP), 3D DRAM was able to improve the I/O data rate from 1066 Mb/s to 1600 Mb/s and decrease the power by up to 50%. Later in 2011, Micron announced the hybrid memory cube (HMC) where 4 layers of DRAM dice were stacked on top of a logic die and interconnected with TSVs [9]. It is announced that compared to conventional DDR3 module, HMC can achieve a 10X improvement in data bandwidth and 70% decrease in power. For 2.5D IC technologies, Xilinx and TSMC released the first 2.5D FPGA product in which four 28 nm node FPGA chips are assembled on a 180 nm node silicon interposer with TSVs [10]. In 2015, their latest 2.5D IC FPGA reached a maximum bandwidth of 400 Gb/s between a digital-analog-converter and Virtex-7 FPGAs [11]. The high bandwidth memory (HBM) technology announced by SK Hynix utilizes 3D IC and 2.5D IC technologies simultaneously. In HBM, 3D DRAM dice are assembled on a silicon interposer with logic chips [12]. It was first used in AMD's Fiji GPU and can improve the memory bandwidth per watt by 3X [13]. Recently, NVidia

announced their Tesla P100 GPU using the second generation HBM technology [14]. Compared to conventional board level integration with DDR4 modules, P100 can improve memory bandwidth and GPU performance by 2X, and can achieve a performance improvement by up to 5X for specific applications such as deep learning [14].

Table 1: Selected 3D/2.5D IC products

Product/Year		Technology	Performance Improvement Compared to 2D ICs
Samsung 3D DRAM 2009 [8]		3D Integration with TSV	50% increase in I/O data rate; 50% power reduction.
Micron HMC 2011 [9]		3D Integration with TSV	10X improvement in bandwidth; 70% power reduction.
Xilinx Virtex-7 2011 [10]		2.5D Silicon Interposer	Aggregate bandwidth up to 400 Gbps; Up to 70% power reduction.

AMD Fiji 2015 [13]		HBM (3D + 2.5D IC)	3X in memory bandwidth per watt
NVidia Tesla P100 2016 [14]		HBM2 (3D + 2.5D IC)	2X improvement in memory bandwidth and GPU performance.

Prior research in academic has focused on the modeling and measurements of TSV channels [15] – [29]. Compact physical models for resistance, inductance, conductance and capacitance (RLGC) were reported in [15]. Similar RLGC models for high-frequency were also reported by C. Xu, et al. [16]. R. Fang et al. [17] developed an analytic TSV capacitance model and investigated the impact of different design parameters including dielectric layer thickness, substrate doping concentration, core material, etc. I. Ndip, et al. [18] investigated different signal propagation modes including slow wave, quasi-TEM and skin-effect modes, as well as the impact of substrate resistivity. It is found silicon substrates with higher resistivity have lower TSV insertion loss. The effect of slow wave and quasi-TEM modes were also reported by J. S. Pak, et al. [19]. TSV capacitance models considering depletion/inversion layer for a single TSV and ground-signal (GS) TSV pairs were reported in [20] and [21], respectively. The depletion/inversion capacitance will decrease the total TSV capacitance, especially when the frequency is lower than 1 GHz. TSV capacitance with conventional silicon dioxide isolation layer was characterized by M. Brocard et al. [22] for different voltage bias and frequency. Alternative isolation materials

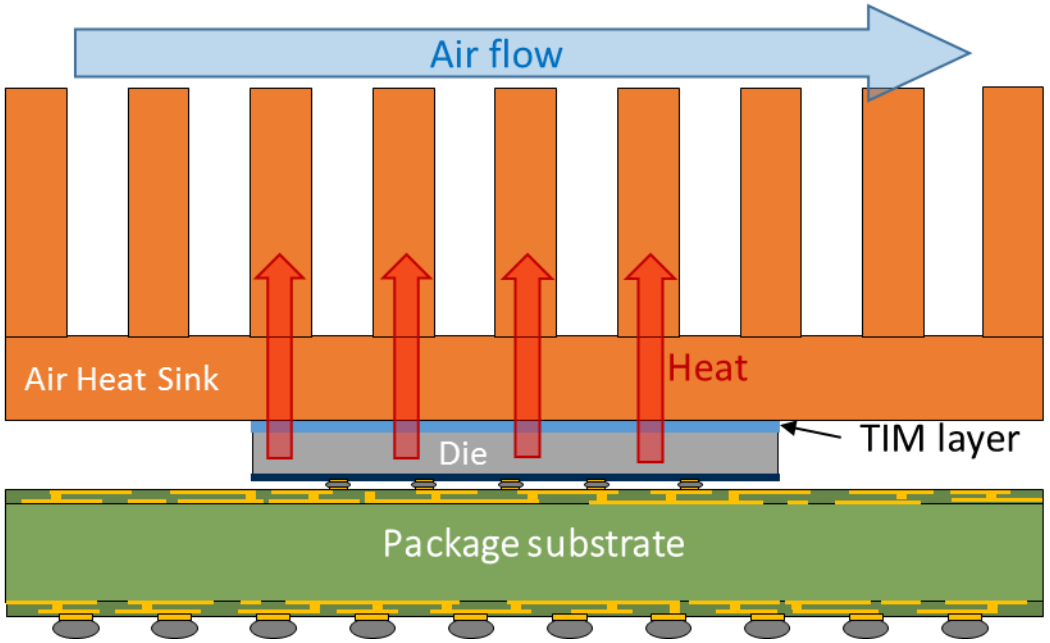
including polymer [23] and air [24] were also reported. The results showed a decreased TSV capacitance and improved reliability. The channel loss, reflection and eye-diagrams of TSV channels including TSVs and horizontal wires have been extensively investigated [25]. H. Kim et al. [26] compared the loss of a conventional multichip module (MCM) channel to a 2.5D IC channel, which showed smaller loss. K.-S. Choi et al. [27] characterized the TSV link with high resistivity silicon substrate and polymer isolation layer. The channel loss is significantly lower than those with low resistivity silicon substrate and silicon dioxide isolation layer. X. Gu et al. measured a TSV channel with micro-bumps up to 40 GHz [28]. The channel loss was demonstrated to be much lower than printed circuit board (PCB) level channels.

Even though prior research has focused on a wide range of topics in 3D/2.5D integration, the interaction of TSVs and on-chip wires has not been thoroughly investigated. Experimental exploration of how TSVs and on-chip wires impact the overall performance of 3D IC links will be reported in Chapter II.

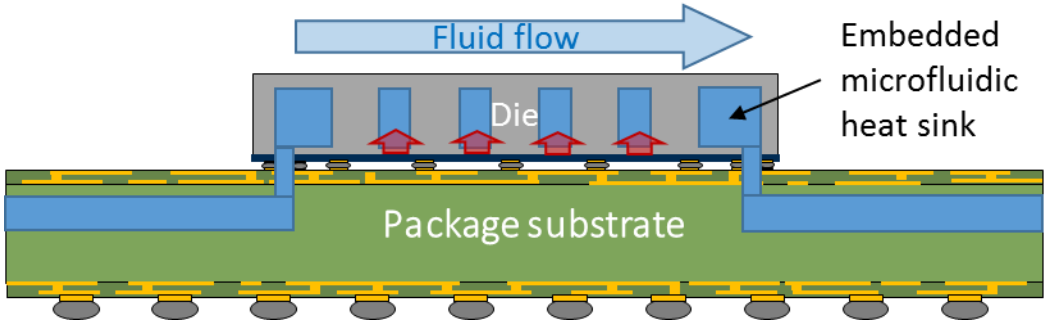
1.2.2 Embedded microfluidic cooling

Researchers have shown the possibility of using embedded microfluidic cooling for high performance microelectronics [30] – [39]. Figure 5 illustrates conventional air cooling and embedded microfluidic cooling. Compared to conventional air cooling, the advantages of embedded microfluidic cooling include: (a) fluidic coolants such as deionized water (D.I. water) has much higher heat capacity than air; (b) embedded microfluidic heat sink can be integrated into silicon substrate, therefore the thermal resistance from the transistor layer to the heat sink is smaller compare to that of air cooling; (c) for the case of 3D/2.5D

ICs, the embedded microfluidic cooling heat sink is vertically scalable such that multiple heat sinks can be integrated into all of the silicon dice and interposer, while the air cooling heat sink can only be applied to the very top layer of the stack.



(a)



(b)

Fig. 5 Schematic of conventional air cooling (a) and embedded microfluidic cooling (b).

Table 2 summarizes the evolution of microfluidic heat sink designs. In 1981, Tuckerman and Pease [30] demonstrated single-phase microfluidic cooling for the first time using D. I. water. By using microchannels (50 μm channel width, 50 μm wall width,

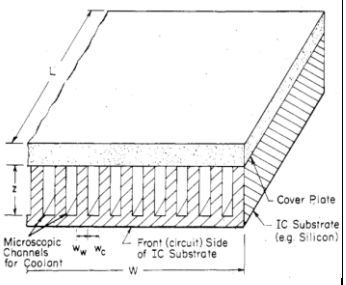
and 302 μm cavity height), they were able to dissipate a heat flux of 790 W/cm^2 with maximum substrate temperature rise of 71 ^{o}C. Brunschwiler et al. [31] studied a three-tier single-phase microfluidic cooled 3D IC stack with a footprint of 1 cm^2 and maximum power of 390 W. They found that when the microchannel wall width equals the micropin-fin diameter (50 μm), with the same pitch (100 μm) and cavity height (100 μm), micropin-fin design has smaller convective thermal resistance in general while microchannels can improve cooling for strongly localized hotspots due to better tier-to-tier coupling. Peles et al. [32] investigated heat transfer and pressure drop phenomena of micropin fin heat sinks for single-phase cooling. They concluded that cylindrical micropin fin arrays are superior to plain microchannel based cooling.

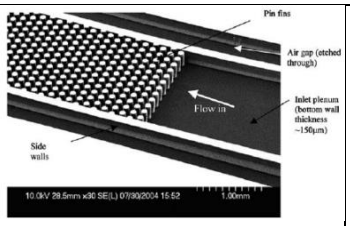
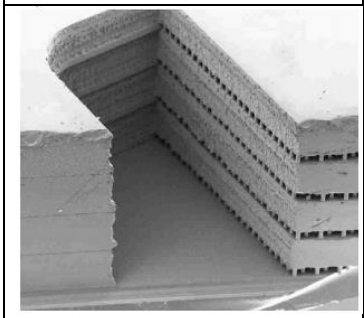
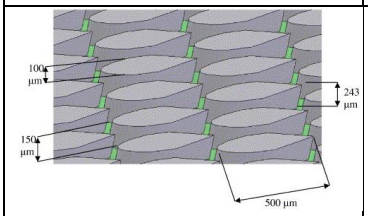
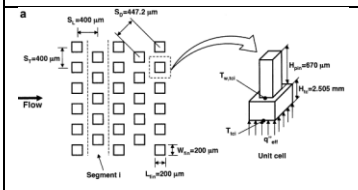
For two phase cooling, Qu et al. [33] studied flow boiling heat transfer of water in an array of staggered square micro-pinfins covering an area of 3.38 cm by 1 cm. The cross-section area of a single pin was 200 μm by 200 μm, and height was 670 μm. They observed that the two-phase heat transfer coefficient decreased with increasing heat flux at low quality, and was fairly constant at a vapor quality greater than 0.15. Reeser et al. [34] recently compared heat transfer and pressure drop characteristics of HFE-7200 and deionized (D.I.) water in inline and staggered micropin-fin arrays. Studied heat fluxes ranged from 1 to 36 W/cm^2 and 10 to 110 W/cm^2 for HFE-7200 and water, respectively. Heat transfer coefficients behavior differed significantly for HFE-7200 and D.I. water due to different material properties of both working fluids. Kosar et al. [35] studied flow boiling of R-123 for micro hydrofoil shaped pin-fins with heat fluxes up to 312 W/cm^2 and mass fluxes up to 2,349 kg/m^{2}s. The fins are 243 μm tall and 150 μm apart. The heat transfer coefficient was found to increase with heat flux until a maximum was reached, and then

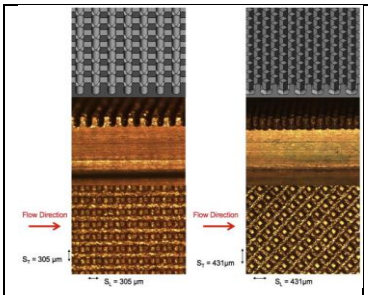
decreased monotonically with heat flux until critical heat flux (CHF) was reached. Kim et al. [36] investigated micro-gap-channels which are 10 mm wide by 37mm long, with channel heights varying from 110 μm to 500 μm and heat flux of 20 W/cm^2. Krishnamurthy et al. [37] studied flow boiling of water in a 1.8 mm wide, 1 cm long and 250 μm deep microchannel with staggered circular pin-fins. The dissipated heat flux was up to 350 W/cm^2 at mass fluxes up to 794 kg/m^{2}s. They found that the two-phase heat transfer coefficient was moderately dependent on mass flux, and independent of heat flux, for the range of mass fluxes and heat fluxes tested. Bowers et al. [38] dissipated heat fluxes up to 256 W/cm^2 with microchannel heat sink of 510 μm diameter with R113 as the working fluid and volumetric flow rates up to 95 ml/min.

Two embedded two-phase cooling microfluidic heat sink testbeds were fabricated and measured to investigate microfluidic cooling for high power density applications and will be reported in Chapter III and IV.

Table 2: Selected microfluidic heatsink designs

Reference	Structure/Type/coolant	Dimensions (μm)	Experiment results
 Tuckman, et al. [30] 1981	Si microchannel Single-phase Water	W_W = 50; W_{Ch} = 50; H = 302.	R_{total} = 0.09 K/W ΔP = 213.9 kPa ΔT = 71℃ q_{max} = 790 W/cm^2

 Peles, et al. [32] 2005	Staggered Si micropin-fin Single-phase water	D = 100; P = 150; H = 243.	R_{total} = 4 K/W ΔP = 14.7 kPa ΔT = 23℃ q_{max} = 36 W/cm^2
 Brunschwiler, et al. [31] 2009	Si microchannel and in-line micropin-fin Single-phase water	W = 50; D = 50; P = 100; H = 50.	R_{total} = 0.26 Kcm^2/W ΔP = 100 kPa ΔT = 54.7℃ q_{max} = 390 W/cm^2
 Kosar et al. [35] 2008	Staggered hydrofoil Si micropin-fin 2-phase R-123	W = 100; L = 500; P = 150; H = 243.	h_{tp} = 70 kW/m^{2}K ΔT_{tp} = 60℃ q_{max} = 312 W/cm^2
 Qu et al. [33] 2009	Staggered square Si micropin-fin 2-phase water	W = 200; P = 400; H = 670.	h_{tp} = 90 kW/m^{2}K ΔT_{tp} = 40℃ q_{max} = 248.5 W/cm^2

 Reeser et al. [34] 2014	Staggered and in-line square Cu micropin-fin 2-phase water and HFE-7200	W = 153; P = 305; H = 305.	$h_{tp\text{-}water}$ = 35 kW/m^{2}K $h_{tp\text{-}HFE}$ = 16 kW/m^{2}K $\Delta T_{tp\text{-}water}$ = 45℃ $\Delta T_{tp\text{-}HFE}$ = 70℃ $q_{max\text{-}water}$ = 118 W/cm^2 $q_{max\text{-}HFE}$ = 36 W/cm^2

1.2.3 Alterative heterogeneous integration technologies

In addition to the electrical and thermal challenges, 3D and 2.5D integration technologies have other undesired characteristics. For 3D stacking technology, TSVs not only impact signal performance, but also increase assembly complexity and may decrease yield, which will impact manufacturing cost. Keep out zones of TSVs occupy on-die real estate, which may also impact cost. For 2.5D interposer technology, the interposer size is limited by the reticle field, yield and cost [40], which limits its application in large scale systems. TSVs in silicon interposer are usually for high-frequency off-chip signaling, where the lossy TSVs may exacerbate signal integrity. These shortcomings of conventional 3D/2.5D integration technologies motivate us to seek alternative high performance heterogeneous integration solutions without the limitation of TSVs and interposer size.

Table 3 summarizes the comparison of alternative heterogeneous integration technologies with conventional 3D/2.5D integration technologies. Silicon-less interconnect technology (SLIT) was developed by Xilinx in 2014 [41]. A schematic of SLIT and the comparison of SLIT to silicon interposer technology are shown in Fig. 6. SLIT removes the bulk silicon of the interposer and thus eliminates the need of TSVs.

However, the system scale is limited by the size of the interposer. The reliability of the metal and dielectric layers is potentially more vulnerable to warpage without the mechanical support of the bulk silicon.

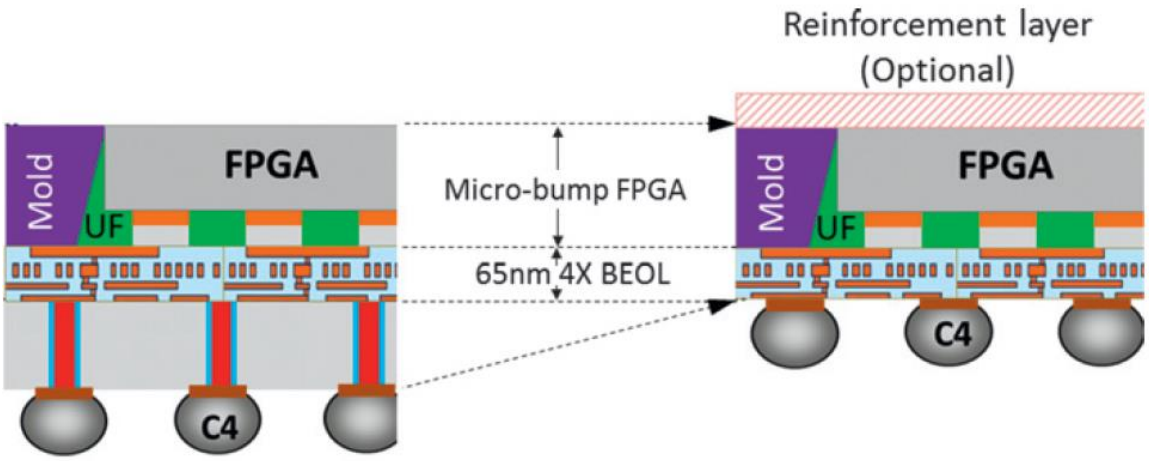


Fig. 6 Schematic of SLIT (right) and comparison to silicon interposer technology [41].

Embedded multi-die interconnect bridge (EMIB) technology developed by Intel eliminates the use of TSVs by embedding a bridge chip in organic substrate and connecting the active dice with fine-pitch wires on the bridge chip [40], [42]. A schematic and a scanning-electron-microscope (SEM) image of the EMIB technology are shown in Fig. 7. A package build-up layer can be found between the active die and the bridge chip. This layer of organic material may potentially limit the I/O density and increase parasitics. Embedding silicon bridge chip into organic substrate may bring reliability concerns due to the coefficient of temperature expansion (CTE) mismatch between the two materials. In addition, it is unclear whether the EMIB technology can apply to package materials besides organic.

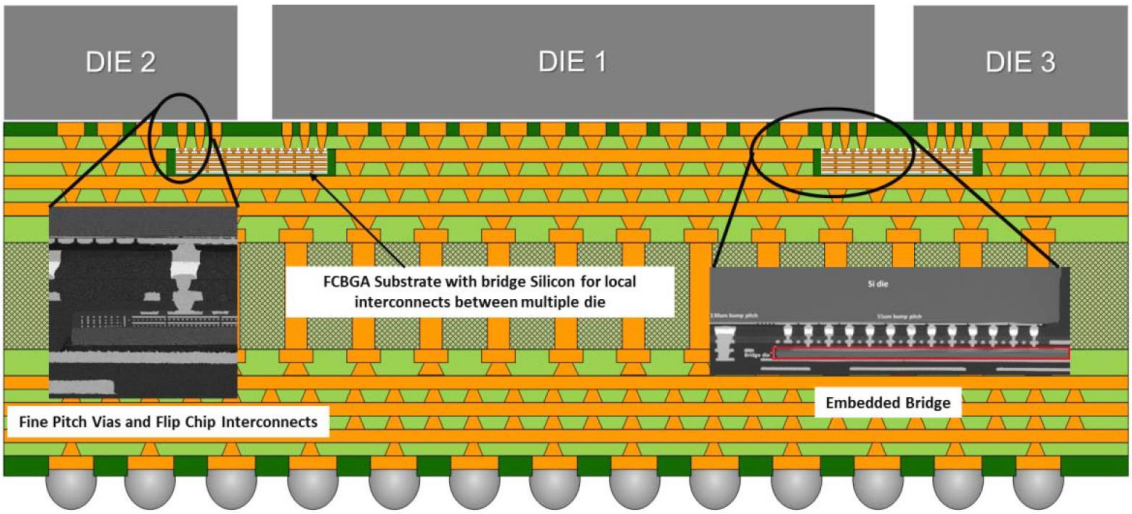


Fig. 7 Schematic and SEM image of the EMIB technology [40].

Table 3: Comparison of dense fine pitch interconnect solutions

	Alternative Technologies			Conventional Technologies	
	HIST (This work)	EMIB [40]	SLIT [41]	Silicon Interposer [10]	Chip Stacking [43][44]
Dense I/O pitch	< 20 µm	~50 µm	45 µm	30 - 60 µm	> 7.6 µm
Footprint	Scalable	Scalable	Limited	Limited	Scalable (vertical)
Interface	Si-Si Face-to-face	Si-Organic-Si	Si-Si	Si-Si	Si-Si
Require TSV	No	No	No	Yes	Yes
Agnostic to substrate	Yes	No	-	-	-

To preserve all the benefits and avoid shortcomings of the aforementioned technologies including 3D stacking, 2.5D interposer and EMIB, a heterogeneous interconnect stitching technology (HIST) platform is presented to enable the interconnection of multiple dice (or “chiplets”) of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and

packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost [29]. Figure 8 illustrates the schematic of the HIST platform. In the HIST platform, a stitch IC with fine pitch interconnects and passive components is "sandwiched" between the active chips and the substrate. Fine pitch interconnects are used to provide high density channels between the active chips while coarse pitch interconnects are used to interconnect the active chips to the substrate. Note that the coarse pitch interconnects also transverse the thickness of the stitch IC. HIST is based on die-to-die face-to-face bonding, and thus there are no intermediate package levels as in the case for EMIB (i.e., package buildup layers as the embedded silicon chips are buried within the package), which enables higher signal I/O pitch and lower capacitance; and lastly, HIST can be applied to any packaging substrate (organic, ceramic, etc) since HIST is augmented to the top-most surface of the package substrate. Two HIST testbeds were fabricated and measured and will be reported in Chapter V. The high frequency performance of the HIST platform as well as the RF performance of the CMIs were characterized and will be reported in Chapter VI.

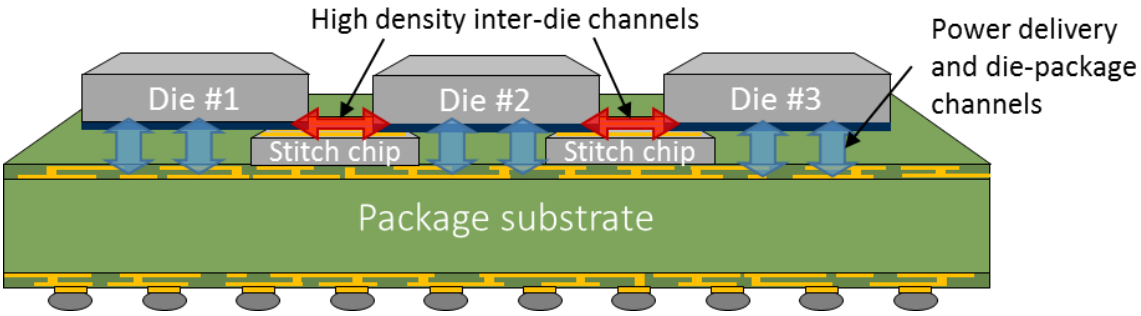


Fig. 8 Schematic of the HIST technology.

1.3 Organization of This Thesis

In this thesis, testbeds were designed, fabricated and measured to overcome the aforementioned challenges in heterogeneous integrations. The contributions of this work include:

1. Development of a compact physical model of TSV capacitance and a circuit level model of the signal delay for 3D IC links considering frequency dependency. The models are verified with experimental measurements for different TSV and wire configurations. A testbed including TSV capacitance structures and 3D IC links was fabricated. The impact of TSV on electrical performance of 3D IC, including insertion loss, signal delay and eye-diagrams were experimentally analyzed. L-2L de-embedding technology was used to investigate the interaction of on-chip wires and TSVs. The results demonstrate that placing TSVs closer to their drivers can effectively improve the performance of 3D IC links.

2. Fabrication and characterization of background cooling testbeds with embedded micropin-fin heat sinks. Two micropin-fin arrays are designed on a 1 cm X 1cm heated area, each with a nominal pin height of 200 μm and pin diameters of 90 μm and 30 μm. Boiling of de-ionized water (D.I. water) in large micropin-fin arrays at sub-atmospheric pressures was investigated for the first time. The maximum heat transfer coefficient reached up to 60 kW/m^2K with mass flow rate of 0.001 kg/s and heat flux ranged from 30 W/cm^2 to 470 W/cm^2.

3. Fabrication and characterization of hotspot cooler testbed for convective boiling experiments in extreme-micro-gap with integrated micropin-fins and heat loss minimization. The 300 μm long, 200 μm wide, 10 μm tall microgap with 4 μm diameter micropin-fins are fabricated in silicon with a 200 μm X 200 μm Pt heater. A 40 μm wide,

180 μm deep air gap around the heater and a SiO2 passivation layer are used to provide thermal isolation. The device is tested with two phase (boiling) micro-fluidic cooling using R134a refrigerant as the coolant with a heat flux of up to 4.75 kW/cm^2 and flow rate range of 0.1 – 0.8 ml/min. A reduction in thermal resistance of 3.5% was observed with the surface area enhancement of the micropin-fins with a tradeoff of a large increase in pumping power.

4. A HIST platform was proposed to acheive heterogeneous multi-die and TSV-less packaging as well as providing a highly-scalable package solution that extends beyond the reticle limits of traditional silicon interposer solutions. Fine-pitch (10 μm) Cu-Au microbumps and fine-pitch (20 μm) compressible microinterconnects (CMIs) were used to provide high density interconnects between chips. In this activity, two HIST testbeds were fabricated and characterized. The average post-assembly resistance values of the fine-pitch micro-bumps and CMIs were measured to be 0.117 mΩ and 145.38 mΩ, respectively. Vertical elastic deformation of up to 13 μm and 30 μm were characterized for fine-pitch and coarse-pitch CMIs, respectively. A circuit model was built to investigate the performance of HIST channels. The bandwidth density of the HIST platform can reach up to 9.3 Tbps/cm at a power efficiency of 0.24 pJ/bit.

5. The high frequency performance of the HIST platform was characterized. CMIs are one of the key components in the HIST platform. The high-frequency characteristics of CMIs can impact the performance of the HIST platform. A testbed including CMIs and low-loss conductive back co-planar waveguide (CBCPW) was fabricated and measured. The insertion loss of the HIST channel were found to be 0.85 dB at 50 GHz. The RLGC values of the CMIs were extracted from the measured S-parameters.

CHAPTER II

IMPACT OF ON-CHIP INTERCONNECT ON THE PERFORMANCE OF 3D ICS WITH TSVS

2.1 Introduction

The demand for dense, low-energy and high-bandwidth interconnects continues to grow in both high-performance and mobile applications [45], [46]. Through-silicon via (TSV) based three-dimensional integrated circuits (3D ICs) have become a promising solution for high-bandwidth and high-density heterogeneous systems [47] - [49]. One of the advantages of TSV-based 3D ICs is the ability to realize high-density short vertical interconnects [50], which lead to high bandwidth density and low energy-per-bit signaling.

Even though it is appealing, the integration of TSVs introduces new challenges. Prior research has focused on the fabrication technology [51], [52], mechanical [53], thermal [54], [55] and electrical attributes of 3D ICs. The electrical properties of TSVs are of particular interest. Experimental analysis of 3D IC links, including wires and TSVs, has been reported [15], [56], but the interconnects were designed for interposer applications; and therefore, contained much larger dimensions than those suited for on-chip applications. Other experimental efforts addressed the I/O circuitry rather than the interconnects [57]. Thus, there is a need to further experimentally explore how TSVs and on-chip wires impact the overall performance of 3D IC links.

In this chapter, TSV arrays and 3D IC links with TSVs and horizontal wires (representing on-chip wires) are fabricated, measured, and analyzed. The models are compared with simulations and measurements. In Section 2.2, the delay model for 3D IC electrical links

is introduced along with an analytical model for TSV capacitance. Section 2.3 summarizes the experimental design and the fabrication process. Section 2.4 is divided into two parts: the first part compares the TSV capacitance model to the measurements; the second part reports 3D IC link analysis including eye-diagrams and link delay. The link delay model is verified for various wire lengths. Moreover, the impact of TSV diameter scaling is analyzed using the experimentally verified models. Finally, conclusions are presented in Section 2.5.

2.2 Analytical Models for 3D IC Links and TSV Capacitance

A simple 3D link consisting of input/output (I/O) drivers and receivers, on-chip interconnects and TSVs is shown in Fig. 9. The equivalent circuit model for the 3D link is shown in Fig. 10.

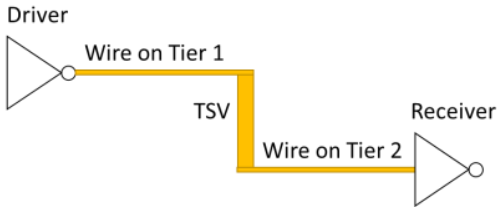
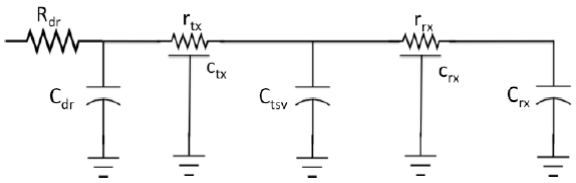


Fig. 9. Schematic of a simple 3D IC link.



(a) (b)

Fig. 10. An equivalent circuit model of a 3D IC link.

The 50%-50% delay of the link can be calculated using the Elmore delay model [58]:

$$\tau_{50\%-50\%} = 0.69(R_{dr} + r_{tx}L_{tx})C_{tsv}$$

$$+0.69R_{dr}(c_{tx}L_{tx} + c_{rx}L_{rx} + C_{rx} + C_{dr})$$
$$+0.69r_{tx}c_{rx}L_{tx}L_{rx}$$
$$+0.38(r_{tx}c_{tx}L_{tx}^2 + r_{rx}c_{rx}L_{rx}^2) \quad (1)$$

where R_{dr} and C_{dr} are the driver resistance and capacitance, respectively, r_{tx}, c_{tx}, and L_{tx} are the resistance per unit length, the capacitance per unit length, and the length of the on-chip wire on the driver side (Tier 1 in Fig. 9), respectively, and r_{rx}, c_{rx} and L_{rx} are the same for the on-chip wire on the receiver side (Tier 2 in Fig. 9). C_{tsv} is the capacitance of the TSV, and C_{rx} is the load capacitance of the receiver.

The first term in (1), i. e., the delay due to the driver side resistance combined with the TSV capacitance, dominates the total delay. Therefore, it is very important to understand and accurately model the TSV capacitance. A circuit model for two TSVs in a TSV array is shown in Fig. 11 (a). This model is simplified for low- and high- frequency cases. Due to the metal-insulator-semiconductor (MIS) structure, TSVs may operate at either slow wave mode or quasi-TEM mode depending on the frequency, TSV dimensions, and substrate resistivity [19]. When the operating frequency is lower than 0.3 times the characteristic frequency of the slow-wave mode (0.3 fsw) [18], which is typically in the KHz and MHz range, the TSV is in the slow wave mode. In this mode, TSV capacitance is mainly determined by its oxide capacitance, which we define as the low-frequency capacitance. As frequency increases, there is a transition from the slow wave mode to the quasi-TEM mode, allowing complete penetration of the E-field and H-field through the silicon substrate [18], [59]. In this mode, the TSV capacitance is saturated by the silicon substrate capacitance, C_C in Fig. 11 (c). In our simulation, the quasi-TEM mode is observed at frequencies higher than ~10 GHz (depending on TSV dimensions). In this mode, the

overall TSV capacitance is constant and equal to C_C. In this paper, we assume that the substrate is floating and is not biased during the measurement.

The admittance of the substrate between two TSVs can be calculated as [18]

$$Y = G_C + j2\pi f C_c \tag{2}$$

where G_C is the substrate conductance and f is the frequency of operation. At low frequencies, G_C dominates the admittance. Therefore, the substrate capacitance is shorted out, reducing the model to the one shown in Fig. 11 (b). As a result, the TSV capacitance to the substrate is approximately the TSV liner capacitance. Depending on the number of ground TSVs surrounding the signal TSV, including the pad capacitances, the effective low-frequency capacitance is given by

$$C_{LF} = \frac{1}{\left(\frac{1}{N_{GND}C_{OX}+C_{GPAD}}\right)+\left(\frac{1}{C_{OX}+C_{SPAD}}\right)} \tag{3}$$

where C_{OX} is the TSV liner capacitance, C_{GPAD} is the capacitance from the ground pad to the substrate, C_{SPAD} is the capacitance from the signal pad to the substrate, and N_{GND} is the number of ground TSVs surrounding the signal TSV.

At high frequencies, the capacitive admittance is much larger relative to the conductance of the substrate. As a result, the conductance of the substrate is ignored, as shown in Fig. 11 (c). The substrate capacitance (C_c) for each of the TSV array configurations is estimated using *Synopsys Raphael*. The effective high-frequency capacitance as a function of the TSV array configurations is given by

$$C_{HF} = \frac{1}{\left(1+\frac{1}{N_{GND}}\right)\left(\frac{1}{C_{OX}}\right)+\frac{1}{C_c}} + C_{SGPAD} \tag{4}$$

where C_{HF} is the high-frequency capacitance, and C_{SGPAD} is the capacitance from the signal to ground pads.

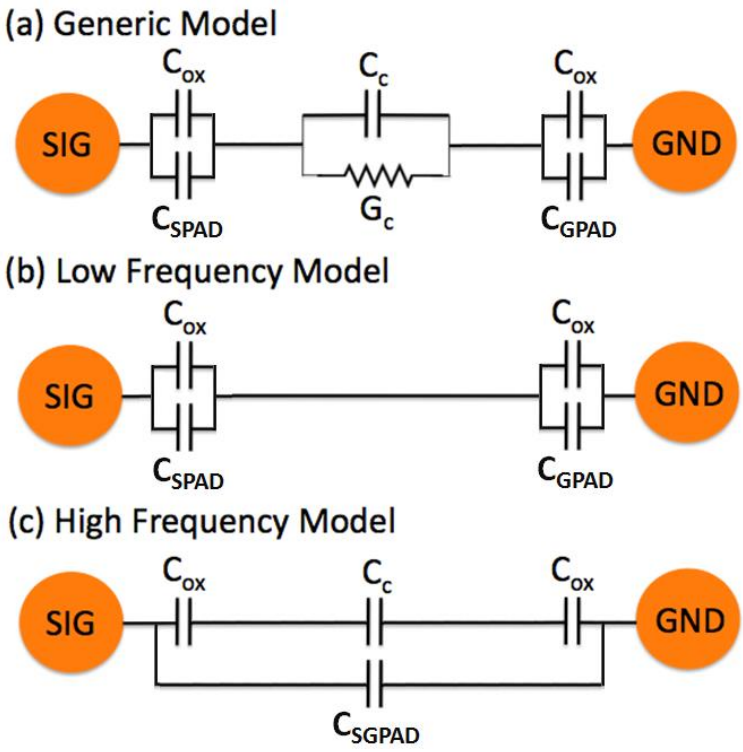
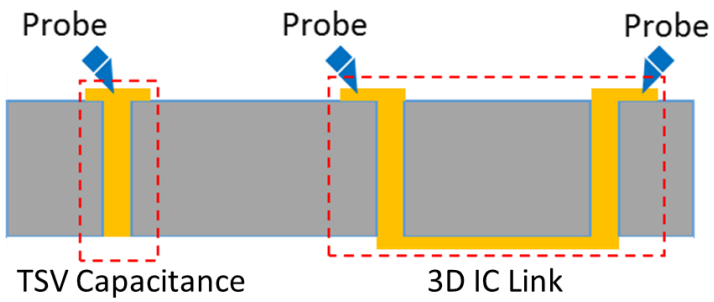


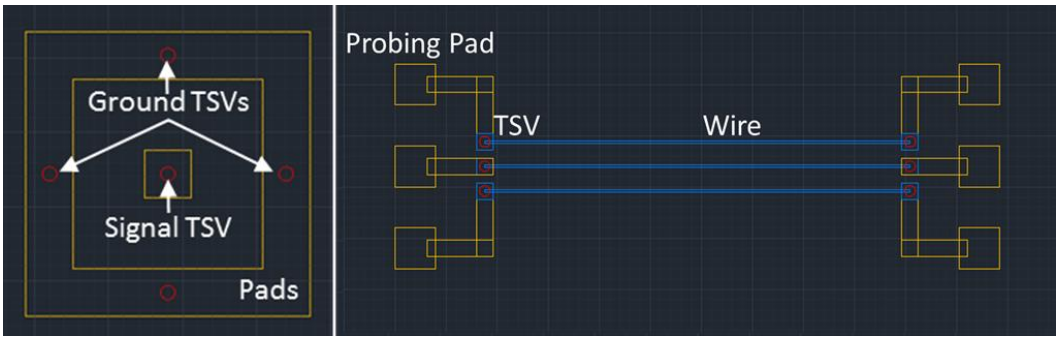
Fig. 11. TSV capacitance circuit models showing the capacitance between signal and ground TSVs at (a) any frequency (b) low-frequency (c) high-frequency.

2.3 Experiment Design and Fabrication

Two design sets for the experimental evaluation of TSVs and on-chip wires are illustrated in Fig. 12. For TSV capacitance extraction, single-port measurements are used, while for TSV-wire-TSV 3D IC links, two-port measurements are used. The dimensions of all interconnect structures are summarized in Table 4.



(a)



(b) (c)

Fig. 12 The experimental design for TSV capacitance and TSV-wire-TSV 3D IC link measurements: (a) Design overview of TSV capacitance and 3D IC link measurements, (b) TSV capacitance design: one signal TSV with different number of ground TSVs for TSV capacitance extraction, and (c) 3D IC link design: the link with probing pads, TSVs, and wires on the back side.

Table 4: Dimensions of structures of the 3D IC link testbed

Structure	Dimensions
TSV	Diameter = 14 μm, Pitch = 30 μm (3D IC link), 50 μm, 100 μm (TSV capacitance), Height = 300 μm, Liner thickness = 0.4 μm
Wire	Length = 0.5 mm, 1 mm, 2 mm, 4 mm, 8 mm
	Width = 3 μm, Pitch = 30 μm, Thickness = 0.1 μm
Probing pads	Width = 40 μm, Pitch = 100 μm, Thickness = 0.6 μm

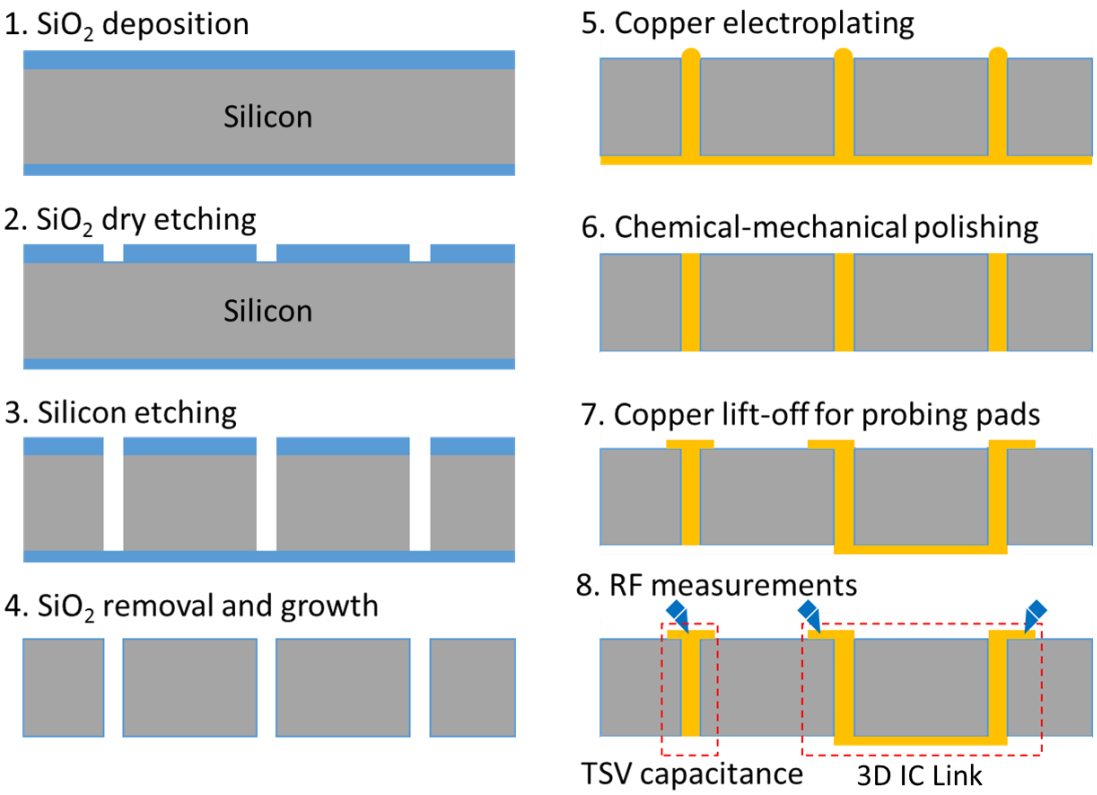


Fig. 13. Overall fabrication process for TSV capacitance and 3D IC link characterization.

The fabrication process begins with a 300 μm thick double-side polished silicon wafer. Silicon dioxide is deposited on the top side of the wafer using plasma-enhanced chemical vapor deposition (PECVD) and patterned using dry etching. The silicon vias are then etched using the Bosch process with silicon dioxide as the mask. Following the Bosch process, the wafer is immersed in buffered oxide etchant (BOE) to remove the silicon dioxide. Next, a liner of silicon dioxide is thermally grown. A seed layer of titanium and copper is then deposited on the back side using electron beam evaporation, followed by a bottom-up copper electroplating. The over-electroplated copper is removed by chemical-mechanical polishing to expose the TSVs. Finally, probe pads and wires are patterned using a lift-off process on the front and back sides of the wafer, respectively. The fabrication

process is summarized in Fig. 13.

Six designs are fabricated to extract the capacitance of TSVs, as shown in Fig. 14. Each design contains one signal TSV in the center surrounded by various number of ground TSVs with a shorted probe pad. The number of ground TSVs in the second through sixth designs is 2, 4, 4, 6, and 8, respectively.

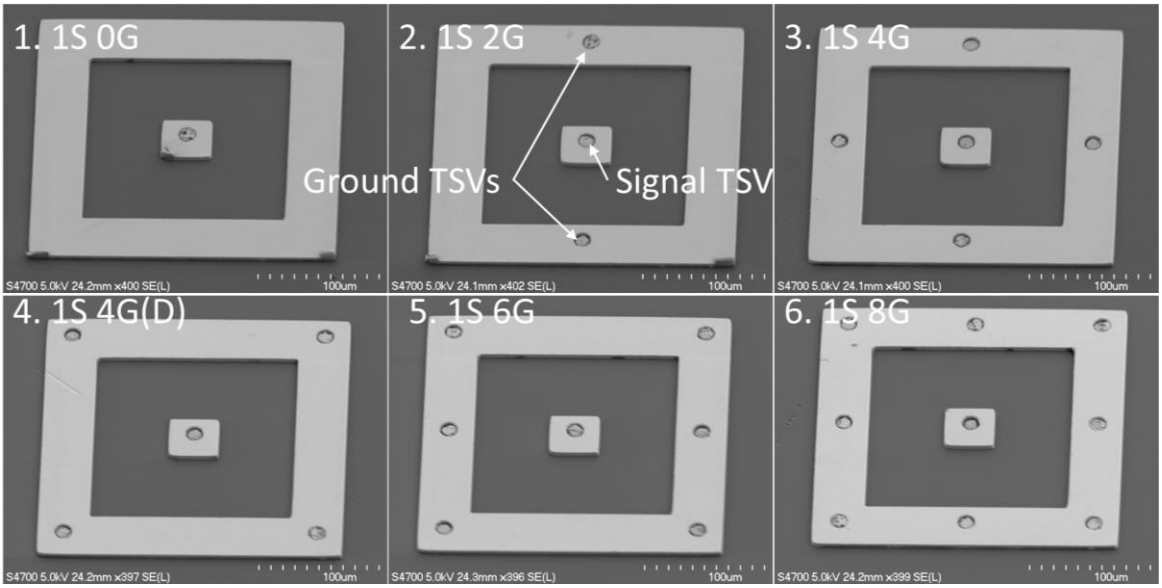
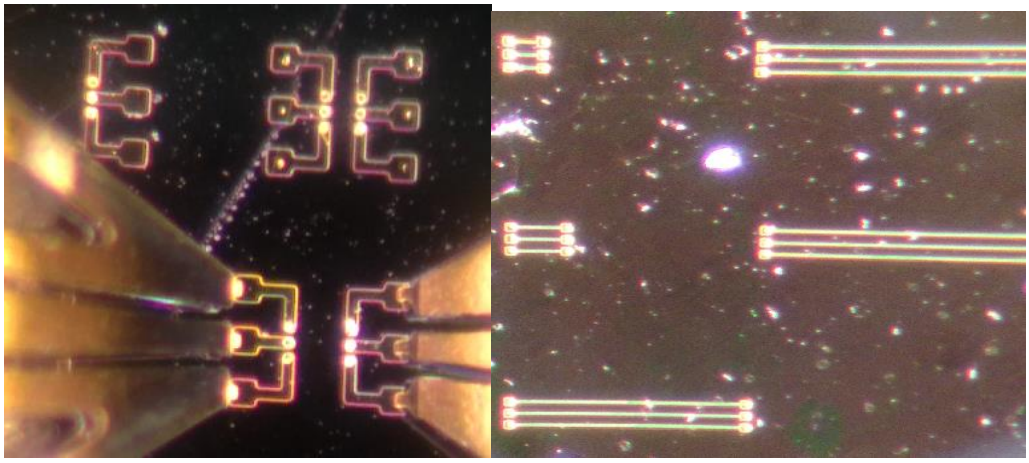


Fig. 14. SEM images of six TSV sets with various number of ground TSVs ranging from 0 to 8 (1S 0G indicates 1 signal TSV and 0 ground TSV).

For 3D IC links, coplanar waveguide (CPW) configured ground-signal-ground (GSG) wires are used to emulate on-chip wires. The dimensions of the structures were selected to emulate the electrical parameters of a 3D IC link based on the ITRS 2013 report [60]. The overall wire thickness is 100 nm, including 30 nm thick titanium, 50 nm thick copper, and 20 nm thick gold. Optical images of the fabricated testbed are shown in Fig. 15.



(a) (b)

Fig. 15. Images of the tested samples: (a) the front side, and (b) the back side.

2.4 Characterization of TSV capacitance and 3D IC Link

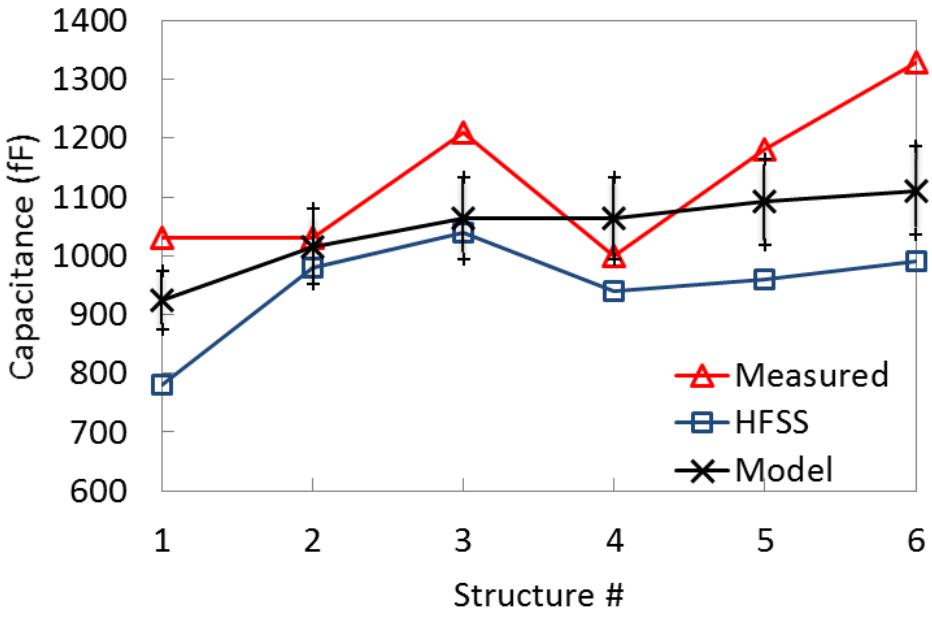
The fabricated testbed is measured using an Agilent N5245A network analyzer to obtain the S-parameters from 10 MHz to 50 GHz at a 250 MHz step. Single port S11 parameters are measured for TSV capacitance extraction. For 3D IC link measurements, 2-port S-parameters are measured. The probe pads are de-embedded using L-2L de-embedding [61]. Finally, the S-parameters are imported into Keysight Advanced Design System (ADS) to extract the time-domain response of the links.

2.4.1 TSV Capacitance

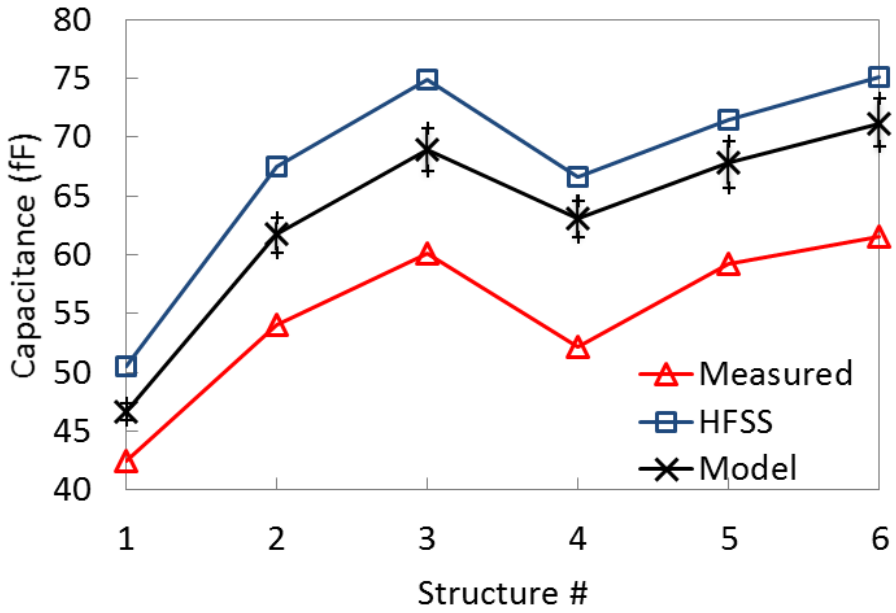
For each of the TSV array configurations described in the previous section, the experimentally obtained values of capacitance are compared to those extracted through HFSS and analytical/extracted models. Error bars are added to the modeled capacitance to reflect TSV diameter variation of ±1 μm due to fabrication process variation.

The effective capacitance obtained through this model is compared to experimental results. The error in the low-frequency model is <17%, as shown in Fig. 16 (a). At a TSV pitch of

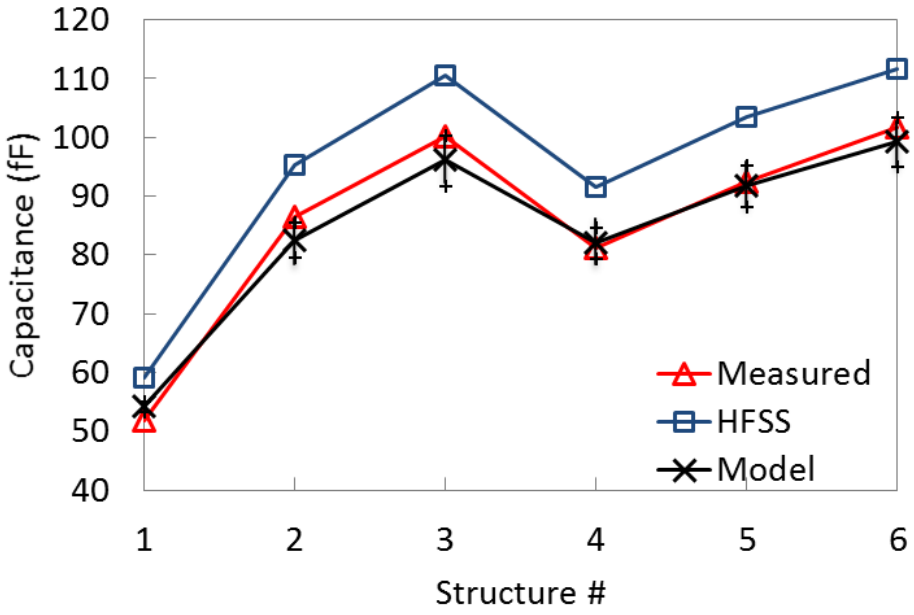
100 μm and at high-frequency, although the maximum error is approximately 21% for structure 4, the trend of capacitance values is well matched between the model, simulation, and measurements, as shown in Fig. 16 (b). For a TSV pitch of 50 μm, the model has an error of <5%, as shown in Fig. 16 (c). It is worth noting that for all 6 structures, the 50 μm pitch TSVs have larger high-frequency capacitance than the 100 μm pitch TSVs due to the larger impact of substrate capacitance at high frequencies, which is consistent with the result in [56].



(a)



(b)



(c)

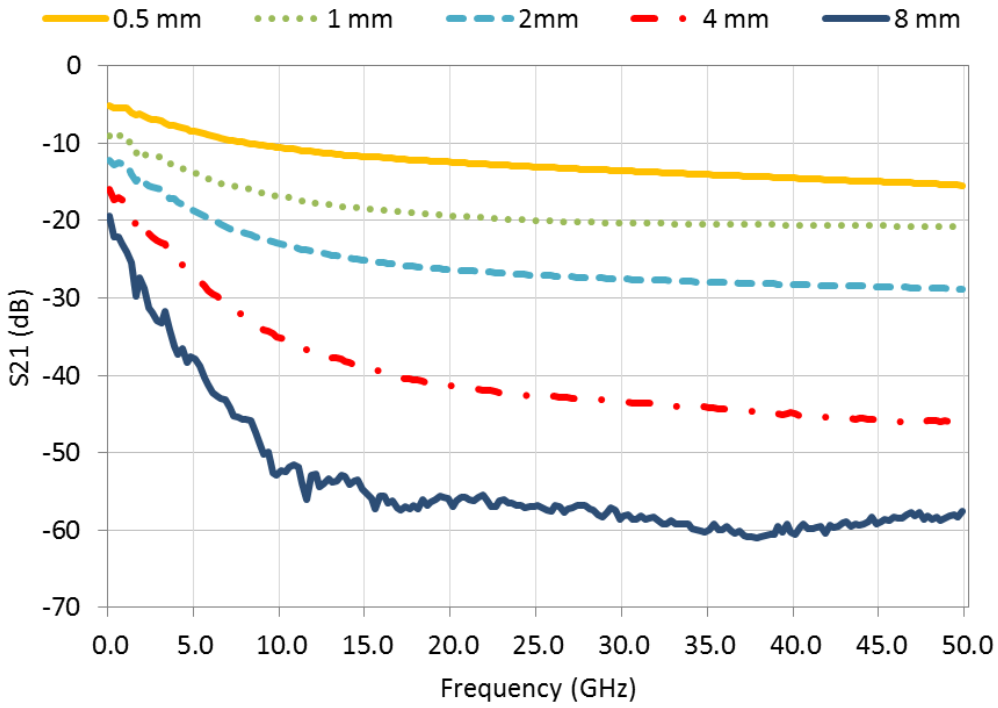
Fig. 16. Low-frequency capacitance (a) and High-frequency capacitance (pitch =100 μm (b) and picth = 50 μm (c)) of different TSV array configurations.

2.4.2 3D IC Links

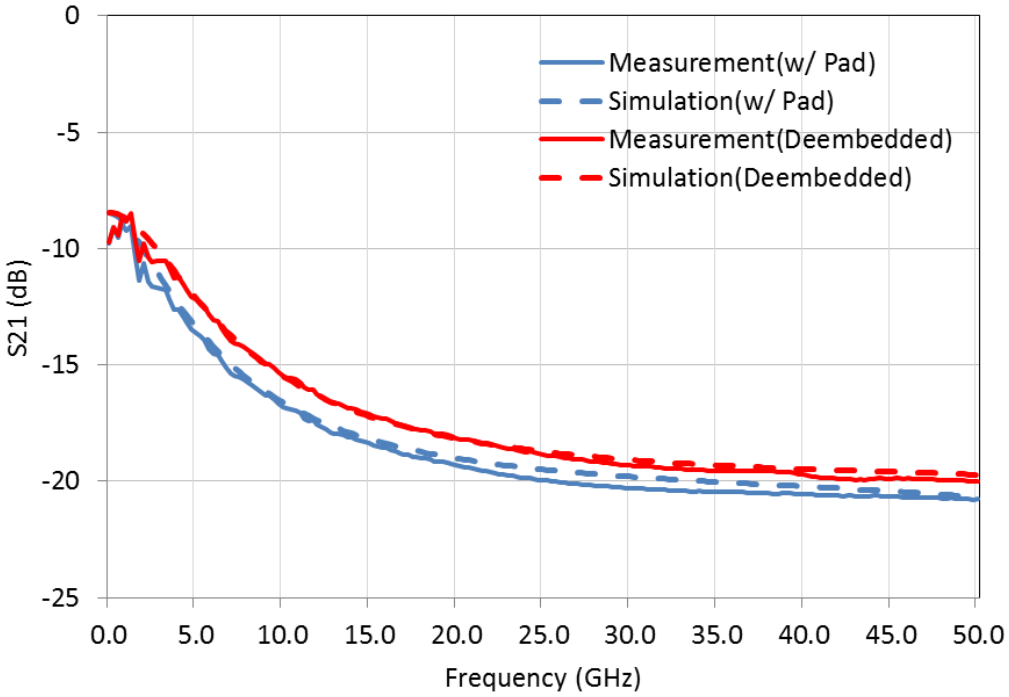
Five sets of links with different wire lengths are measured, and the results are shown in Fig. 17 (a). The loss increases with frequency and wire length as expected. It is evident that the loss of these links is large even at low frequency. The insertion loss of the 1 mm long link at 10 MHz is as high as -9.75 dB. This is due to the high DC resistance of the wires. It should also be noted that the measurement of the 8 mm long wire exhibits some noise, which is believed to be due to the small values of S_{21}.

The L-2L de-embedding method is adopted to eliminate the probe pads [61]. Figure 17 (b) shows the originally measured S_{21}, the de-embedded S_{21}, and the values obtained via HFSS simulations of a 3D IC link. The HFSS simulations correlate well with the measurements, with an average difference of 1.25%.

After de-embedding the probe pads, the effective link consists of two TSVs interconnected with a wire, i.e. a TSV-wire-TSV link. Next, the TSVs are de-embedded to obtain the S-parameters of only the wire (TSVs on both sides are de-embedded), the wire-TSV link (the TSV on the driver side is de-embedded) and the TSV-wire link (the TSV on the receiver side is de-embedded).


0.5 mm
1 mm
2mm
4 mm
8 mm
0
-10
-20
-30
-40
-50
-60
-70
S21 (dB)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
50.0
Frequency (GHz)

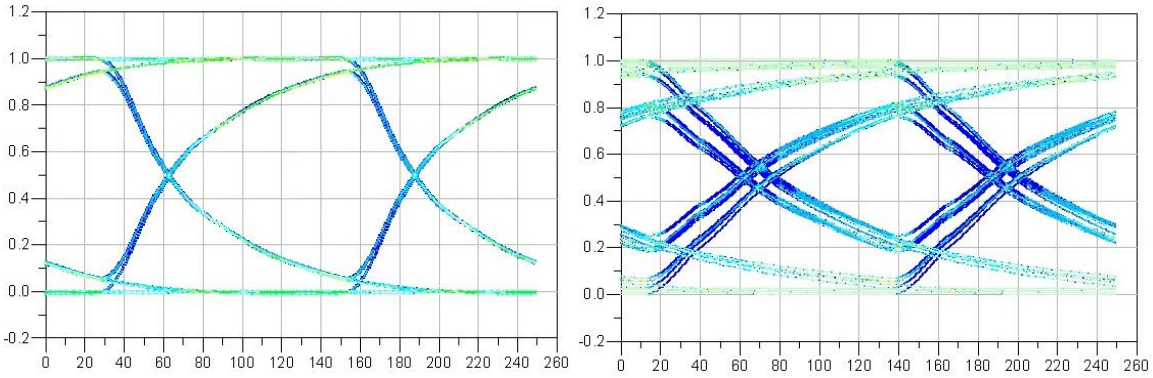
(a)


Measurement(w/ Pad)
Simulation(w/ Pad)
Measurement(Deembedded)
Simulation(Deembedded)
0
-5
-10
-15
-20
-25
S21 (dB)
0.0
5.0
10.0
15.0
20.0
25.0
30.0
35.0
40.0
45.0
50.0
Frequency (GHz)

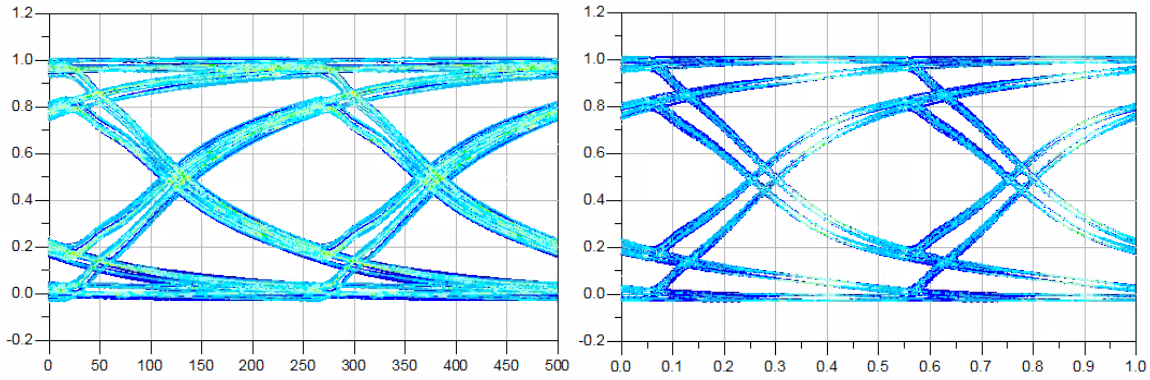
(b)

Fig. 17. (a) Measured S_{21} of TSV-wire-TSV links for five different wire lengths; (b) measured and simulated S21 before and after de-embedding for TSV-wire-TSV links.

The S-parameters are imported into Keysight ADS to extract the eye diagram and delay. The driver resistance and receiver capacitance are from the ITRS 2013 14 nm node [60]. The eye diagrams for wire-TSV links are shown in Fig. 18. At a data rate of 8 Gbps, the eye is closed for links longer than 2 mm. However, they can still achieve an eye-opening of 50% at lower bit rates, as shown Fig. 18 (c) and (d). Figure 19 shows the impact of the TSV by comparing four structures of the same wire length at a date rate of 8 Gbps. Compared to the wire-TSV link shown in Fig. 19 (c), the TSV-wire link in Fig. 19 (b) improves the eye opening from 510 mV to 650 mV. This demonstrates that the performance of the link is improved when the TSV is placed closer to the driver. The reduced eye opening of the wire-TSV link is due to the interaction of the driver side wire resistance and the TSV capacitance. By placing the TSV closer to the driver, the driver side wire resistance becomes smaller and therefore a larger eye opening is achieved.

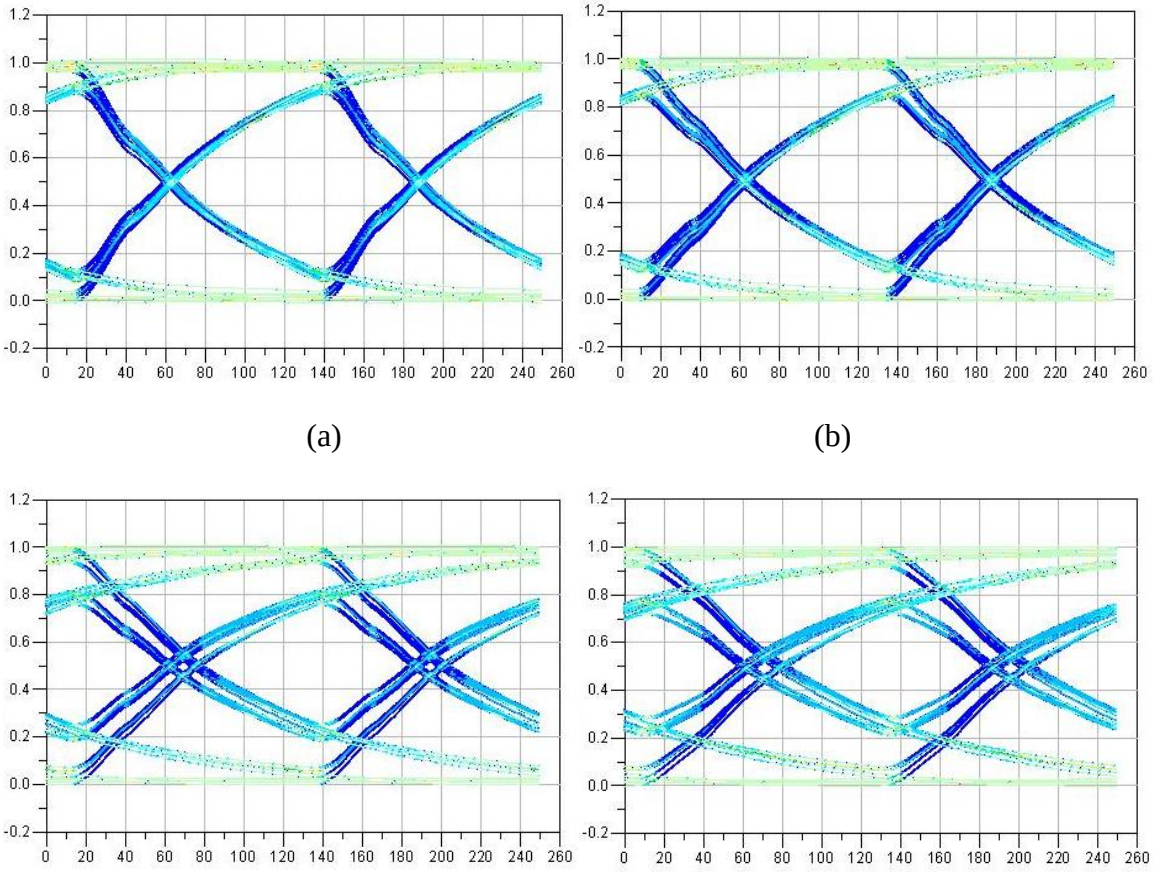


(a) (b)



(c) (d)

Fig. 18. Eye diagrams of four structures with different wire lengths: (a) 0.5 mm at data rate of 8 Gbps, (b) 1 mm at 8 Gbps, (c) 2 mm at 4 Gbps, and (d) 4 mm at 2 Gbps

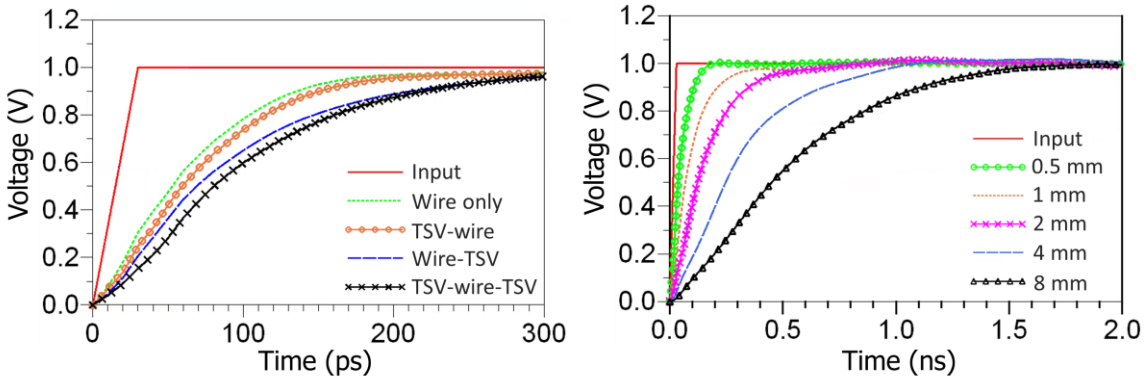


(a) (b)

(c) (d)

Fig. 19. Eye diagrams of the four structures: (a) wire only, (b) TSV-wire, (c) Wire-TSV, and (d) TSV-wire-TSV for 1 mm wire length at data rate of 8 Gbps.

Figure 20 (a) shows the step response of four links with the same wire length. Compared to the wire only 50%-50% delay of 37.6 ps, the delay of the wire-TSV link is 53.9 ps, an increase of 43.4% due to the presence of the TSV. Moving the TSV to the driver side (e.g. TSV-wire link) decreases the delay to 44.5 ps, an improvement of 17.4% and an increase of 18.4% compared to the wire only case. Figure 20 (b) shows the response of the wire-TSV link for five different wire lengths.



(a) (b)

Fig. 20. Step response of: (a) TSV-wire-TSV, wire-TSV, TSV-wire and wire only for 1 mm wire length, (b) five links with different wire length: 0.5 mm, 1 mm, 2 mm, 4 mm, 8 mm.

The delay of the wire-TSV link at five different wire lengths is modeled using the analytical model presented in Section 2.2 and compared to measurements, as shown in Fig. 21. For each wire length, we measured two identical structures and the results are marked as crosses. In the model, the wire resistance, wire capacitance, and TSV capacitance values

are extracted from the measurements. The maximum difference between the modeled and measured delays is approximately 8.5% at a wire length of 8 mm. Even though the wires are longer than typical on-chip wires, the time of flight (TOF) was ignored in the model due to the high resistance of the wires [62].

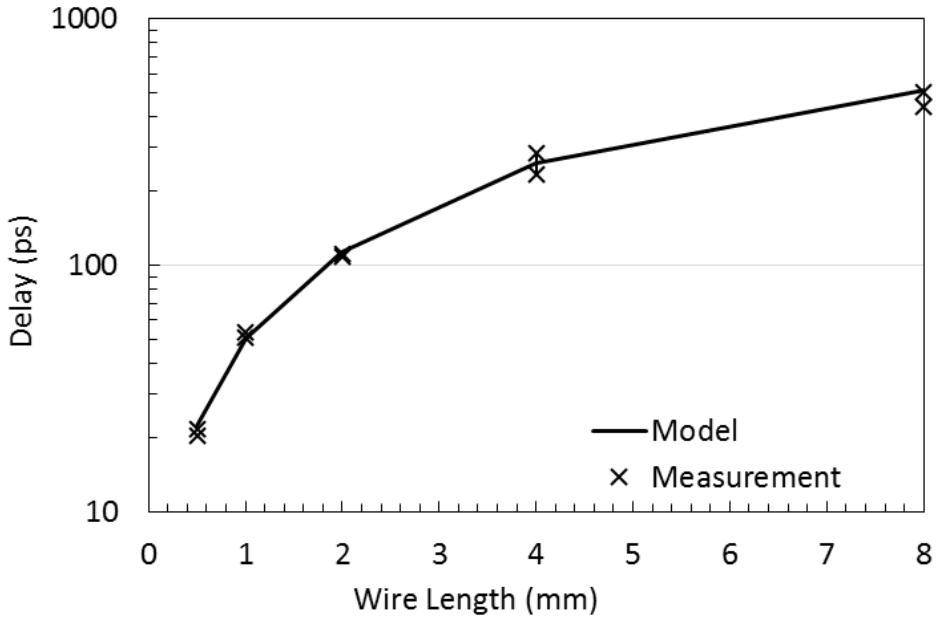


Fig. 21. Modeled and measured delay as a function of wire length.

The impact of TSV geometry scaling on the TSV capacitance and link delay is analyzed with the verified models, as shown in Fig. 22. In this analysis, the TSV aspect ratio is assumed to be 10:1. Moreover, the silicon dioxide liner thickness is assumed to be 1/10 of the TSV diameter, and the M1 wire length is set to 10 μm. The link delay decreases significantly as the TSV diameter decreases. When the TSV diameter scales below 1 μm, the link delay becomes saturated. This is because the TSV capacitance becomes comparable to the on-chip wire capacitance, and the delay begins to be dominated by the on-chip wires.

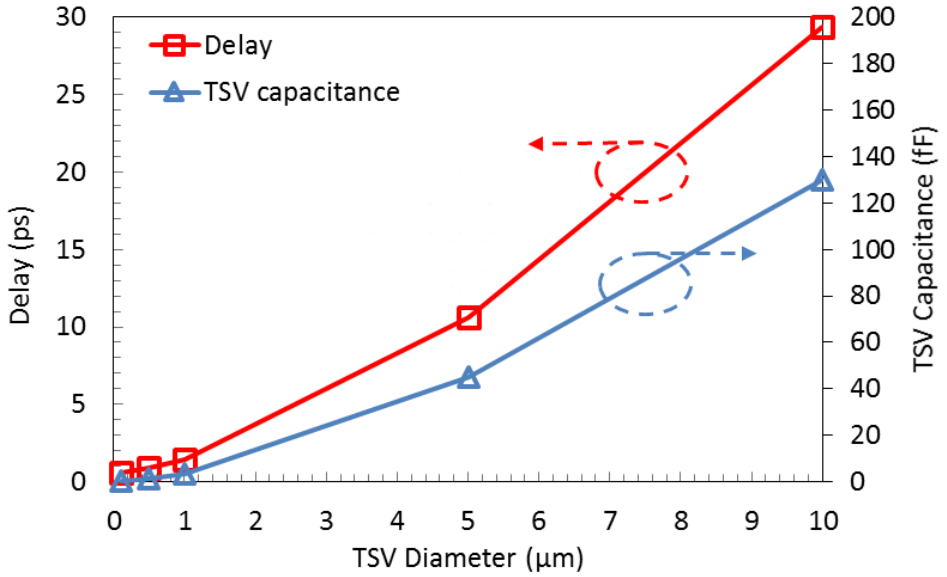


Fig. 22. Impact of TSV geometry scaling on TSV capacitance and link delay.

2.4 Conclusion

In this chapter, TSV arrays and 3D IC links with TSVs and horizontal wires are fabricated, measured, and analyzed. The TSV capacitance and link delay models are verified with measurements. It is shown that the TSV capacitance and the driver side wire resistance can dominate the link performance and could potentially be the key bottleneck for digital 3D ICs. The delay and eye opening of the link can be significantly improved by placing TSVs closer to their drivers. Furthermore, reducing the length of on-chip wires and height and diameter of the TSVs have a significant impact on 3D IC link performance.

CHAPTER III

EMBEDDED MICROFLUIDIC COOLING IN 3D IC I: BACKGROUND COOLING

3.1 Introduction

Today, system performance and power dissipation are both constrained and are partly dictated by on- and off-chip interconnects [63], [64]. Three-dimensional integrated circuits (3D ICs) with through silicon vias (TSVs) shorten the length of interconnects, which improves performance and reduces the energy consumption of high performance systems [5], [65]. However, as increasing integration levels push the power density higher in 3D ICs, cooling becomes a major challenge [66], [67]. The heat dissipation may exceed the capability of conventional air-cooled heat sinks. A switch from air cooling to microfluidic cooling is believed to be a promising solution [68]. Staggered cylindrical micropin-fin heat sinks are of particular interest because of their enhancement of surface area and high convective heat transfer [66]. Fig. 23 shows one possible 3D IC scheme with an embedded micropin-fin heat sink. Stacked dice are cooled by liquid coolant flowing through the micropin-fins. The electrical interconnects are implemented by TSVs embedded in the micropin-fins.

The thermal performance of the heat sink is determined by the geometry of the heat sink, the coolant, the coolant flow rate and its thermophysical properties. There has been significant prior research focused on this area for signal-phase and two-phase cooling, as shown in Chapter I. However, flow boiling of water in micropin-fin arrays at reduced pressures was rarely reported. By operating at reduced pressures, boiling in water can be

initiated at below 100 ^{o}C, which is desired for Si CMOS. In this chapter, two micropin-fin array heat sinks with different micropin-fin densities were fabricated and tested with heat sink outlet pressure below atmospheric pressure. Heat transfer performance of single-phase and two-phase flow in the micropin-fin area of both heat sinks were characterized and compared.

The chapter is organized as follows: Section 3.2 introduces the design and fabrication process of the heat sinks; Section 3.3 summarizes the testing setup and data reduction; Thermal testing results and analysis are shown in Section 3.4; the potential trade-off between thermal and electrical performance in 3D IC with embedded microfluidic cooling is shown in Section 3.5; and finally conclusions are drawn in Section 3.6.

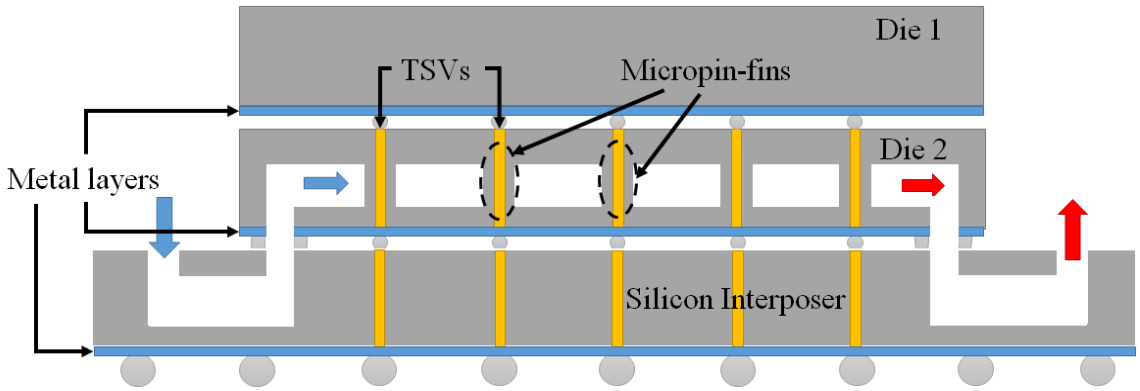


Fig. 23. Schematic of 3D IC with microfluidic cooling.

3.2 Design and Fabrication Process of the Heat Sinks

The heat sink testbed consists of a 1 cm x 1 cm array of staggered micropin-fins, as shown in Fig. 24. In addition to fluid inlet and outlet ports, pressure ports are included on either side of the micropin-fin array in order to accurately measure pressure drop across the micropin-fin array while excluding pressure drop due to rapid flow

constriction/expansion at the inlet and outlet ports. A single line of micropin-fins is also introduced on either side of the micropin-fin array under test in order to promote an even flow distribution. Oval shaped structures were added near the inlet and outlet for mechanical support. Four serpentine platinum heaters/resistance temperature detectors (RTDs) generate heat load and provide temperature measurements in four sections along the flow length (between inlet and outlet). A fabricated sample can be seen in Fig. 24.

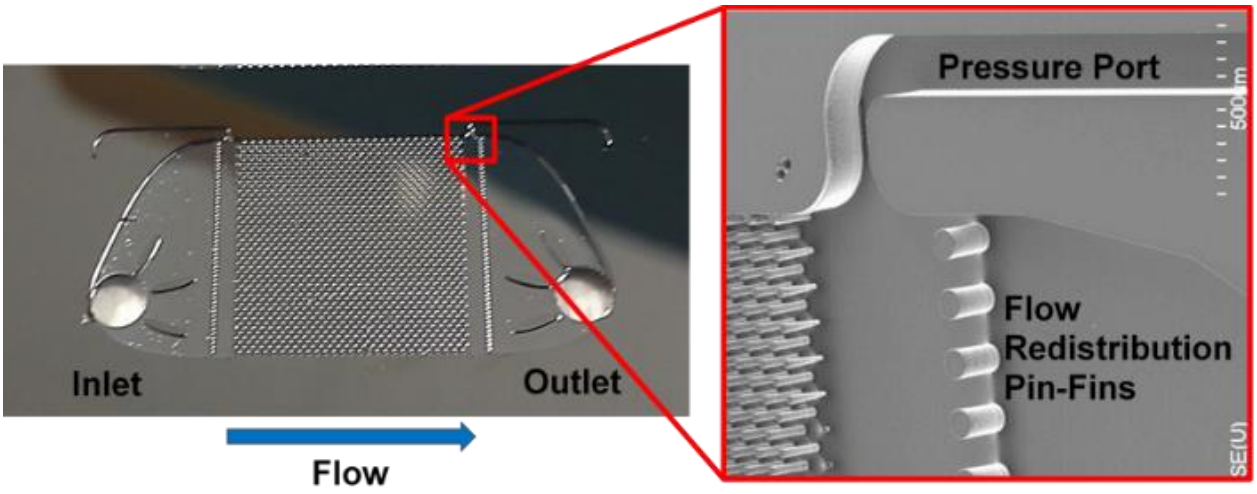


Fig. 24. Optical and SEM image of the heat sink.

The micropin-fin dimensions and arrangement are shown in Fig. 25. The transverse pitch, longitudinal pitch, and diameter are 135 μm, 225 μm and 90 μm for sample 1; and 90 μm, 30 μm and 30 μm for sample 2, respectively. The micropin-fin height is 200 μm for both samples.

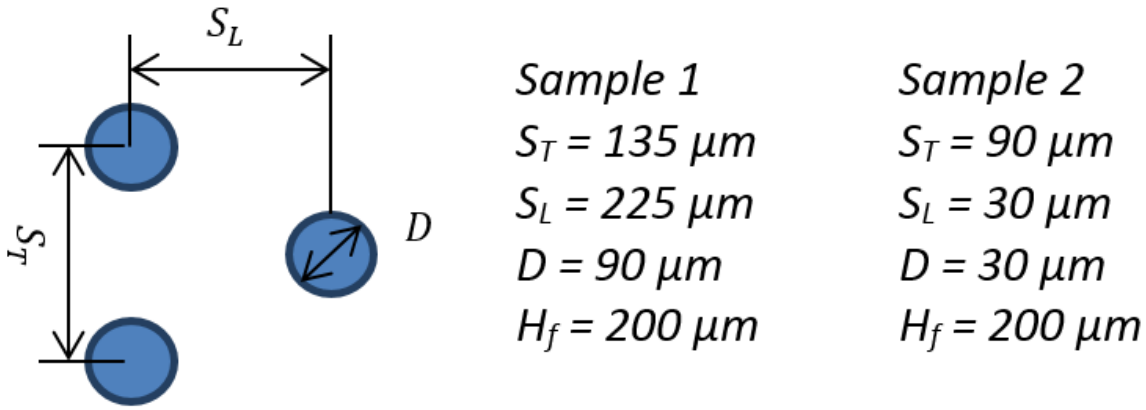


Fig. 25. Pin fin array dimensions.

The process used to fabricate the heat sink testbed is shown in Fig. 26. The process begins with a 500 μm thick double side polished wafer. A standard Bosch process with alternating SF_6 (for etching) and C_4F_8 (for passivation) was used to create the 200 μm (±5 μm) height micropin-fins and manifolds. The pitches and diameters of the micropin-fins can be different from die to die across the wafer. Next, the etched silicon wafer was cleaned with piranha solution (5:1 mixture of 98% sulfuric acid and 30% hydrogen peroxide) at 125 ^{o}C. The cavities formed during etching were then sealed using a pyrex cap with anodic bonding with voltage of 800 V at 350 ^{o}C. The bonded wafer was then flipped and a 2 μm thick insulating silicon dioxide layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). Platinum heaters of 200 nm (± 5 nm) thickness and 500 nm (±10 nm) thick gold pads were then sputtered on the SiO_2 layer. Lastly, inlet, outlet, and pressure measurement ports were etched using Bosch process from the same side of the wafer.

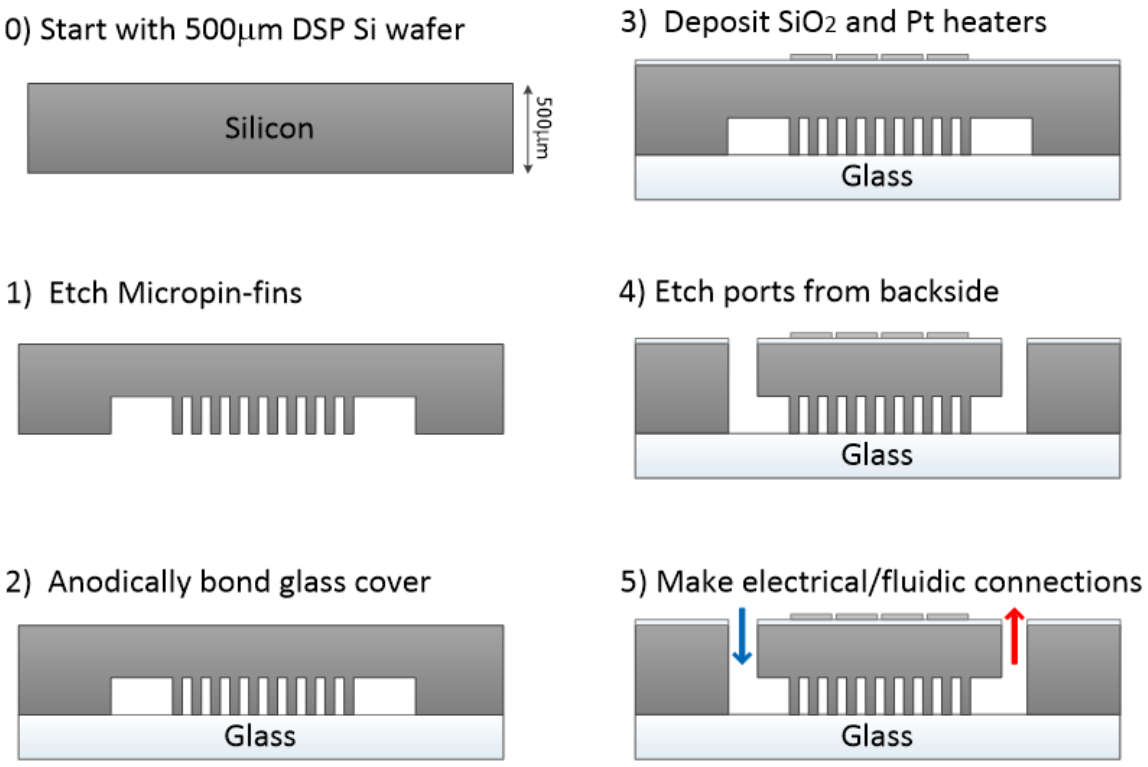


Fig. 26. Fabrication process of the heat sink sample.

3.3 Testing Setup and Data Reduction

The test flow loop consists of a gear pump, filter, flow meter, preheater, test section, heat exchanger and fluid reservoir. The filter has a pore size of 7 µm and is used to remove contamination that may be present inside the flow loop system. The flow meter is used to measure the volumetric flow rate of the fluid, and it has a range of 50 ~ 500 mL/min. Heated fluid is condensed in the heat exchanger, which is cooled by a thermostatic bath circulator. The stainless steel fluid reservoir can hold up to 300 mL of fluid. Fluid pressure is measured at four locations, while temperature is measure at five locations. Measurement locations within the experimental facility are marked in Fig. 27.

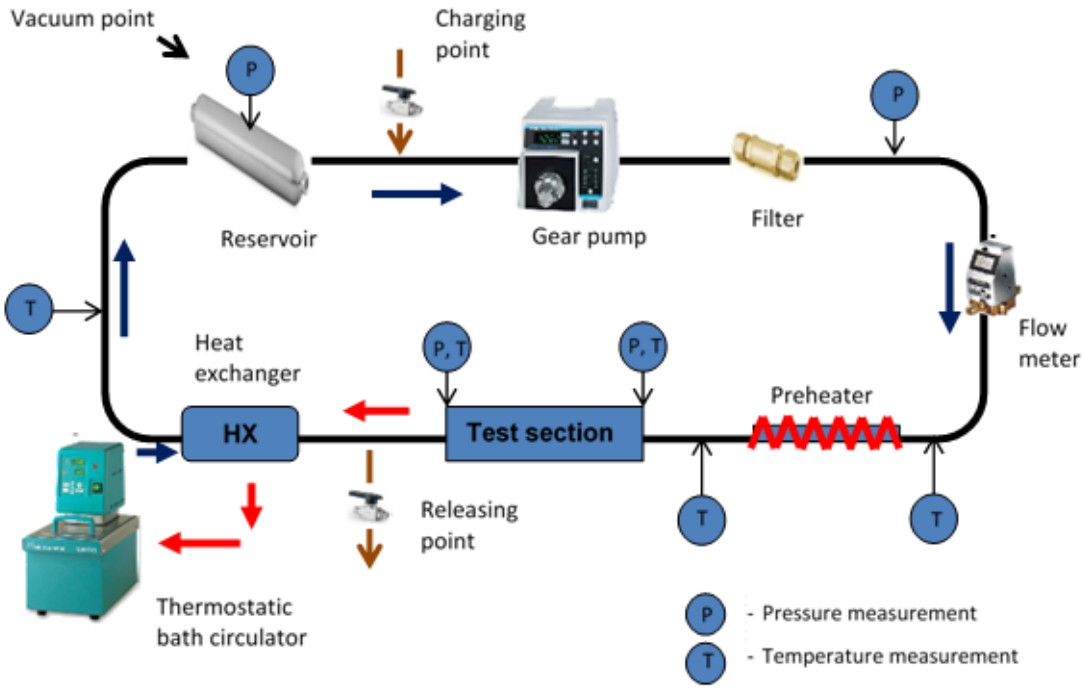


Fig. 27. Testing flow loop schematic.

Before testing, the heaters were calibrated in an oven to obtain the resistance-temperature curve for each heater from 20 to 145 °C. Heater resistance varies with temperature linearly. The calibrated device was packaged and then connected to the closed flow loop. The system was evacuated and charged with D.I. water. The D.I. water was boiled for 30 minutes to remove any dissolved gas before charging the flow system. The testing parameters are summarized in Table 5 and the measurement uncertainty is shown in Table 6.

Table 5: Testing parameters

Parameter	Sample 1	Sample 2
Mass flow rate	1.07-1.09 g/s	0.97-1.06 g/s
Inlet temperature	5-8 ^{o}C	12-18 ^{o}C

Table 6: Uncertainty during testing

Flow rate	± 0.8 mL/min
Pressure drop	± 3 kPa
Fluid temperature	± 0.5 ^{o}C
Wall temperature	± 1.4 ^{o}C
Hear transfer coefficients	± 0.5 kW/m^{2}K
Heat flux	± 0.1 W/cm^2

During testing, both single-phase and two-phase experiments were performed. To estimate heat loss, the power required to increase the water temperature from the inlet to the outlet was calculated and subtracted from the total power supplied to the heaters for single phase experiments, as shown in the following equation:

$$Q_{loss} = P_{total} - \dot{m}C_p(T_{out} - T_{in}) \quad (5)$$

where $\dot{m}$ is the mass flow rate of water. The total power was calculated from the measured voltage and current of the heaters. The estimated heat loss percentage was about 11% for both devices at the highest heat flux for single-phase measurements, and this was applied to two-phase data to obtain effective heat flux.

Mass flux, G, is defined as

$$G = \frac{\dot{m}}{A_{c,min}} \quad (6)$$

where $A_{c,min}$ is the minimum cross-sectional area of the heat sink cavity. Thus

$$A_{c,min} = \left(W_{ch} - \frac{W_{ch}}{S_T} D\right) H_f \quad (7)$$

W_{ch} and H_f are the heat sink cavity width and micropin-fin height, respectively. The effective heat flux is calculated as

$$q_{eff}" = \frac{P_{total} - Q_{loss}}{A_h} \quad (8)$$

where A_h is the total heated area.

The effective heat flux for single-phase can also be calculated as:

$$q_{eff}" = \dot{m}C_p(T_{out} - T_{in}) \tag{9}$$

The single-phase heat transfer coefficient is calculated from the following equation

$$q_{eff}"A_h = h_{sp}\left(\bar{T}_{m,w} - \bar{T}_{m,f}\right)\left(\eta_f A_f N_t + A_h - N_t A_c\right) \tag{10}$$

where $\bar{T}_{m,w}$ and $\bar{T}_{m,f}$ are the mean wall temperature and the mean fluid temperature, respectively. A_f is the surface area of a single micropin-fin, and A_C is the cross-sectional area of a single micropin-fin. N_t is the total number of micropin-fins. Assuming that the micropin-fin tips are insulated, the fin efficiency η_f can be calculated using

$$\eta_f = \frac{\tanh(mH_f)}{mH_f} \tag{11}$$

where

$$m = \sqrt{\frac{h_{sp}P_f}{k_s A_c}} \tag{12}$$

k_s is the solid material thermal conductivity and P_f is the micropin-fin perimeter. The convective thermal resistance of a microfluidic heat sink gives a good metric for its heat removal capability; the convective resistance for single-phase is calculated using overall fin efficiency η_o,

$$R_{CONV} = \frac{1}{\eta_o h_{sp} A_t} \tag{13}$$

where A_t is the total area exposed to fluid, and $\eta_o = 1 - \frac{NA_f}{A_t}(1 - \eta_f)$.

The local two-phase heat transfer coefficient h_{tp} in a unit cell area containing a single micropin-fin is evaluated from

$$q_{eff}"A_{uc} = h_{tp}(A_{uc} - A_c)(T_w - T_{sat}) + h_{tp}\eta_f A_f (T_w - T_{sat}) \tag{14}$$

where A_{uc} is the base area of a unit cell. Thus

$$A_{uc} = S_T S_L \tag{15}$$

T_w is micropin-fin base temperature over the last quarter of the chip, calculated from the

last heater temperature, T_h. This is the region in which both liquid and gas phases exist. Assuming one dimensional conduction in the heat sink base, T_w can be determined from

$$q_{eff}" = \frac{T_h - T_w}{\frac{t_{Si}}{k_{Si}} + \frac{t_{SiO2}}{k_{SiO2}}} \quad (16)$$

where t_{Si}, t_{SiO2}, k_{Si} and k_{SiO2} are thickness of silicon and silicon dioxide, thermal conductivity of silicon and silicon dioxide, respectively.

The exit quality was calculated from

$$x = \left[\frac{q_{eff}"A_h - \dot{m}C_p(T_{sat} - T_{in})}{h_{fg}}\right] / \dot{m} \quad (17)$$

where T_{sat} and h_{fg} are water saturation temperature and latent heat of vaporization, both of which are evaluated at device exit pressure.

Reynolds number is defined by

$$\mathrm{Re} = \frac{\rho V_{max} D}{\mu} \quad (18)$$

where ρ is the density and μ is the dynamic viscosity. The maximum velocity of the fluidic V_{max} is defined by

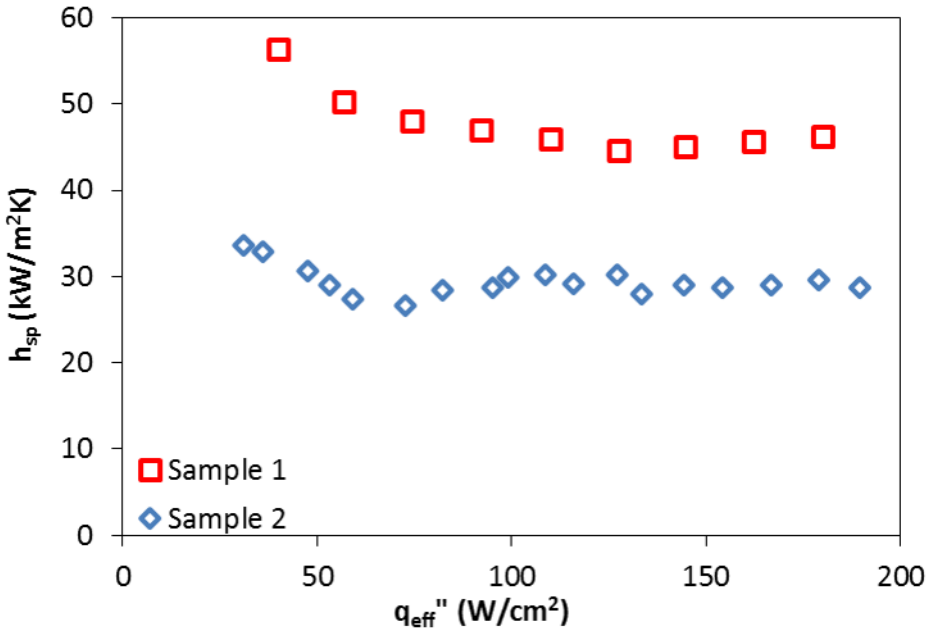
$$V_{max} = \frac{\dot{m}}{\rho A_{c,min}} \quad (19)$$

3.4 Thermal Testing Result and Analysis*

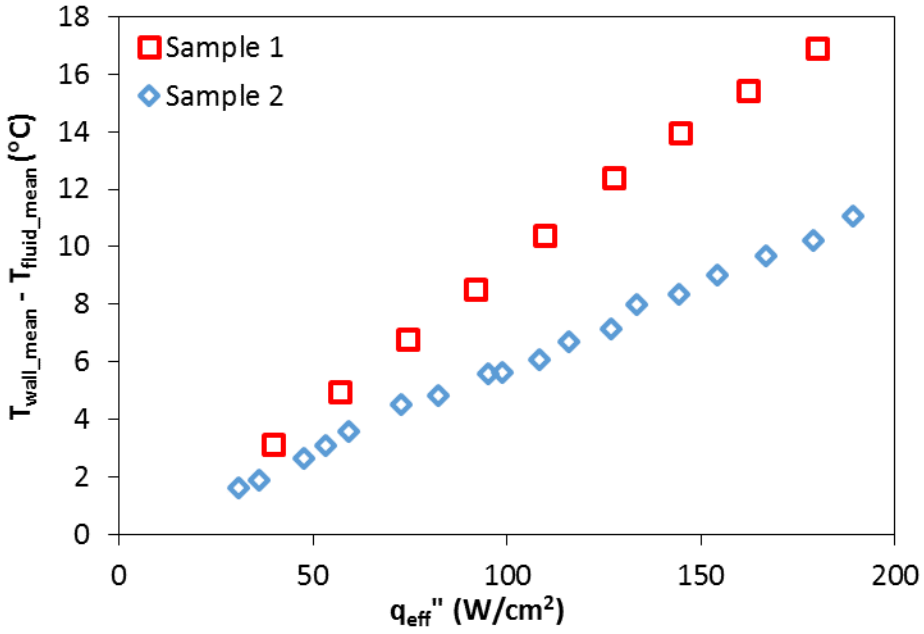
The heat transfer coefficient, mean temperature difference from wall to fluid, convective thermal resistance and pressure drop for both samples in the single-phase region are shown in Fig. 28. The single-phase heat transfer coefficient is almost independent of heat flux, as shown in Fig. 28 (a). Sample 2, with higher pin density, has a lower heat

* This work is a collaboration with X. Han and Y. Joshi. Their contributions to thermal testing are highly appreciated.

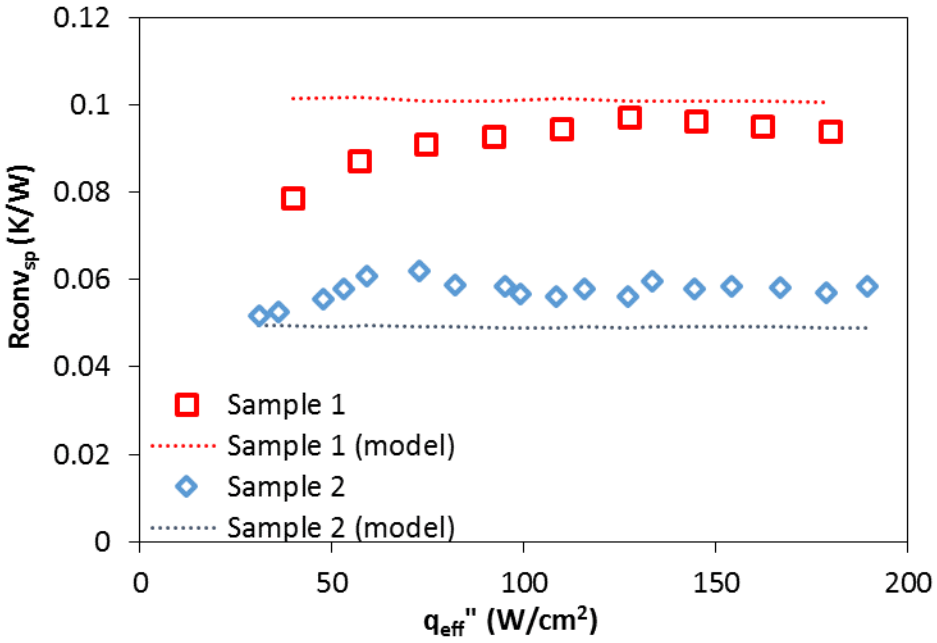
transfer coefficient and higher pressure drop than sample 1, but at the same mean temperature difference from heat sink wall to fluid, sample 2 dissipates higher power than sample 1, as shown in Fig. 28 (b). Sample 2 also has lower convective resistance as compared in Fig. 28 (c). This is because the surface area of sample 2 is almost three times that of sample 1. The experimentally derived convective thermal resistances are compared to the correlation from Tullius et al. [69] and the average error is 9.05% for sample 1 and 14.33% for sample 2. This correlation will be used again in section 3.5 to explore the trade-off between electrical and thermal performance. As the heat fluxes increase, the fluid temperature increases, which leads to a decrease of pressure drop due to the decrease of viscosity, as shown in Fig. 28 (d). The average Re in the single phase region are 171.4 and 25.4 for sample 1 and sample 2, respectively.



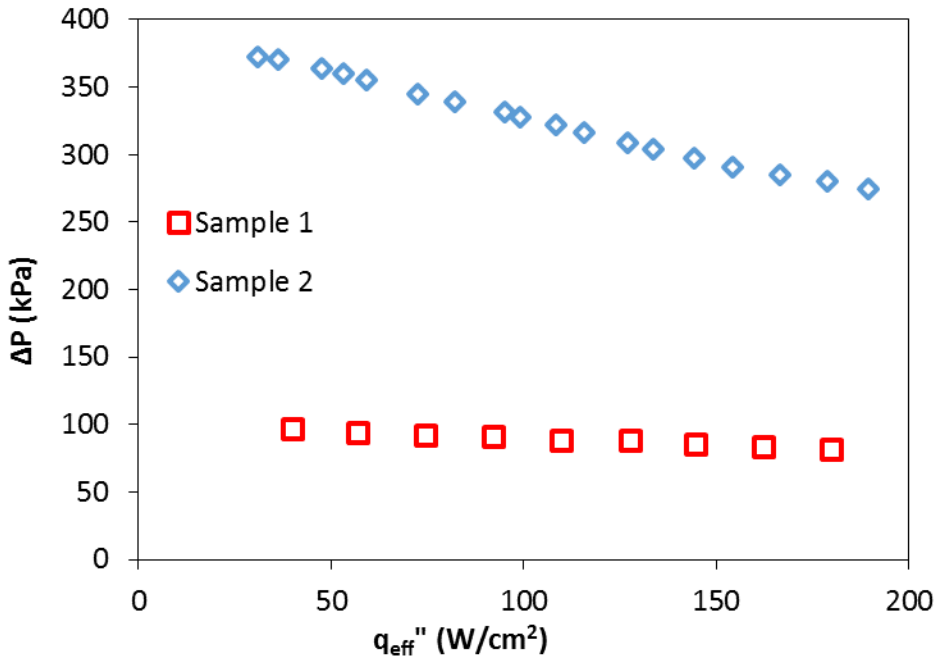
(a)


Sample 1
Sample 2
$T_{wall\_mean} - T_{fluid\_mean}$ (°C)
q_{eff}" (W/cm²)
0
2
4
6
8
10
12
14
16
18
0
50
100
150
200

(b)


Sample 1
Sample 1 (model)
Sample 2
Sample 2 (model)
$Rconv_{sp}$ (K/W)
q_{eff}" (W/cm²)
0
0.02
0.04
0.06
0.08
0.1
0.12
0
50
100
150
200

(c)



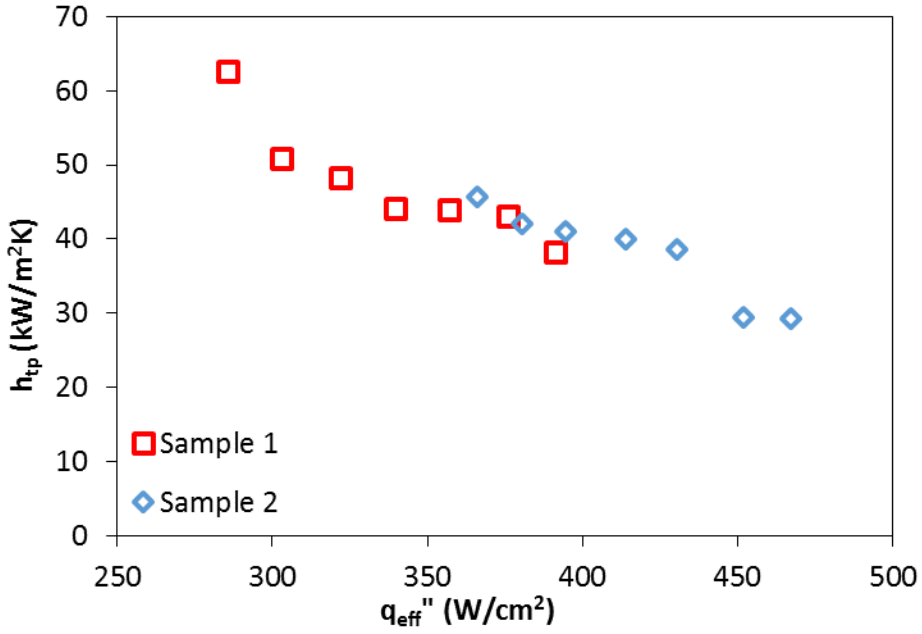
(d)

Fig. 28. Single-phase testing data: (a) Heat transfer coefficient; (b) mean temperature difference from wall to fluid; (c) convective resistance and (d) pressure drop for single-phase.

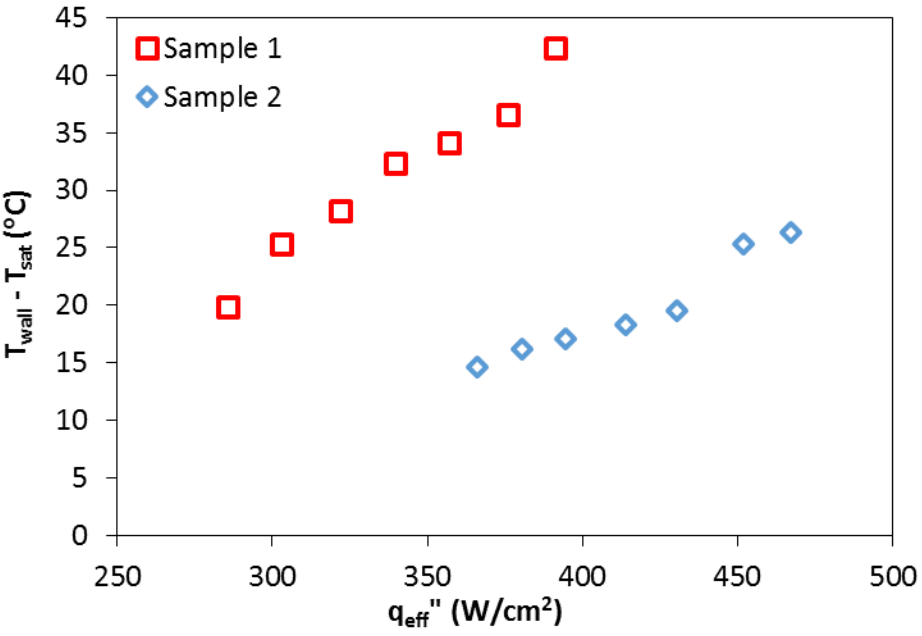
With further increases in heat flux, boiling initiated in the exit manifold outside the finned region, and the flow transitions from single-phase to two-phase. Fig. 29 compares results when heat fluxes were high enough to induce boiling in the finned area. Local two-phase heat transfer coefficients are shown in Fig. 29 (a), and they decrease with increasing heat flux. Similar trends were also reported by Qu et al. [33]. Boiling was observed only in the last quarter of the micropin-fin array close to passage exit due to inlet sub-cooling. Bubble nucleation begins at certain micropin-fins and expand rapidly in a triangular wake of liquid and vapor mixture, as shown in Fig. 29 (e). Increase of vapor quality in the liquid vapor mixture degraded heat transfer as heat flux increased. A sudden drop in local heat

transfer coefficient of sample 2 is observed when heat flux exceeds 450 W/cm^2. One possible reason is thinning of liquid film and the approach of partial dry out. Fig. 29 (b) shows the boiling curves for both tests, and sample 2 with denser pins had lower wall superheat at the same heat fluxes. When boiling was first observed in the finned area, vapor appeared only at the row of pins closest to the channel exit. As supplied power increased, the vapor front moved towards the channel inlet. At the highest heat fluxes achieved, boiling was observed in the last quarter of the finned area close to the channel exit. Therefore, at the beginning of boiling, the majority of the finned area was still in single-phase, and pressure drop showed single-phase (i.e., a decrease with an increase in heat flux) behavior for sample 2 as shown in Fig. 29 (c). This was not observed for sample 1 because sample 1, with fewer micropin-fins, had lower pressure drop, and the effects of the viscosity decrease due to fluid heating did not overshadow the pressure increase due to existence of vapor phase. Exit vapor qualities are plotted in Fig. 29 (d), and they increased roughly linearly with increasing heat flux.

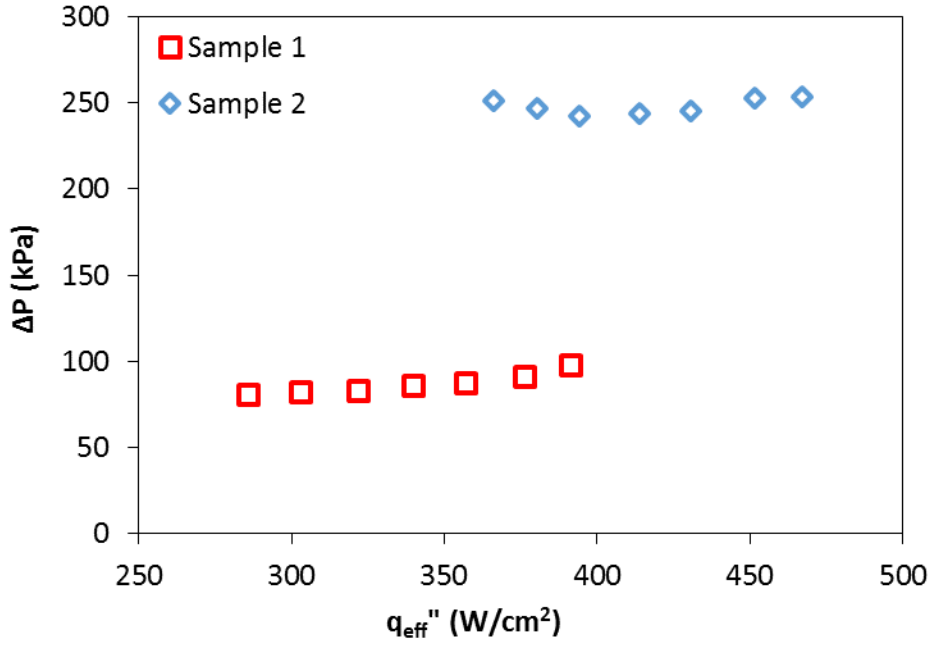
By comparing Fig. 28 and Fig. 29, it can be found that for the studied micropin-fin dimensions, two-phase cooling can improve the heat transfer coefficient. Increasing the micropin-fin density will increase the pressure drop for the same mass flow rate and can effectively decrease the convective thermal resistance, but not necessarily improve heat transfer coefficient.


70
60
50
40
30
20
10
0
250
300
350
400
450
500
h_{tp} (kW/m^{2}K)
q_{eff}" (W/cm^2)
Sample 1
Sample 2

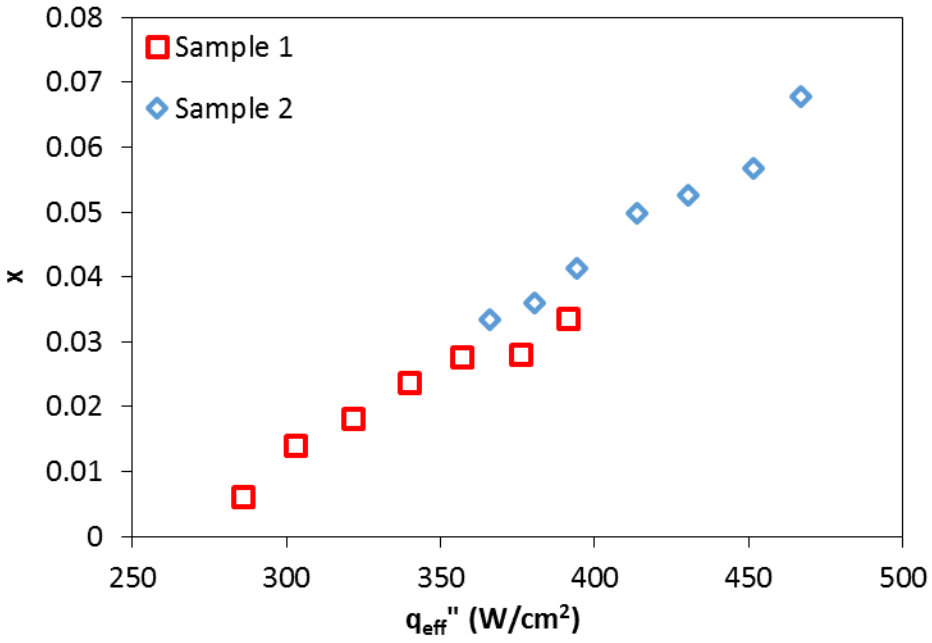
(a)


45
40
35
30
25
20
15
10
5
0
250
300
350
400
450
500
T_{wall} - T_{sat} (°C)
q_{eff}" (W/cm^2)
Sample 1
Sample 2

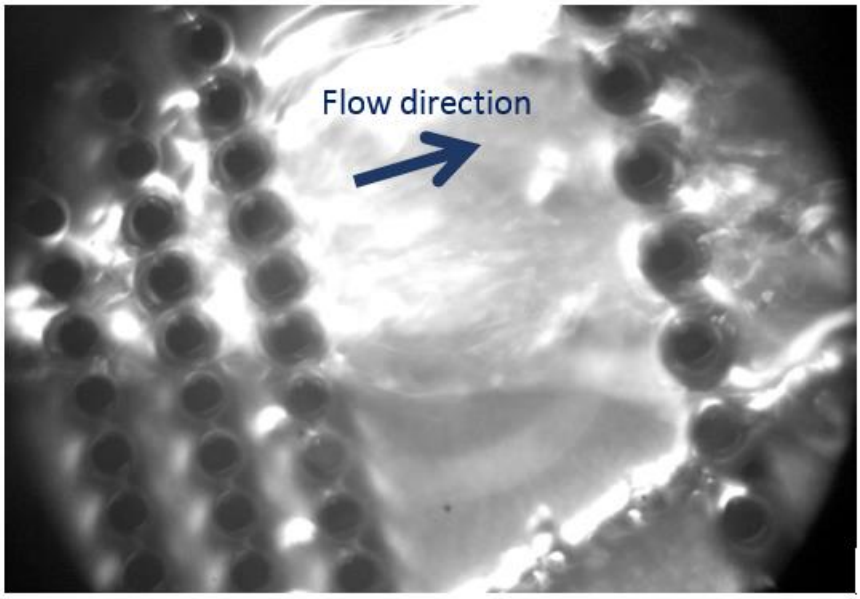
(b)


Sample 1
Sample 2
ΔP (kPa)
300
250
200
150
100
50
0
250
300
350
400
450
500
qeff" (W/cm2)

(c)


Sample 1
Sample 2
x
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0
250
300
350
400
450
500
qeff" (W/cm2)

(d)



(e)

Fig. 29. Two-phase testing data: (a) Local two phase heat transfer coefficient; (b) boiling curve; (c) pressure drop; (d) vapor quality and (e) Flow visualization of Sample 1 at 381W.

3.5 Potential Impact of Microfluidic Cooling on Electrical Performance of 3D IC Interconnects

The impact of micropin-fin heat sink design on the electrical performance of 3D interconnects is evaluated to a first order in this section. Fig. 30 shows a simple 3D interconnect link with embedded microfluidic cooling in which a transmitter in tier 1 of the stack communicates with a receiver located in tier 2; the signal transmission occurs through the on-chip wires on tier 1 and tier 2 as well as the TSV. The TSVs are embedded within the micropin-fins, which are submerged in coolant.

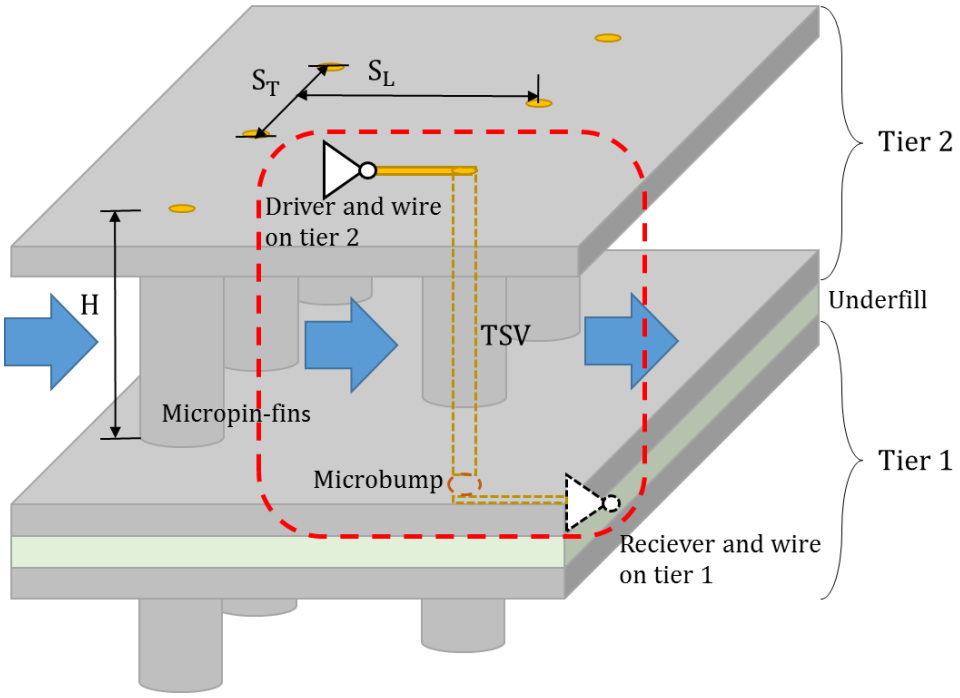
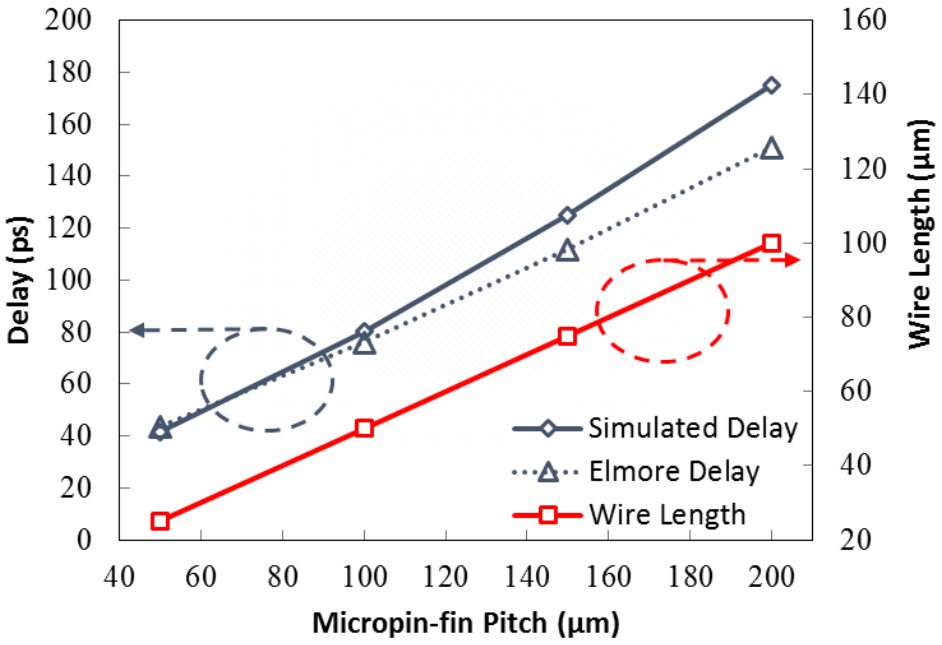


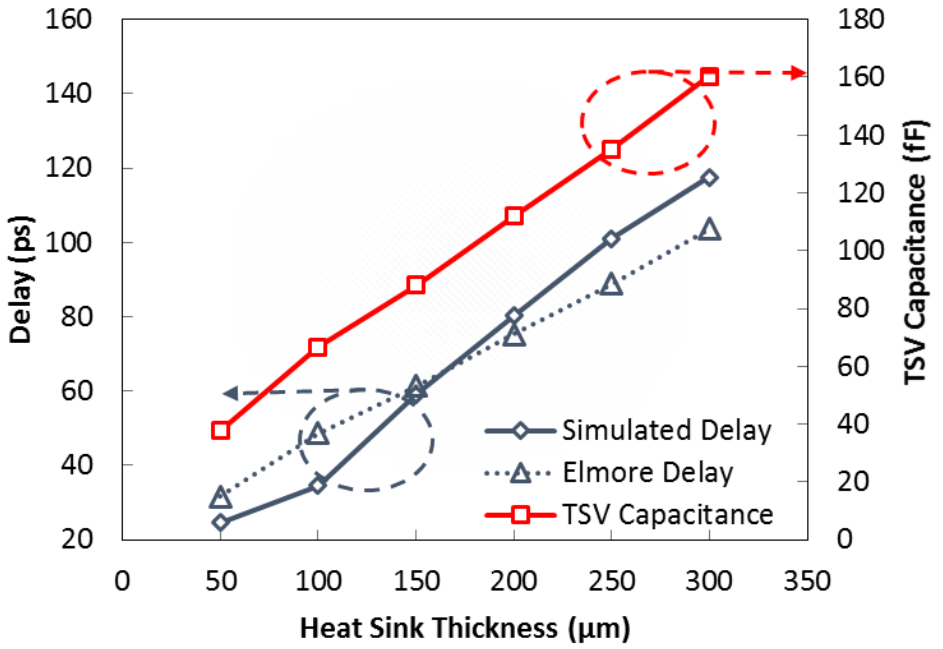
Fig. 30. 3D interconnect link.

The 50% delay of the 3D interconnect was evaluated using a simple Elmore model [58] as well as commercial simulation tools to attain an initial insight. The equivalent resistance and capacitance of the driver and receiver were taken from the 2012 ITRS projection for 14nm CMOS [60]. The wires and TSVs were simulated with ANSYS HFSS software to extract the S-parameters up to 50 GHz [70], which were then imported into Agilent ADS. The TSV capacitance was also extracted from the S-parameters at 2 GHz. For simplicity, the interconnects were ground-signal-ground (GSG) configured. We assumed the length of the wires on tier 1 and tier 2 to be half of the micropin-fin pitch; this was a worst case scenario where the driver and receiver were placed at the center between two micropin-fins. The impact of the coolant was neglected in this analysis.

The 50% delay of the 3D link and TSV capacitance vs. micropin-fin pitch is shown in Fig. 31 (a). The micropin-fin height is fixed at 200 μm. As micropin-fin pitch increases, delay increases with pitch because the wire length is assumed to be half of the pitch. When the micropin-fin pitch is fixed at 100 μm and the micropin-fin height increases, TSV capacitance and link delay increase, as shown in Fig. 31 (b). While the delay value will change when the impact of the coolant is included, the delay trend vs. micropin-fin pitch and heat sink thickness will be similar.



(a)



(b)

Fig. 31. Delay and TSV capacitance vs. (a) Micropin-fin pitch, (b) TSV height.

The delay and R_{CONV} vs. micropin-fin longitudinal pitch and heat sink thickness are shown in Fig. 11. R_{CONV} is calculated by empirical models [69] for single-phase cooling. In the model, the Nusselt number is calculated by:

$$Nu = 0.08\left(\frac{H_f}{D}\right)^{0.25}\left(\frac{S_L}{D}\right)^{0.2}\left(\frac{S_T}{D}\right)^{0.2}\left(\frac{Pr}{Pr_s}\right)^{0.25}\left(1+\frac{d_H}{D}\right)^{0.4} Re^{0.6} Pr^{0.36} \quad (20)$$

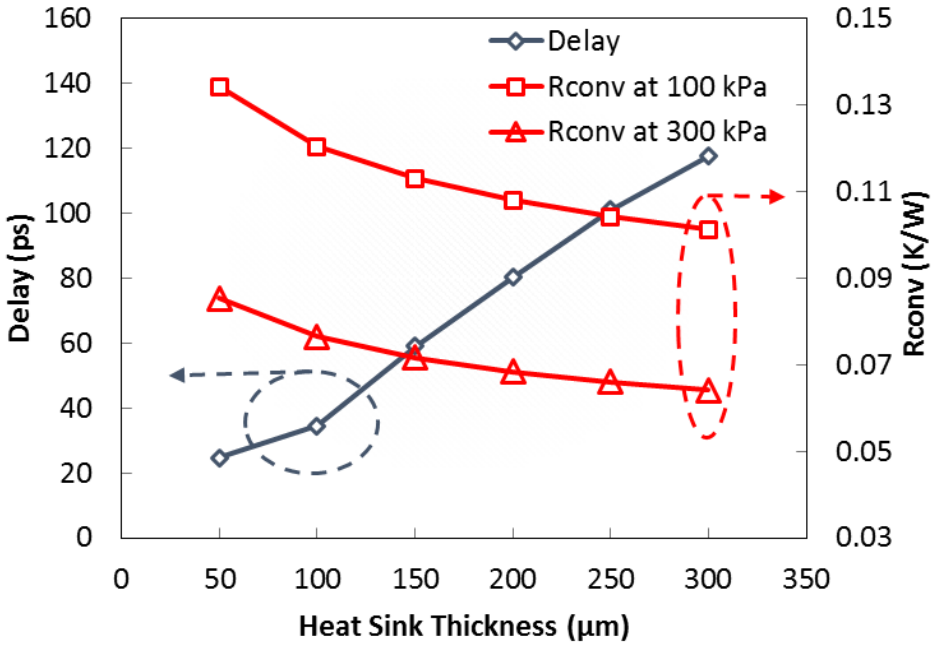
where H_f, D, S_L and S_T are the micropin-fin height, diameter, longitudinal pitch and transverse pitch, respectively. We assume the micropin-fins are bonded to the cap, therefore channel clearance d_H is set to be 0.

The average heat transfer coefficient can be calculated as:

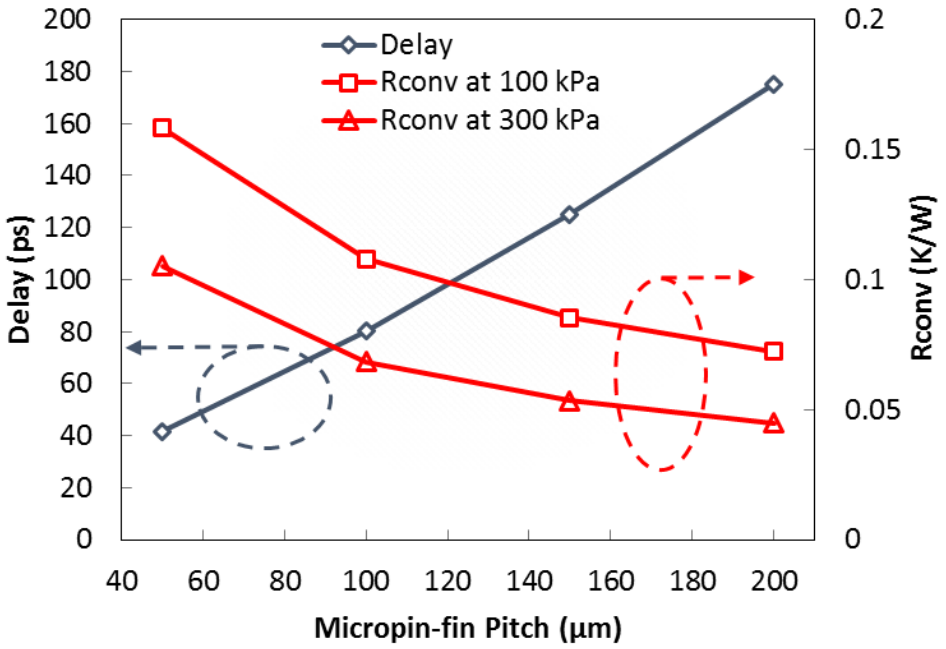
$$h = \frac{Nu * k_f}{D} \quad (21)$$

and R_{CONV} is calculated using Equation (13). In the calculation, pressure drop of 100 kPa and 300 kPa were selected. Increase of either longitudinal pitch or micropin-fin height will lead to an increase of Nusselt number and therefore a decrease R_{CONV} in the range of pressure drop and dimensions studied.

A clear trade-off between electrical and thermal performance can be observed in Fig. 32 (a) when the longitudinal pitch increases, R_{CONV} decreases. However, the link delay increases due to longer wires connecting the TSVs embedded in the micropin-fins. In Fig. 32 (b), increasing micropin-fin height can decrease R_{CONV}, but it will increase TSV height and capacitance and therefore increase the delay.



(a)



(b)

Fig. 32. Delay and R_{CONV} vs. (a) Micropin-fin pitch, (b) TSV height.

3.6 Conclusion

This chapter reports on novel thermal testbeds with embedded micropin-fin heat sinks that were designed and microfabricated in silicon. Two micropin-fin arrays were presented, each with a nominal pin height of 200 µm and pin diameters of 90 µm and 30 µm. Single phase and two phase thermal testing of the micropin-fin array heat sinks were performed using deionized (D.I.) water as the coolant. The tested mass flow rate was 0.001 kg/s, and heat flux ranged from 30 W/cm^2 to 470 W/cm^2. The maximum heat transfer coefficient reached was 60 kW/m^{2}K. The results obtained from two testbeds were compared and analyzed, showing that density of the micropin-fins has a significant impact on thermal performance.

CHAPTER IV

EMBEDDED MICROFLUIDIC COOLING IN 3D IC II: HOTSPOT COOLING

4.1 Introduction

Driven by the rapidly increasing demand of high performance computing, the integration level and power density of electronics continue to increase, which subsequently necessities advances in cooling. Moreover, the non-uniform power dissipation in modern chips presents an additional challenge to the design of an effective cooling solution [71]. The temperature of the hotspot region, rather than the temperature of the background, often limits a chip's performance by locally driving temperature above operating limits and becoming the thermal design limiter [72]. Novel methods for cooling hotspots with high heat flux is required, and embedded microfluidic cooling is believed to be a promising solution [73], [74].

Microfluidic cooling has been widely explored for decades, including heat sink design [75], [76], fabrication technologies [77] and reliability [78]. Forced convection in microchannels using both single phase and boiling (two-phase flow) are of particular interest. Two-phase convective cooling in microgap coolers has a potential for hotspot mitigation as the low thermal resistance in the thin liquid layer covering the microgap surface was shown to offer ultra-high heat removal rate [79]. Prior studies of two-phase micro-coolers have shown the dissipation of heat fluxes up to 350 W/cm^2 [34]-[38], as shown in Chapter I. However, experiments of extreme-microgap with multi-kW/cm^2 heat fluxes have not been reported. In this chapter, a hotspot cooler testbed for convective

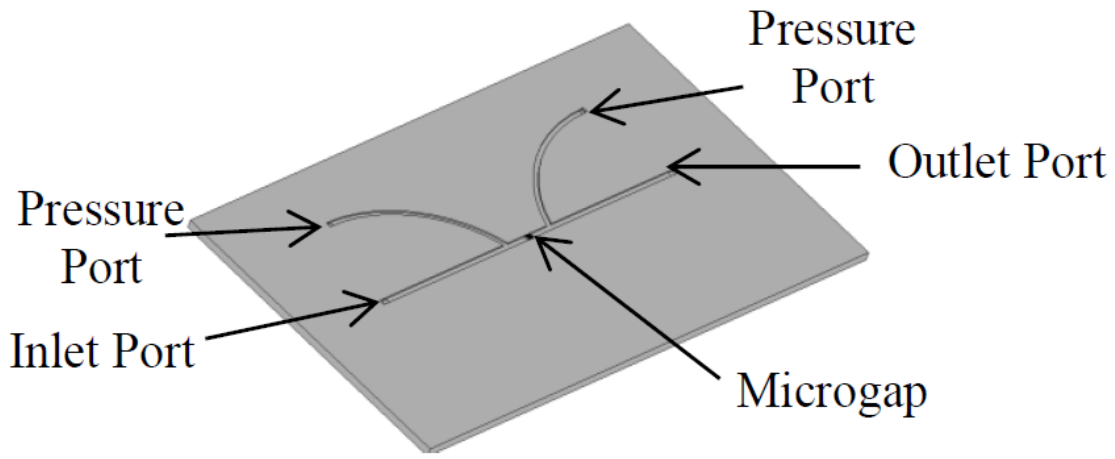
boiling experiments in extreme-microgap with integrated micropin-fins was designed, fabricated and tested. The detailed fabrication technologies are presented. The maximum heat flux during testing was 4.75 kW/cm^2 with flow rates in the range of 0.1 – 0.3 ml/min. The thermal resistance and pressure drop of the device were characterized and compared with a reference device without micropin-fins (Note: for the remainder of the chapter, this device will be referred to as 'empty gap' device). A reduction in thermal resistance was observed with the surface enhancement of the micropin-fins. A tradeoff to this improved thermal performance is a large increase in pumping power resulting from the high constriction of fluid flow. In addition, the reliability analysis shows that the device can sustain 3000 kPa static pressure and 1000 kPa pressure drop across the microgap.

The chapter is organized as follows: Section 4.2 introduces the design and fabrication process of the heat sinks; Section 4.3 summarizes the testing setup and procedure; Thermal testing results and analysis are shown in Section 4.4; Section 4.5 shows the reliability modeling of the channel; and finally conclusions are drawn in Section 4.5.

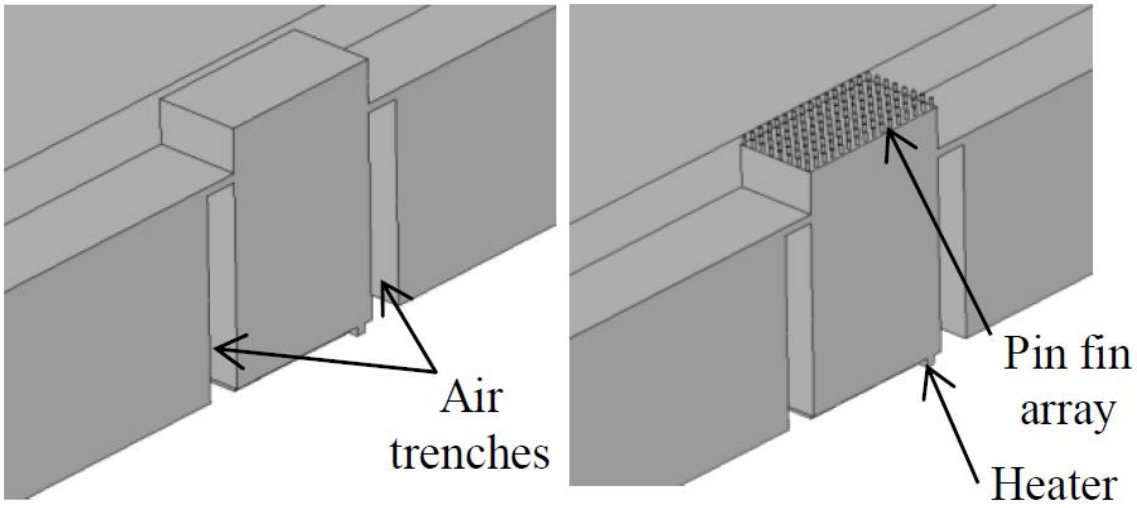
4.2 Design and Fabrication Process of the Heat Sinks

An overview of the empty gap devices and micropin-fin devices is shown in Fig. 33 supplemented by optical and SEM images in Fig. 34. Subcooled fluid enters the device through a 200 μm diameter inlet port and flows through the inlet plenum, which is 50 μm deep to minimize parasitic pressure drop at the fluid entry/exit domains. The microgap test section is 300 μm long × 200 μm wide × 10 μm tall and is located in the middle of the device with a platinum resistance heater deposited on the back side. The heater generates a controlled heat load through Ohmic heat generation and also serves as a resistance temperature detector (RTD) for temperature measurement. Three additional RTDs are

located on each side of the heater (six total), orthogonal to the coolant flow direction, solely for temperature measurement in the vicinity of the heater (Fig. 34b). The RTDs are 80 μm × 55 μm spaced at ~17.5 μm between each other. Pyrex glass seals the top of the microgap and allows for flow visualization. Air trenches are 40 μm wide and etched 180 μm deep into silicon from the back (heater) side of the device to reduce conduction heat spreading in the bulk silicon. The pin fin device contains an array of 32 × 20 inline cylindrical pin fins, which are 10 μm tall (i.e., no clearance to the top of the microgap), 4 μm in diameter and 10 μm apart contributing a surface area enhancement factor of 2.27.

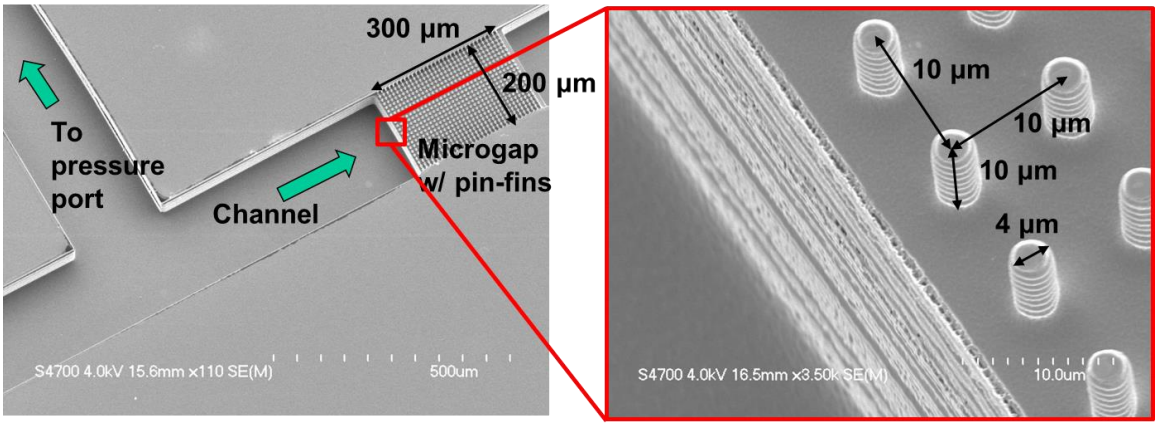


(a)

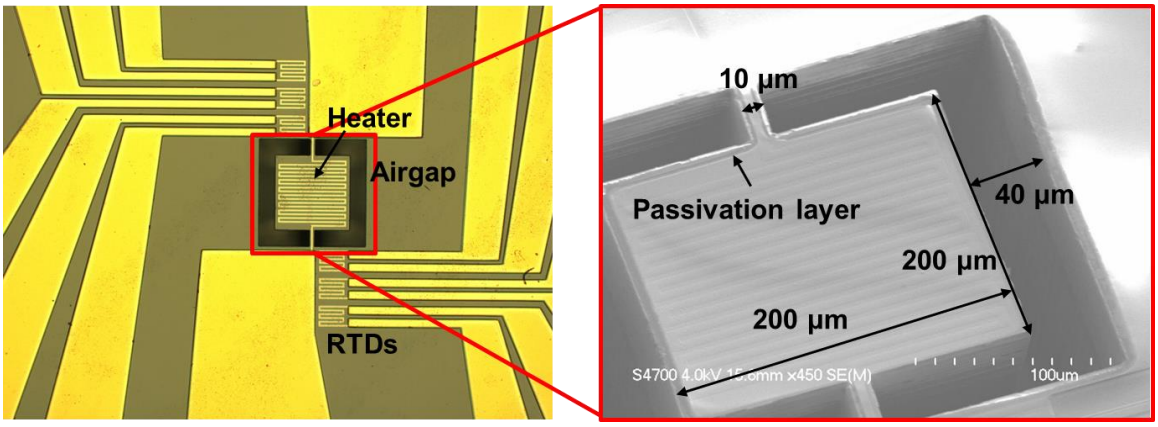


(b) (c)

Fig. 33. Overview of the hotspot testbed: (a) the overview; (b) cross-section of the empty gap device; (c) micropin-fin device.



(a)



(b)

Fig. 34. Optical and SEM images of the pin fin device showing dimensions: (a) gap side and (b) heater side.

The fabrication process of the testbed is shown in Fig. 35. The process begins with a 280 μm thick double side polished wafer. A standard Bosch process with alternating of SF_6 (for etching) and C_4F_8 (for passivation) was used to create the 10 μm (± 0.5 μm) tall micropin-fins and the microgap. A second Bosch process was then used to etch the 50 μm (± 3 μm) deep channel. Next, the microgap was sealed using a pyrex cap with anodic bonding under the voltage of 800 V at 350 ^{o}C. The bonded wafer was then flipped and a 1 μm thick insulating silicon dioxide layer was deposited using low pressure chemical vapor deposition (LPCVD). The 200 nm (±5 nm) thick Platinum heater/RTDs and 500 nm (±10 nm) thick gold pads were then deposited on the SiO_2 layer. A second SiO_2 layer was deposited on the heater/RTDs as a passivation layer using LPCVD. The air trenches were then etched using Bosch process. Lastly, inlet, outlet, and pressure measurement ports were etched using the Bosch process from the same side of the wafer.

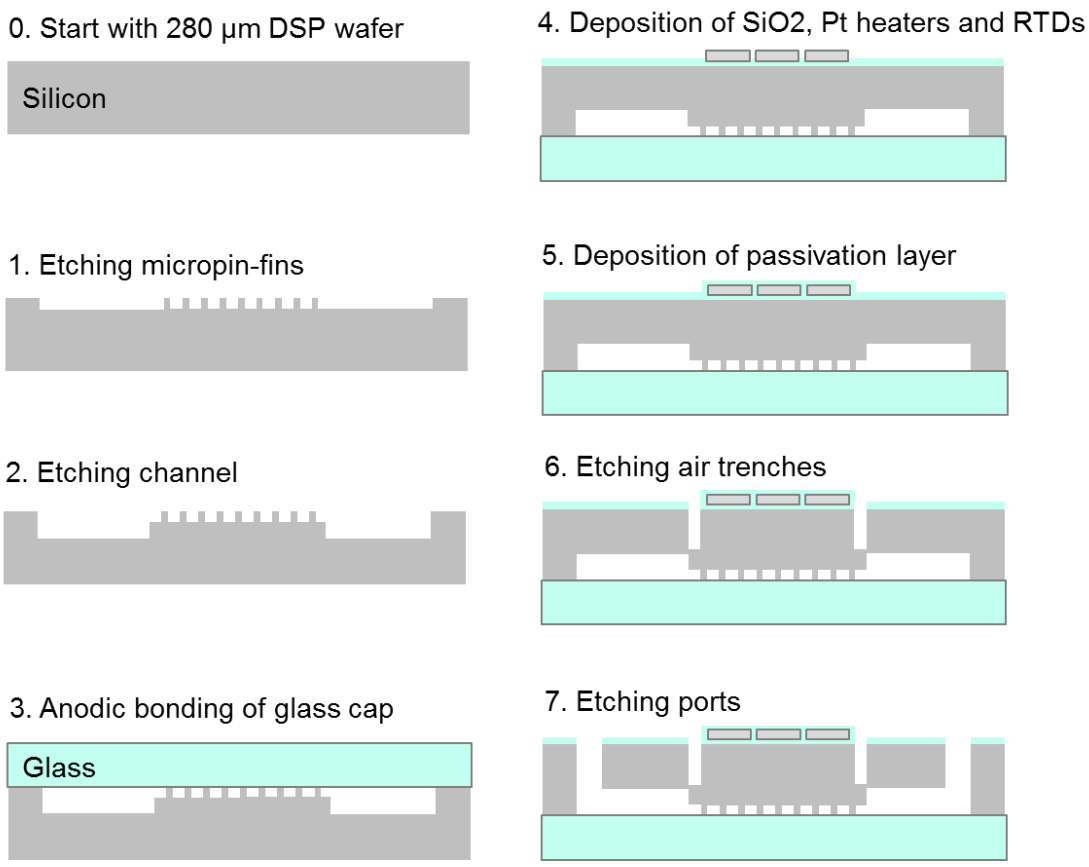


Fig. 35. Fabrication process of the heat sinks.

4.3 Testing Setup and Procedure

An overview of the experimental setup is presented in Fig. 36. The device is housed in a Polyether ether ketone (PEEK) package with machined O-ring groves for airtight sealing of the inlet/outlet ports and pressure taps. A cross-sectional view of the packaged device that makes up the test section is shown in Fig. 37. The pressure drop, heater resistance, circuit current, inlet/outlet fluid temperatures and fluid reservoir temperature were recorded with an Agilent 34970A data acquisition unit. A KDS Scientific Legato 270 series syringe pump was used to drive refrigerant through the test section at the desired flow rate. The fluid temperature measurements were obtained with Omega K-type thermocouples. The pressure drop was measured with Omega PX 309 series pressure

transducers. The power was supplied to the device heaters with an Agilent E3641A power source. A fan cooled WBA series thermoelectric was used to condense vapor exiting the test section. The reservoir tank was heated by electrical wire heaters with an Omega CN4000 PID controller to drive refrigerant into the system.

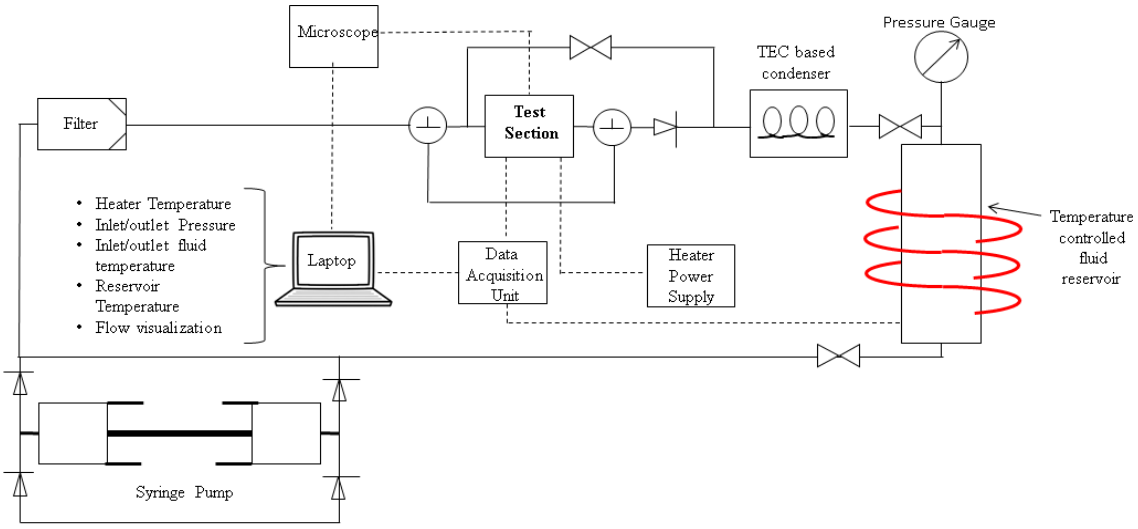


Fig. 36. Testing Setup Schematic.

Linear correlation between the heater resistance and temperature was obtained before testing by calibrating test devices in a vacuum controlled oven. Experiments began by evacuating the experimental setup to remove air in the system followed by charging the test loop with R134a. The reservoir tank, filled with refrigerant, was pressurized with wire heaters to ensure complete filling of the experimental loop with liquid. R134a was pumped to the test section at 22.4 ^{o}C inlet temperature with flow rates ranging from 0.1 – 0.3 ml/min. Power was applied to the heaters in 0.1-0.25 W increments until steady state temperatures and pressures were achieved. Power to the heaters was turned off when local

dryout was observed in the microgap or when the inlet pressure was approaching glass syringe limits to avoid catastrophic failure.

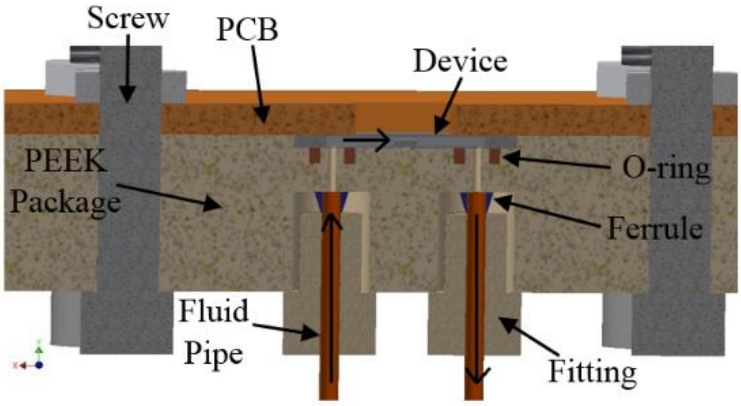


Fig. 37. Cross-sectional view of the test section with airtight packaging.

The error of the K-type thermocouple used for heater calibration is +/- 0.9 °C, the error in power applied to the heaters from Agilent E3641A power source is +/- 0.011 W, the error in the mass flow rate from syringe pump is +/- 0.01 mL/s, and the error in the pressure transducer measurements is +/- 8.62 kPa. The error in microgap height, air trench depth, and micropin-fin height is within +/- 5% of the reported dimensions, and the error in the heater length and width is within +/- 1% of the reported dimensions. Error propagation was applied to assess the uncertainty in heat flux and thermal resistance which are found to be +/- 1.5% and +/- 1.7%, respectively. The average uncertainty of pumping power in the empty gap and micropin-fin devices is +/- 46.2 % and +/- 8.8 %, respectively. The lager uncertainty of pumping power in the empty gap device is due to the low pressure drop across the microgap which is comparable with the error in pressure measurements.

4.4 Testing Results and Analysis*

The minimum overall thermal resistance after the onset of boiling in the microgap at each tested flow rate for devices with and without micropin-fins is shown in Fig. 38. The thermal resistance is calculated as,

$$R'' = \frac{T_h - T_f}{q_h''}, \tag{22}$$

where T_h is the heater temperature, T_f is the ambient air temperature outside the device, and q_h'' is the heat flux at the heater area, calculated as the ratio of the power input to the heater to heater surface area (200 μm x 200 μm).

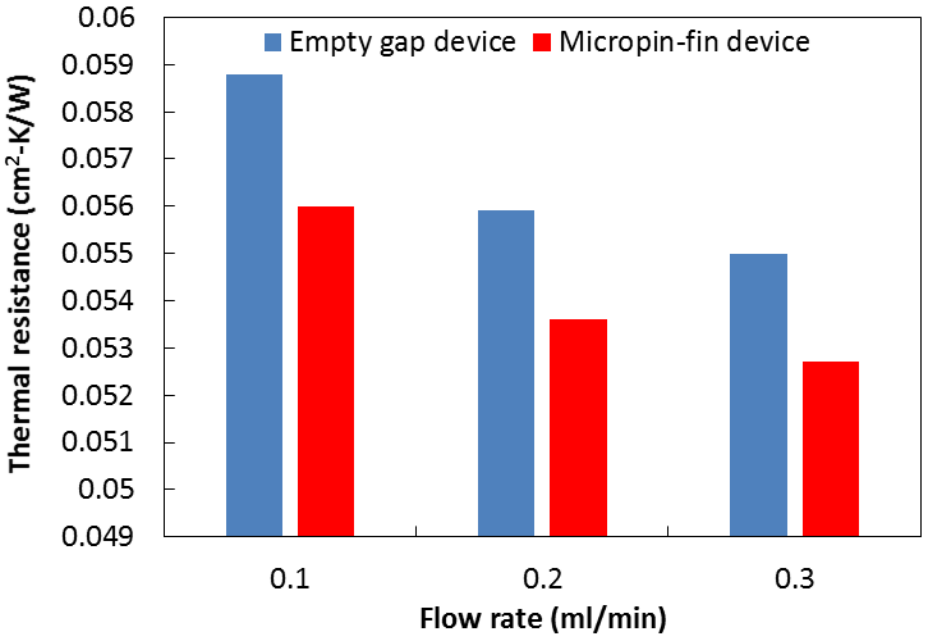


Fig. 38. Minimum thermal resistance after the onset of boiling vs flow rate comparing the micropin-fin device with the empty gap device without micropin-fins.

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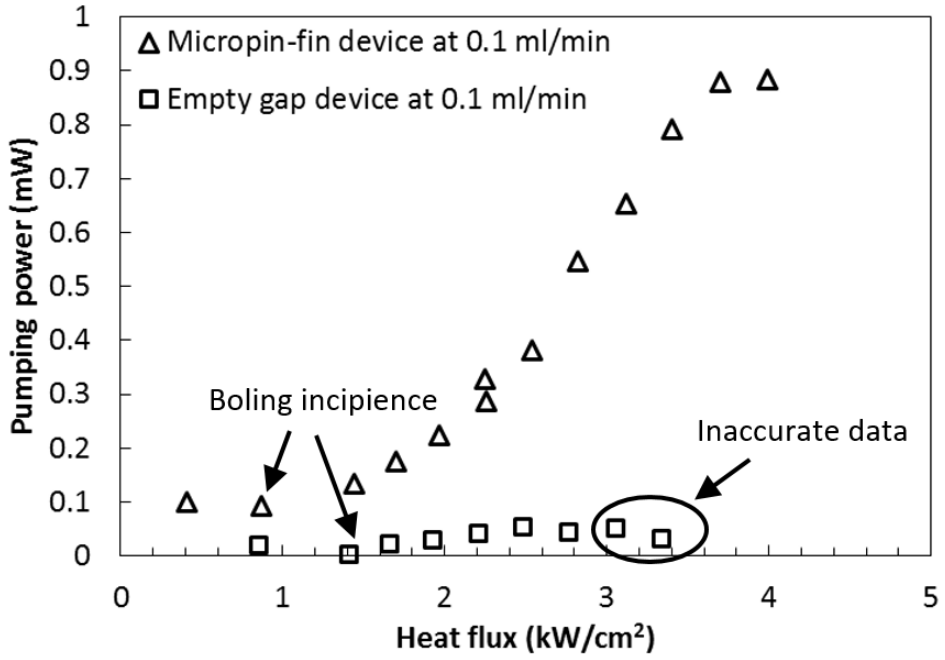
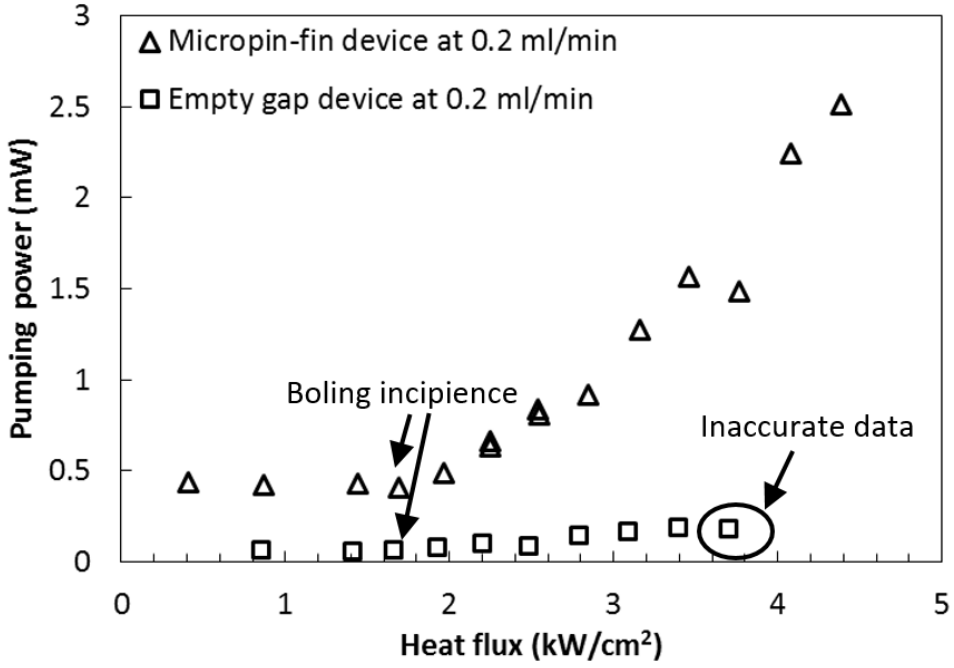
* This work is a collaboration with M. Nasr, Y. Joshi and A. G. Fedorov. Their contributions to thermal testing are highly appreciated.

The minimum thermal resistance of the micropin-fin device is slightly smaller than the empty gap device. Given that the surface area is enhanced by a factor of 2.27 in the micropin-fin device, it was expected that the thermal resistance would be reduced by approximately the same factor since it is inversely proportional to the surface area. However, in two phase convective boiling, the highest heat removal rate occurs when a continuous thin liquid film covers the microgap surface; the thinner the film, the higher the heat removal rate [80]. Although the micropin-fins increase surface area by a factor of 2.27, they have the unintended effect of breaking up the thin film that dominates convective boiling mechanism in microgaps of ultra-small gap height [80]. The combined effects of an increase in surface area and the existence of a thin film, although broken up, in the micropin-fin device reduce the thermal resistance beyond that of an empty microgap without micropin-fins for the same heater heat flux; however it is difficult to predict the reduction given the complexity associated with the physics of boiling. This is contrary to single phase convective cooling, where the effect of a surface area enhancement increase directly correlates to a reduction in thermal resistance by approximately the same factor.

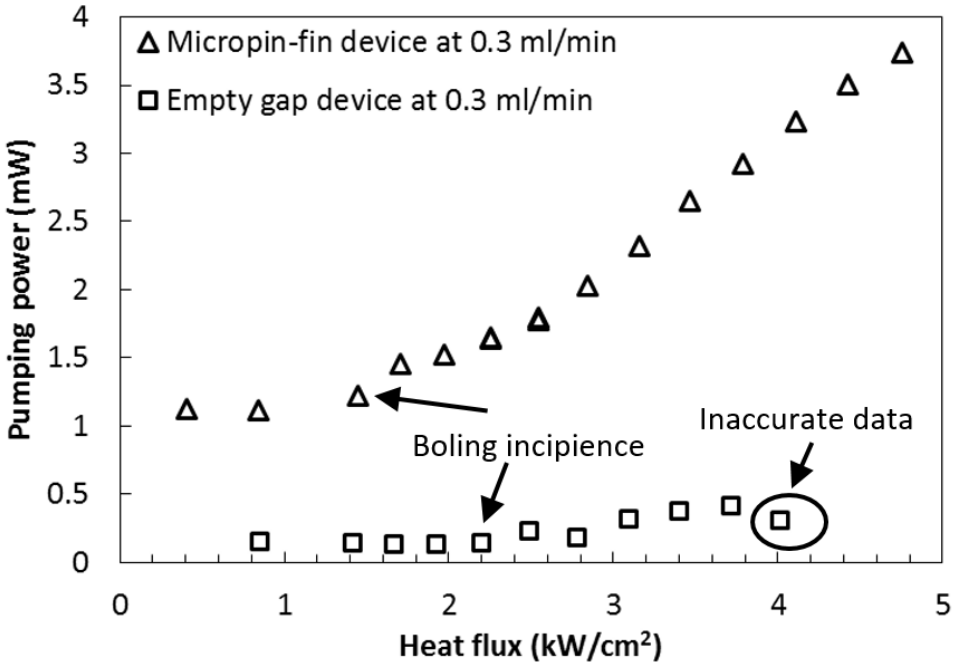
The pumping power as a function of heat flux for the micropin-fin device and empty gap device are compared in Fig. 39. The volumetric flow rates were ranging from 0.1 ml/min to 0.3 ml/min in both devices. The volumetric flow rates were limited to 0.3 ml/min because maximum pressure at qualities approaching unity reached 2000 kPa, which is at the upper limit of glass syringes used to pump the fluid before catastrophic failure.


Micropin-fin device at 0.1 ml/min
Empty gap device at 0.1 ml/min
Boling incipience
Inaccurate data
Pumping power (mW)
Heat flux (kW/cm²)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
1
2
3
4
5

(a)


Micropin-fin device at 0.2 ml/min
Empty gap device at 0.2 ml/min
Boling incipience
Inaccurate data
Pumping power (mW)
Heat flux (kW/cm²)
0
0.5
1
1.5
2
2.5
3
0
1
2
3
4
5

(b)

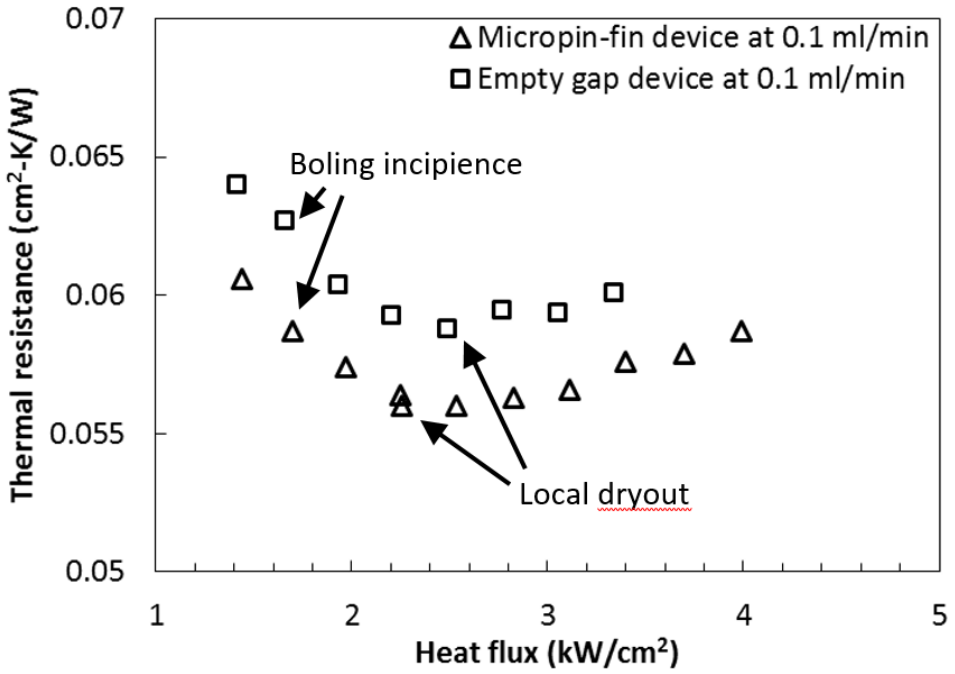


(c)

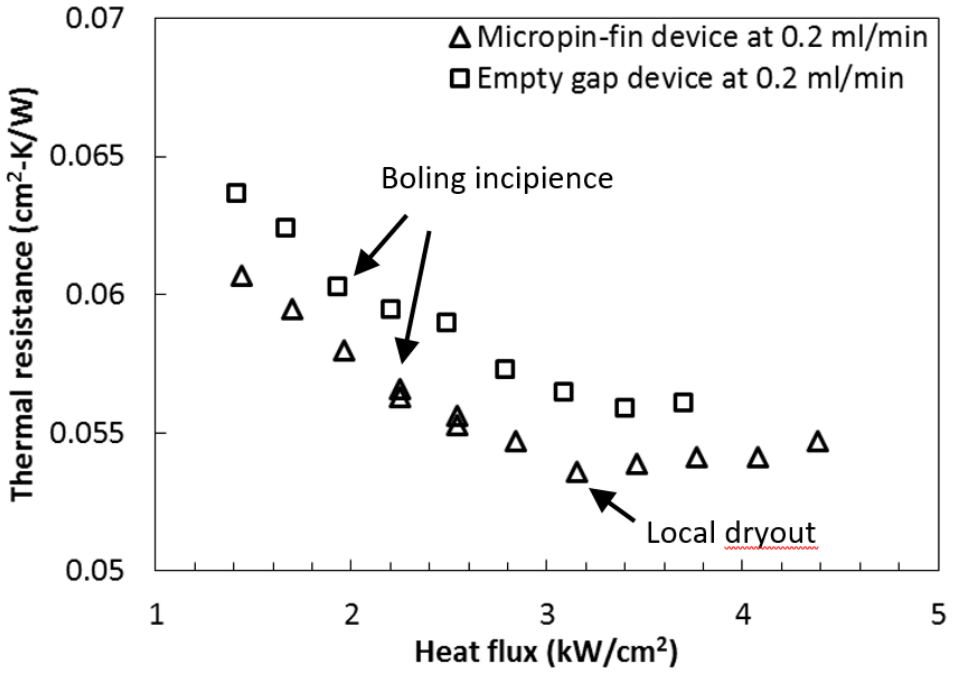
Fig. 39. Comparison of pumping power vs. heat flux between the micropin-fin device and empty gap device at flow rates of (a) 0.1 ml/min, (b) 0.2 ml/min and (c) 0.3 ml/min.

In the single phase domain, pumping power is nearly constant with increased heat flux in both devices. The onset of boiling in the microgap that occurs with increases in applied heater heat flux causes an increase in pumping power due to the acceleration between liquid and vapor states as well as viscous losses. The last data points where pumping power decreased in the empty microgap device are not accurate representations of the actual two phase pressure drop in the microgap, but result from boiling incipience in the inlet plenum where the pressure tap is located. The pressure transducing element, located further away from the test section, detects saturation pressure at ambient temperature, which is lower than the saturation pressure at the inlet of the microgap. In micropin-fin device tests, the recorded pumping power accurately represents two-phase

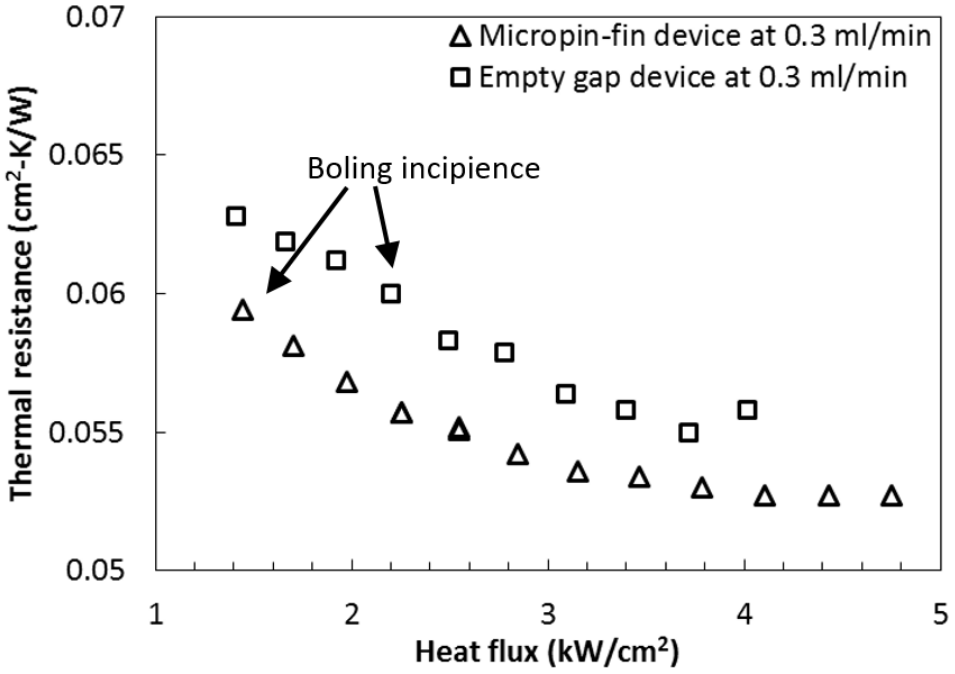
pressure drop across the microgap for all heat fluxes because boiling was not observed in the inlet plenum. The tight placement of micropin-fins (10 μm pitch) highly constricts fluid flow, increasing hydrodynamic resistance and viscous losses thereby driving the pressure drop much higher than that of an empty gap. As a result, the pumping power in the micropin-fin devices is much higher than that of the empty gap devices for the flow rates investigated.



(a)



(b)



(c)

Fig. 40. Comparison of thermal resistance vs. heat flux between the micropin-fin device and empty gap device at flow rates of (a) 0.1 ml/min, (b) 0.2 ml/min and (c) 0.3 ml/min.

The comparison of thermal resistance as a function of heat flux between the micropin-fin device and empty gap device at various flow rates is shown in Fig. 40. In the single phase domain, a decrease of thermal resistance with respect to heat flux is observed. We believe this is due to an improvement in heat rejection of the device by natural convection to the ambient air. Detailed explanation can be found in [80]. Upon the onset of boiling, the thermal resistance continues to decrease with respect to heat flux due to convective boiling in the microgap prior to the onset of local dryout, which is evident for the empty gap device at 0.1 ml/min and the micropin-fin device at 0.1 ml/min and 0.2 ml/min. At the onset of local dryout, the continuous liquid layer covering the heated surface of the microgap boils away, leaving mostly dry area. Therefore, the thermal resistance increases as fluid available for heat removal is reduced. The local dryout is not observed in the 0.3 ml/min plot because the test did not go to high enough heat fluxes to reach local dryout. Heater degradation limits the maximum heat fluxes tested in these experiments.

Compared to the empty gap device, the thermal resistance of the micropin-fin device has an average reduction of 3.5% due to the surface area enhancement. However, the cost associated with the very large increase in pumping requirement does not justify the integration of micropin-fins for the dimensions studied. Although the empty gap device, which only exploits the high heat removal rates of thin film convective boiling, was more efficient than the micropin-fin enhanced device, there may be other configurations of micropin-fins (e.g. larger spacing) that reduce the pressure drop to the point where an optimization of micropin-fin surface enhancement and the pumping requirement can be achieved.

4.5 Reliability Modeling

The successful implementation of this on-chip microfluidic cooling architecture requires the effective use of all aspects of co-design including electrical, thermal, fluidic, and mechanical aspects. Reliability modeling is conducted to assess the impact of the anticipated fluidic pressure loads on system integrity for high-performance operating conditions. ANSYS® Mechanical is used to develop the structural finite element model. The resulting stresses are examined and the potential for failure is evaluated for critical locations.

The model geometry is constructed and meshed to accurately match the design architecture. The silicon substrate is modeled including the microchannel and microgap as well as the isolation air trenches surrounding the heaters. The glass cap is also modeled, and it is assumed to be perfectly bonded to the silicon substrate at all contact interfaces. The actual heaters themselves are not included as they have little to no effect on the structure as a whole. Fig. 41 illustrates the model's layout. The model's material properties are shown in Table 7.

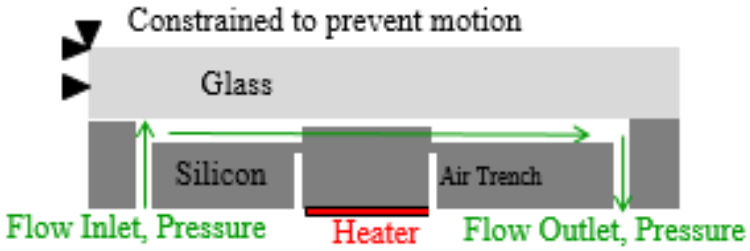


Fig. 41. Side view of hotspot geometry as modeled using ANSYS.

This model is loaded with internal pressures according to the expected working conditions of the device. The high-performance fluid typically flows through the internal

microchannel at working pressures in excess of 2000 kPa. This value depends upon flow rate, heat flux, and temperature of the fluid. In this model, the pressure is assumed to be 3000 kPa at the inlet with negligible pressure loss until it reaches the microgap. Within the microgap the pressure is assumed to linearly decay from 3000 kPa to 2000 kPa due to pressure drop as the fluid flows through the gap. The remainder of the channel is subjected to 2000 kPa static pressure. The model is also constrained at two nodes sufficiently far away from the critical regions of the geometry to prevent rigid body translation and rotation. The results of this simulation are shown in Fig. 42.

Table 7: Material parameters

Parameter	Silicon	Glass
Material Model	Elastic	Elastic
Modulus, E	140 GPa	70 GPa
Poisson's Ratio, ν	0.28	0.16
Conductivity, k	139 W/mk	1.14 W/mk
CTE, α	2.6 e^{-6}/ ^{o}C	3.8 e^{-6}/ ^{o}C

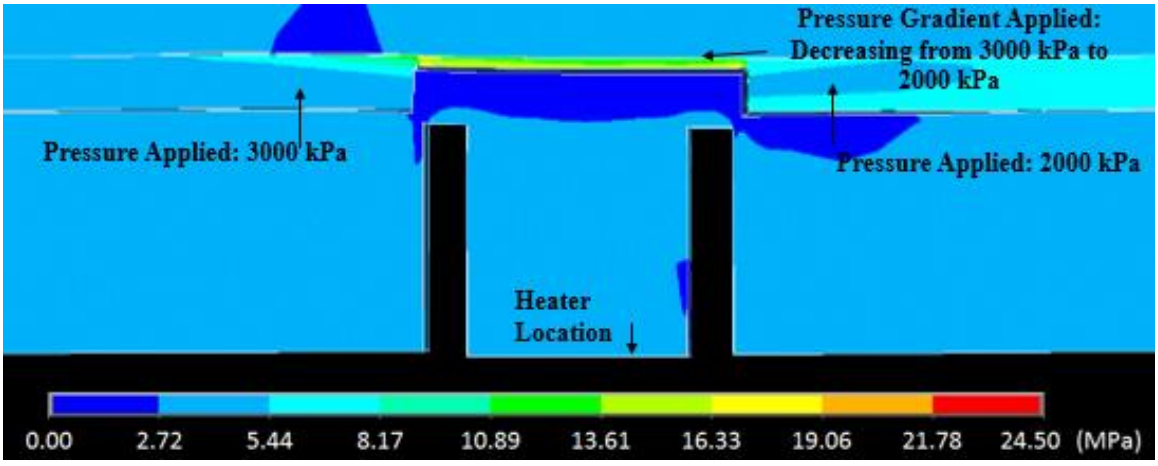


Fig. 42. First principal stress results for high pressure loading of 3000 kPa.

For this pairing of brittle materials, first principal stress is chosen as the critical stress value. The microgap itself experiences the highest principal stress of 24 MPa due to the high pressure drop across that section. A defect or crack size of approximately 300 μm would be required for fracture of these materials at such a low principal stress as the fracture toughness of silicon and glass is 0.8 and 1.0 MPa$\sqrt{\text{m}}$, respectively [81]. The introduction of the isolation air trenches in this configuration has negligible effect on the reliability of the system from a structural standpoint. Further parametric analysis may be performed to examine the limits on etch depth and width of this air trenches.

4.6 Conclusion

In this chapter, a hotspot cooler testbed for convective boiling experiments in extreme-microgap with integrated micropin-fins and isolation air trenches was designed, fabricated and tested. The maximum heat flux during testing reached up to 4.75 kW/cm^2 with flow rates ranging from 0.1 – 0.3 ml/min. A reduction in thermal resistance of approximately 3.5% was observed with the surface enhancement of the micropin-fins with a tradeoff of a large increase in pumping power resulting from the high constriction of the fluid flow. In addition, the reliability analysis showed that the device can sustain 3000 kPa pressure and 1000 kPa pressure drop across the microgap.

CHAPTER V

HETEROGENEOUS INTERCONNECT STITCHING TECHNOLOGY WITH COMPRESSIBLE MICROINTERCONNECTS FOR DENSE MULTI-DIE INTEGRATION

5.1 Introduction

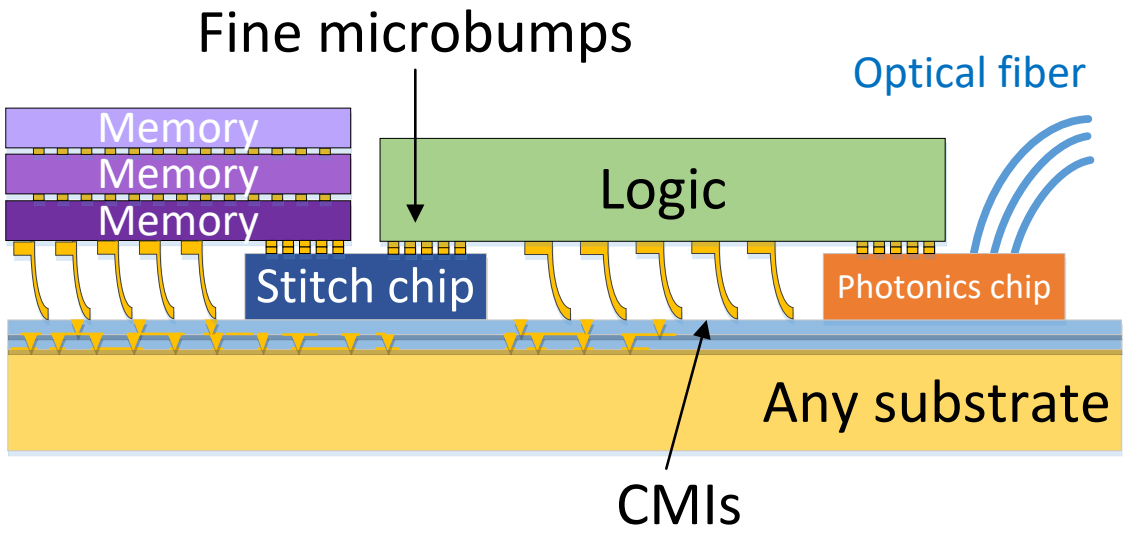
There is an ever increasing need to integrate multiple dice of various functionalities, including ASICs, CPUs, GPUs, FPGAs, microsensors, photonics, MEMS, and RF components into a single package [82], [83]. This need has spurred significant research in heterogeneous interconnection platforms, including silicon interposer (2.5D IC [10], [11]), Silicon-Less Interconnect Technology (SLIT) [41], embedded multi-die interconnect bridge (EMIB) technology [40], and chip stacking (3D IC [43], [44], [47]). Unfortunately, while each of the aforementioned solutions has benefits, they also have limitations, as noted in Table 3.

To avoid these shortcomings, we present a heterogeneous interconnect stitching technology platform to enable the interconnection of multiple dice (or "chiplets") of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. Figure 43 illustrates schematics of the HIST platforms. A stitch chip with high-density fine pitch wires is placed between the substrate and the chiplets. In Fig. 43 (a), fine-pitch microbumps are used to bond chiplets to the stitch chip to provide high-bandwidth density and low-

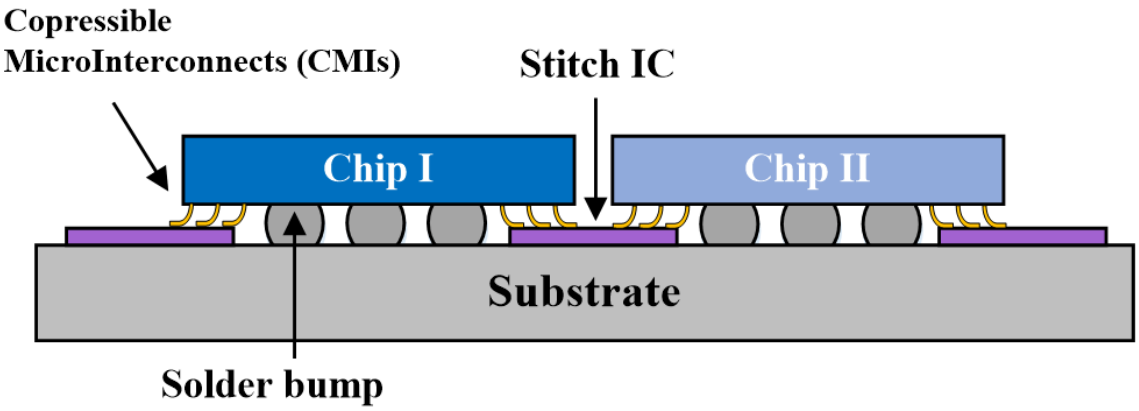
energy signaling. Compressible microinterconnects (CMIs) are used to compensate for package non-planarity and enable chiplet-package interconnection. CMIs are pressure-contact based interconnects designed to mate with a pad on the package substrate. An alternative solution is shown in Fig. 43 (b), where fine-pitch CMIs are used to bond chiplets to stitch chips and solder bumps are used to connect chiplets and package. Compared to competitive solutions, the advantages of HIST include the following: HIST achieves a similar signal bandwidth density as the silicon interposer technology [8], but is not reticle-size limited, thus making it very scalable in size; HIST eliminates the need for through-silicon-vias (TSVs) in the substrate for decreased cost and improved signaling [9]; HIST is based on die-to-die face-to-face bonding, and thus there are no intermediate package levels as in the case for EMIB (i.e., package buildup layers as the embedded silicon chips are buried within the package), which enables higher signal I/O pitch and lower capacitance; and lastly, HIST can be applied to any packaging substrate (organic, ceramic, etc) since HIST is augmented to the top-most surface of the package substrate. The presence of CMIs can also improve system mechanical reliability. In addition, the integration of silicon photonics is another promising application of HIST, as illustrated in Fig. 43.

In this chapter, two HIST testbeds are designed, fabricated and measured. The average post-assembly electrical resistance values of the fine-pitch microbumps, fine-pitch CMIs, coarse-pitch solder bumps and coarse-pitch CMIs are characterized as 0.117 mΩ, 145.38 mΩ, 1.31 mΩ and 195.99 mΩ, respectively. Vertical elastic deformation of up to 30 μm and 13 μm were characterized for fine-pitch and coarse-pitch CMIs, respectively. This chapter is organized as follows: Section 5.2 summarizes the design, fabrication

process and measurement of the HIST testbed with fine-pitch microbumps; Section 5.3 introduces the HIST testbed with fine-pitch CMIs; the electrical performance of HIST channels is modeled in Section 5.4, and conclusions are presented in Section 5.5.



(a)



(b)

Fig. 43. Schematics of HIST platform: (a) the solution with fine-pitch microbumps and (b) the solution with fine-pitch CMIs.

5.2 HIST Testbed with Fine-Pitch Microbumps

In this testbed, two dummy chiplets emulating active dice are assembled to a stitch chip and silicon substrate, as shown in Fig. 44. The stitch chip on the package substrate was emulated by a step-like structure that is approximately 40 μm in height. 20 μm and 10 μm pitch Cu-Au microbumps are used to bond the chiplets to the stitch chip. The microbumps are approximately 5 μm in height, including 3 μm of Cu and 2 μm of Au, as shown in Fig. 45. The gold-coated NiW alloy CMIs are approximately 55 μm in height, 20 μm in width at the tip, 200 μm in length, and are on a 200 μm pitch, as shown in Fig. 46 (a). Since CMIs are lithographically defined, they can be miniaturized. In this demonstration, the microbumps and CMIs are fabricated on the chiplets, as shown in Fig. 46 (b). However, the CMIs can be fabricated on substrate. In order to maximize the vertical elastic range of motion, an approximately tapered design is adopted to distribute the stress along the body of the CMI during deflection. The upward-curved profile of the CMI ensures that the tip of the CMI remains in contact with the mating pad during deflection.

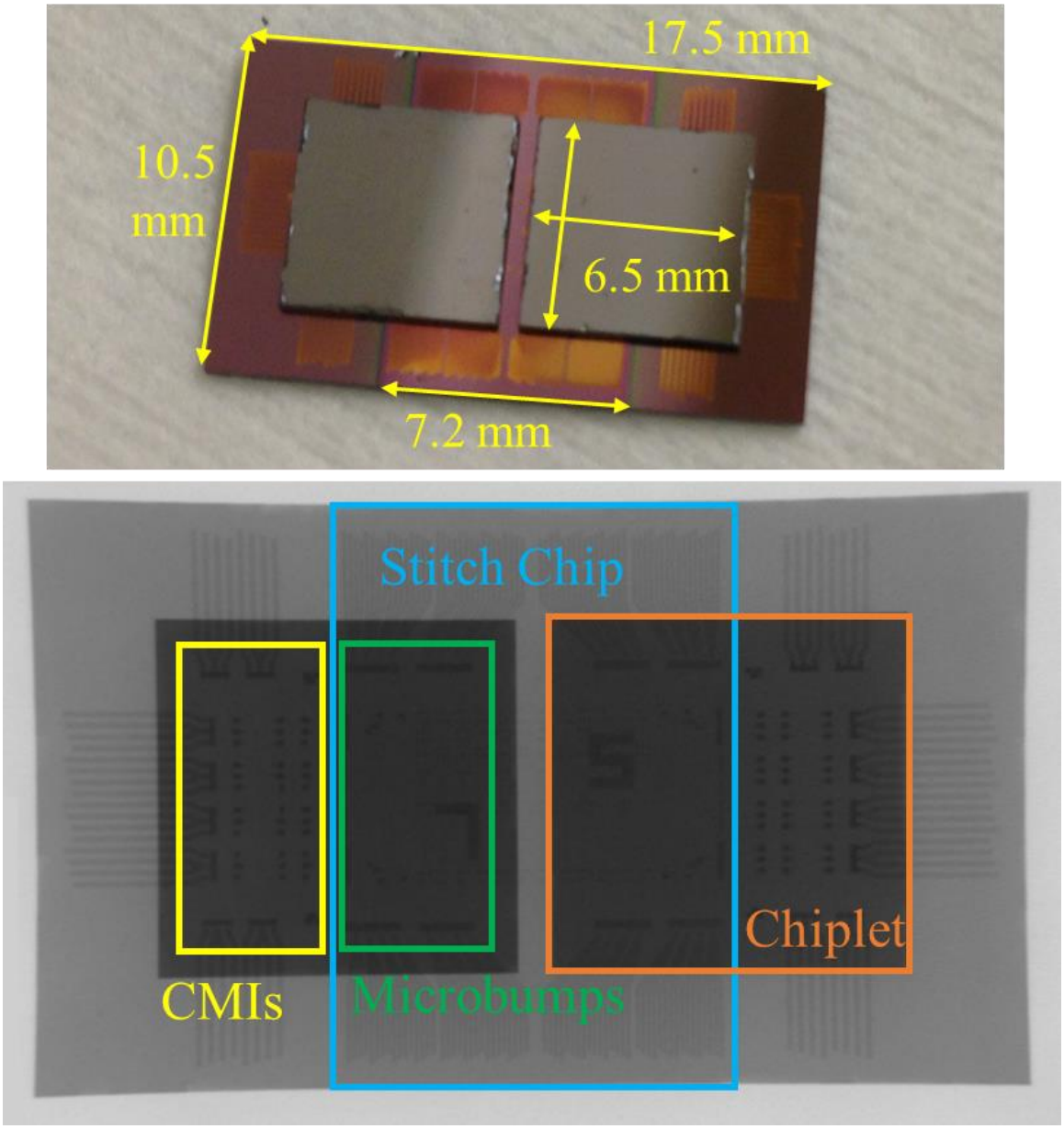
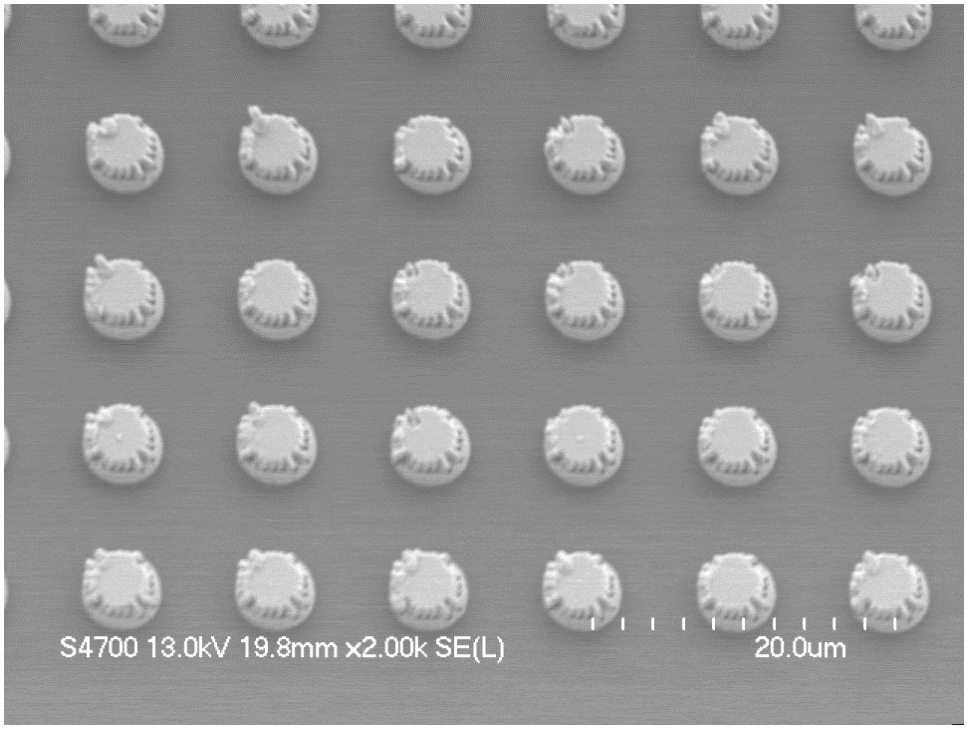
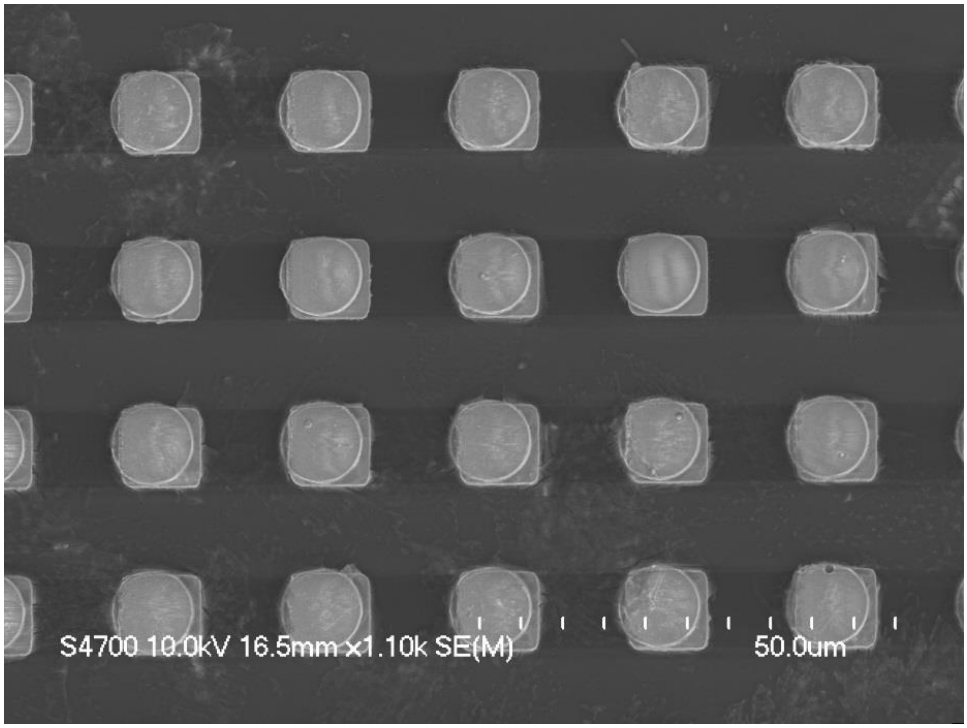


Fig. 44. Die micrograph and X-ray image of the HIST testbed.

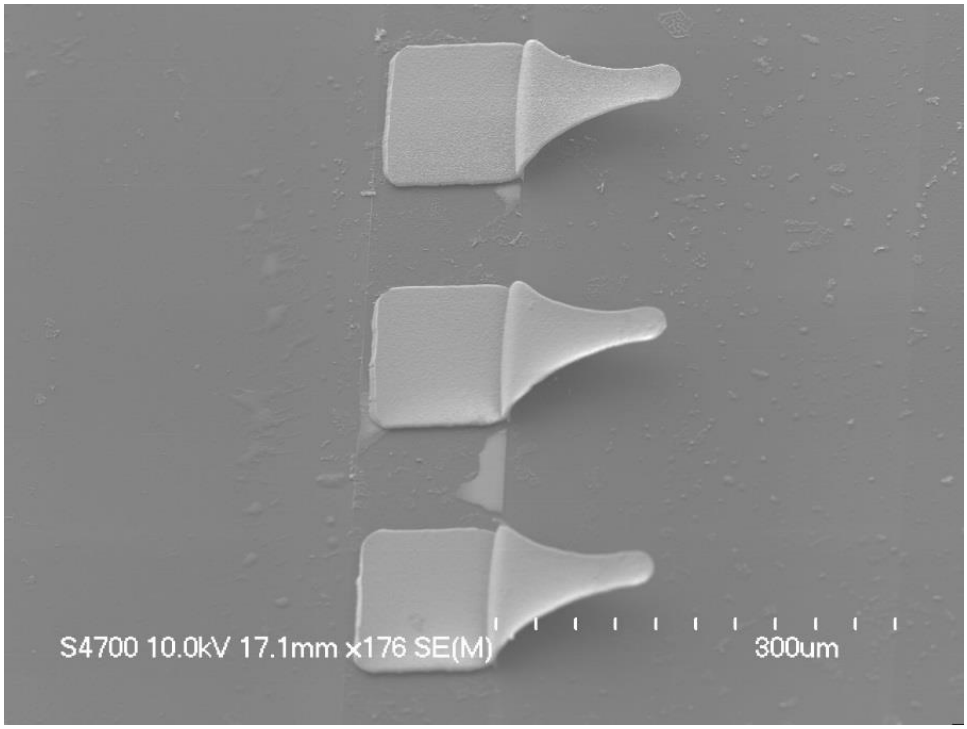


(a)

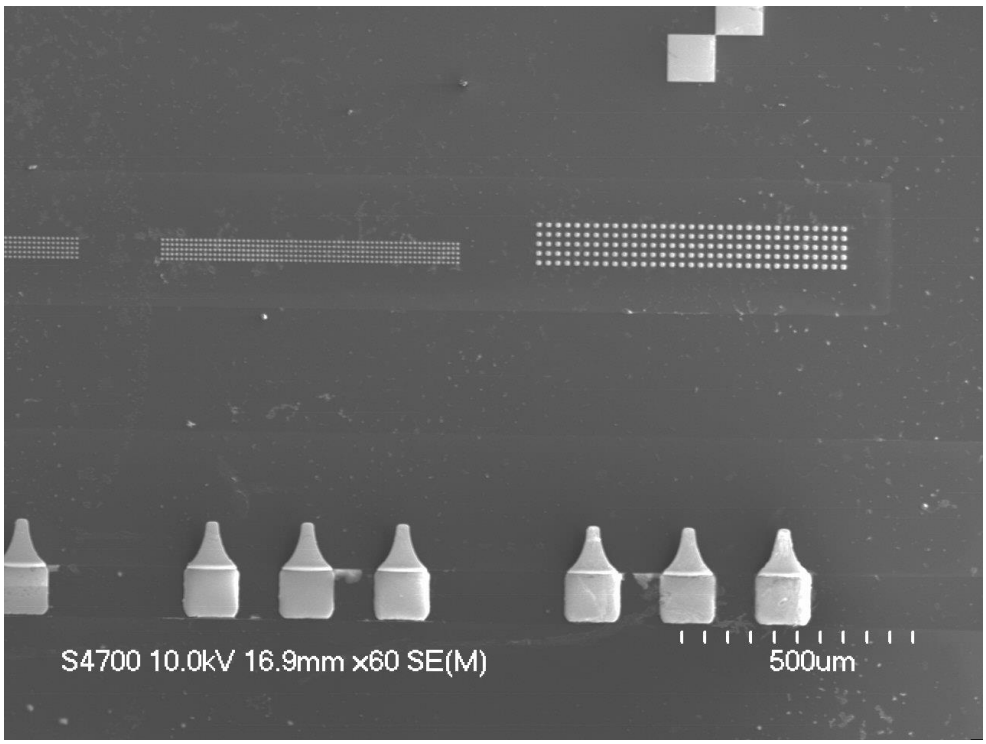


(b)

Fig. 45. SEM images of the microbumps: (a) 10 μm pitch and (b) 20 μm pitch.



(a)



(b)

Fig. 46. SEM images: (a) CMIs and (b) CMIs and microbumps on the chiplet.

The fabrication process of the dummy chiplets begins with depositing of the silicon nitride on the 300 μm thick silicon wafer with PECVD. Next, the wires and the first layer of microbumps are patterned with a Cu lift-off process, followed by an Au lift-off process to fabricate the second layer of microbumps. After the microbumps are fabricated, a thick sacrificial photoresist layer, which height determines the height of CMIs, is spin coated onto the surface. During lithography step, a upward curved sidewall is patterned in order to form the compressible CMI body. A Ti/Cu/Ti seed layer with thickness of 50 nm/300 nm/30 nm is deposited using sputterer followed by spray coating of a 10 μm thick photoresist layer to make the electroplating molds. After patterning the electroplating molds, NiW is electroplated in the mold to constitute the CMIs. NiW is used to form the CMIs since NiW has higher yield strength compared with Cu. After electroplating, the spray coated photoresist layer, the Ti/Cu/Ti seed layer, and the sacrificial photoresist layer are removed in consecutive order leaving free-standing CMIs. Lastly, a thin gold layer is deposited on CMI surfaces by electroless gold plating; the gold layer prevents the oxidation and enhances the electrical performance of NiW.

The stitch chip is emulated by a step-like structure on the silicon substrate formed by a Bosch etching process. Next, a silicon dioxide isolation layer is deposited on the stitch chip and the substrate, followed by a Cu-Au lift-off process to fabricate the kelvin resistance measurement structures and metal pads. Finally, the chips are diced with an in-house dicing saw. The overall fabrication process is shown in Fig. 47.

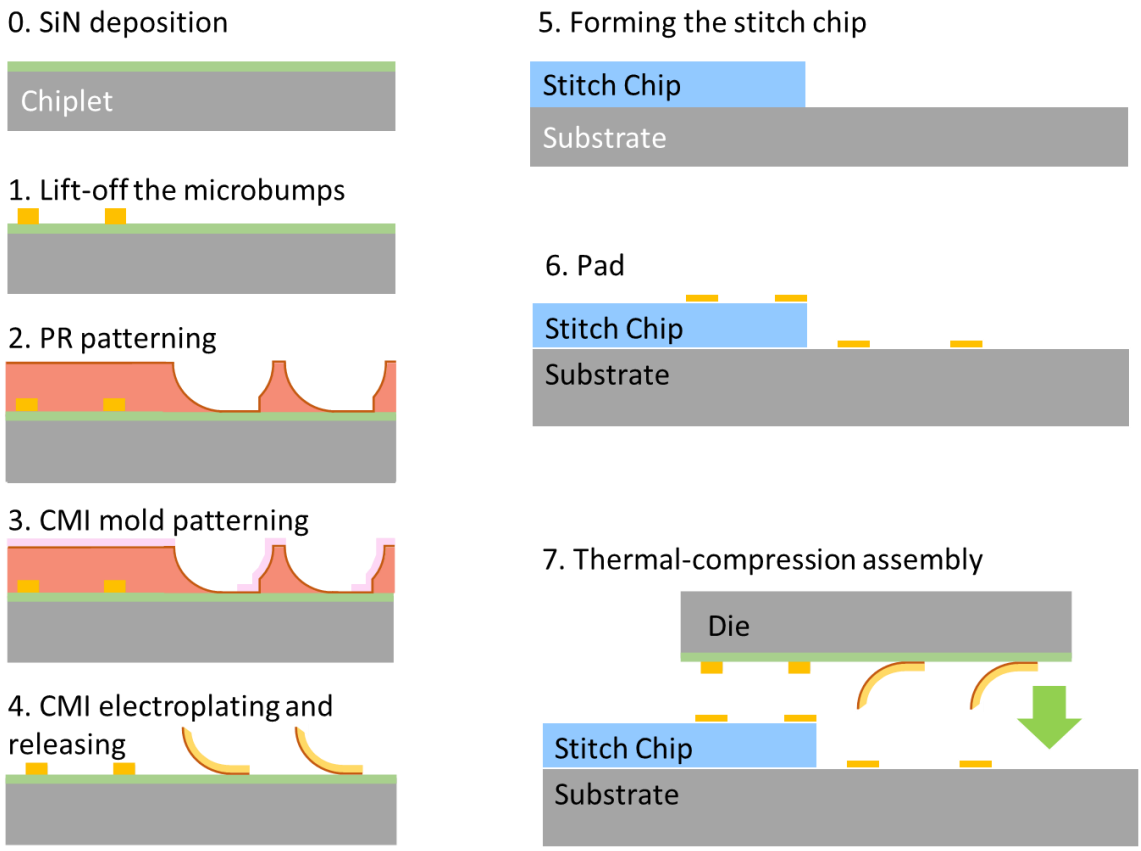
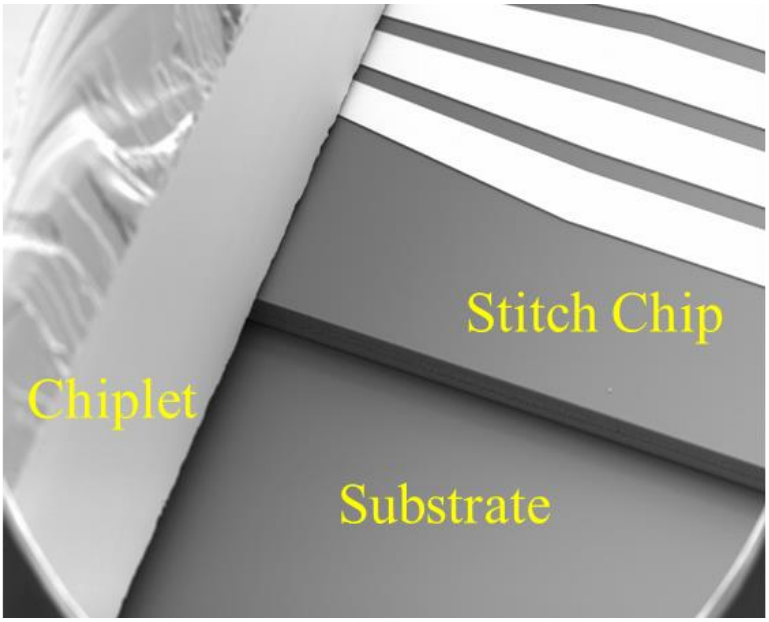


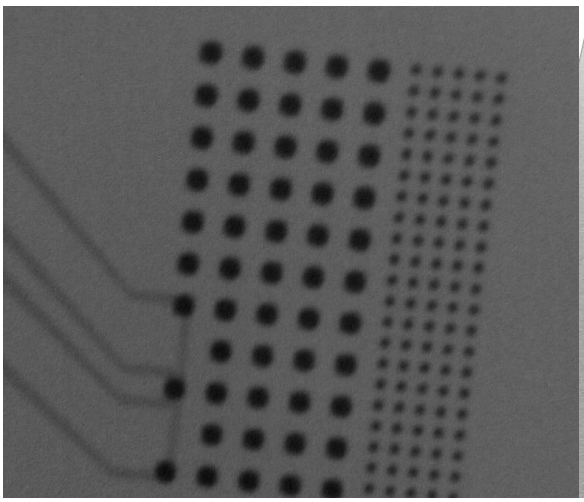
Fig. 47. Overall fabrication process of the HIST testbed.

The chiplets were assembled with a Finetech Fineplacer Lambda flip-chip bonder using a thermal compression process. A force of 5 N was applied during bonding with a maximum temperature of 300 °C. SEM and x-ray images of the assembled chiplets are shown in Fig. 48. As shown in the SEM image, part of the chiplet is bonded to the stitch chip, while the rest of the chiplet is suspended above the substrate and supported by the CMIs. Note that the CMIs traverse the height of the stitch chip that is "sandwiched" between the package substrate and the chiplets to provide the needed electrical interconnection to the package substrate (power delivery and other signaling needs). For testing purposes, approximately half of the chiplet area is occupied by microbumps to support high density interconnects to the stitch chip, while the other half is occupied by

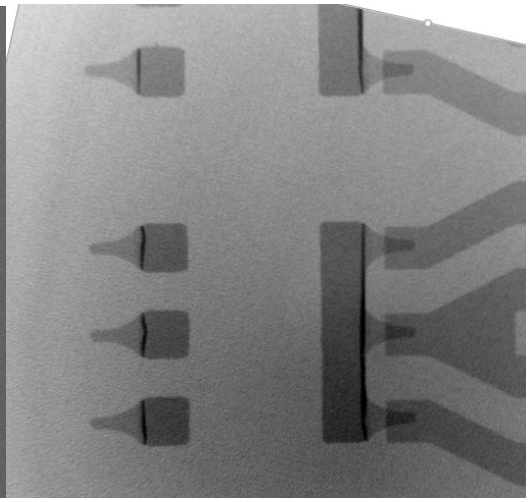
CMIs that interconnect to the package substrate. In this testbed, the dice are not underfilled. However, technologies for applying underfill within the small gap and the high-density microbumps have been demonstrated in [84] and may be used when needed.



(a)

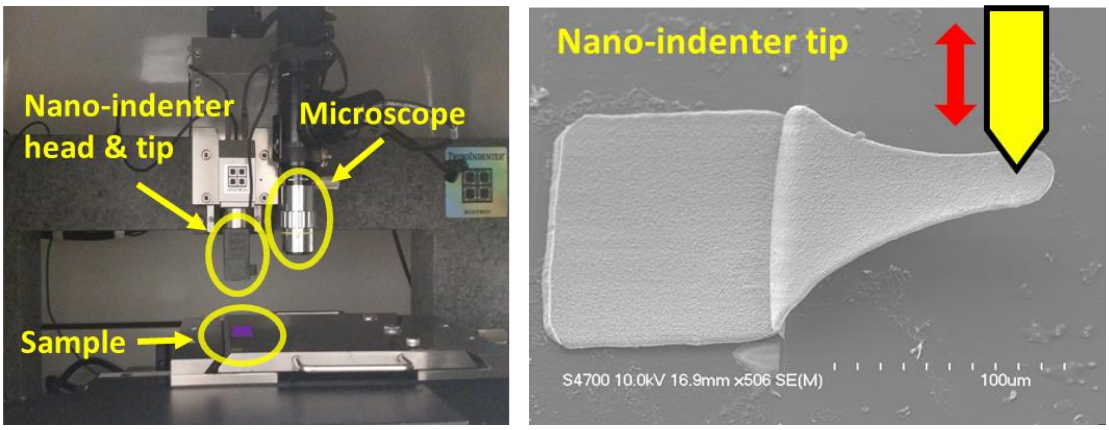


(b)

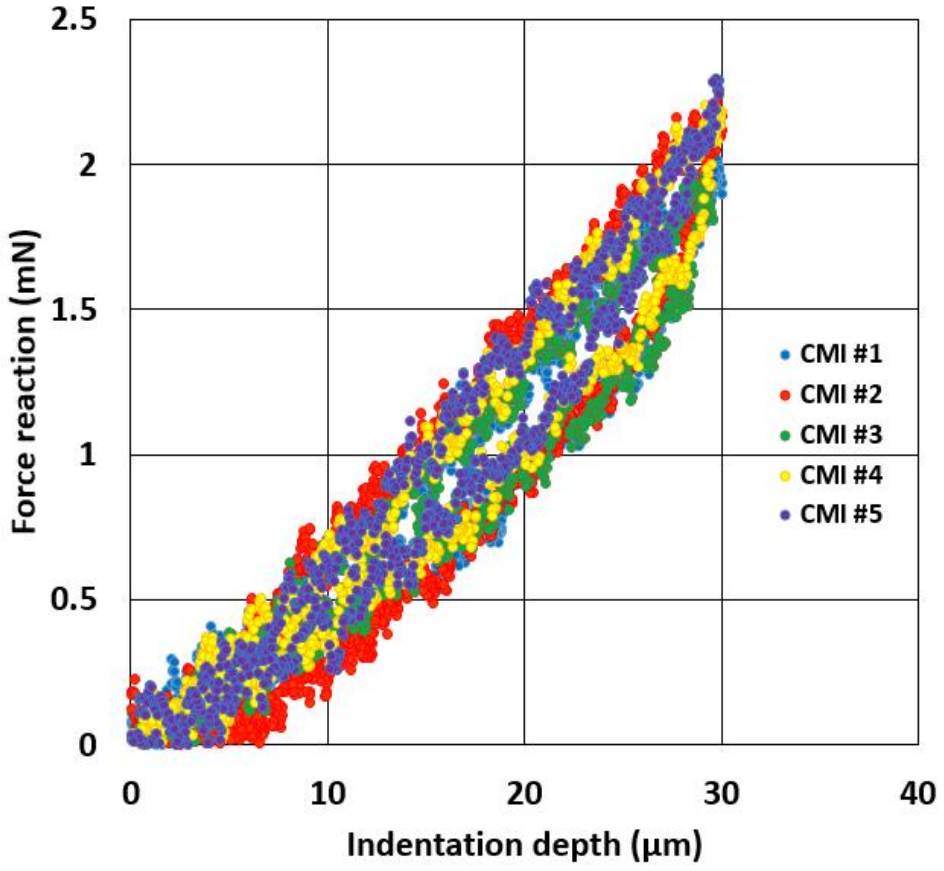


(c)

Fig. 48. SEM and x-ray images of the assembled testbed: (a) SEM image showing the edge of the stitch chip (b) x-ray image of the microbumps and (c) x-ray image of the CMIs.



(a)



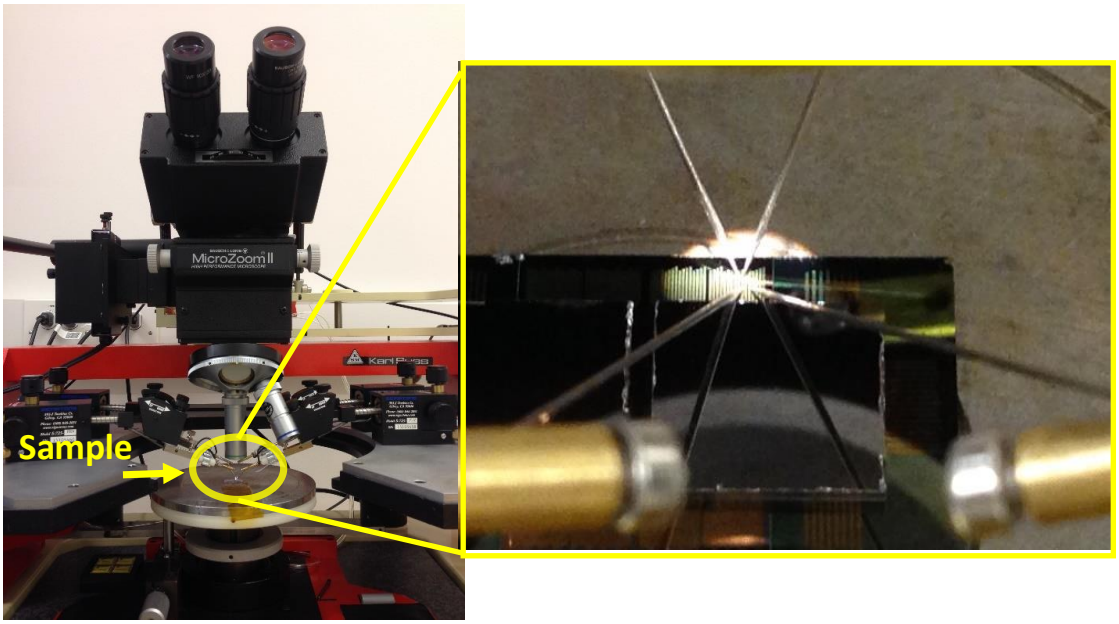
(b)

Fig. 49. CMI indentation measurement: (a) testing setup and (b) result.

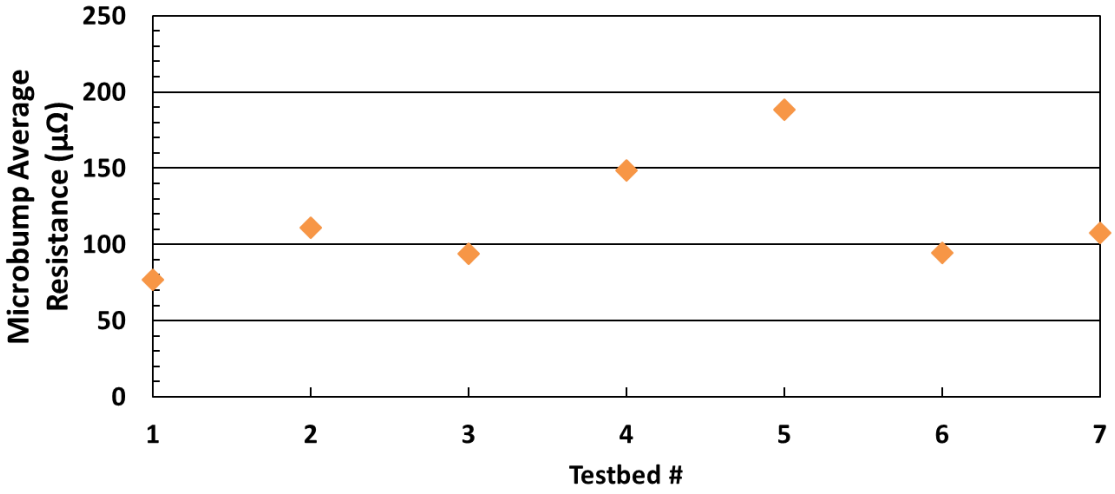
Mechanical compliance is a key property of the CMI and was measured using a Hysistron Triboindenter, as shown in Fig. 49. Five CMIs located at different regions of the

chiplets were measured, and the results are shown in Fig. 49. The indentation results show that the mechanical compliance is approximately 13.7 mm/N, and CMIs can achieve up to 30 μm of vertical elastic deformation.

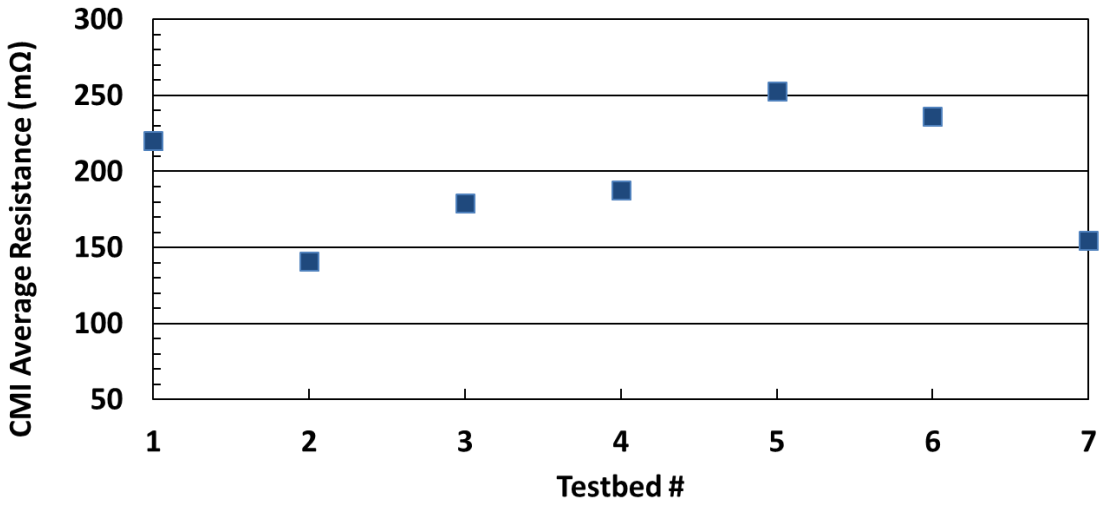
The post-assembly resistance values of the 20-μm pitch microbumps and the CMIs is measured with Kelvin resistance structures. A Keithley 2182A voltmeter and a Keithley 6220 current source are used to perform the measurement with a Karl-Suss probe station, as shown in Fig. 50. The resistance of the microbumps ranges from 77.8 μΩ to 188.3 μΩ. The cause of the data variation is the misalignment of the assembled testbeds due to limits of our in-house flip-chip bonder. The resistance of the CMIs (including contact resistance) ranges from 141.2 mΩ to 252.9 mΩ. The current carrying capability of flexible interconnects of similar materials and approximate dimensions has been demonstrated to be up to 1 A [85]. Simulations using ANSYS HFSS show that the insertion loss of the CMIs is approximately 0.26 dB at 20 GHz. This value is significantly lower than the loss of TSVs [10], [86]. The inductance (extracted from the simulated S-parameters at 1 GHz) of the CMIs is approximately 156 pH. The size of the CMIs can be decreased since they are lithographically-defined, which will further decrease the loss and inductance.


MicroZoom II
Sample

(a)


Microbump Average Resistance (µΩ)
250
200
150
100
50
0
1
2
3
4
5
6
7
Testbed #

(b)

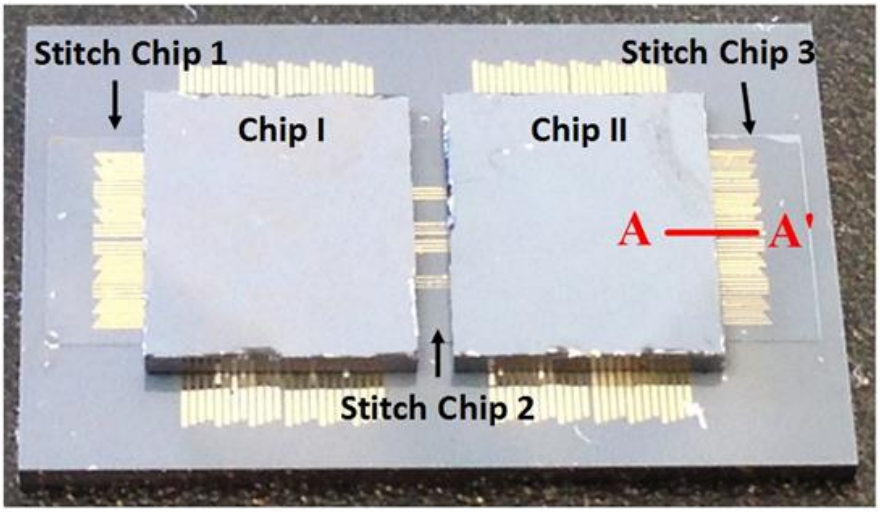


(c)

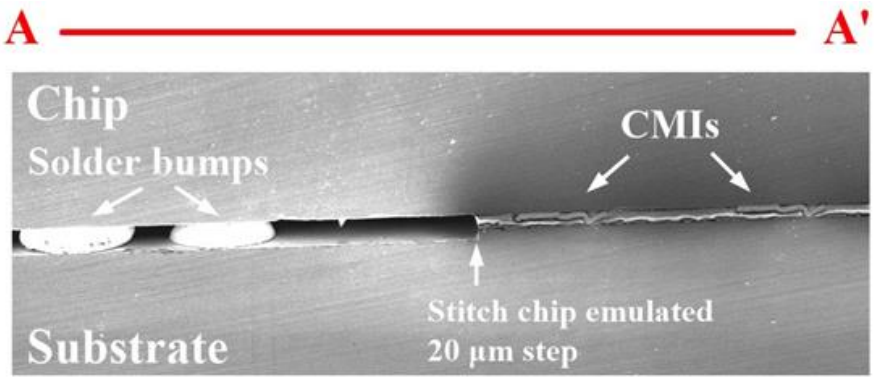
Fig. 50. Kelvin resistance measurement: (a) testing setup, (b) microbump resistance values and (c) CMI resistance values.

5.3 HIST Testbed with Fine-Pitch CMIs

In this testbed, two dummy chiplets emulating active dice are assembled to a silicon substrate with three stitch chips, as shown in Fig. 51. Fine-pitch (as small as 20 μm) flexible and elastically deformable CMIs are used to interface the dense signaling paths on the stitch chips to the bonding pads on the chiplet. Solder bumps are used to bond the chiplets to the package substrate while providing electrical interconnections (power delivery and signaling) as well as mechanical bonding. The solder bumps are approximately 50 μm in height and 200 μm in pitch while the lithographically-defined CMIs are approximately 40 μm in height and are formed on a 20 μm in-line pitch, as shown in Fig. 52.

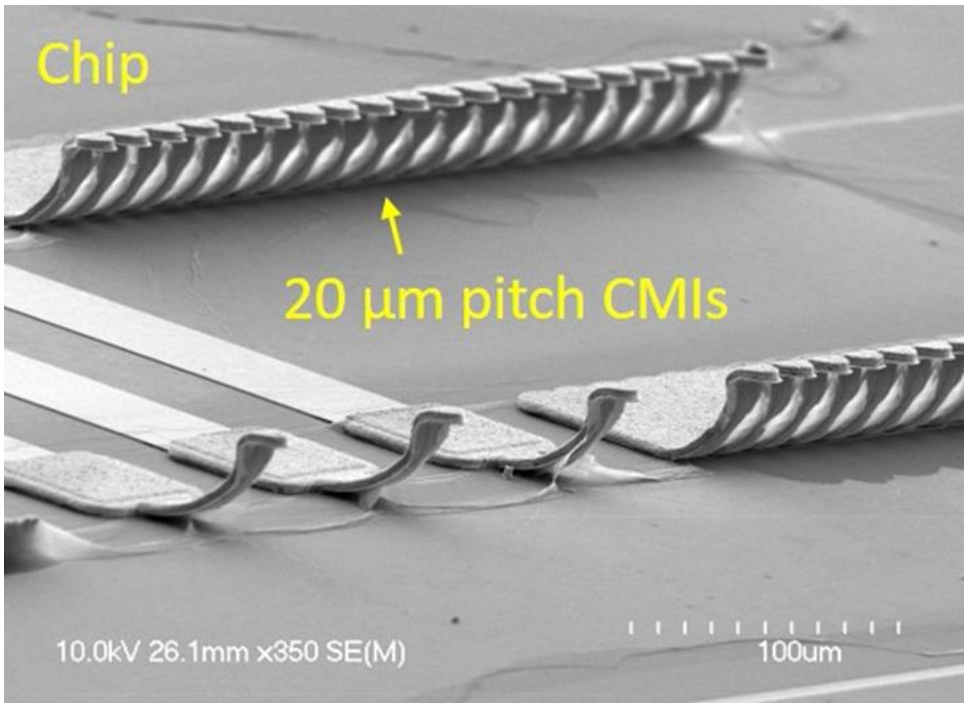


(a)

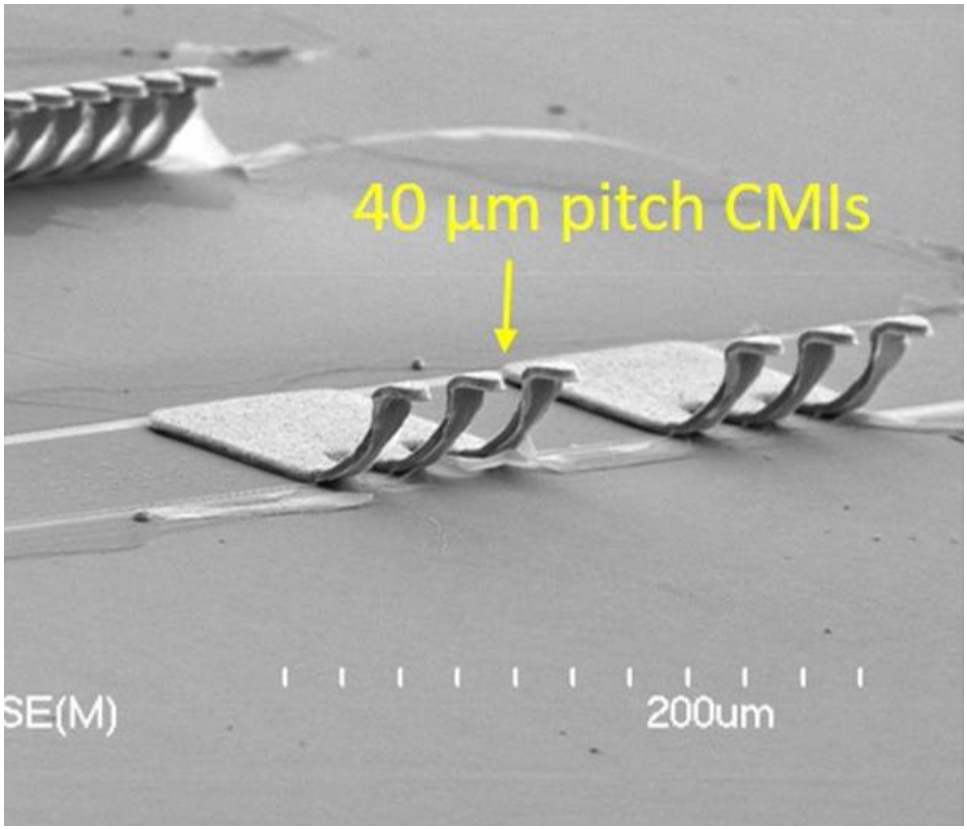


(b)

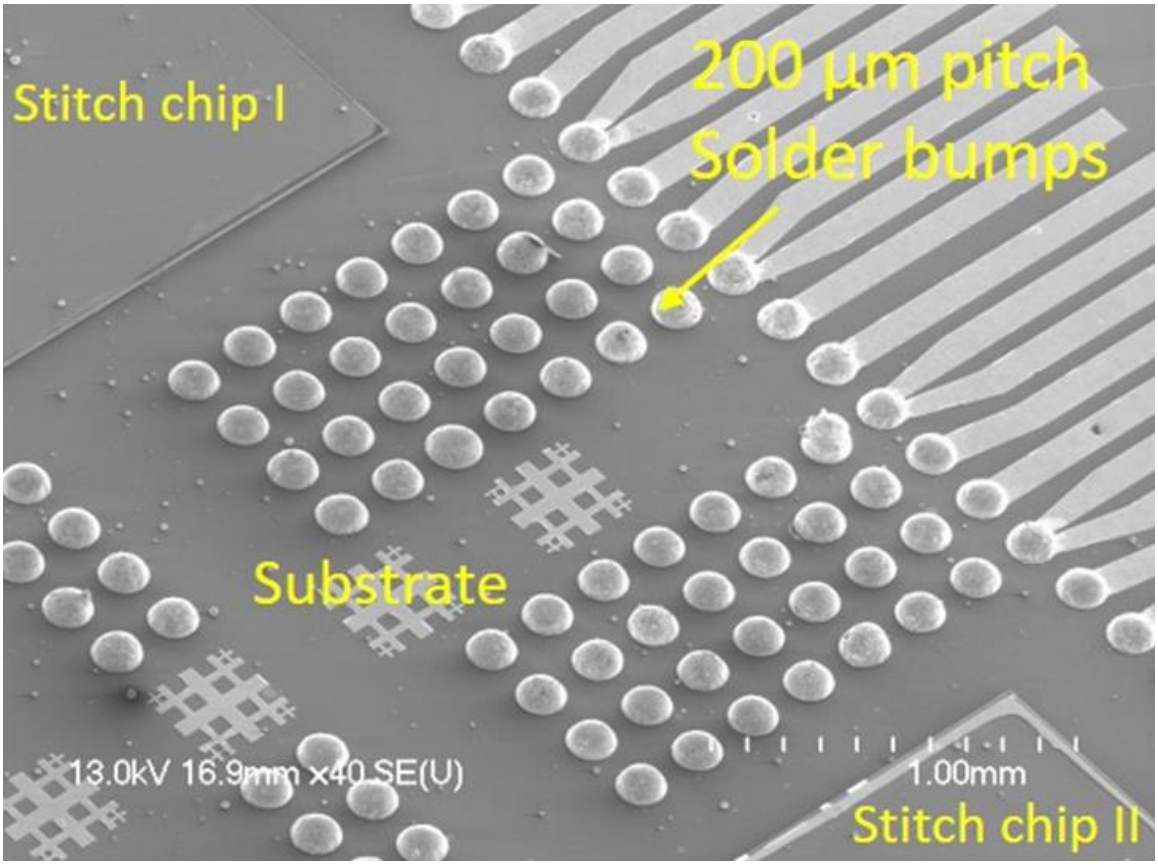
Fig. 51. Image of the HIST testbed: (a) Die micrograph (b) SEM image of the cross-section.


Chip
20 µm pitch CMIs
10.0kV 26.1mm x350 SE(M)
100um

(a)


40 µm pitch CMIs
SE(M)
200um

(b)



(c)

Fig. 52. SEM images of the testbed: (a) 20 µm pitch CMIs, (b) 40 µm pitch CMIs, and (c) the substrate with 200 µm pitch solder bump and stitch chips.

The advantages of CMIs are their ability to mechanically compensate for surface non-planarity and stitch chip thickness variations, as a single active die may be interfaced to multiple stitch chips (of different functions) on its four edges. The reasons CMIs are used instead of fine-pitch solder bumps for the interface include: a) CMIs do not suffer from solder shorting as pitch is scaled as they are a pressure-based interconnection; b) owing to their mechanical flexibility, the restrictions on stitch chip thickness uniformity can be decreased which is expected to improve assembly yield, and c) we eliminate the

need for strict uniformity control on microbump thickness, which eases fabrication constraints.

The overall integration process flow is shown in Fig. 53. The integration process begins with fabricating wires and solder bumps on the package substrate. The Cu-Au wires are fabricated using a lift-off process and the solder bumps are electro-plated. Next, the stitch chips with fine-pitch gold coated Ni-W alloy CMIs are batch fabricated and assembled on the package substrate. Finally, the active dice are flip-chip bonded to the package substrate. In this demonstration, the stitch chips on the package are emulated by a 20 μm tall step (though larger step is possible) and the CMIs are fabricated on the assembled chiplets. A tapered CMI design is adopted in order to distribute the stress along the body during deflection; this can increase the vertical elastic range of motion. The upward-curved CMI design ensures that the tip of the CMI remains in contact with the receiving pad during deflection.

Optical and SEM images of the assembled testbed are shown in Fig. 51 and Fig. 54. The chiplets are assembled with a Finetech Fineplacer Lambda flip-chip bonder. The two chiplets in Fig. 51 are placed side-by-side onto the three stitch regions and the substrate. The center of the chiplet is bonded to the substrate using solder bumps, while two edges of the chiplet are suspended above the steps (i.e., the stitch chips) and supported by the fine-pitched CMIs. As shown in Fig. 54 (b), the CMIs are compressed downward during assembly and form a pressure-based contact with the substrate.

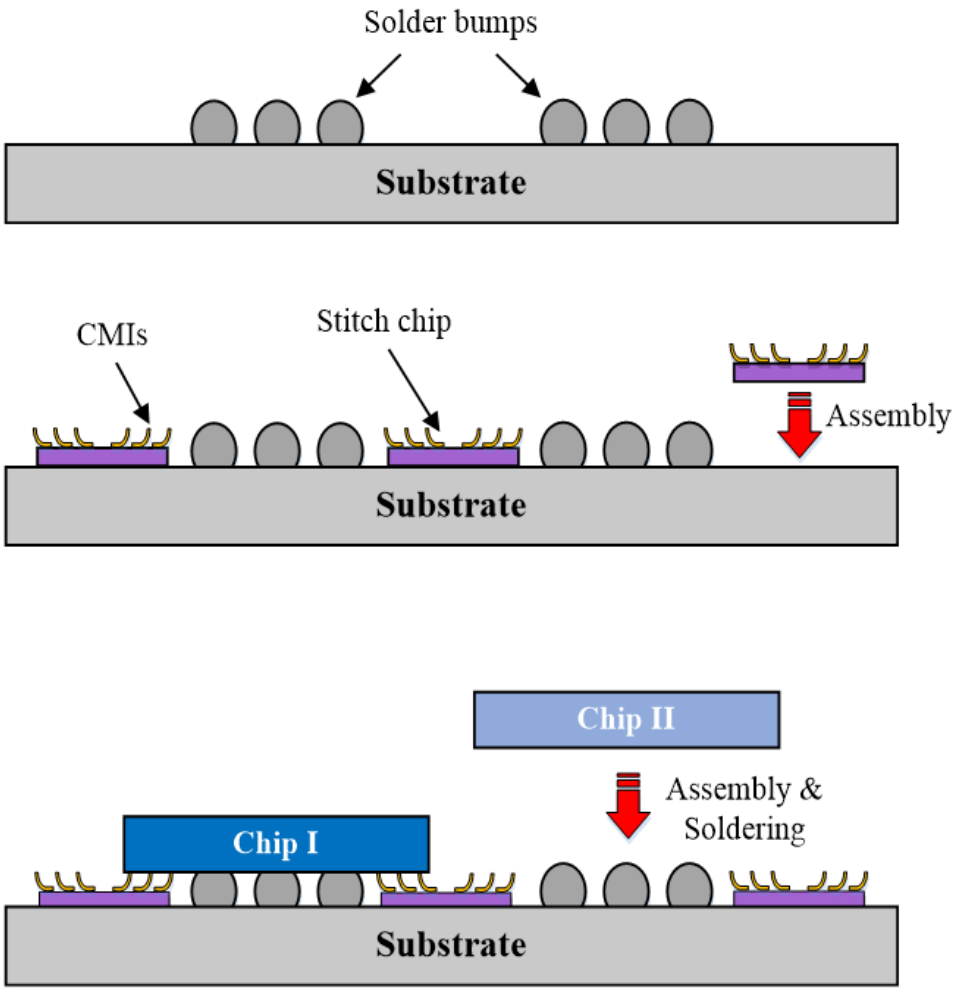
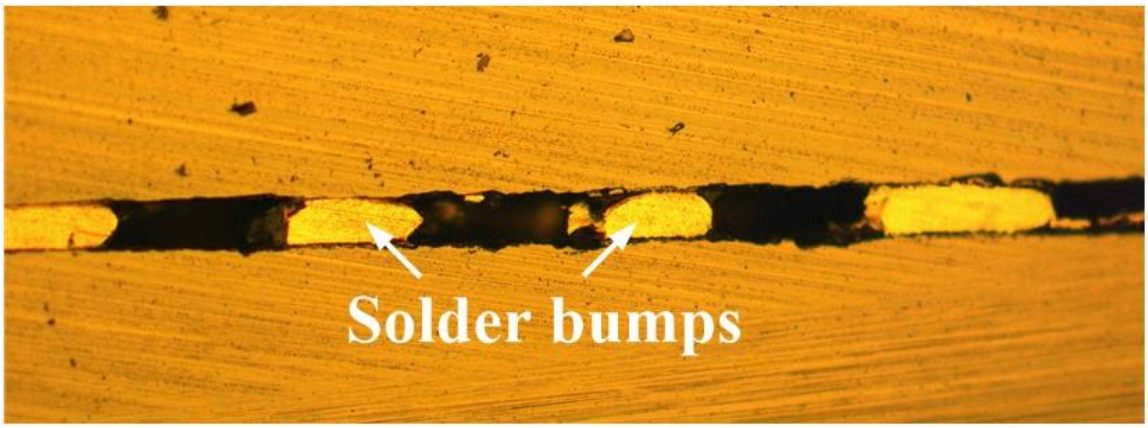
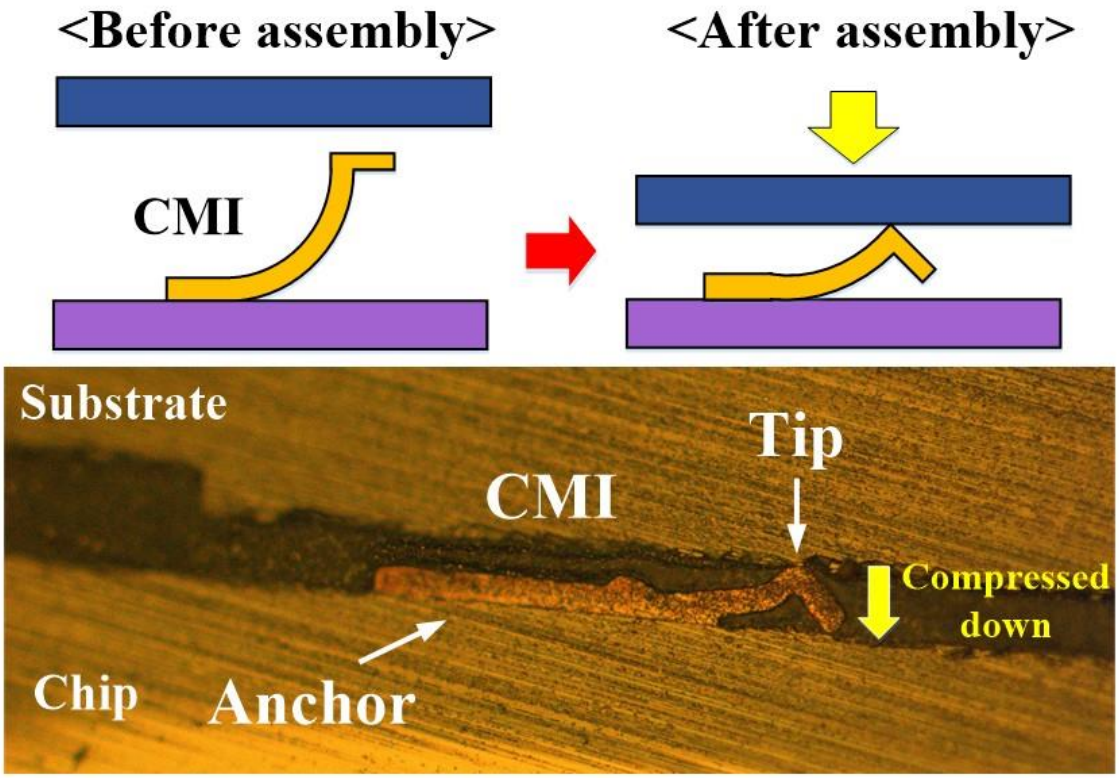


Fig. 53. The overall integration process flow.



(a)



(b)

Fig. 54. Microscope cross-sectional images of (a) solder bumps and (b) CMI.

Mechanical compliance, a key property of CMIs, is measured using a Hysistron Triboindenter. Three CMIs fabricated on different regions of the chip were indented; in each indentation cycle, the nano-indenter tip moves downward and then upward while measuring the reaction force from the CMIs. The indentation results show that the compliance is approximately 3.47 mm/N, and the CMIs can achieve up to 13 μm of vertical elastic range, as shown in Fig. 55. The post-assembly resistance measurements of the solder bumps and the CMIs are captured using a Karl-Suss probe station, and the results are shown in Fig. 56. The average resistance of the solder bumps is 1.31 mΩ, and the resistance of the CMIs, including contact resistance, is 145.38 mΩ.

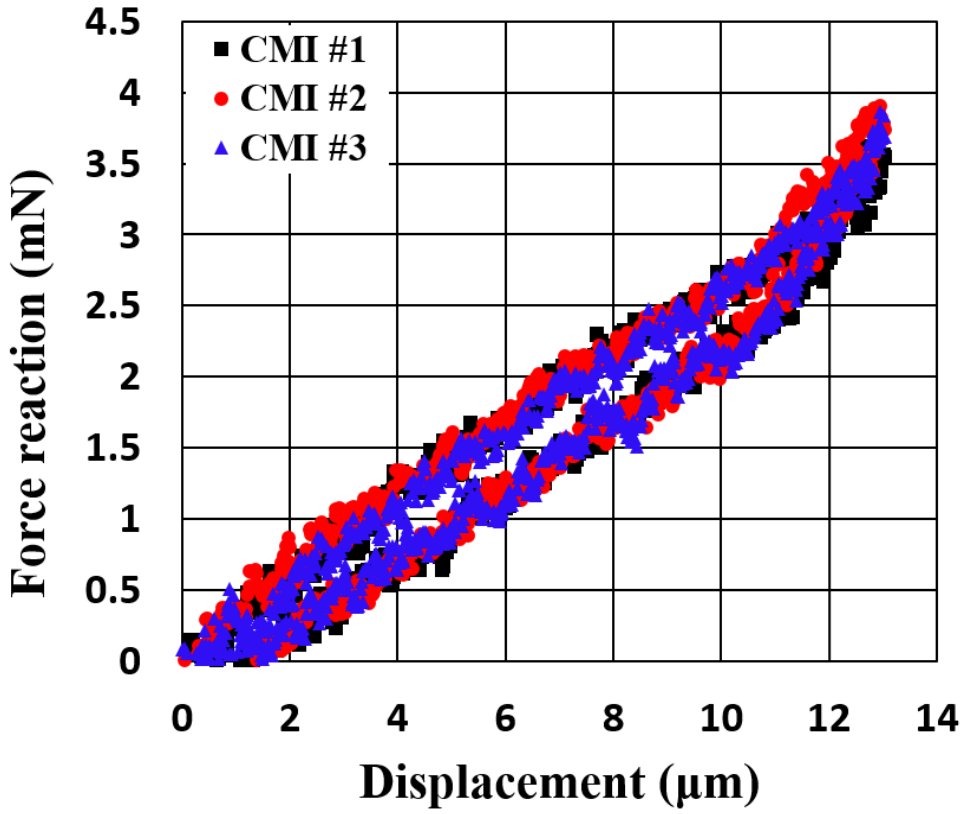
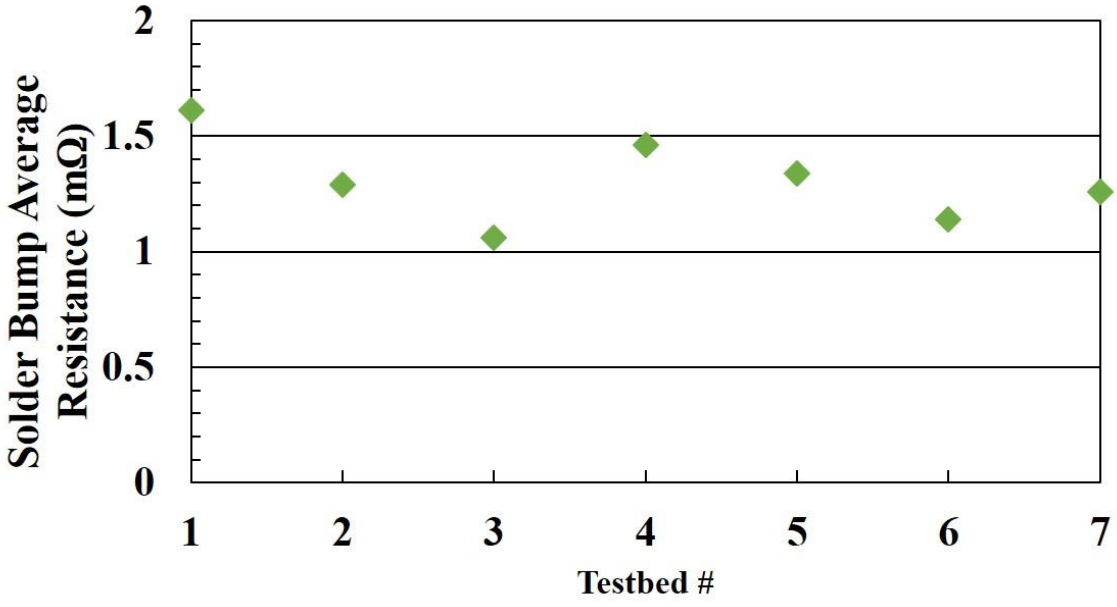
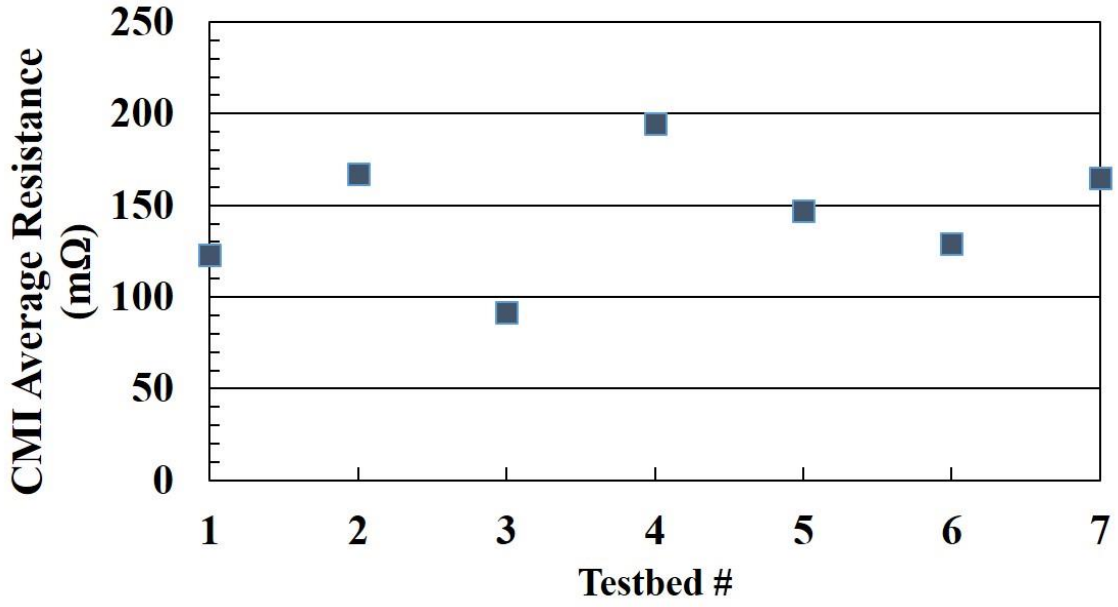


Fig. 55. CMI compliance measurement results.



(a)



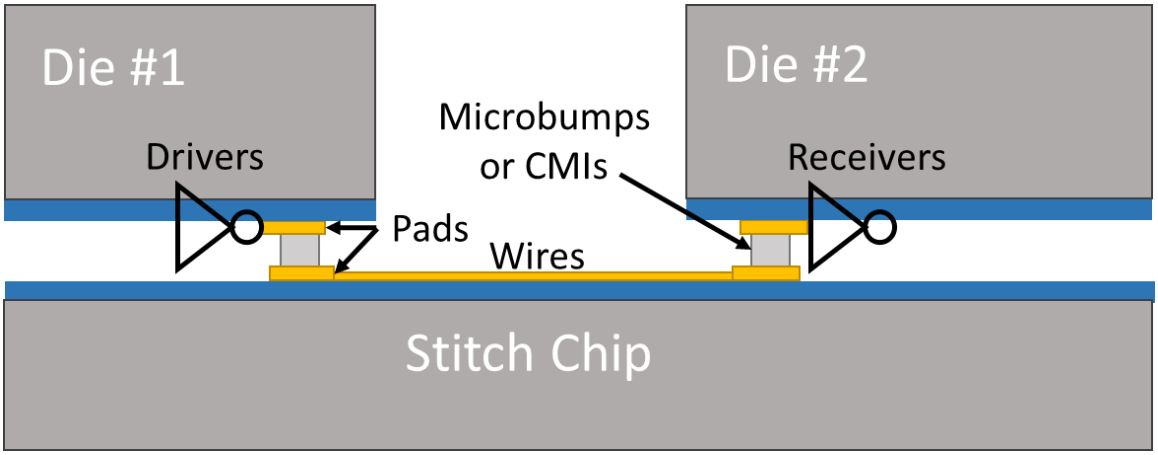
(b)

Fig. 56. Kelvin resistance measurement results.

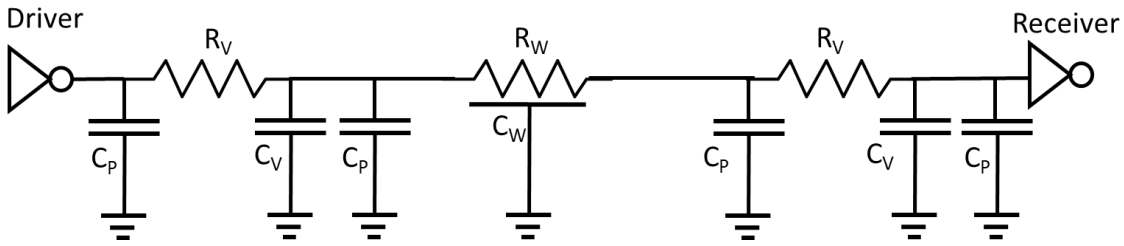
5.4 Modeling of HIST Channels for Digital Applications

A simple HIST channel consisting of input/output (I/O) drivers and receivers, microbumps/CMIs and horizontal wire is shown in Fig. 57 (a). The equivalent circuit model for the 3D link is shown in Fig. 57 (b). where C_P is the pad capacitance; R_V and C_V are the vertical interconnect (e.g. microbump or CMI) resistance and capacitance, respectively. R_W, and C_W are the p.u.l. resistance and capacitance of the wires on the stitch chip. Synopsys HSPICE was used to simulate the signal delay and energy efficiency of the HIST channel. The device models were from PTM 45 nm HP library [87] and the wire specifications were from FreePDK45 [88] top global wire models. The parameters investigated and the equations used are summarized in Table 8 and Table 9, respectively. In this model, CMIs are emulated by cylindrical conductors for simplicity. Multiple driver

stages with a constant fan-out of 4 (FO4) between stages were selected in this design [89]. Energy-delay-product (EDP) was used to optimize the number of driver stages [90].



(a)



(b)

Fig. 57. Schematic of a simple HIST channel (a) and its equivalent circuit model (b).

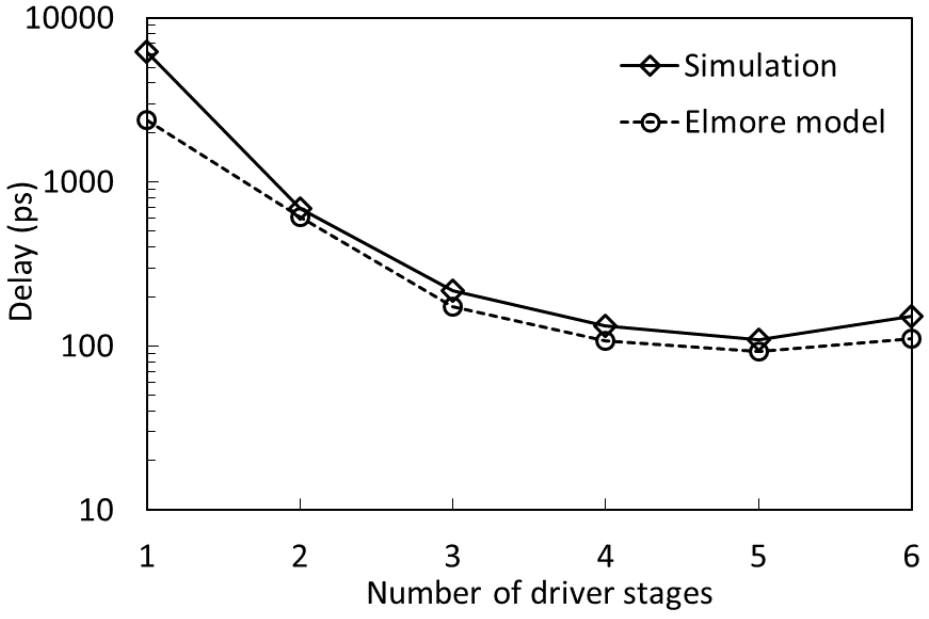
Table 8: Parameters used in simulation

Parameter	Values
Wire length (mm)	0.2, 0.5, 1, 2, 5
Wire pitch (µm)	1.6
Pad width (µm)	5, 10, 20, 50
Microbump diameter/height (µm)	0.8*pad width
Driver stages	1-5

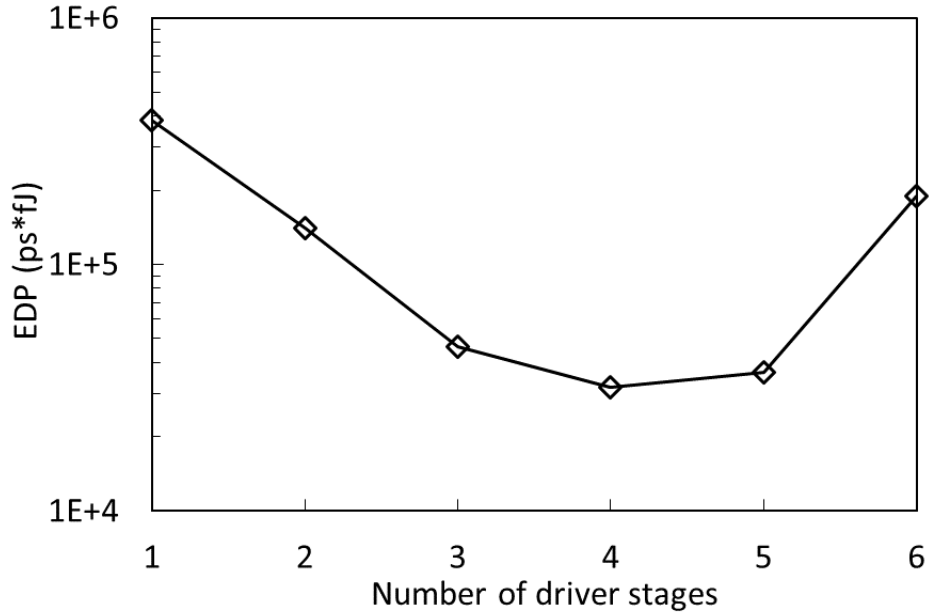
Table 9: Equations used in the simulation

Component	Equation
Pad capacitance: C_P [15]	$C_P = \varepsilon_0 \varepsilon_r \frac{W_P^2}{t_{ox}}$ (23) where W_P is the pad width and t_{ox} is the dielectric layer thickness.
Microbump resistance: R_V	$R_V = \rho \frac{H_{bump}}{\pi R_{bump}^2}$ (24) where H_{bump} is the microbump height and R_{bump} is the microbump radius.
Microbump capacitance: C_V [15], [18]	$C_V = \varepsilon_0 \varepsilon_r \frac{2\pi H_{bump}}{arcosh(\frac{P_{bump}}{2R_{bump}})}$ (25) where P_{bump} is the microbump pitch.

Figure 58 shows the performance of a 1 mm long HIST channel with different number of driver stages. The delay values from simulation is compared with Elmore delay model [58] and have a good agreement, as shown in Fig. 58 (a). The EDP values are shown in Fig. 58 (b). In this scenario, four stage drivers have the minimum EDP and thus are considered as the optimal design.



(a)

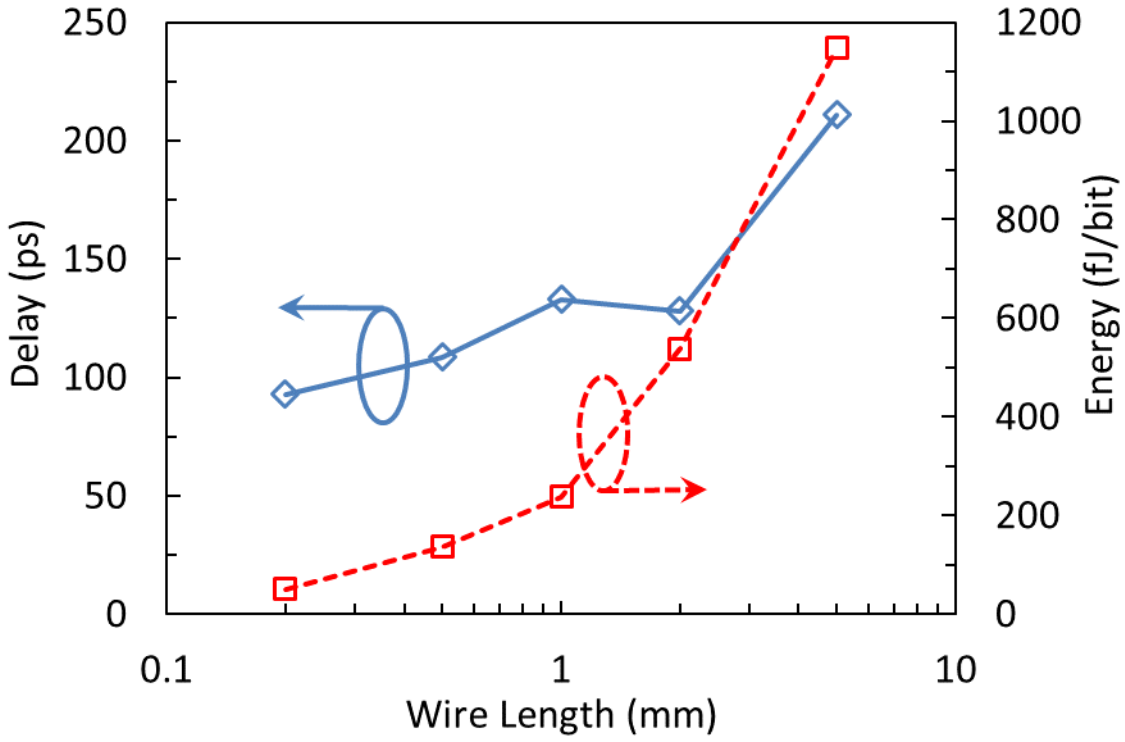


(b)

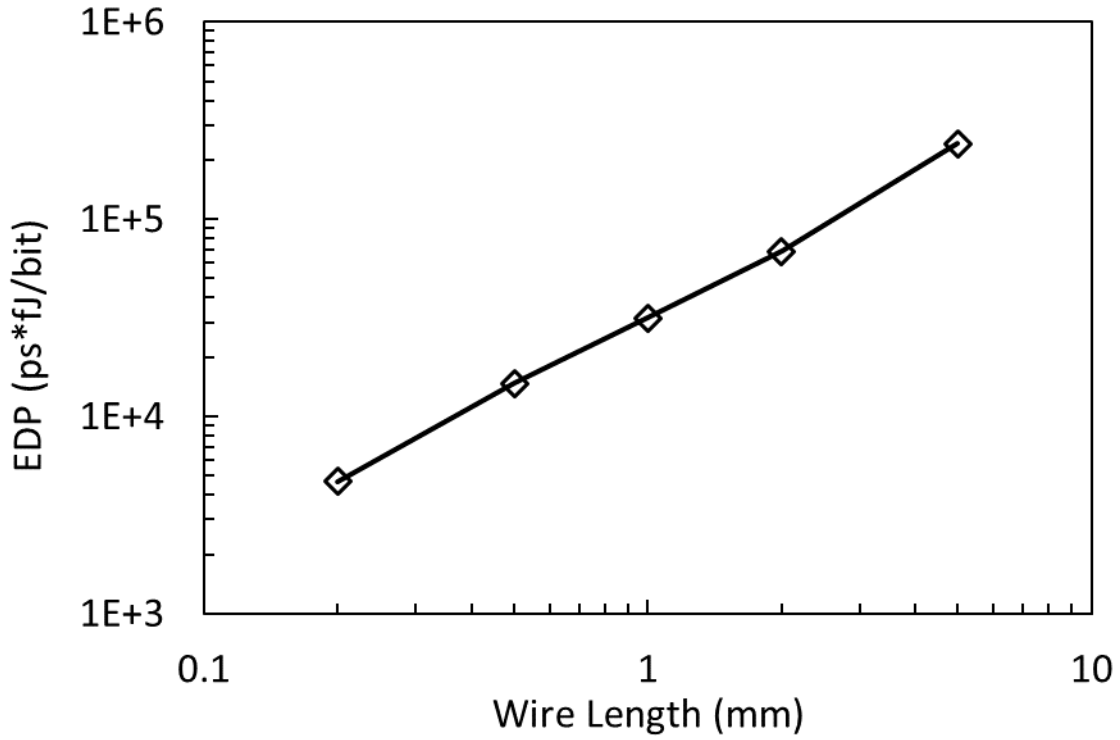
Fig. 58. Performance of a typical 1-mm HIST channel with different number of driver stages: (a) Delay and (b) EDP.

The 50%-50% delay and energy-per-bit (EPB) of optimized HIST channels with a wide range of wire lengths are shown in Fig. 59 (a). A clear trade-off between the signal performance and wire length can be observed. Note that the delay of 2-mm channel is smaller than the 1-mm channel. This is because the optimal driver design for 2-mm channel has one more stage than the 1-mm channel. Thus, the delay is decreased at a cost of much higher EPB, as shown Fig. 59 (b). Figure 59 also shows a wide range of possible selections of channel length and data rate options. For example, if the operating signal frequency needs to be lower than $(10*\text{delay})^{-1}$ to accommodate the timing jitter in the system, the typical 1-mm long HIST channel can support up to 1.5 Gbps data rate with double-data-rate at a EPB of 0.24 pJ/bit. The aggregate bandwidth density in this scenario is up to 9.3

Tbps/cm. Alternatively, if low data rate signaling was selected for lower I/O power, the bandwidth density of HIST can achieve up to 1.25 Tbps/cm with 200 Mbps data rate as in the case of silicon interposer [11]. As the trade-off between the EPB and the channel length is more significant for longer wires, it is less appealing to design HIST channels longer than 2 mm.



(a)



(b)

Fig. 59. Performance of the optimized HIST channel vs. wire length: (a) signal delay and EPB, (b) EDP.

The pad and microbump size may also impact the signal performance. Figure 60 shows the trade-off between the signal performance and pad size for a 0.5-mm long HIST channel. Scaling pad size from 50 μm to 5 μm can decrease EPB by 25% and delay by 9% due to lower parasitic values. Further decreasing the size of the pad blurs the boundary between off-chip and on-chip wires to a point that the performance of the HIST channels becomes comparable to on-chip wires. In addition, smaller pads can decrease the size of stitch chip and thus decrease the average channel length. Note that the pad size of HIST is as small as 5 μm, which gives it an advantage in signal integrity and EPB compared to competitive 2.5D technologies.

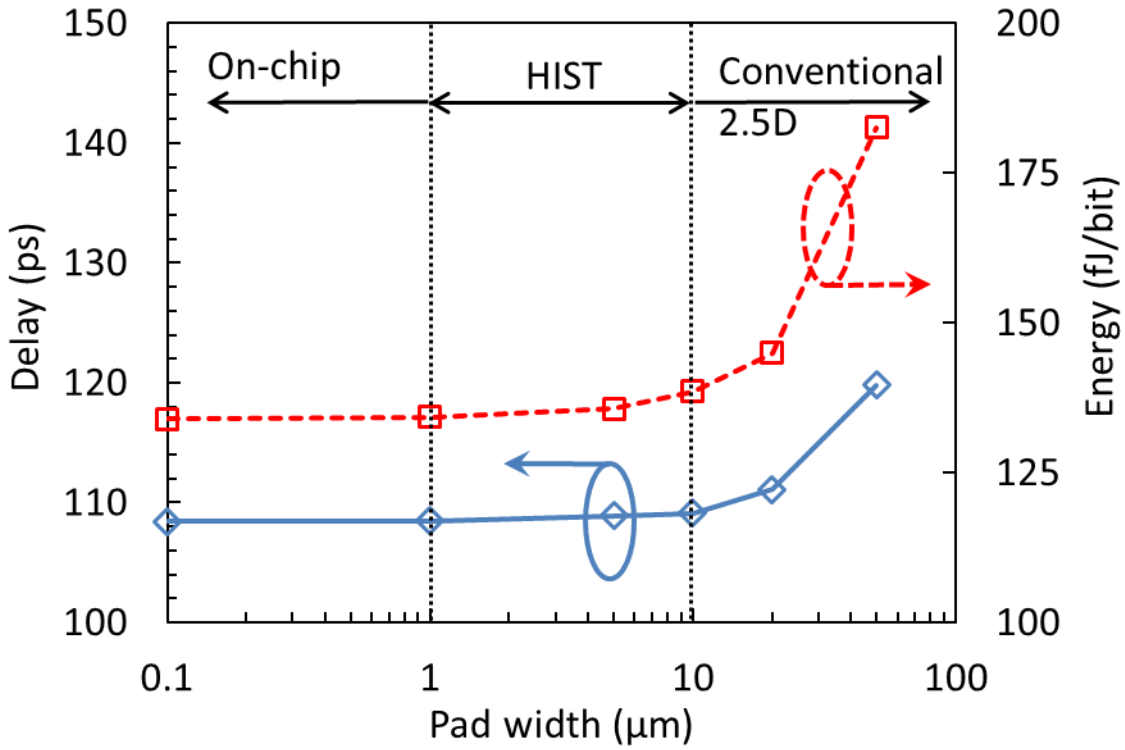


Fig. 60. Trade-off between the signal performance and pad size in a 0.5-mm long HIST channel.

5.5 Conclusion

In this chapter, a Heterogeneous Interconnect Stitching Technology (HIST) platform is presented. Two HIST testbeds are fabricated, assembled and characterized. A circuit model was developed to investigate the performance of HIST channels. The bandwidth density of HIST platform can reach up to 9.3 Tbps/cm at a power efficiency of 0.24 pJ/bit. The mechanical compliance of the CMIs is also measured. Vertical elastic deformation of the CMIs is up to 30 μm. The HIST platform strives to achieve monolithic-like performance, yet utilizes TSV-less high density interconnection using stitch chips that are integrated between the chiplets (i.e., logic-, memory-, sensors-die, etc) and the package substrate.

CHAPTER VI

RF CHARACTERIZATION OF THE HIST PLATFORM

6.1 Introduction

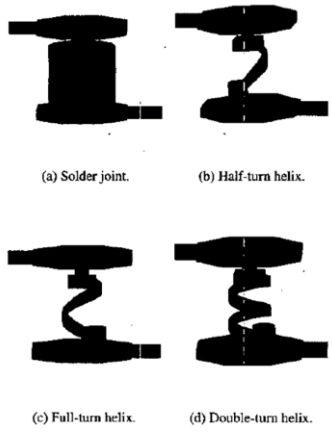
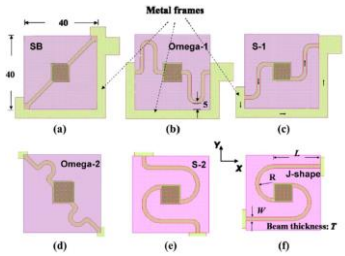
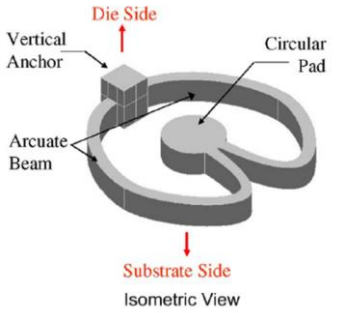
Spurred by the ever-increasing need of system level integration of functionally-diverse components, significant research has been conducted in heterogeneous interconnection platforms including silicon interposer [10], [11], silicon-less interconnect technology (SLIT) [41], and embedded multi-chip interconnect bridge (EMIB) [40] which are commonly referred to as 2.5D integration technologies. While each of the 2.5D integration solutions has benefits, they also have limitations. A heterogeneous interconnect stitching technology (HIST) was proposed to avoid those shortcomings [91]. Compared to other 2.5D integration technologies, HIST eliminates the need for TSVs, enables system size scalability and is agnostic to the substrate technology, as summarized in Table 3.

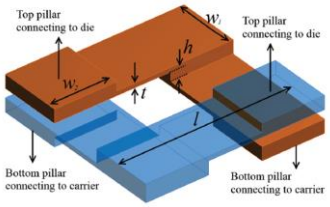
The potential applications of HIST include integration of ASICs, CPUs, GPUs, FPGAs, microsensors, photonics, MEMS, and RF components into a single package. For RF/analog applications, the high frequency performance of HIST channels are of particular interest. Research into low-loss transmission-lines (TLs) on silicon substrates has been widely investigated. Reig et al. demonstrated a coplanar waveguide (CPW) on high resistivity silicon (HRS) substrates with an insertion loss as low as 0.1 dB/mm at 20 GHz [92]. However, the higher cost of HRS wafers makes it less appealing than low resistivity silicon (LRS) wafers. Low-k polymer materials were used to decrease loss on LRS wafers. Leung et al. demonstrated a CPW on 20-µm low-k benzocyclobutene (BCB) layer with signal attenuation as low as 0.3 dB/mm at 30 GHz [93]. Newlin et al. showed a CPW on 200-µm thick SU-8 that achieves ultra-low loss of 0.02 dB/mm at 20 GHz [94]. However,

the compatibility of polymer materials in standard CMOS processes is a concern. For TLs on LRS substrates, Kato reported a CPW on SiO_2 that achieves an insertion loss of 0.4 dB/mm at 6 GHz [95]. Recently, Dehlaghi showed a stripline design with 4.5 dB/mm insertion loss at 25 GHz [96].

Compressible microinterconnect (CMI) is one of the key components of the HIST platform. The upward-curved profile and tapered design of the CMIs maximize the vertical elastic range of motion and thus improve the tolerance of surface/thickness variations of the dice in the HIST platform. It is important to understand the RF characteristics and the parasitics of the CMIs for RF/analog systems. RF characteristics of compressible/compliant interconnects are summarized in Table 10. Braunisch et al. compared helical spring structures with solder joint and showed that increasing the number of turns increases inductance [97]. For high frequency applications, the additional inductance may help compensate the pad capacitance. Liao et al. investigated six planar microspring designs and the RLGC parameters of the interconnect were extracted at 10 GHz [98]. The analysis was limited to a single vertical interconnect, thus the inductance and capacitance values of the interconnect may be inaccurate when multiple vertical interconnects are used in an array. Kacker et al. simulated the resistance and inductance of a helical interconnect [99]. However, the reported self-inductance value was the loop inductance of the single helical interconnect. In a real system where return paths are well defined, the extracted inductance can be significantly larger than the reported self-inductance. Recently, Xu reported the insertion loss of a 100 μm X 100 μm double helix interconnect. The insertion loss is 0.4 dB at 50 GHz [100].

Table 10: RF characteristics of selected compliant interconnects

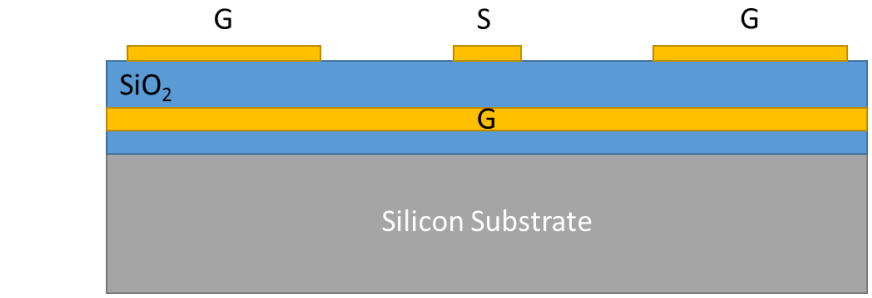
Reference	Structure and dimensions (µm)	Mechanical compliance (mm/N)	RF characteristics
 Braunisch, et al. [97] 2004	Helical spring	N/A	S_{21} > 1 dB R = 5 Ω L = 250 pH G = 1 mS C = 130 fF @ 40 GHz
 Liao, et al. [98] 2009	Planar microspring A = 40 X 40 W = 2 T = 2	20 - 170	R = 340 mΩ L = 35 pH C = 21.5 fF @ 10 GHz
 Kacker, et al. [99] 2009	Helical spring A = 70 X 70 W = 4 T = 8	0.7-6.47	R = 270 mΩ L = 32.5 pH @ 50 GHz

 Xu, et al. [100] 2014	Double helix A = 100 X 100 W = 35 T = 2.5	0.28	S_{21} = 0.4 dB @ 50 GHz

In this Chapter, a low-loss via-less conductor backed coplanar waveguide (CBCPW) was fabricated and measured. The insertion loss is 0.85 dB/mm at 50 GHz. The RF performance of CMIs measured is experimentally analyzed. The inductance and capacitance are extracted from the measurements. Section 6.2 reports the design and fabrication of the testbeds; Section 6.3 introduces the performance of the low-loss CBCPW; the results of the CMIs are summarized in Section 6.4; and conclusions are presented in Section 6.5.

6.2 Design and Fabrication of the Testbed

Figure 61 shows a schematic of the CBCPW. A 5-μm dielectric layer of SiO_2 is used to isolate the bottom ground plane and the CPW. The Cu-Au signal wire has a width of 9 μm and thickness of 2 μm. The 50-nm Au layer was used to prevent Cu oxidation. The spacing between the ground and signal wire is 40 μm and the width of the ground wire is 50 μm. 25 μm X 25 μm pads on a pitch of 50 μm are added to both ends of the TL for probing, as shown in the top-view of the structure in Fig. 61 (b).



(a)

(b)

Fig. 61. Schematic of the CBCPW: (a) cross-section, and (b) top-view.

The fabrication process starts with SiO_2 deposition on a 300-µm LRS wafer. 1 µm of SiO_2 was deposited with plasma-enhanced chemical vapor deposition (PECVD) at 250 ^oC. Next, the 1-µm Ti-Cu-Au ground plane was deposited with e-beam evaporator. A second dielectric layer of PECVD SiO_2 is then deposited. Finally, the top CPW and pads are fabricated with a lift-off process. The overall fabrication process is shown in Fig. 62.

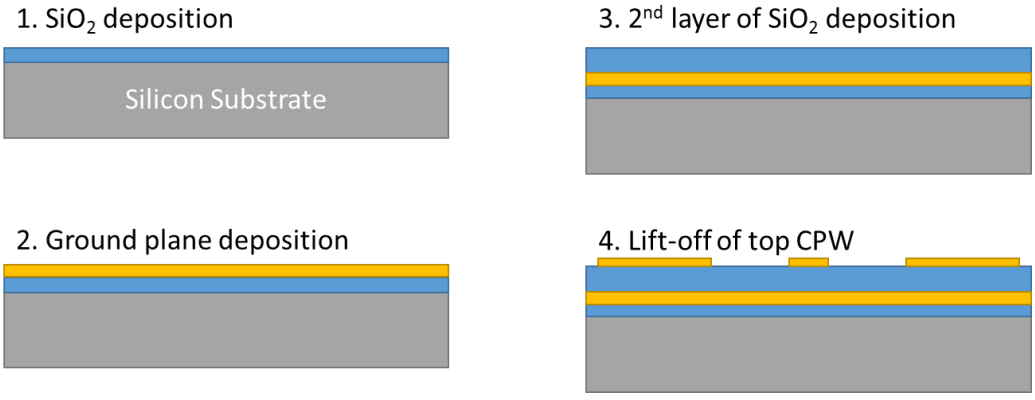
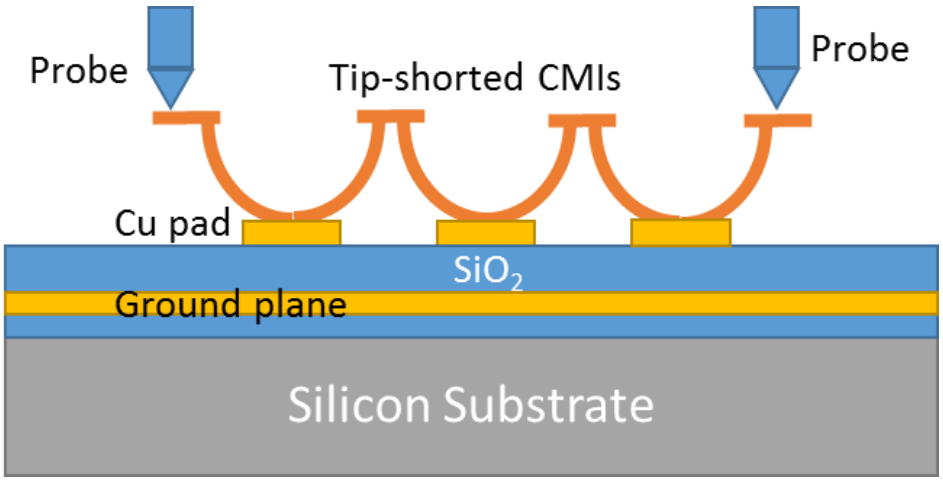
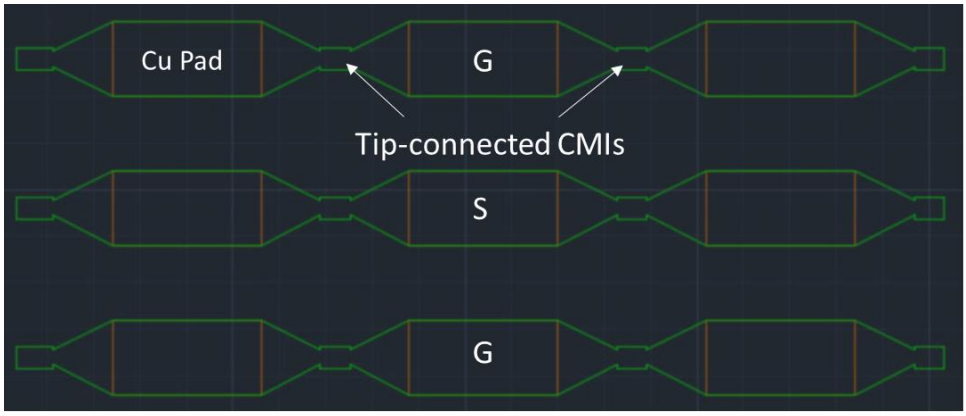


Fig. 62. Fabrication process of the CBCPW.

Daisy-chain structures are used to characterize the performance of the CMIs, as shown in Fig. 63. The number of CMIs in a daisy-chain ranges from 2 up to 8. The CMIs are fabricated on 100 µm X 100 µm Cu anchor pads with a pitch of 200 µm. The tip of CMI is approximately 20 µm above the substrate surface. The length of the CMI tip is 80 µm and the metal thickness is approximately 5 µm. The top-view of a CMI is shown in Fig. 63 (b). Note that a ground-signal-ground (GSG) configuration is adopted for CMI characterization and an additional ground plane was fabricated under the pads to isolate the lossy silicon substrate. Optical and SEM images of the fabricated CMIs are shown in Fig. 64. The fabrication process of the CMIs is similar to the process shown in Chapter V and will not be described here.



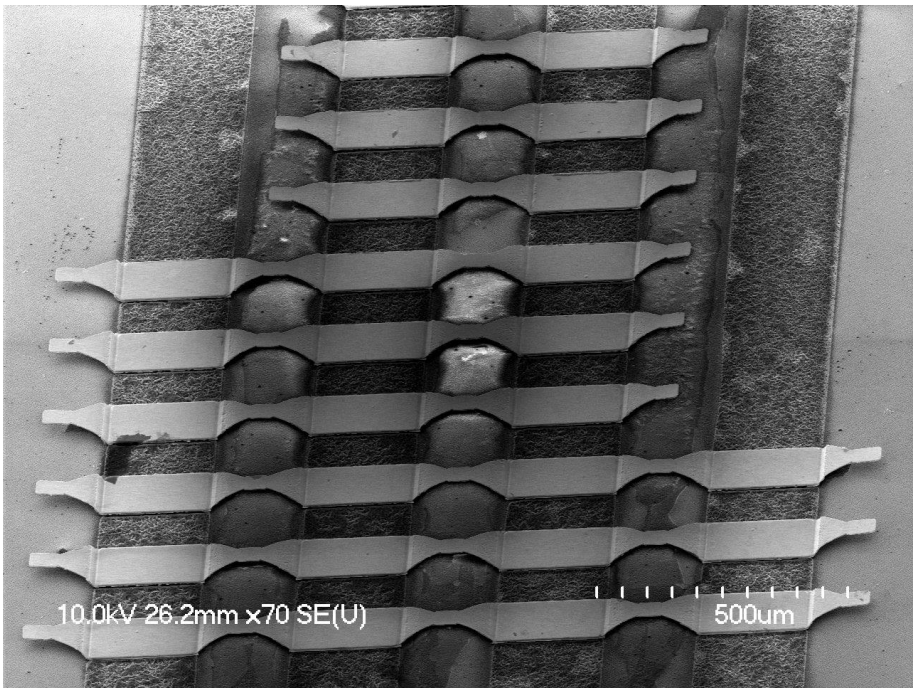
(a)



(b)

Fig. 63 Schematic of a daisy-chain with 6 CMIs: (a) cross-section, and (b) top-view.

(a)



(b)

Fig. 64 SEM images of the daisy-chain with: (a) 2 CMIs, and (b) 4, 6 and 8 CMIs.

6.3 Characterization of the Low-loss CBCPW

The fabricated interconnects are measured using an Agilent N5245A network analyzer to obtain the S-parameters from 10 MHz to 50 GHz at a 250 MHz step. The measured S_{21} of interconnects with length of 0.2 mm, 0.5 mm and 1 mm are shown in Fig 65. HFSS simulation results are compared with measurements and have a good agreement. A clear trade-off between the loss and interconnect length can be observed.

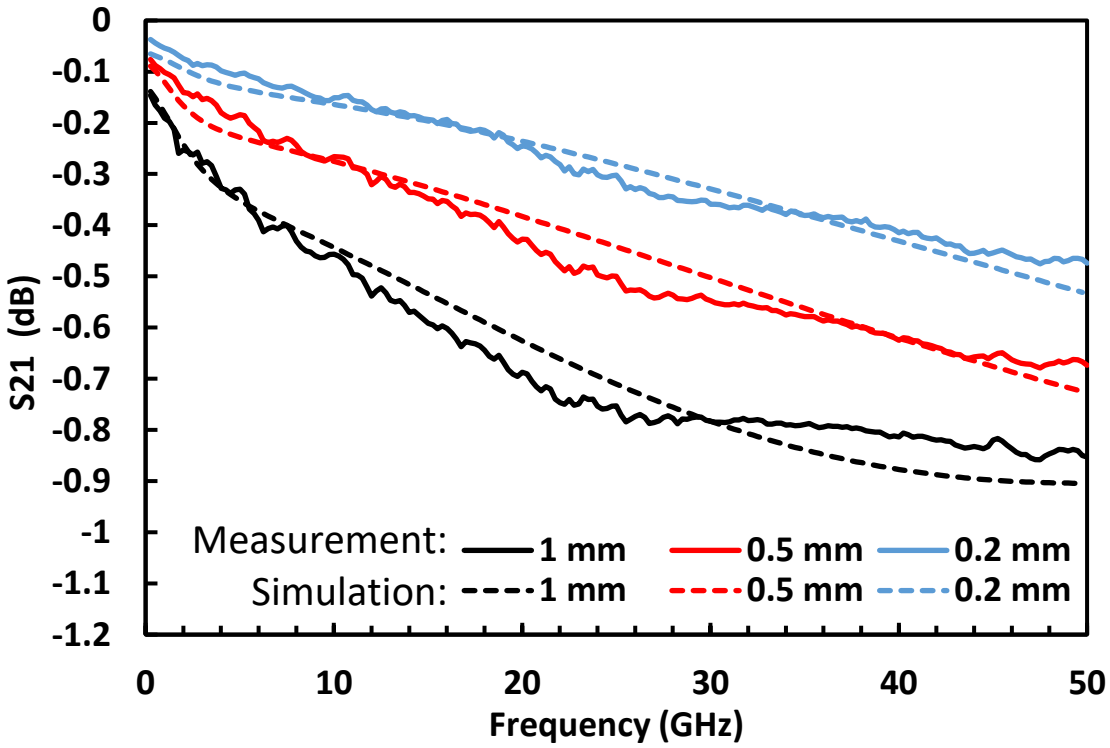


Fig 65. Measured S_{21} of the CBCPW for three wire lengths.

A L-2L de-embedding method is adopted to eliminate the impact of the probe pads [61] and the results are shown in Fig. 66. The per-unit-length (p. u. l.) insertion loss of the interconnect is 0.85 dB/mm at 50 GHz, 0.4 dB/mm at 20 GHz and 0.25 dB/mm at 10 GHz.

The loss is significantly lower than the results reported in publications with LRS substrates shown in Section 6.1.

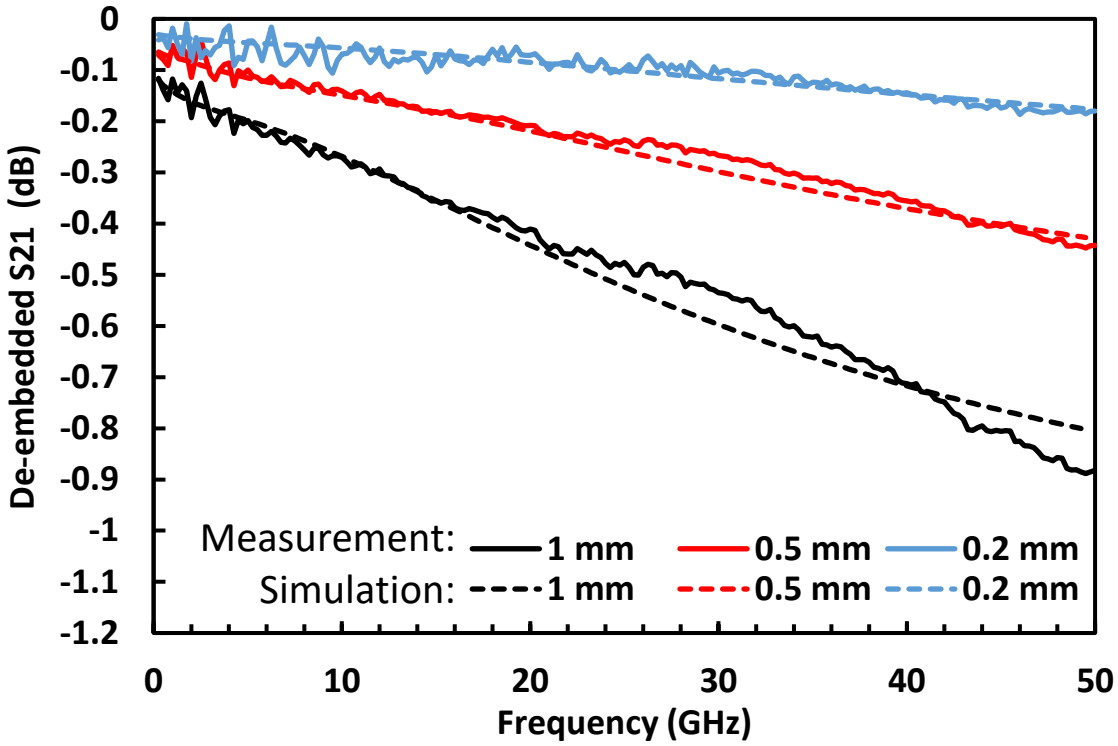


Fig 66. De-embedded S_{21} of the CBCPW for three wire lengths.

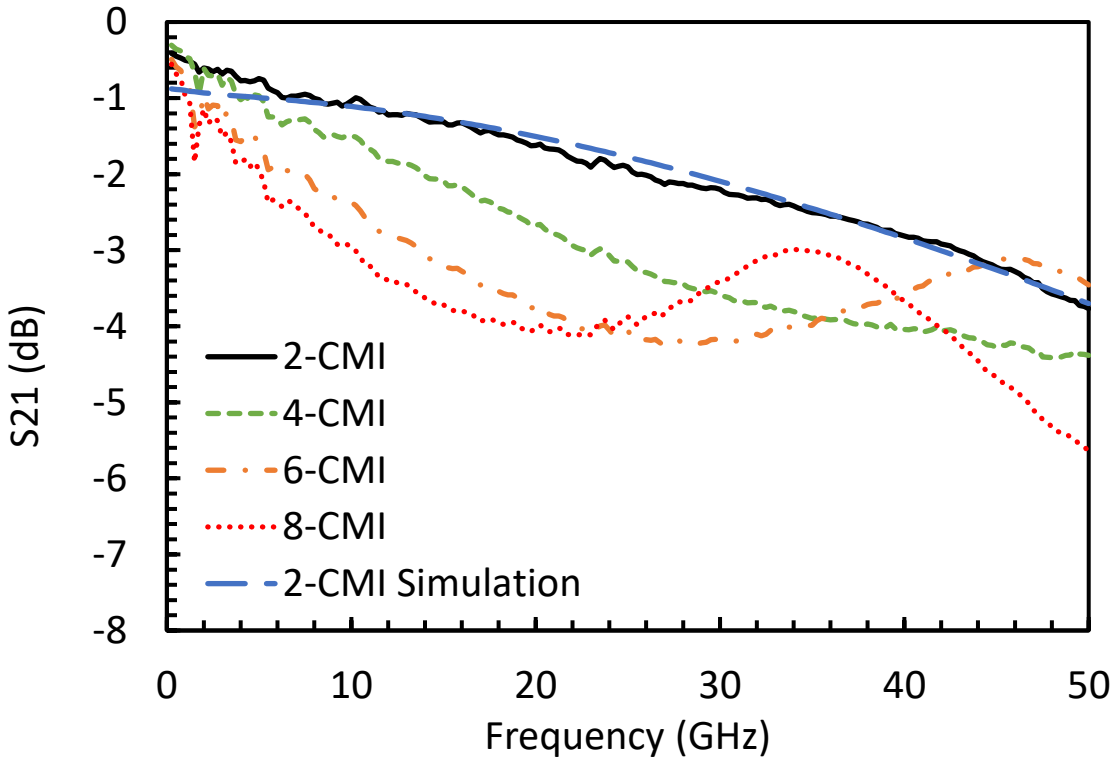
6.4 Characterization of the CMI

Daisy-chain structures with 2, 4, 6 and 8 CMIs are measured with an Agilent N5245A network analyzer from 10 MHz to 50 GHz at a 250 MHz step. Figure 67 shows the original measured S-parameters and simulation results of the 2-CMI structure with ANSYS HFSS. The curves of the 6-CMI and 8-CMI structures show resonances at 46 GHz and 34 GHz, respectively. The measured S-parameter matrices were transferred to impedance-parameter matrices (Z-matrix) and admittance-parameter matrices (Y-matrix) to extract the inductance and capacitance of the CMIs using the following equations [86]:

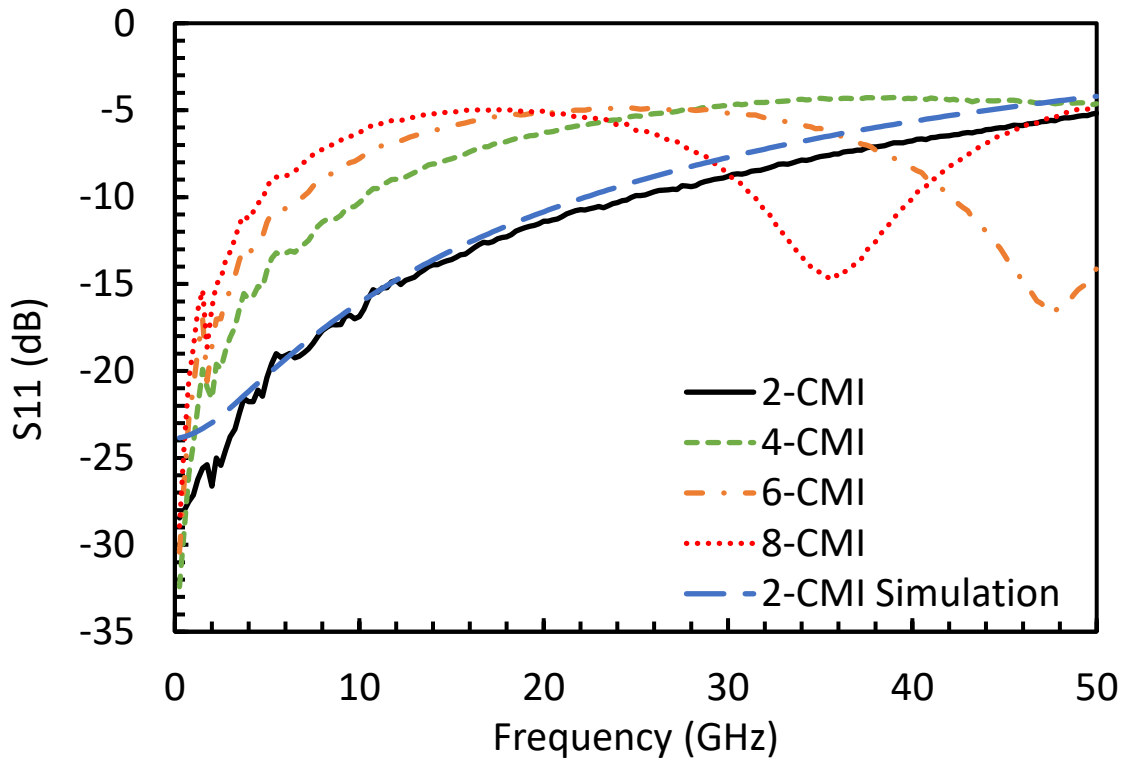
$$L = (j\omega)^{-1}*Im(Z_{11}-Z_{12}-Z_{21}+Z_{22}) \quad (26)$$

$$C = (j\omega)^{-1} * Im(Y_{11}+Y_{12}+Y_{21}+Y_{22}) \quad (27)$$

Note that the CMIs are considered as lumped components for parasitics extraction. The maximum extraction frequency is set to be 15 GHz, 20 GHz, 30 GHz and 50 GHz for the structures with 8, 6, 4 and 2 CMIs, respectively. Therefore the physical length of the structures is smaller than 1/10 of the wavelength at the selected frequency, as summarized in Table 11.



(a)



(b)

Fig. 67 Measured S-parameters of the daisy-chain structures: (a) S_{21} and (b) S_{11}.

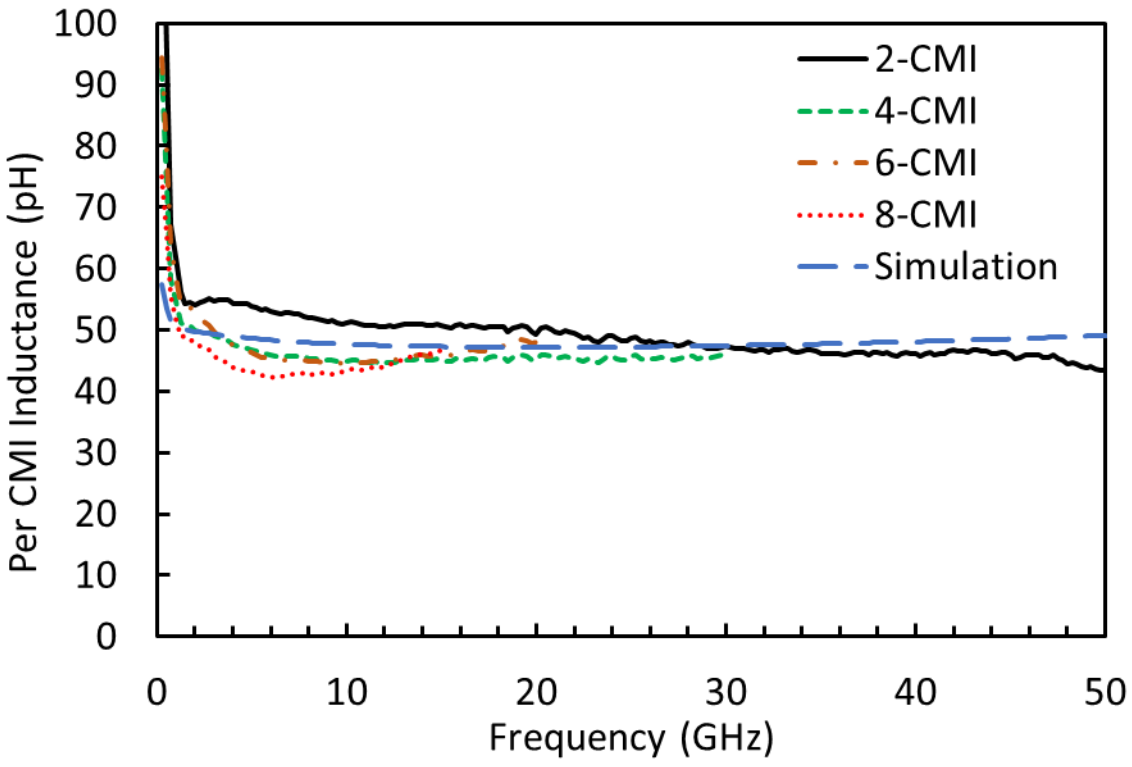
Table 11: Physical length and maximum extraction frequency

Structure	Physical length	Frequency and 1/10 wavelength
8-CMI	1.5 mm	15 GHz, 2 mm
6-CMI	1.1 mm	20 GHz, 1.5 mm
4-CMI	0.75 mm	30 GHz, 1 mm
2-CMI	0.37 mm	50 GHz, 0.6 mm

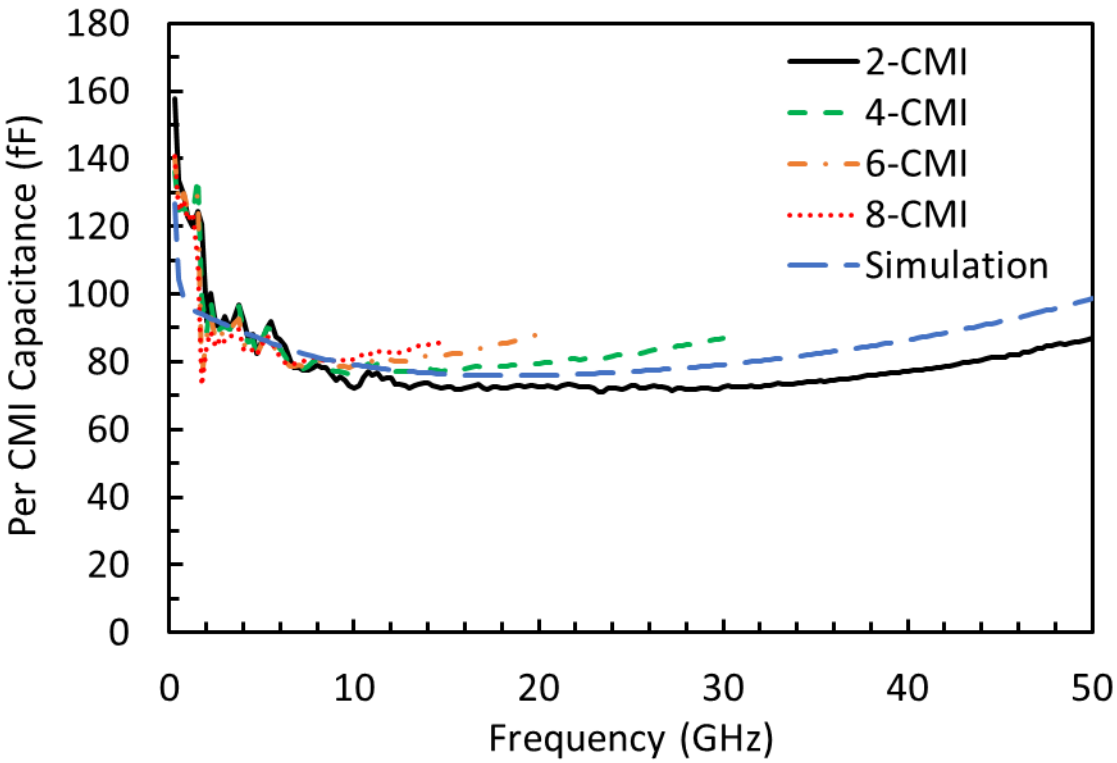
The extracted per CMI inductance and capacitance values are shown in Fig. 68. Simulation results are also shown and compared with measurements. The values obtained from measurements and the simulation show a good agreement. It can be observed that the inductance and capacitance values are significantly larger at very low frequency and reach

to steady values as frequency increases. This is because at low frequency, the ground CMIs in the GSG configuration provide the return path for the signal. As frequency increases, the capacitive coupling between the ground CMIs and the ground plane makes them a continuous return path [101]. The increase of capacitance at higher frequencies is due to resonances shown in Fig. 67.

The anchor pads are also measured and extracted to better understand the parasitics of the CMIs. The inductance and capacitance values of the pad are compared with the CMI parasitics and shown in Fig. 69. The pad capacitance contributes to approximately 80% of the CMI capacitance while the pad inductance contributes to less than 40% of the CMI inductance.

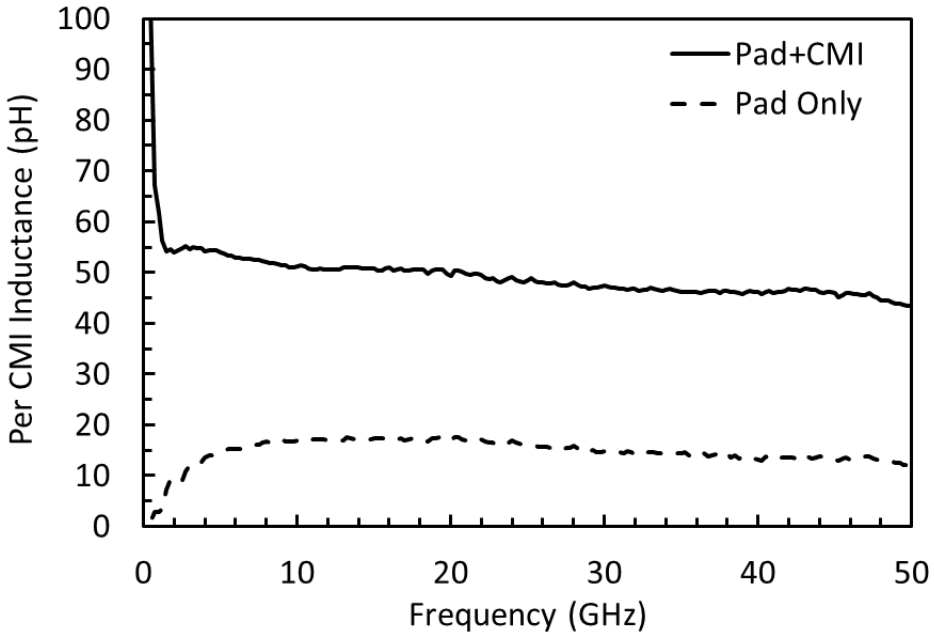


(a)

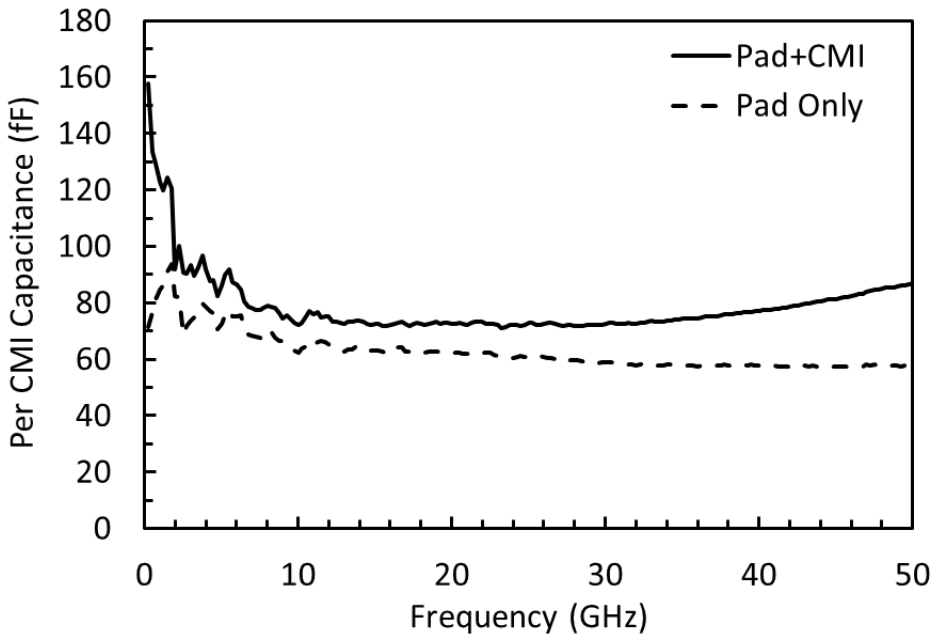


(b)

Fig. 68. Extracted per CMI inductance (a) and capacitance (b).



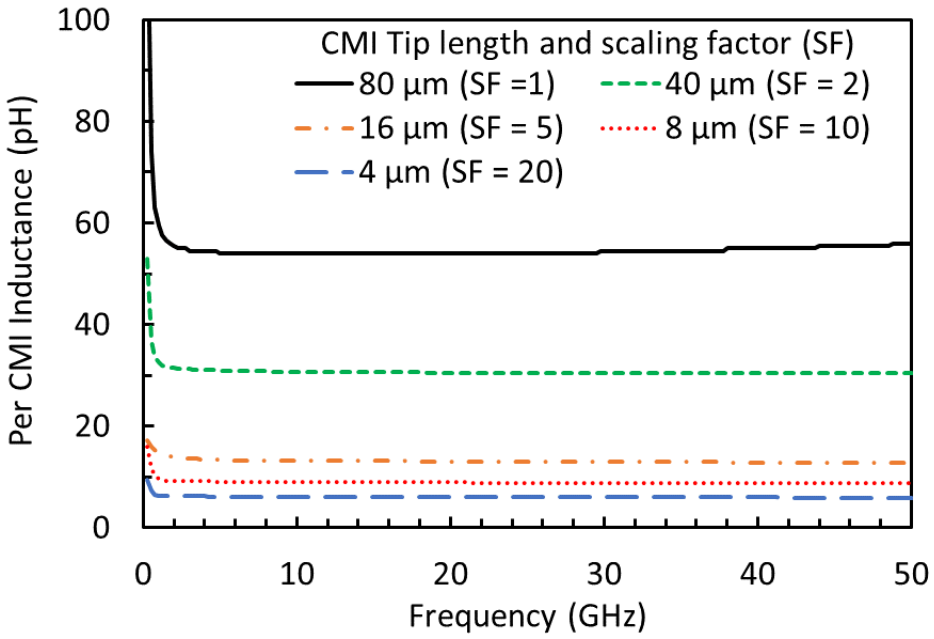
(a)



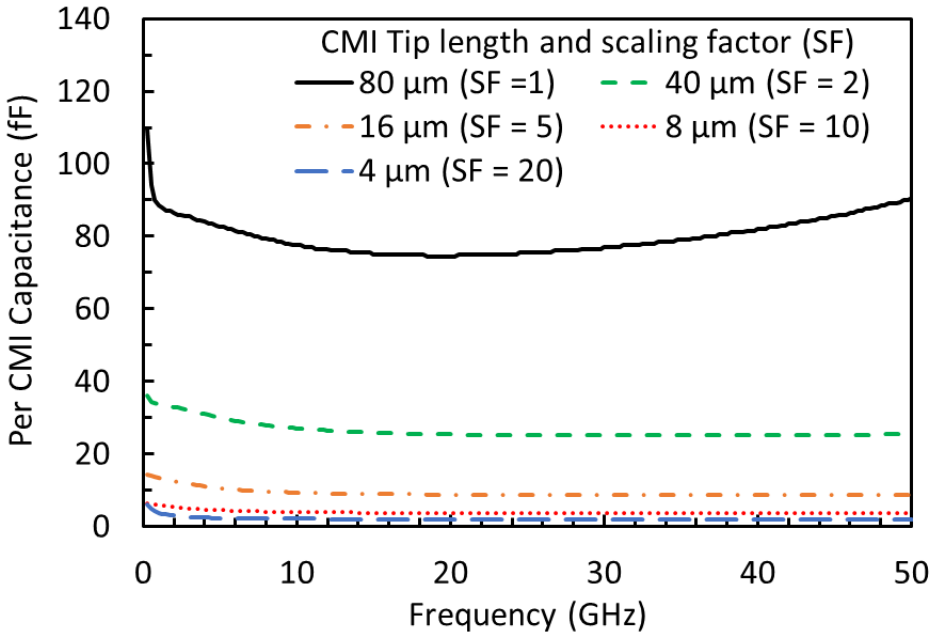
(b)

Fig. 69 Comparison of the parasitics of the CMI and the anchor pad: (a) inductance and (b) capacitance.

The impact of scaling on the inductance and capacitance values of the CMIs are analyzed with HFSS and the results are shown in Fig 70. Scaling factor of 1 represents the current design where the CMI tip length is 80 μm and the pad size is 100 μm X 100 μm. Decreasing the dimensions by half (e.g. scaling factor of 2) can decrease the inductance and capacitance by approximately 43% and 65%, respectively. Further decreasing CMI length to 4 μm and pad size to 5 μm X 5 μm (e.g. scaling factor of 20) can decrease the inductance and capacitance by approximately 89% and 97%, respectively.



(a)



(b)

Fig 70. Impact of scaling on CMI parasictics: (a) inductance and (b) capacitance.

6.5 Conclusion

In this chapter, a testbed including CMIs and low-loss conductive back co-planar waveguide (CBCPW) was fabricated and measured. The insertion loss of the HIST channel is 0.85 dB/mm at 50 GHz. The inductance and capacitance values of the CMI are extracted from the measured S-parameters for a wide range of frequency. The average inductance and capacitance values are approximately 50 pH and 80 fF for the current design where the CMI tip length is 80 μm and the anchor pad size is 100 μm X 100 μm. It is found that the pad contributes to most of the capacitance and the flexible interconnect portion contributes to most of the inductance. In addition, scaling of CMI is analyzed with HFSS simulations. Decreasing the dimensions by half can decrease the inductance and capacitance for approximately 43% and 65%, respectively.

CHAPTER VII

SUMMARY AND FUTURE WORK

7.1 Summary of the Presented Work

The objective of this research is to experimentally investigate the electrical and thermal challenges in 3D/2.5D ICs and explore new heterogeneous integration solutions that can avoid the short comings of conventional 3D/2.5D integration technologies.

7.1.1 Impact of on-chip interconnect of 3D IC with TSVs

TSVs are key enablers of 3D/2.5D IC technologies. Compared to on-chip interconnects, TSVs have much higher capacitance values which may impact the system performance. Therefore, it is important to understand the electrical characteristics of the TSVs, especially capacitance, and how TSVs impact the overall performance of interconnect links and other devices in 3D IC.

In Chapter II, TSV arrays and 3D IC links with TSVs and horizontal wires are fabricated, measured, and analyzed. The TSV capacitance and link delay models are verified with measurements. It is shown that the TSV capacitance and the driver side wire resistance can dominate the link performance and could potentially be the key bottleneck for digital 3D ICs. The delay and eye opening of the link can be significantly improved by placing TSVs closer to their drivers. Furthermore, reducing the length of on-chip wires and height and diameter of the TSVs have a significant impact on 3D IC link performance.

7.1.2 Embedded microfluidic cooling in 3D IC

As 3D/2.5D integration technologies further increase the power density of high performance computing systems, the heat dissipation may exceed the capability of conventional air-cooled heat sinks. A switch from air cooling to microfluidic cooling is believed to be a promising solution.

In Chapter III, novel thermal testbeds with embedded micropin-fin heat sinks were designed and microfabricated in silicon. Two micropin-fin arrays were presented, each with a nominal pin height of 200 μm and pin diameters of 90 μm and 30 μm. Single phase and two phase thermal testing of the micropin-fin array heat sinks were performed using deionized (D.I.) water as the coolant. The tested mass flow rate was 0.001 kg/s, and heat flux ranged from 30 W/cm^2 to 470 W/cm^2. The maximum heat transfer coefficient was 60 kW/m^{2}K. The results obtained from two testbeds were compared and analyzed, showing that density of the micropin-fins has a significant impact on thermal performance.

In Chapter IV, a hotspot cooler testbed for convective boiling experiments in extreme-microgap with integrated micropin-fins and isolation air trenches was designed, fabricated and tested. The maximum heat flux during testing reached up to 4.75 kW/cm^2 with flow rates ranging from 0.1 – 0.3 ml/min. A reduction in thermal resistance of approximately 3.5% was observed with the surface enhancement of the micropin-fins with a tradeoff of a large increase in pumping power resulting from the high constriction of the fluid flow. In addition, the reliability analysis showed that the device can sustain 3000 kPa pressure and 1000 kPa pressure drop across the microgap.

7.1.3 Heterogeneous Interconnect Stitching Technology for dense multi-die integration

Conventional 3D and 2.5D integration technologies have become a promising solution for high performance computing. However, their limitations including lossy TSVs, complex assembly and limited reticle size of the silicon interposers have spurred research into alternative heterogeneous integration solutions. The EMIB technology eliminates the need for TSVs and silicon interposers. However, it has an organic layer between the silicon chips which may limit the I/O density. In addition, the EMIB technology may only be applied to organic package substrate.

To preserve all the benefits and avoid shortcomings of the aforementioned technologies including 3D stacking, 2.5D interposer and EMIB, a HIST platform is presented to enable the interconnection of multiple dice of various functionalities in a manner that mimics monolithic-like performance, yet utilizes advanced off-chip interconnects and packaging to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost.

In Chapter IV, two HIST testbeds are designed, fabricated and measured. The average post-assembly electrical resistance values of the fine-pitch microbumps, fine-pitch CMIs, coarse-pitch solder bumps and coarse-pitch CMIs are characterized as 0.117 mΩ, 145.38 mΩ, 1.31 mΩ and 195.99 mΩ, respectively. Vertical elastic deformation of up to 30 μm and 13 μm were characterized for fine-pitch and coarse-pitch CMIs, respectively. A circuit model was built to investigate the performance of HIST channels. The bandwidth density of HIST platform can reach up to 9.3 Tbps/cm at a power efficiency of 0.24 pJ/bit.

In Chapter V, a testbed including CMIs and low-loss conductor backed co-planar waveguide (CBCPW) was fabricated and measured. The insertion loss of the HIST channel

was found to be 0.85 dB/mm at 50 GHz. The inductance and capacitance values of the CMI were extracted from the measured S-parameters for a wide range of frequency. The average inductance and capacitance values are approximately 50 pH and 80 fF for the current design. It is found that the pad contributes to most of the capacitance and the curved tip contributes to most of the inductance. In addition, scaling of CMIs is found to be very effective in decreasing the parasitics of the CMIs.

7.2 Future Work

The potential opportunities for advancing the researches in this dissertation will be discussed in the following sections. Opportunities that continue exploiting embedded microfluidic cooling will be discussed first, including heat sink design optimization and thermal-electrical co-design for 3D IC with microfluidic cooling. Next, possible extension of the HIST platform will be discussed, including demonstration of HIST on selected package substrates (organic, ceramic, etc.) with active dice, and the integration of silicon photonics in HIST platform.

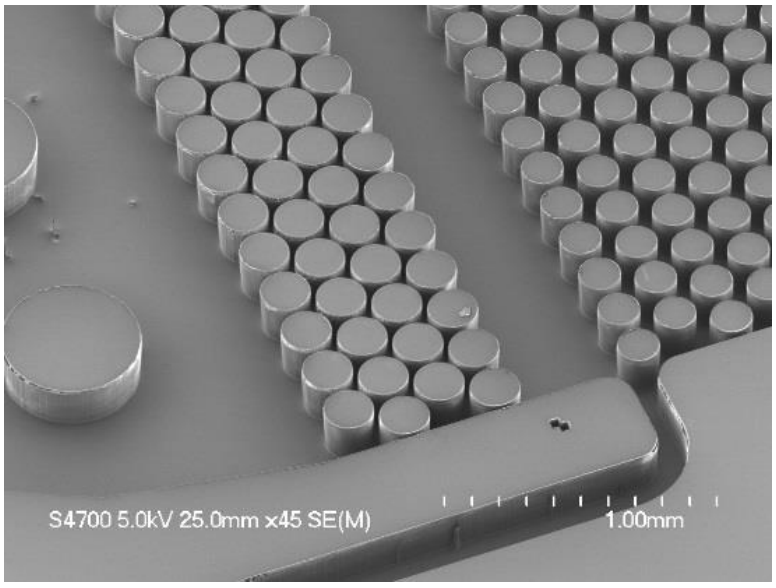
7.2.1 Continue exploiting embedded microfluidic cooling

In this dissertation, multiple embedded microfluidic heat sink designs have been investigated and important findings have been reported. However, there are still opportunities for improving the performance of the heatsink designs, as shown below.

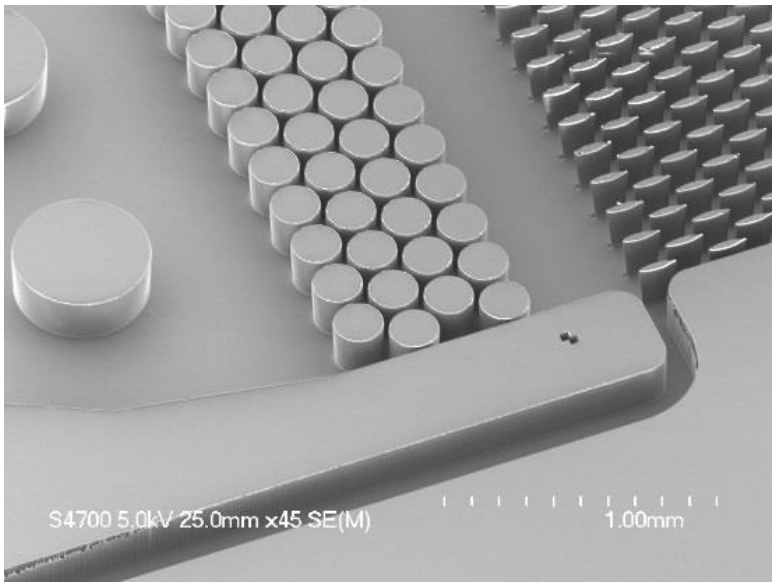
7.2.1.1 Heat sink design optimization

To maximize the surface area of the heat sinks, various heat sink designs (micro-channels, cylindrical micropin-fins and hydrofoil micropin-fins, etc.) have been investigated in prior researches, as discussed in Chapter I. In these designs, cylindrical micropin-fins and

hydrofoil micropin-fins are of particular interest. A comparison of the performance of cylindrical and hydrofoil micropin-fins under various testing parameters may be very valuable. Fig. 71 shows two testbeds with cylindrical and hydrofoil micropin-fins as an example.



(a)



(b)

Fig. 71. Microfluidic heat sink with (a) cylindrical and (b) hydrofoil micropin-fins.

7.2.1.2 Thermal-electrical co-design

The potential impact of microfluidic cooling on electrical performance of 3D IC was briefly investigated in Chapter III. The analysis was limited to micropin-fin geometries and the permittivity of the coolant was not included. The permittivity of liquid usually varies with frequency. The permittivity of D. I. water is shown in Fig. 72 as an example. Recently, H. Oh reported a high frequency analysis of TSV in microfluidic heatsink with D. I. water [55]. However, it is still unclear how the other common coolants (R134a, R245fa, etc.) and bubbles in two-phase cooling would impact the electrical performance of the 3D IC links. In addition, a thermal-electrical co-optimization for a range of heat sink geometries will be very valuable for future heat sink design references.

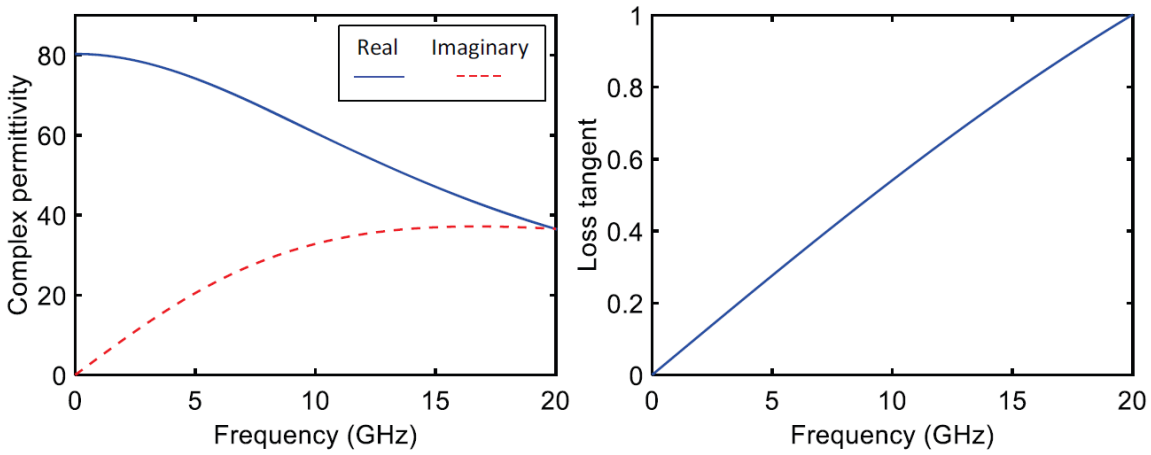


Fig. 72. Real permittivity, imaginary permittivity, and loss tangent (tanδ) of D.I. water up to 20 GHz [102], [103].

7.2.2 Continue exploiting the HIST platform

The HIST platform has been demonstrated in Chapter V and the performance of the HIST channels has been characterized in Chapter VI. However, the potential of this technology has not been fully shown. Demonstrations with active circuitry and silicon photonics will further extend the capability of the HIST platform.

7.2.2.1 HIST platform with active circuitry

In this dissertation, the HIST platform has been demonstrated with dummy chips with back-end-of-line (BOEL) passive interconnects and the stitch ICs were emulated with step-like structures on a silicon substrate. The next step to bring HIST into real applications is to assemble HIST on selected package substrates (organic, ceramic, etc.) with active dice, as shown in Fig. 73. In this demonstration, CMIs will be fabricated on wafers with integrated passive devices (IPDs). After dicing, the stitch chips will be assembled on the package substrate with adhesive material (e.g. polymer or solder). Finally, active dice or chiplets will be assembled and tested.

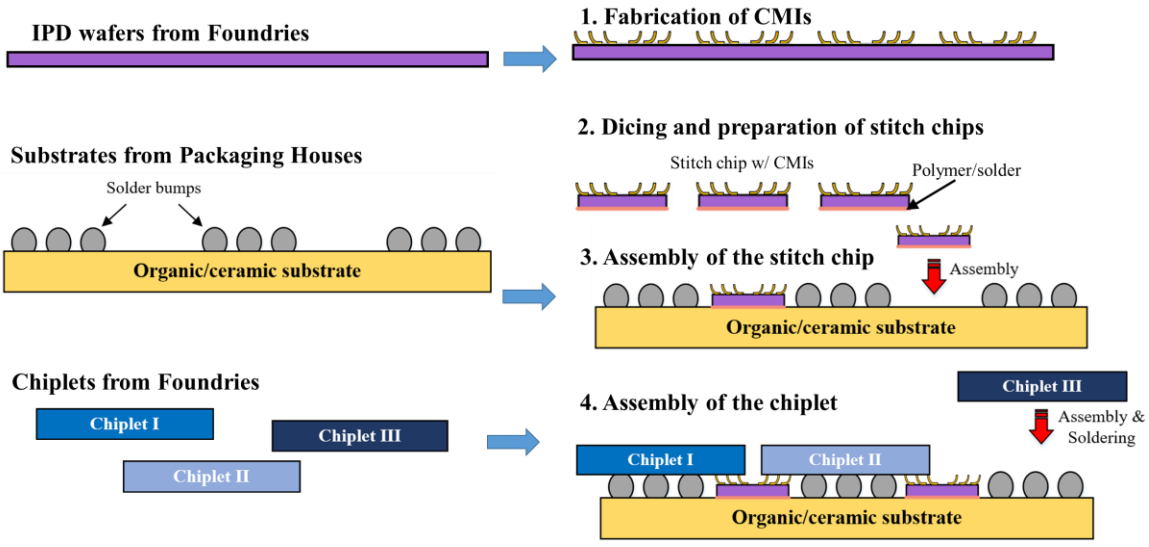


Fig. 73. Demonstration of HIST platform with active dice

7.2.2.2 HIST platform with optics

The vision of the HIST platform is to build a large scale system with subsystems that has high density electrical interconnections inside, and high bandwidth optical links to communicate with other subsystems, as shown in Fig. 74. In a conventional computing system with optical I/Os, the board level interconnects between the photonics receiver and the logic chip can be the potential bottleneck. In the HIST platform, the photonics receiver can be integrated into stitch ICs or assembled in the system as a regular chip. All the data received by the photonics receiver can be transmitted through the high density fine-pitch wires on the stitch ICs inside the subsystem. In this platform, the motherboard will only carry limited number of signals while most of the data traffic will be transmitted via optical cables.

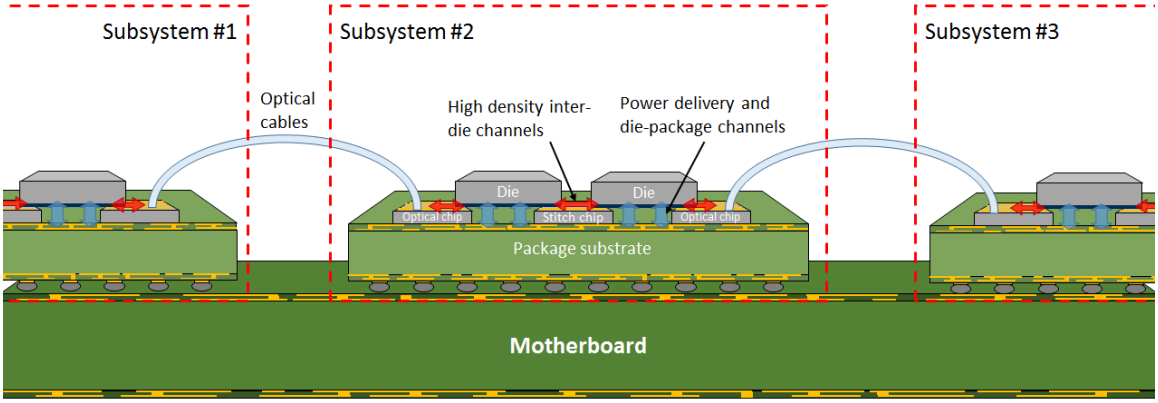


Fig. 74. The vision of HIST platform with optics.

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