LARGE-SCALE SILICON SYSTEM TECHNOLOGIES: THROUGH-SILICON VIAS, MECHANICALLY FLEXIBLE INTERCONNECTS, AND POSITIVE SELF-ALIGNMENT STRUCTURES

A Dissertation
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of Electrical and Computer Engineering

Georgia Institute of Technology
December 2014

LARGE-SCALE SILICON SYSTEM TECHNOLOGIES: THROUGH-SILICON VIAS, MECHANICALLY FLEXIBLE INTERCONNECTS, AND POSITIVE SELF-ALIGNMENT STRUCTURES

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To my wife,

Kyu Yun Kim,

and my parents,

Sung Sun Park and Seong Sam Yang,

for their unlimited love and support.

ACKNOWLEDGEMENTS

First and foremost, I want to thank my advisor Dr. Bakir. It is an honor to be his first Ph.D. graduate, and I consider myself extremely privileged to have worked with someone who is so passionate about semiconductors research. His vision, energy, and enthusiasm for research were sources of motivation when I needed the most, and I am very grateful to have such an exceptional advisor who made my Ph.D. experience such a gratifying experience.

I am also extremely grateful to the I3DS and the GSI group members, including Chaoqi Zhang, Hanju Oh, Yue Zhang, Li Zheng, Reza Abbaspour, Muneeb Zia, Paragkumar Thadesar, Jiun-hong Lai, Jesal Zaveri, Calvin King, and Ashish Dembla. Countless number of discussions, both research and personal, have greatly enriched my experience as a graduate student. I would also like to acknowledge Toby Xu and Jaime Zahorian for the collaboration work involving TSVs and CMUTs.

I would also like to thank the team at Oracle, including Dr. Thacker, Dr. Raj, Dr. Shubin, Dr. Cunningham, and Dr. Mitchell. The internship at Oracle was an eye-opening experience, and the team always provided insights during regular teleconferences that deeply shaped my research. I would like to acknowledge Dr. Thacker in particular for being a great mentor during my internship and serving as a member of my Ph.D. committee. Moreover, I would like to thank Oracle for giving me the permission to use the material from the internship in my dissertation *.

My experimental research would have not been possible if it weren't for the extremely capable and professional staff at the Institute for Electronics and Nanotechnology (IEN). I have had my fair share of mistakes, which undoubtedly caused many headaches for the staff. I would like to thank every cleanroom staff for educating

me rather than suspending me. I would like to especially acknowledge Gary Spinner, Eric Woods, and Vinny Nguyen for answering my very late night and weekend calls.

I would also like to thank my parents, whom I love very dearly. Without their encouragement, support, patience, and trust, this work would not have been possible.

Last but definitely not least, I want to thank my wife, Kyu Yun, whom I love most dearly. Her unconditional and endless love has supported me during the hardest times in my life. Without her, I could never have finished this academic endeavor.

- James

* The work presented in Chapter 6 was completed when the author was a 2011 visiting summer intern in the Photonics, Interconnects and Packaging group in Oracle Labs in San Diego and was published in the ECTC 2012 proceedings [17] and is reproduced as-is in this thesis as Chapter 6 with permission from Oracle.

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SUMMARY

A novel large-scale silicon system platform with 9.6 cm^2 of active silicon interposer area is demonstrated. The platform contains three interposer tiles and two silicon bridges, and a novel self-alignment technology utilizing positive self-alignment structures (PSAS) and a novel mechanically flexible interconnect (MFI) technology are developed and used to align and interconnect tiles and bridges on an FR4 substrate. An accurate alignment <8 μm between silicon bridges and interposer tiles makes it possible to accommodate nanophotonics to enable a high bandwidth and low-energy system in the future. In addition, mechanically flexible interconnects and silicon bridges are used to provide electrical connections between interposer tiles without having to use motherboard-level interconnects. Finally, an elastomeric bump interposer is developed to enable the packaging of PSAS-enabled silicon systems, and PSAS' compatibility with a thermo-compression bonding process is demonstrated to enable a wide range of system configurations involving interposer tiles and bridges, including the multi-chip package configuration used with the elastomeric bump interposers.

CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Motivation

Since the invention of transistors in 1947, integrated circuit (IC) technology has become the main driver of the information revolution that continues to this day. One main force behind the success of IC technology is the close relationship between IC performance and number of transistors. Accordingly, the industry has followed a trend that was famously observed by Gordon Moore, which showed that the number of transistors in a single microchip doubled every two years by scaling down the transistor dimensions (Figure 1); the semiconductor industry is now able to fabricate billions of transistors in a single chip as opposed to the hundreds of transistors that were possible in the 1960s.

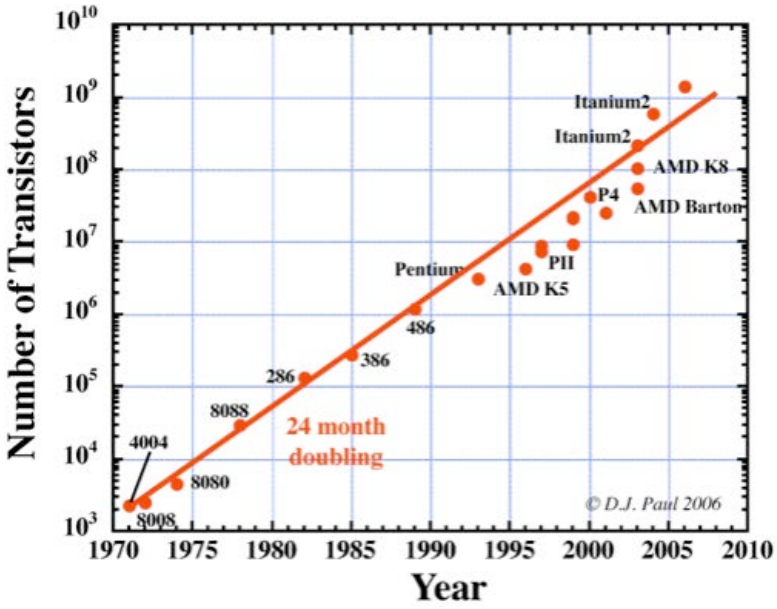


Figure 1: Moore's law for the number of transistors.

The theoretical limits of increasing the number of transistors per chip have been explored in a seminal paper by Meindl [1]. Despite rapid advancement towards the theoretical limits, the author speculated that the practical limits related to the cost of decreasing the minimum feature size, increasing the chip size, and increasing the packing efficiency will determine the ultimate ceiling for the number of transistors per chip.

Therefore, the growing risk and increased capital investment associated with transistor scaling have led the industry to look for ways to radically increase chip size and packing efficiency in parallel to scaling transistors. However, increasing chip size is not a trivial task because chip size negatively affects design complexity, time-to-market, mask costs, and yield. In addition, the limited reticle size imposes a limit on the maximum size of a chip.

Alternatively, multiple chips can be interconnected to form a logically single chip. For example, multiple chips can be assembled on a single package substrate or a printed wiring board (PWB). However, this approach is inefficient in improving performance despite the increased number of transistors because the off-chip interconnect technologies, especially at the package and PWB levels, perform extremely poorly compared to on-chip wires in terms of bandwidth density [2].

1.1.1 A Silicon Interposer

To overcome the interconnect density limitation on package substrates and PWB, silicon interposers have been proposed. A silicon interposer is an intermediary layer inserted between one or more chips and a package substrate, as shown in Figure 2. It contains fine-pitched wires comparable with the metallization layers on a CMOS IC. Therefore, fine-pitched wires are available to interconnect multiple chips that are assembled on top. For the off-module I/Os, through-silicon vias (TSVs) are fabricated inside the silicon interposer, which transfer signals from the top side, where the chips

are located, to the back side, where interconnections to the package substrate can be made.

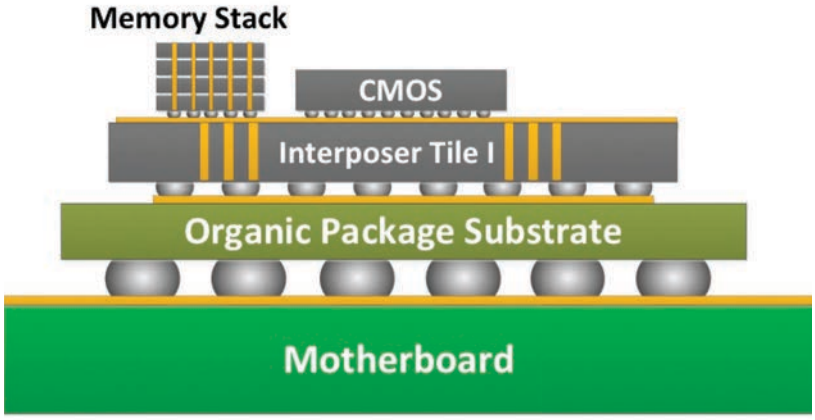


Figure 2: A figure showing a typical single interposer system.

Silicon interposers offer significant performance enhancement, as shown in Figure 3. As a result, the technology's adoption has been rapid in the industry, and many companies have already demonstrated multi-chip systems using a single silicon interposer (Figure 4). Notable demonstrations include:

- IBM's demonstration of 8x10Gb/s synchronous communication between chips using the fine-pitch metallization on the interposer [3];
- Xilinx's [4] and Altera's [5] demonstration of complete 2.5D FPGA systems; and
- Oracle's demonstration of a silicon interposer technology with TSVs and flexible I/Os [6].

However, the increase in parallelism to enable heavily cached, speculative, multi-core and/or multithreaded architectures continues to drive demand for an increased number of transistors [7]. Considering that interposer size, like chip size, is also limited by the reticle size as well as the degrading yield, single-interposer solutions

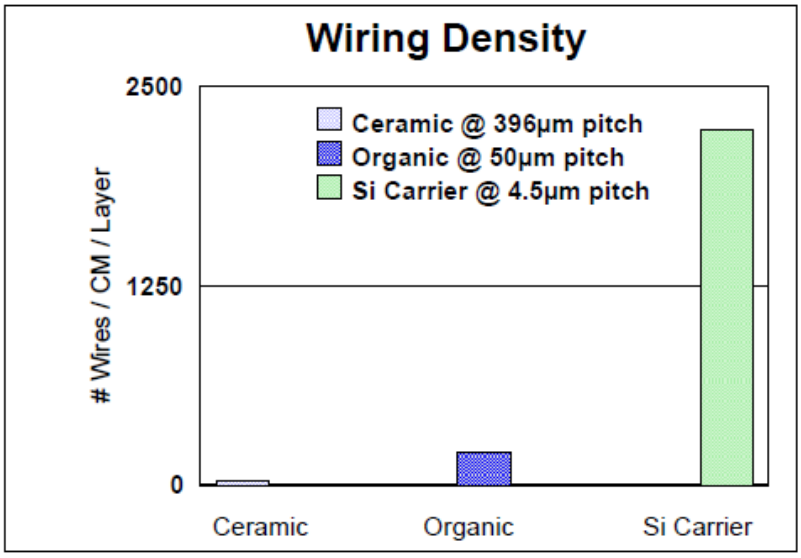


Figure 3: A comparison of wiring density on ceramic and organic package substrates and silicon carriers [2].

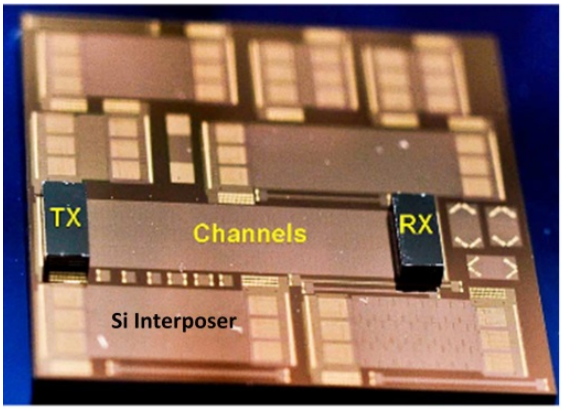
are only partial solutions, and multiple-interposer solutions will eventually become necessary.

1.1.2 Multiple Interposers

For multiple interposer systems, high-bandwidth and energy-efficient interconnects become ever more important. Figure 5 shows that the off-chip bandwidth requirement increases as the number of cores increases [8]. In fact, Figure 6 shows that interconnect bandwidth is the bottleneck that limits system throughput in a multicore system [9]. Moreover, Figure 7 shows that off-chip interconnects already represent 11.60% of the power used by the latest generation of Intel CPUs, and this figure is expected to be significantly higher for multiple interposer systems where the wire length would be significantly longer.

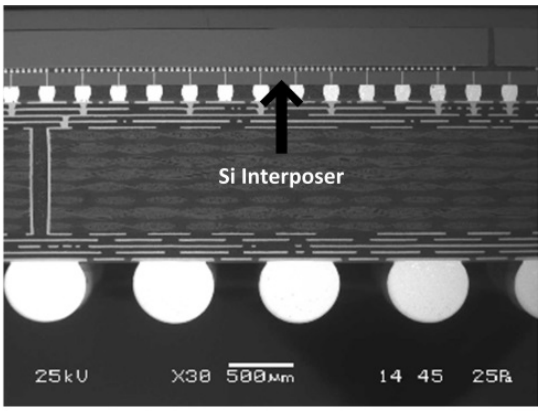
In summary, a multiple-interposer platform with high-bandwidth, low-energy interconnects for interposer-to-interposer communication is critical for future systems.

Dickson T. et. al., IEEE JSSC 2012.



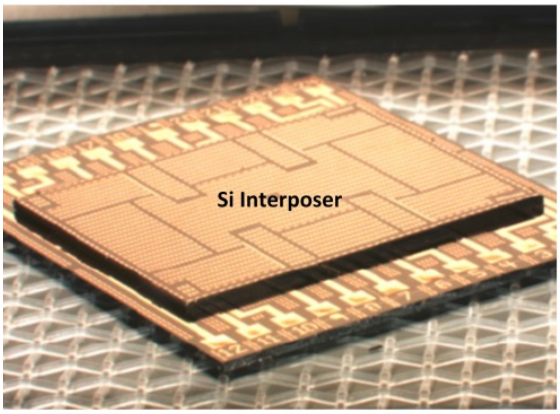
IBM Demonstrated 8x10 Gb/S Over Si Interposer

Banijamali B.et. al., ECTC 2012.



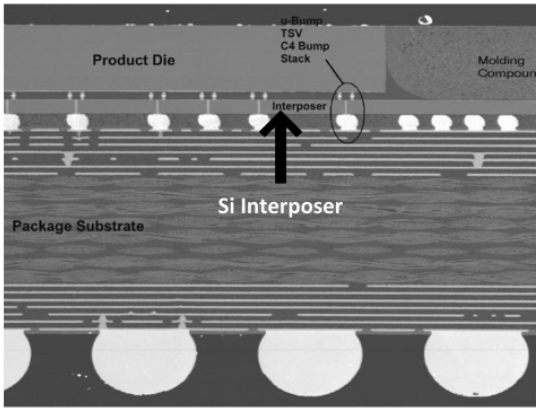
Xilinx/TSMC Demonstrated FPGA Slices Over Si Interposer with TSVs

Shubin I. et. al., ECTC 2013.



Oracle Demonstrated Thick Si Interposer with TSVs and Flexible I/Os

Rahman A. et. al., IITC 2013.



Altera/TSMC Demonstrated FPGA Over Si Interposer with TSVs

Figure 4: Single interposer systems demonstrated by industry [3, 4, 5, 6].

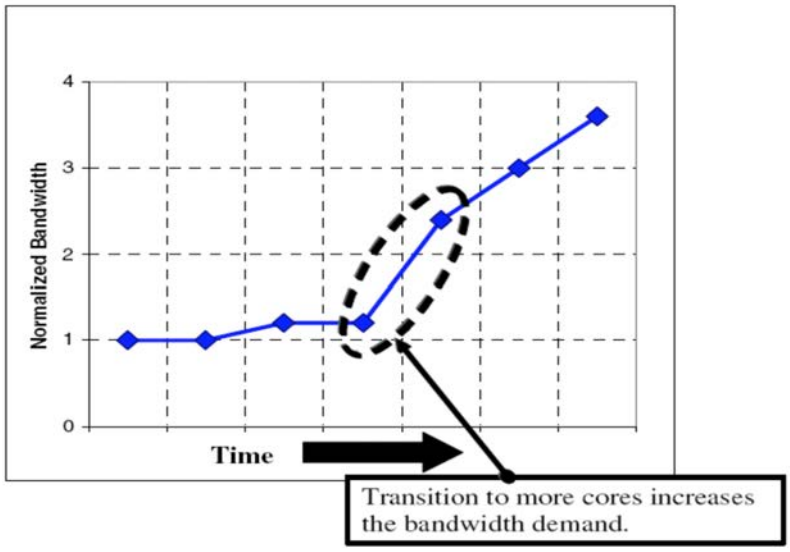
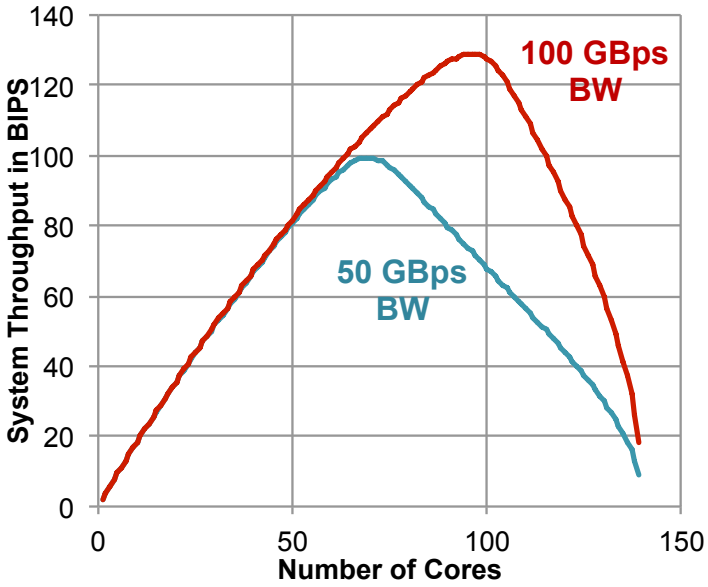


Figure 5: The bandwidth requirement is expected to rise as the number of cores is increased [8].



K. Bowman et al, Impact of Die-to-Die and Within-Die Parameter Variations on the Clock Frequency and Throughput of Multi-Core Processors, TVLSI 2009

Figure 6: For a system with a large number of cores, the throughput is limited by the system bandwidth [9].

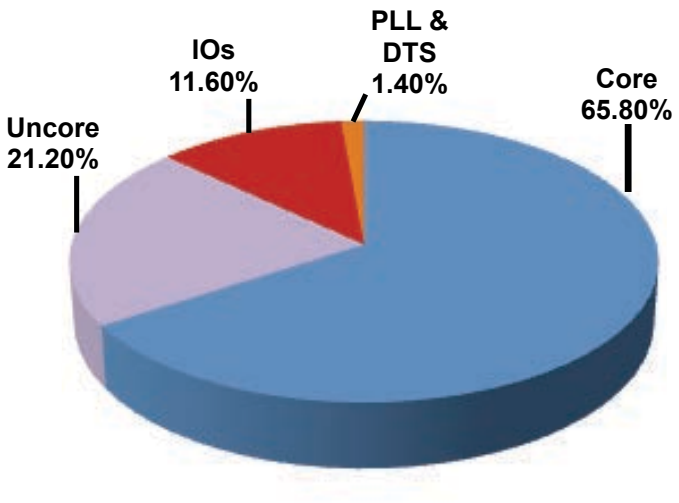


Figure 7: The amount of power used by IOs represents a significant percentage of the total power used for a single CMOS IC. For larger systems with longer interconnects, the power used by IOs is expected to increase significantly.

However, research in this area is largely missing. The development of the multiple-interposer platform, and the development of the interconnect and packaging technologies to enable such a platform, are the goals of this dissertation.

1.2 Interconnecting Multiple Interposers

Figure 8 compares two configurations for interconnecting two silicon interposers in terms of a compound metric; the compound metric is defined as bandwidth density (BWD) over energy-per-bit (EPB) [10]. The analysis show that the use of silicon bridge structures is advantageous for the electrical interconnections. For optical interconnections, the ability to form finer pitched waveguides on silicon bridges also enable higher bandwidth between interposers compared to the configurations involving fibers or polymer waveguides on motherboards Figure 9.

1.2.1 Electrical Modeling Details

The energy-per-bit is calculated by assuming a stripline structure; the pitches of stripline structures on bridges and motherboards are assumed to be 44 μm and 670 μm, respectively. The geometrical dimensions of the transmission line are used to extract R, L, C, and G parameters. The minimum driving current is determined by the receiver noise condition, and the total loss in the transmission line is calculated as described in [11]. The channel data rate used for the analysis is 10Gbps.

1.2.2 Optical Modeling Details

The pitches for the silicon waveguides, motherboard-level polymer waveguides, and optic fiber ribbon are assumed to be 10 μm, 60 μm, and 250 μm respectively. The difference in waveguide pitches are the primary cause of the performance difference between optically interconnected configurations. 10Gbps data rate and 8 WDM channels are assumed.

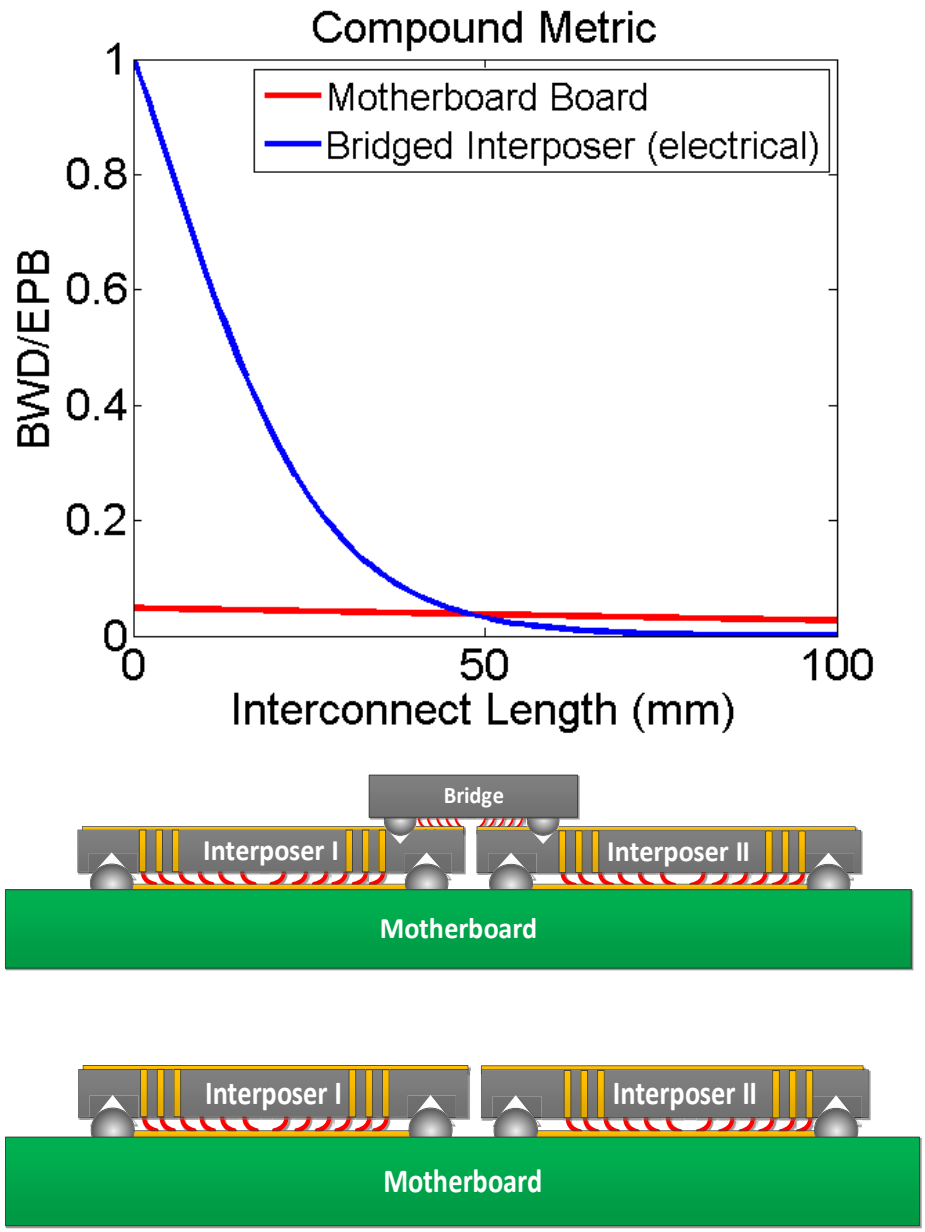


Figure 8: Comparison of a compound metric (bandwidth / energy per bit) for various multiple interposer configurations [10].

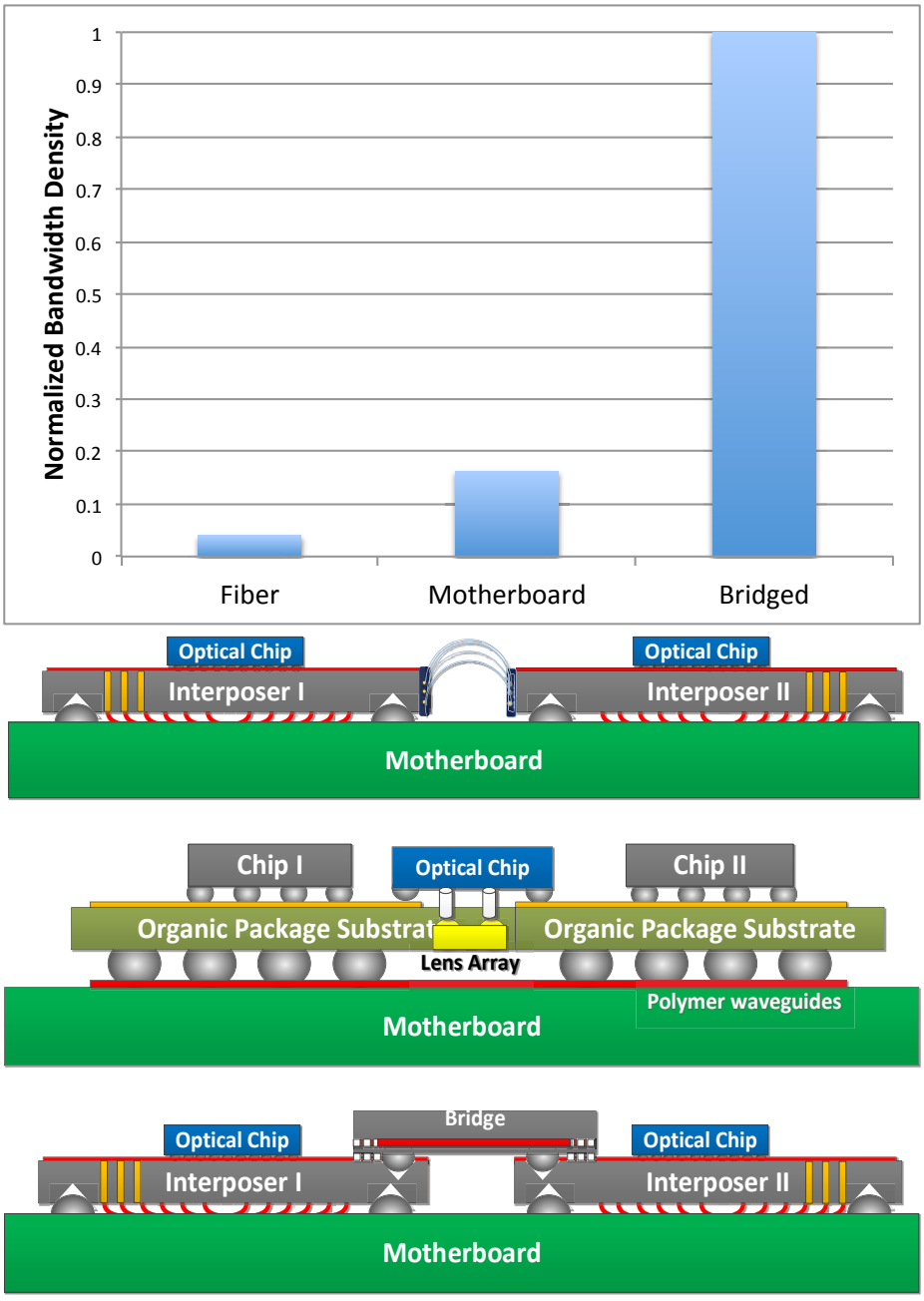


Figure 9: Comparison of bandwidth density for optical interconnections on various interposer configurations.

1.3 Expected Main Contribution

The main contribution of this work is the experimental demonstration of an ultra-large silicon interposer. The use of multiple silicon interposers mean that the available area is not limited by the yield and reticle limits, and this allows even multiple reticle-sized chips to be mounted and interconnected. To the best knowledge of the author, the 9.6cm^2 demonstrated in this work represents the largest silicon interposer area to date.

1.4 Research Statement

The objective of this research is to develop a set of interconnect and packaging technologies to enable a large silicon system composed of multiple interposers ("tiles") and silicon bridges ("bridges"), as shown in Figure 10.

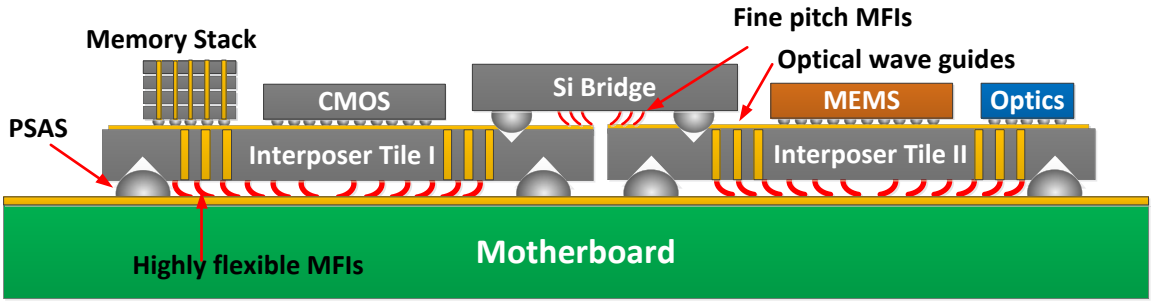


Figure 10: A novel platform with multiple interposers.

More specifically, interconnect and packaging technologies will be developed to enable:

1. area-array interconnection from the front side to the back side of an interposer;
2. rematable electrical interconnections between tiles;
3. accurate self-alignment between tiles and bridges to accommodate nanophotonics communication; and
4. replacing of tiles and bridges after initial assembly.

In addition to the design, fabrication, and characterization of interconnect and package technologies, additional experiments are performed to demonstrate each technology's versatility and compatibility with other processes.

1.5 Platform Overview

This work presents a novel large-scale silicon platform consisting of multiple-interposer tiles, which are essentially silicon interposers assembled directly on the same printed wiring board (PWB) (Figure 10) in a tile-like pattern. Electrical interconnections between the tiles are provided through silicon bridges, which are chips that are mounted on top and span two or more interposer tiles. The tiles and the bridge are electrically interconnected using mechanically flexible interconnects (MFI). In addition, the presence of silicon bridges that span the interposer tiles enables the use of other silicon interconnect technologies (e.g. silicon nanophotonics and capacitive electrical I/Os) for tile-to-tile communication. Positive self-alignment structures (PSAS) and inverted pyramid pits ("pits") passively self-align the interposer tiles with the FR4 PWB and the interposer tiles with the silicon bridges. Interposer tiles also contain TSVs, which form area-array interconnections to the motherboard for off-system I/Os.

1.5.1 Flexible Interconnects

MFIs are scalable, flexible interconnects capable of providing a large elastic and vertical range of movement. MFIs can be fabricated with solder balls at the tip for permanent assembly or with pointy tips for a low-resistance and rematable contact. There are several key advantages to using MFIs instead of rigid interconnects such as solder balls:

1. The height difference between interposer tiles can be compensated. The sources of height differences include the silicon thickness variation and the presence of features below the pads.

2. Warpage resulting from thermo-mechanical stress can be reduced.

3. Reliable contacts can be made to non-uniform surfaces, such as an FR4 substrate or a substrate that is warped due to thermo-mechanical stress.

4. Rematable interconnections enable tiles and bridges to be replaced after the initial assembly process.

While there has been significant research progress in developing novel flexible interconnects, many have focused on providing a lateral compliance. The work on increasing the vertical range of movement is largely missing.

1.5.2 Alignment and Nanophotonics

While on-chip wires have lower latency and use less power than optical links at distances shorter than the size of a single chip, beyond the distance of a few chips, aggressively scaled silicon photonic, or nanophotonic, links become significantly more efficient [7] (Figure 11); a novel silicon nanophotonic technology that consumed an energy per bit (EPB) of 300fJ/bit [12] and integrated receivers with -18.9dBm sensitivity at 5Gb/s for a bit error rate (BER) of 10^{-12} [13] has been reported.

However, a very accurate alignment between substrates is required for nanophotonics because misalignment degrades performance significantly (Figure 12). For example, a nanophotonics system using silicon-based micro-mirrors requires submicron alignment accuracy to achieve less than 3dB of optical loss and a BER below 10^{-12} [14]. Another study that used grating couplers to improve the misalignment tolerance still resulted in 1dB excess loss for a 2 μm misalignment [15]. Misalignment is also known to negatively affect the signal-to-noise ratio (SNR) of capacitive and inductive coupled interconnects [16]. Accordingly, PSAS are used to align tiles and bridges with 5 μm accuracy.

PSAS and pits aim to provide the accurate alignment needed for high-performance nanophotonics-enabled systems; an alignment accuracy of <5 μm is targeted. At the

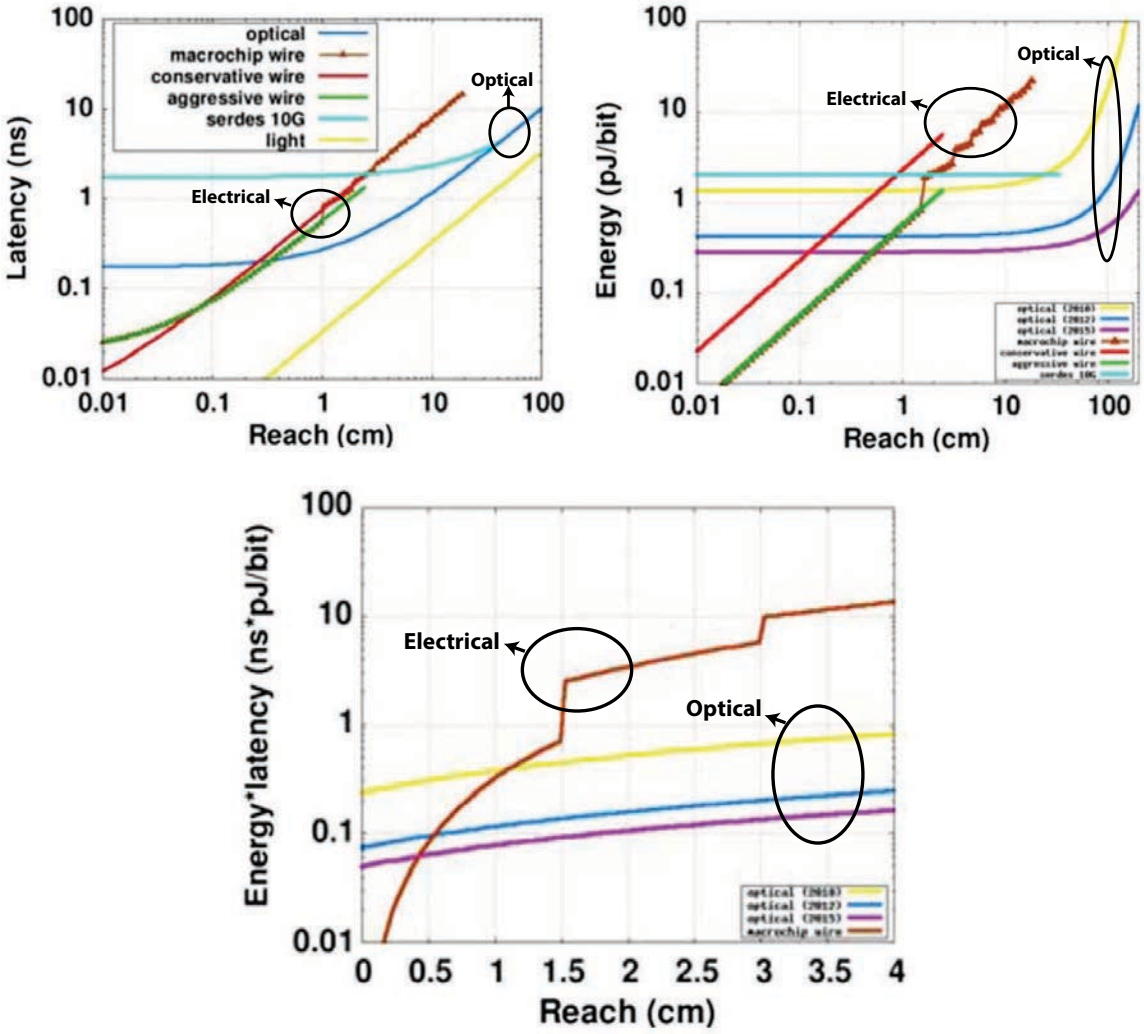


Figure 11: Comparison of electrical links with nanophotonic links [7].

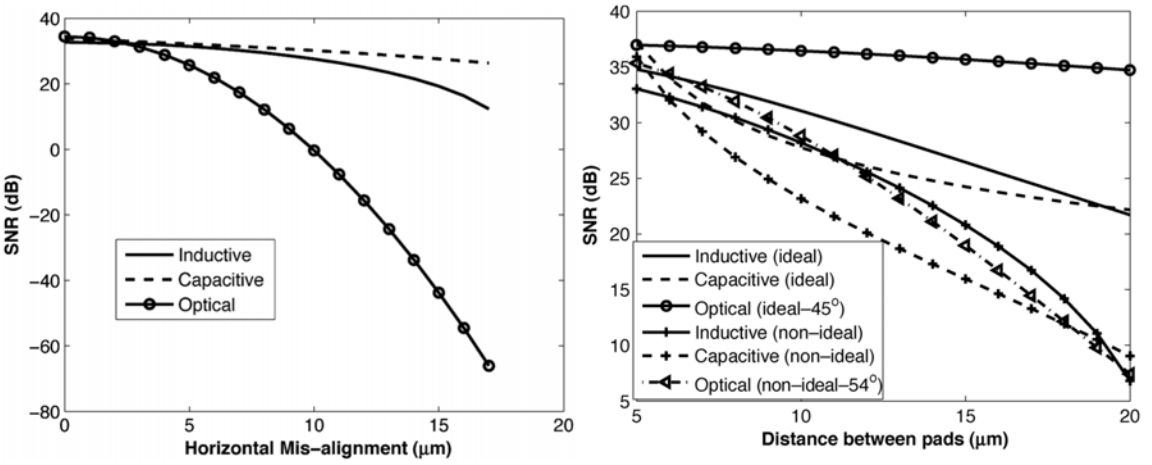


Figure 12: Signal-to-noise ratio (SNR) as a function of lateral (left) misalignment and vertical gap (right). Both electrical and optical link performances are strongly dependent on the lateral alignment accuracy as well as the vertical gap [16].

same time, its self-alignment capability allows for a low-cost assembly without using an accurate placement tool. In addition, it is compatible with MFIs to allow tiles and bridges to be replaced after initial assembly.

1.6 Organization

This document is arranged as follows:

- Chapter 2: TSV technology for silicon interposers is developed. The fabrication, testing, and process integration with a capacitive micro-machined ultrasonic transducers (CMUT) system are included.

- Chapter 3: MFIs with 20 μm + of vertical elastic range of motion is developed. A novel fabrication process, electrical testing, and mechanical simulation and testing are described.

- Chapter 4: PSAS and inverted pyramid pits are developed, and their self-alignment capabilities are characterized.

- Chapter 5: MFIs and PSAS are integrated to experimentally demonstrate a

large silicon system with multiple interposer tiles that are electrically interconnected via silicon bridges.

- Chapter 6: An elastomeric bump interposer, a component needed in packaging PSAS-enabled systems, is fabricated and characterized *.
- Chapter 7: The PSAS technology is used sacrificially to develop an improved flipchip bonding process. The PSAS technology's compatibility with a thermocompression bonding process is demonstrated.
- Chapter 8: Future research topics are discussed.
- Chapter 9: Conclusions of the thesis and the summaries of each chapter are outlined.

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CHAPTER 2

THROUGH-SILICON VIAS (TSVS) FOR SILICON INTERPOSERS

2.1 Introduction

Through-silicon vias (TSVs) (Figure 13) are batch-fabricated interconnects that enable area-array transfer of signals from one side of a silicon interposer to another. In their simplest form, TSVs are via holes in a silicon substrate that are filled with a conductive material such as copper or tungsten, and the side walls of the holes are layered with a non-conductive material, such as silicon dioxide, to prevent electrical conduction to the silicon body.

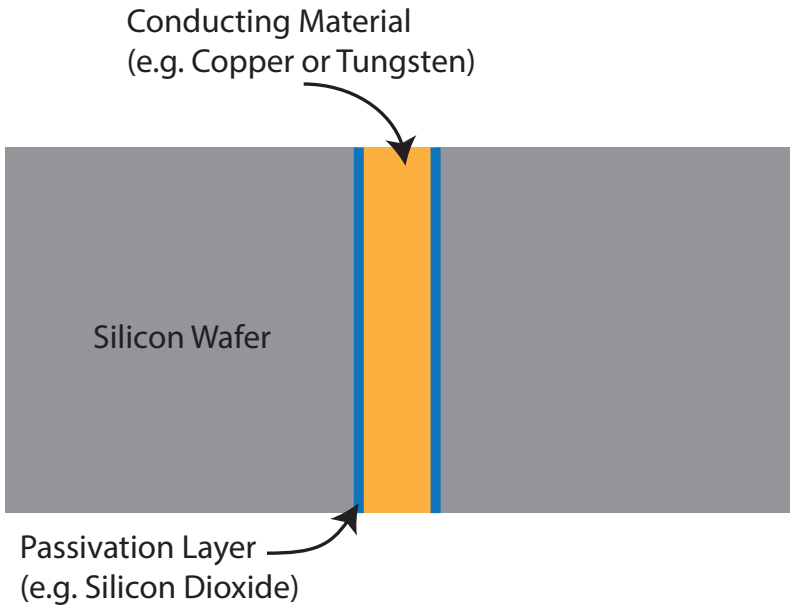


Figure 13: Cross-sectional diagram of a simple TSV.

Despite the simple structure of a TSV, there are a significant number of variations

involving different materials as well as different shapes. Some examples of TSV technologies are described in [18, 19, 20, 21]. Common variables include, silicon thickness, conductor material, and passivation material; these variables in turn affect the pitch, electrical performance, mechanical reliability, and CMOS process compatibility of the TSV technology.

One major focus in developing TSVs has been fabricating TSVs within thinned wafers. This is because there is a significant need for TSVs in stacking state-of-the-art CMOS ICs, where each IC is aggressively thinned down to 50 μm or less. In turn, many TSV fabrication technologies have taken advantage of processing technologies that are only available in thin substrate processing [22, 23, 24, 25].

However, TSVs also have significant benefits in interposer applications, where it is often undesirable to thin the silicon wafers to the extent to which the latest CMOS ICs are thinned. For example, it is shown in [26] that 300-400 μm thick silicon substrates are required for silicon interposers to be mechanically stable and sufficiently devoid of warpage due to the CTE mismatch between silicon interposers and package substrates. In addition, thick silicon wafers would also be required for integrated micro-fluidics to transport coolant to and from 3D ICs mounted on top; micro-fluidics formed inside 3D ICs have been demonstrated in [27, 28].

The ability to form TSVs in thick wafers also has benefits beyond the interposer application, where it is challenging or impossible to use thin silicon wafers. Such limitations are common in chips that contain micro-electro-mechanical systems (MEMS) and other types of sensors and actuators. For example, the ring gyroscope developed in [29] requires trenches that are hundreds of microns deep. Thin wafers are also more prone to higher levels of deflection after packaging, which causes undesirable changes in the behavior of the devices [30].

In sum, there are many applications that can benefit from being able to form TSVs in thick wafers, including in silicon interposers. However, there is yet to be

an efficient method of forming TSVs in thick wafers. In this chapter, a novel TSV technology for thick silicon substrates (500 $\mu m+$) is presented, where the "mesh" seed layer process and the two-metal electroplating process are used to address two common issues in forming TSVs in thick silicon wafers.

2.2 TSV Resistance and Capacitance

Resistance and capacitance are two fundamental electrical parameters of TSVs. This section analyzes the effect of TSV dimensions on resistance and capacitance.

2.2.1 Resistance

The DC resistance of a TSV can be approximated by assuming that the interconnect has a perfectly cylindrical structure; therefore, the DC resistance (neglecting end effects and the skin effect) in [Ω] can be expressed as:

$$R_{DC} = \rho \frac{h}{\pi r^2} [\Omega] \tag{1}$$

where ρ is the metal resistivity; h is the TSV height; and r is the TSV radius. The resistance of TSVs as a function of the diameter for various aspect ratios is plotted in Figure 14.

The figure shows that for a TSV with a given aspect ratio, resistance is decreased as the substrate thickness (i.e., the TSV's diameter) is increased.

2.2.2 Capacitance

The capacitance of a TSV is the series combination of the silicon dioxide capacitance and the depletion capacitance. The capacitance can be expressed as:

$$C_{TSV} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \text{ [31]} \tag{2}$$

$$C_{ox} = \frac{2\pi \epsilon_{ox} h}{ln(\frac{r_{ox}}{r_{metal}})} \text{ [32]} \tag{3}$$

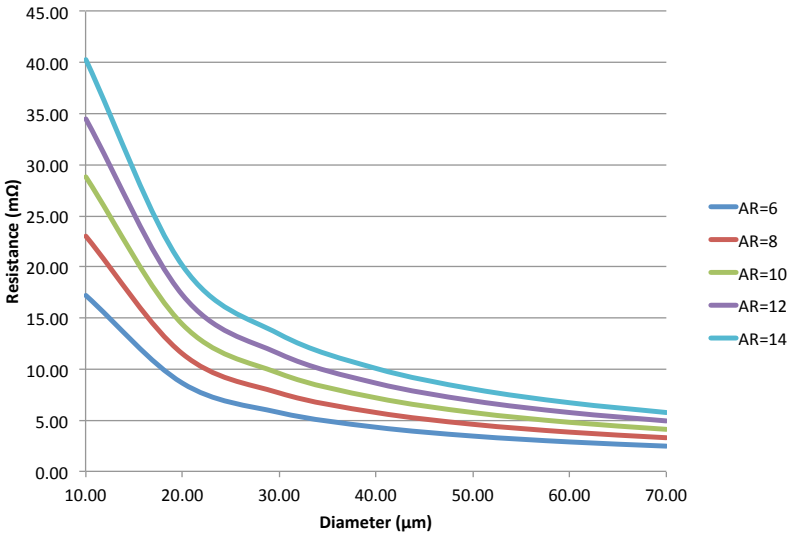


Figure 14: Resistance of a TSV as a function of the diameter (D) and the aspect ratio (AR).

$$C_{dep} = \frac{2\pi\epsilon_{Si}h}{ln(\frac{r_{max}}{r_{ox}})} \tag{4}$$

where r_{ox} is the radius of the dielectric (silicon dioxide) layer around the TSV; r_{metal} is the radius of the TSV; r_{max} is the radius of the depletion region around the dielectric layer; ϵ_{ox} is the electric permittivity of the dielectric material; and ϵ_{Si} is the electric permittivity of silicon.

The capacitance of a TSV has a non-linear relationship with the TSV voltage (V_{TSV}) because of the metal-oxide-semiconductor (MOS) capacitor that is formed by the TSV conductor material, the dielectric layer, and the silicon substrate. As a result, the capacitance is dependent on V_{TSV} and is divided into three operational regions: an accumulation region, a depletion region, and an inversion/deep depletion region (Figure 15) [32].

When V_{TSV} is in the accumulation region, where the voltage is below the flat-band (V_{FB}) voltage, majority carriers are accumulated near the dielectric-substrate interface forming an accumulation layer. As a result, the MOS capacitance can be approximated as C_{ox}, and C_{dep} can be ignored.

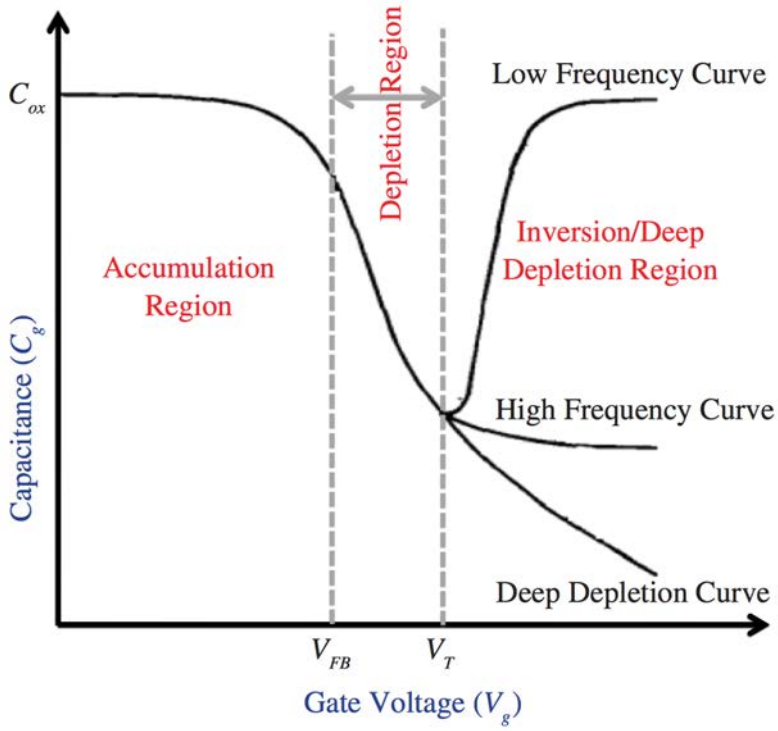


Figure 15: Capacitance of a TSV has a non-linear relationship with the TSV voltage [32].

When V_{TSV} is in the depletion region, where the voltage is between the flat-band voltage and the threshold voltage (V_T), the majority carrier is repelled away from the TSV, which forms a carrier-free region ("depletion region") around the TSV. The depletion region acts as an additional capacitor that is in series with C_{ox}. The thickness of the depletion region increases as V_{TSV} increases, which in turn decreases C_{dep}, and thus, C_{TSV}.

When V_{TSV} is in the inversion or the deep depletion region, where the voltage is above the threshold voltage, the low frequency behavior and the high frequency behavior must be examined separately. At low frequencies, minority carriers begin to be attracted towards the TSV, negating the charge of the depletion region; an inversion layer is formed, which plays the role of the bottom electrode of the C_{ox} capacitor. As a result, C_{TSV} becomes C_{ox}. At high frequencies, the minority carriers are not able to respond to the changes in the depletion caused by the rapid majority

carrier movements, which further decreases C_{TSV}.

While the exact capacitance relationship with the depletion region and the deep depletion region is complex, calculating C_{ox} is simple, and it represents a good approximation of the TSV capacitance in the accumulation region and the inversion region (at low frequencies). C_{ox} is plotted as a function of the diameter and the aspect ratio in Figure 16, which shows that the capacitance increases for thicker substrates if the aspect ratio is fixed.

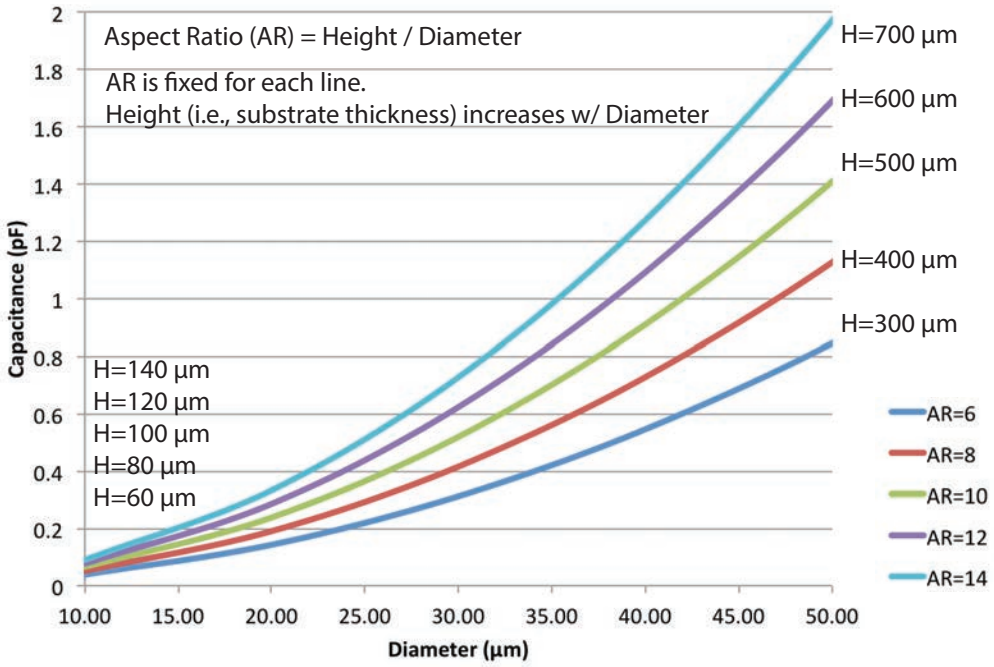


Figure 16: Capacitance of a TSV as a function of diameter and aspect ratio.

2.2.3 Estimated Electrical Parameters

The aspect ratio targeted by the TSV technology in this chapter is 10, and it is aimed for fabrication in 500 μm thick wafers. The estimated resistance and capacitance are 5.76 $m\Omega$ and 1.41 pF, respectively; a copper resistivity of 2.26 $\times 10^{-8}$ $\Omega \cdot m$, silicon dioxide relativity of permittivity of 3.9, and silicon dioxide thickness of 2 μm are assumed.

Since the dimensions of the TSVs are limited by the aspect ratio, the increase in the thickness also increases the diameter. Thus, as the dimensions increase, the resistance decreases and the capacitance increases. However, the resistance of TSVs is several orders of magnitude less than output resistance of driver circuits, and the capacitance of TSVs, especially in thick substrates, can be significantly larger than capacitances of on-chip wires. Therefore, it is primarily the capacitance of TSVs, and not the resistance, that affects the delay. To overcome TSV capacitance issue, thick polymer dielectric layers may be used to form low-capacitance TSVs, as described in Section 2.6.

2.3 Fabrication of TSVs in Thick Wafers

An electroplating process is the most common method of filling via holes in thick wafers because the volume of the conducting material required is too large for other deposition methods such as a plasma deposition or an evaporation method. To fill the via holes using the electroplating process, it is essential to form a conductive seed layer that suspends over the open via holes (Figure 17). In addition, it is necessary to planarize the excess material that is over-electroplated (Figure 18) because the electroplating process is an inherently non-uniform process in which precise control of the deposition rate across the wafer is difficult.

There have been several publications that describe the fabrication of TSVs in thick wafers using the electroplating process to fill the via holes. A representative example of such work is a TSV fabrication technique reported in [33] and described in Figure 19. In the paper, TSVs are fabricated on a 400 μm wafer by etching the via hole using a deep reactive-ion etching (DRIE) process, depositing a seed layer on one of the surfaces, and electroplating until the seed layer around the circumference of the via closes ("pinches off"). Since the diameter of the via hole is around 50 μm, the resulting metal layer is also around 50 μm. Using the new bulk metal as a seed

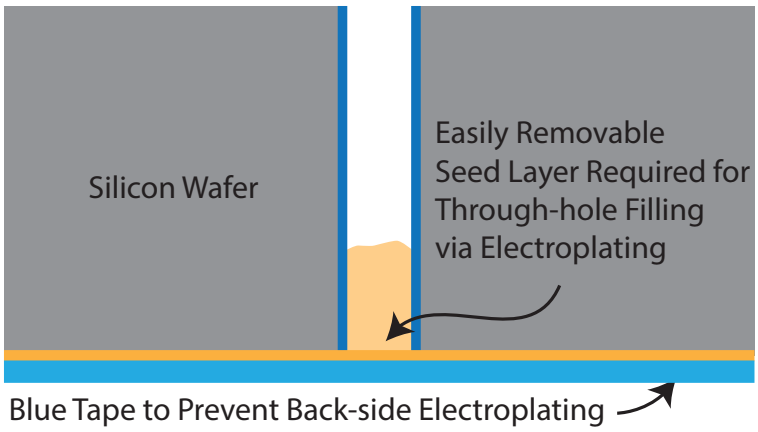


Figure 17: Ideal seed layer for filling via holes via electroplating.

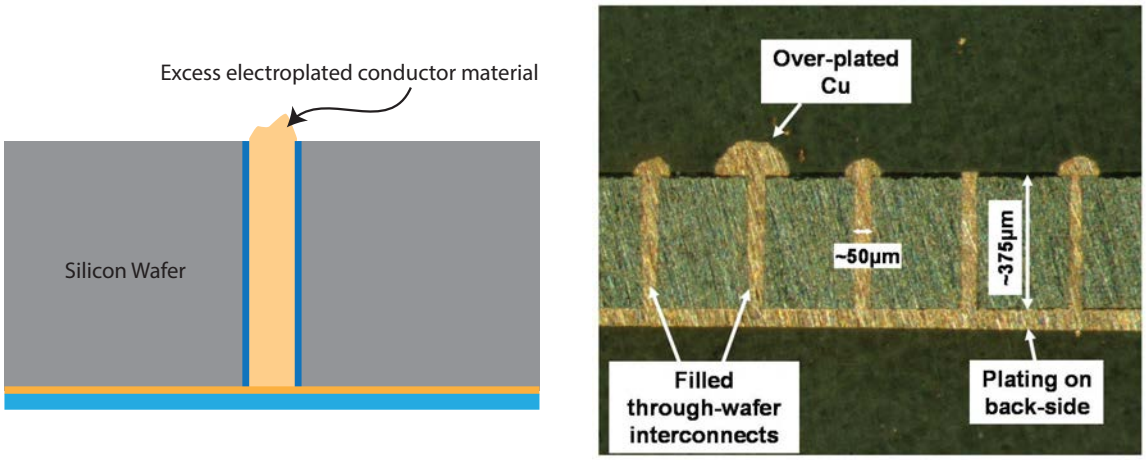


Figure 18: Excess copper resulting from electroplating is non-uniform and highly irregular. The cross-sectional image is from [34].

layer, the via hole is then electroplated with copper. A chemical and mechanical planarization (CMP) technique is used to planarize both sides of the wafer.

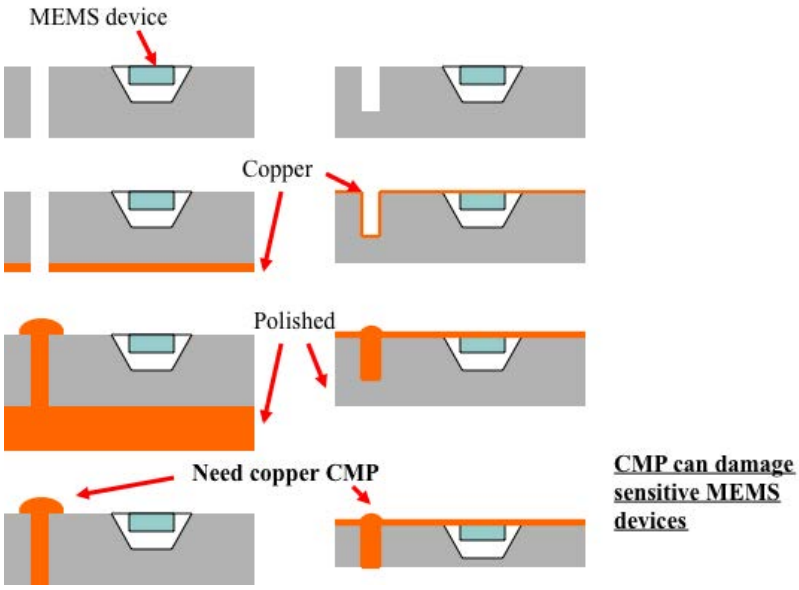


Figure 19: Conventional methods of making the seed layer for filling TSVs using electroplating result in a thick bulk metal layer that takes a significant amount of time to remove.

However, despite the seemingly simple process flow, the process requires several hours of pinch-off time and the time consuming removal of the thick bulk metal formed during the pinch-off process. In addition, CMP processes are required on both sides of the wafer, which can damage existing devices on the wafer; this becomes a significant hurdle in fabricating TSVs as the last process. The ability to fabricate TSVs as the last process is critical as many foundries do not accept preprocessed wafers because of contamination issues. In addition, the presence of copper TSVs may limit subsequent processes. For example, a high temperature process may cause chips to crack because of the mismatched CTE.

In this work, an improved method of forming and removing a seed layer for the bottom-up plating of TSVs is developed. The process diagram for the improved TSV process is illustrated in Figure 20 and Figure 21. The process enables the fabrication of TSVs in thick wafers without prior thinning of the wafers. Therefore, it can be used

in applications where wafer thinning is not an option. The technology also features a "mesh" seed layer, to reduce pinch-off time and a non-mechanical planarization process to allow removal of the excess copper without damaging sensitive features, such as passives on silicon interposers.

2.3.1 Novel TSV Fabrication Process using "Mesh"

The TSV fabrication process using the mesh seed layer is described in Figure 20. The process begins by forming a SiO_2 layer on top of a silicon wafer via a PECVD or a thermal oxidation process. The layer is used as a stop layer in the subsequent DRIE process that forms the via hole; a suspended SiO_2 layer is formed upon the completion of the etch process. It is vital that ultrasonic processes are not used from this point until the via holes are completely filled.

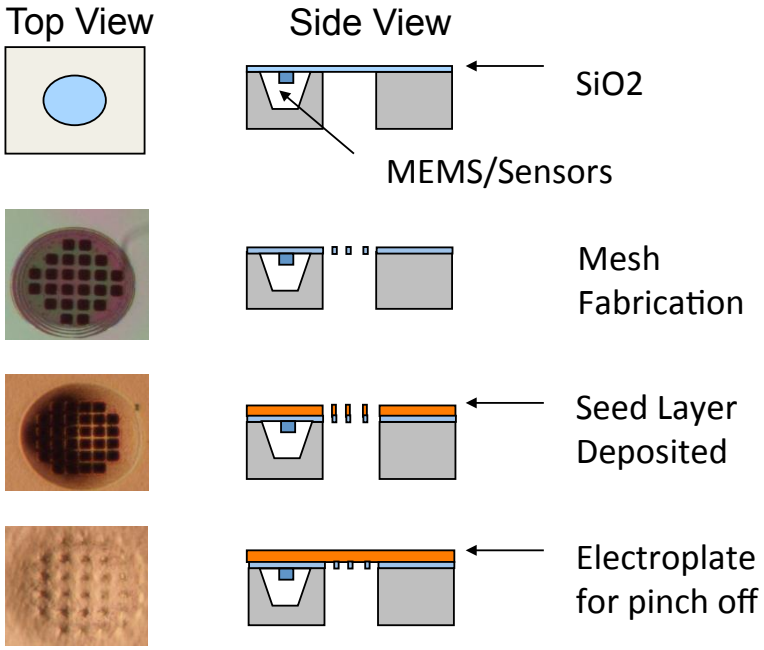


Figure 20: The "mesh" TSV fabrication process enables efficient formation of seed layer in large diameter TSV holes. It also allows planarization of the device side with excess copper without using the detrimental CMP process.

A mesh pattern is etched on the suspended SiO_2. Experiments show that the thickness of the suspended SiO_2 layer can range from 1 μm to 4 μm. A thinner SiO_2

layer results in breakage during subsequent processes, while a thicker layer makes it difficult to form the mesh pattern as the photoresist-to-SiO_2 etch selectivity is low. Experiments also show that a 3 μm mesh grid size is optimal [35]; smaller grids have been determined to be mechanically unstable, which results in breakage. The side wall passivation layer can be formed at this stage. A thermal oxidation process can be used to grow a high-quality silicon dioxide layer, or a low-temperature PECVD process can be used to enable the post-CMOS fabrication of TSVs.

A metal seed layer is deposited on top of the mesh layer. An e-beam evaporation process is used to minimize the metal deposition inside the via hole because the deposition of metal on the side wall at this stage can cause air to be trapped during the electroplating process that is used to completely fill the via hole. Copper is used as the seed metal layer in this work, however it is possible to use other materials that can be wet etched. A short electroplating process closes the mesh holes by depositing the metal laterally from the edges of the mesh holes. The newly formed metal is now exposed from the inside of the via hole.

The surface of the wafer with the SiO_2 mesh layer is covered using a blue tape to prevent further electroplating on top, and another electroplating process is performed with the SiO_2 layer facing away from the electrode. The process begins filling the via holes from the exposed metal through the mesh pattern. The fabrication results show that the presence of the mesh oxide patterns does not create voids during the electroplating process, as shown in Figure 22.

Two different metals are used to electroplate the via hole. The first metal is used as a wet etch stop layer, and a 2-3 μm layer is electroplated first. Then, the second metal fills the rest of the via hole. Using the two metals to fill the via hole allows the seed layer to be etched chemically. In choosing the two metals, it is imperative that the first metal is not etched in the etchant that is used to remove the seed-layer material. In this work, nickel is used as the stop layer, and copper is used to fill the

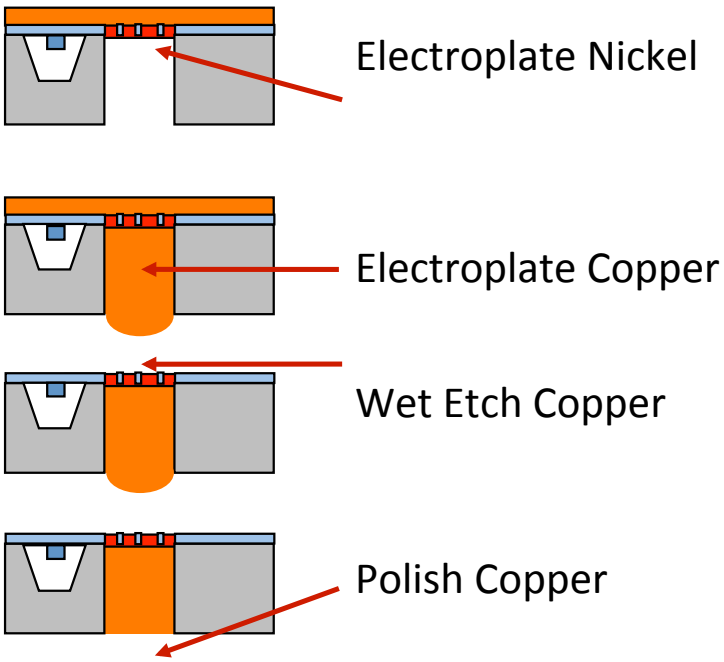


Figure 21: The "mesh" TSV fabrication process enables efficient formation of seed layer in large diameter TSV holes. It also allows planarization of the device side with excess copper without using the detrimental CMP process.

via hole; copper etchants, including diluted sulfuric acid and APS Cu Etchant, do not etch nickel.

After electroplating the via holes using this approach, the blue tape is removed, and the wafer is dipped in a bath containing a copper etchant. The wafer is removed from the bath once the seed layer removal is visually confirmed (i.e., the nickel stop layer becomes visible). The excess copper that is electroplated on the back side of the wafer is removed using a chemical and mechanical planarization (CMP) process. The Cu CMP slurry from Cabot electronics and polyurethane pads are used for the CMP process.

2.3.2 Mesh for Efficient Seed-layer Formation

The major benefit of the mesh process in this work lies in its ability to form the seed layer for the via filling process efficiently. Because of the small mesh hole openings, pinch-off time is significantly reduced, and the thickness of the resulting metal layer

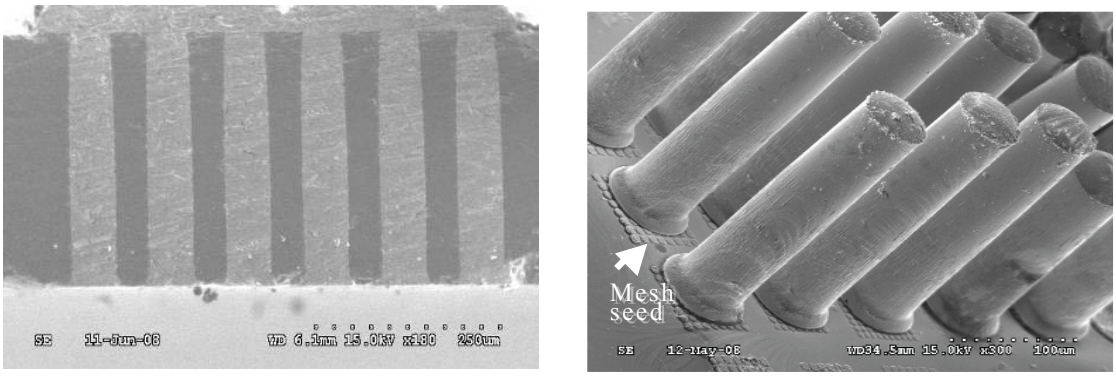


Figure 22: The cross-sectional image of a silicon chip containing TSVs shows that despite using "mesh" technique, the TSVs are electroplated to completely fill the via hole without voids.

is also reduced. The thin metal layer, in conjunction with the two-metal process described next, can be removed quickly using a wet etch process.

2.3.3 Two-metal Process to Eliminate CMP Process

The electroplating of nickel prior to the filling of the via hole with copper enables planarization of the mesh side of the wafer using a wet etch process. This is critical for applications where TSVs are fabricated last, as many devices can be damaged during the CMP process.

2.3.4 Low-Temperature Side Wall Passivation

There is a wide range of options for forming a side wall passivation layer. One common method is thermally growing a silicon dioxide layer; however, this approach is performed in a high temperature environment and may not be compatible with temperature sensitive wafers, such as wafers with CMOS circuits. As a result, it is critical to demonstrate a method of forming a side wall passivation layer using a low-temperature process.

In this work, silicon dioxide and/or silicon nitride layers are formed using a plasma-enhanced chemical vapor deposition (PECVD) tool. PECVD processes, unlike thermal oxidation processes, have relatively poor conformal deposition capabilities, especially in deep trenches, such as inside high-aspect-ratio TSV holes. As a result, two PECVD deposition processes are performed from each side of the wafer. First, 2 μm of SiO_2 is deposited from the back side of the wafer. It is possible to see, after the first deposition step, that the "mesh" hole becomes smaller, which indicates that the deposition does occur at the deepest part of the via hole. However, the hole only becomes smaller by less than 2 μm, indicating that the deposition rate is slower at the bottom of the via hole.

After the initial PECVD deposition, the wafer is flipped with the mesh layer facing the top, and another 1 μm of SiO_2 is deposited. The deposition through the "mesh" side is possible because of the mesh hole openings.

2.4 Electrical Verification

2.4.1 Resistance

The resistance of a single TSV is measured using a sample with the oxide mesh and the seed layer still intact. Two measurement configurations, as shown in Figure 23, are used to measure the resistance of the seed layer connecting two adjacent TSVs, and the resistance of a TSV and the seed layer between the two vias. The first measurement is then subtracted from the second measurement to yield the resistance of a single TSV only.

The average resistance from four randomly chosen locations for measuring the seed layer resistance is 9 $m\Omega$ +/-1 $m\Omega$. The average resistance of the same set of TSVs with the seed layer is 17.75 $m\Omega$ with the lowest and highest measured values being 16 $m\Omega$ and 21 $m\Omega$, respectively. To approximate the resistance of a single TSV, the two averages can be subtracted to yield a value of 8.75 $m\Omega$. The measured

resistances of the TSVs include the oxide mesh, and as a result, these results reflect more on the uniformity of the plating process than the resistance of each via.

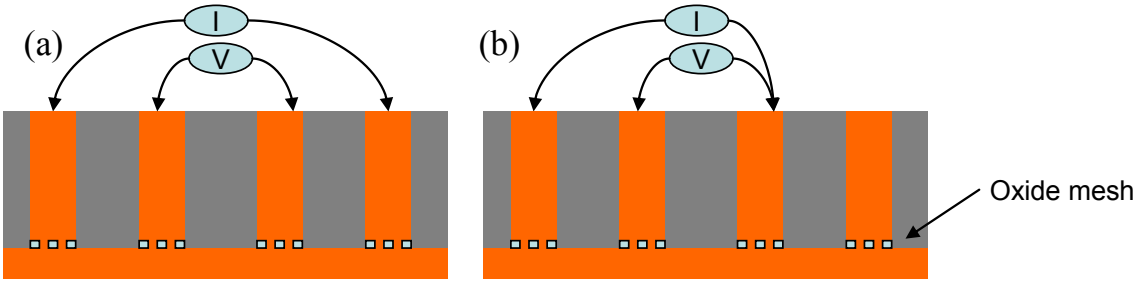


Figure 23: Experimental setup of TSV resistance measurement.

2.4.2 Leakage Current between TSVs

To determine the quality of the side wall passivation layer and to make sure that the film deposited is not porous, a leakage test was performed between two adjacent TSVs. The result is shown in Figure 24. The graph shows that the PECVD side wall passivation method results in a nano-ampere range of leakage between two TSVs with 200V bias. Breakdown of the passivation layer is not observed during the 0V to 200V sweep.

2.5 Capacitive Ultrasonic Micro-machined Transducers

This section describes the integration of the "mesh" TSV process with a monolithically integrated capacitive ultrasonic micro-machined transducers (CMUTs) technology for intravascular ultrasonic (IVUS) imaging applications. The key demonstration is the CMOS process compatibility of the TSV process that enables TSVs to be fabricated post CMOS. The CMOS compatibility is relevant for interposer applications because some applications require active silicon interposers such as the one described in [36]. This work is performed in collaboration with Professor Degertekin's research group at Georgia Tech's School of Mechanical Engineering, and the detailed work relating to the CMUT technology is described in [37].

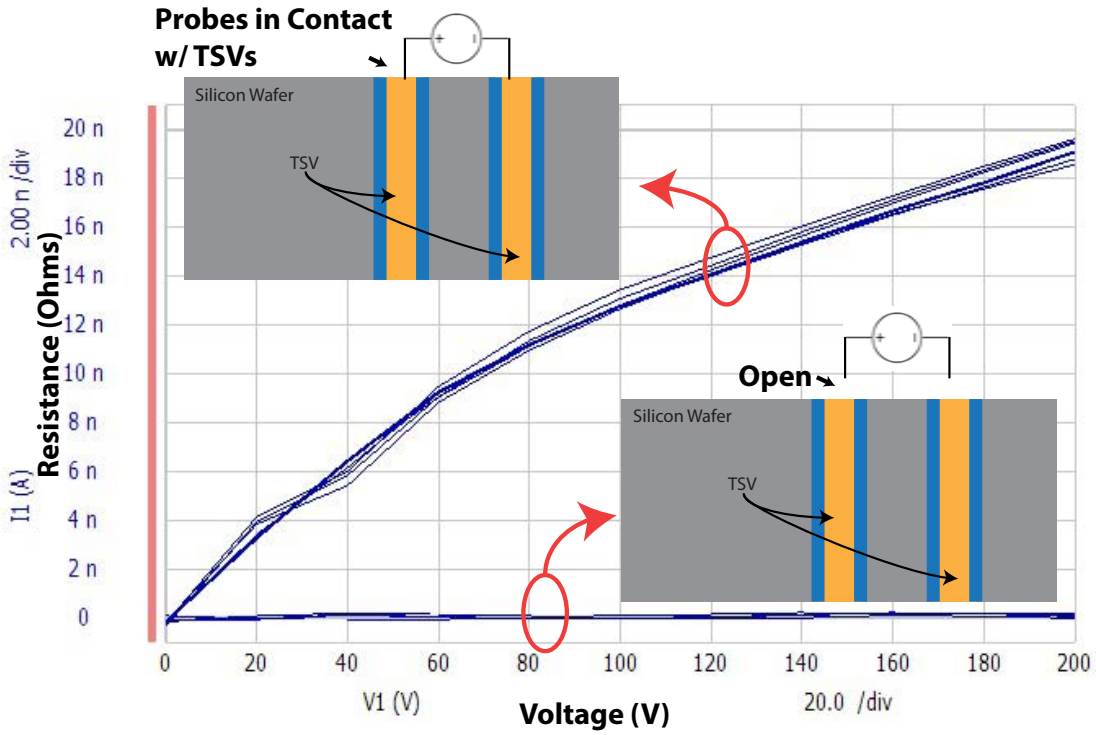


Figure 24: The graph shows the leakage current between two TSVs fabricated in blank Si wafers using the "mesh" process. TSV side walls are passivated using the PECVD process.

2.5.1 CMUT System Background

The IVUS system in this work includes one dual ring array for forward-looking imaging and four annular ring arrays for side-looking imaging in coronary arteries. The aim of this work is to integrate the five CMUT arrays into an IVUS catheter 1-2mm in diameter. To achieve the small form factor needed for this application, multiple CMUT arrays are assembled on a single flexible tape substrate, which is folded as shown in Figure 25.

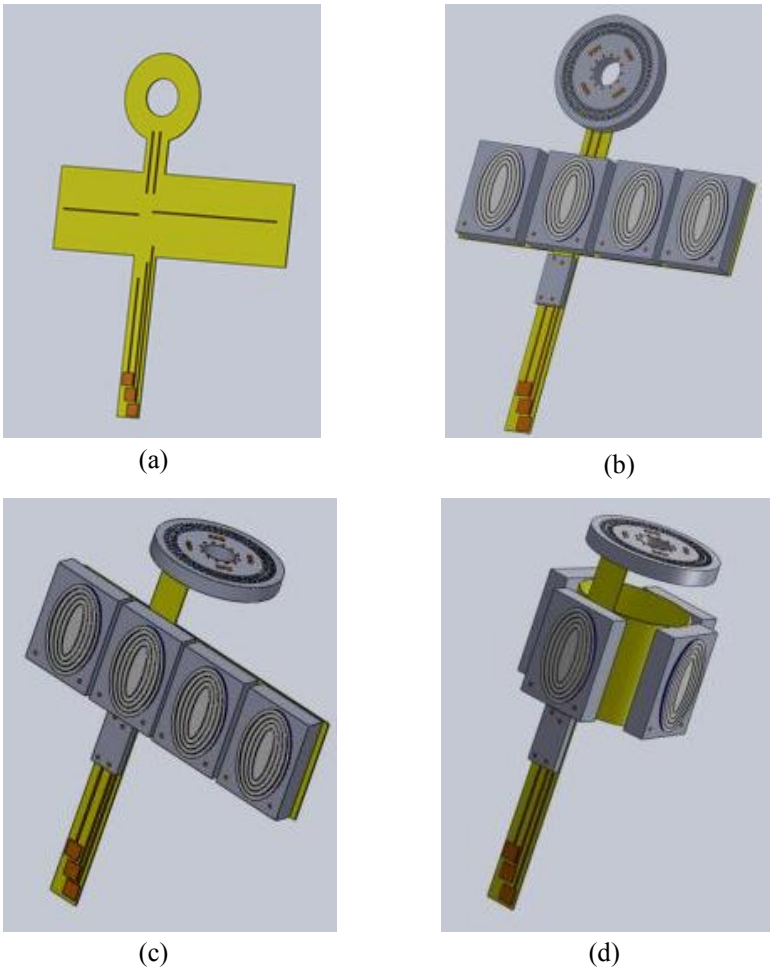


Figure 25: One forward-looking dual ring CMUT arrays and four side-looking annular ring CMUT arrays are assembled to a single flexible substrate that is then folded to fit inside a 1-2mm IVUS catheter [37].

One of the key challenges in building the IVUS system is in the assembly of integrated CMUT arrays onto the flexible substrate. The challenge is that the CMUT arrays must face outwards for imaging, but the electrical interconnections must interface with the flexible substrate from the back side of the chip. Therefore, novel electrical interconnect structures are needed to transfer the signal from the front to the back of the chip.

There have been two notable attempts at addressing this issue. The first approach involves a flex tape connection (which is different from the flexible substrate) to the front of the chip where the CMUT array is located; the tape is then passed through the openings in the silicon to the back for connections to the electrical wires on the flexible substrate (Figure 26). This approach requires careful micro-manipulation of the flex tapes, which makes the process very complex and potentially unsuitable for mass production.

The second approach involves the use of a TSV technology (Figure 27). However, previous attempts involved the fabrication of TSVs in CMUT arrays that have not been integrated with CMOS electronics [38]. As a result, the presence of TSVs between the CMUT array and the electronics introduced extra parasitic capacitance, which affected the CMUT performance significantly because the CMUT's transducer capacitance is in the sub-picofarads range.

In this work, TSVs are fabricated in integrated CMUT arrays. Therefore, the associated parasitic capacitance is inserted after the signal amplification and the buffering stages, which makes the impact of the parasitics negligible.

2.5.2 Fabrication

The fabrication of TSVs begins on a 0.35 μm CMOS wafer taped out from TSMC (this work was done on a diced piece); FEOL, BEOL, and the final CMP process are performed prior to the TSV fabrication. The inter-level dielectric (ILD) material used

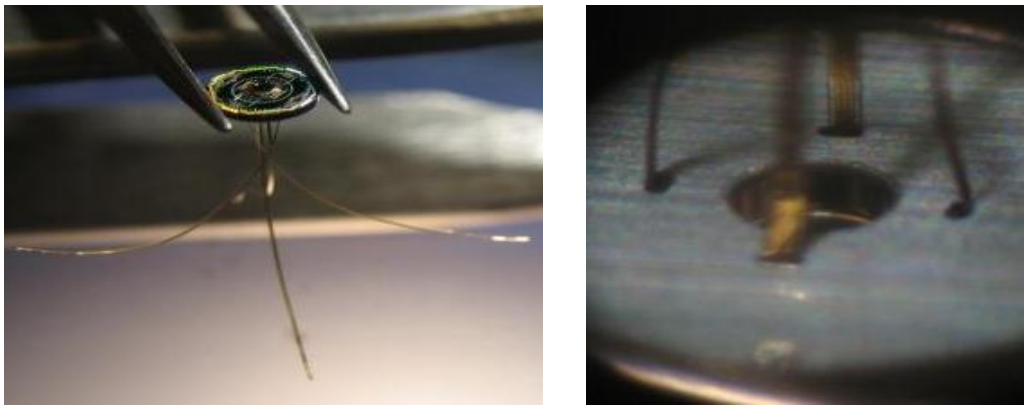


Figure 26: The previous approach involved flex tapes connected to the CMUT array at the front and routed through holes in the silicon to the back [37].

by the manufacturer is unknown; however, experiments suggest that it can be etched by a reactive ion etching (RIE) tool and that it has a thickness of 10 μm (Figure 28).

DRIE Etch TSV holes are patterned on the back side of the CMOS wafer piece. A back side alignment (BSA) technique is used to align the TSV holes to the CMOS features that are only visible from the top side. Figure 29 shows TSV holes that are patterned on the back (unpolished) side of the CMOS piece.

Using the patterned photoresist, a DRIE tool (STS-ICP) is used to etch the silicon. The etched holes are 50 μm in diameter and 300 μm in depth. The ILD is used as the etch stop layer, and the holes become visible from the front side once the entire depth of the silicon is etched (Figure 30).

Mesh Formation Forming the mesh layer on the thick ILD layer is a challenge because of the poor selectivity between the photoresists and the ILD during the RIE etching. As a result, a new mask material with a higher selectivity is used.

A chrome film is selected as the mask material because of its high selectivity and its ability to be patterned using a wet etchant. The thickness of the chrome layer required to withstand the etching of 10 μm of ILD is experimentally determined to be 500nm. However, at this thickness, chrome is opaque, and this makes it impossible

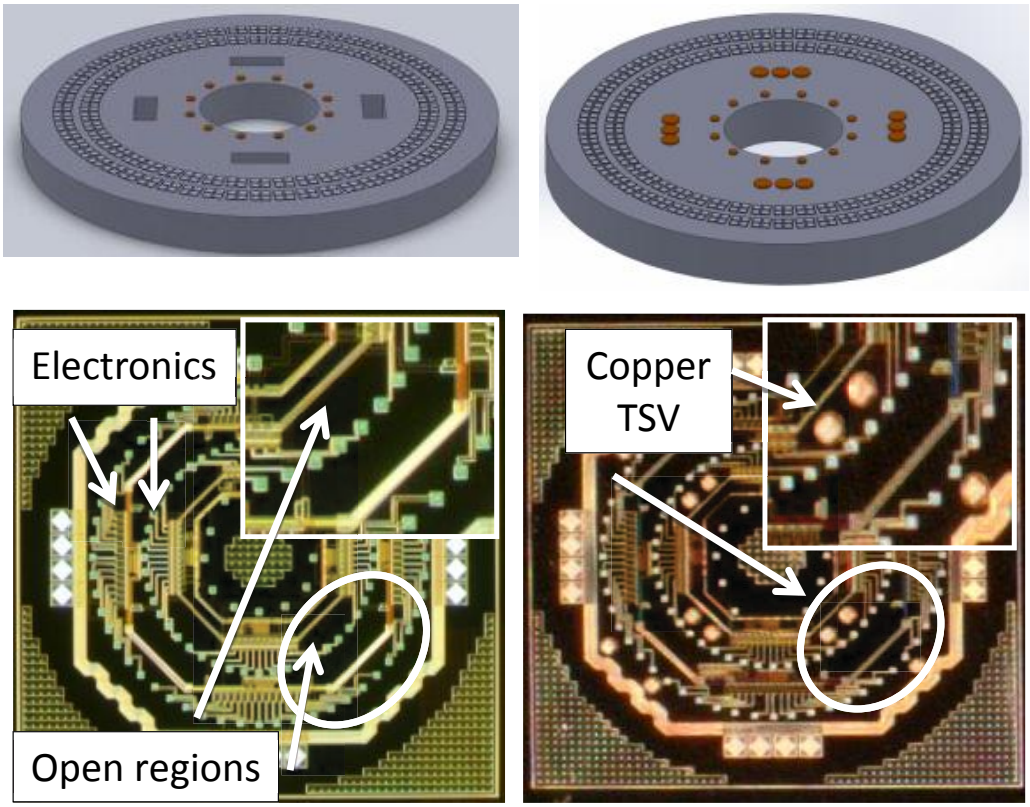


Figure 27: Images showing the regions used on the CMOS IC for flex tape routing (left) and TSVs (right) [37].

to align the mesh pattern to the underlying TSV holes that are otherwise visible through the ILD layer. Therefore, the first step is to etch the ILD (200nm only) with the TSV hole pattern; the small step height causes the chrome layer to become visible for alignment with the mesh patterned mask in subsequent photolithography steps. Piranha cleaning is performed before the deposition of the chrome layer.

The chrome layer is deposited using a sputterer, but it can also be deposited using an e-beam evaporator or other low-temperature deposition process. The mesh photoresist layer is patterned on top of the chrome layer, and the chrome layer is etched with a wet etchant, CR-7S. Once the mesh pattern is formed on the chrome layer, the ILD layer is etched with an ICP RIE tool. The recipe used for the etch process is shown in Table 1. Once the mesh pattern is etched on the 10 μm ILD layer, the photoresist and the chrome layer are removed. Piranha cleaning is performed once

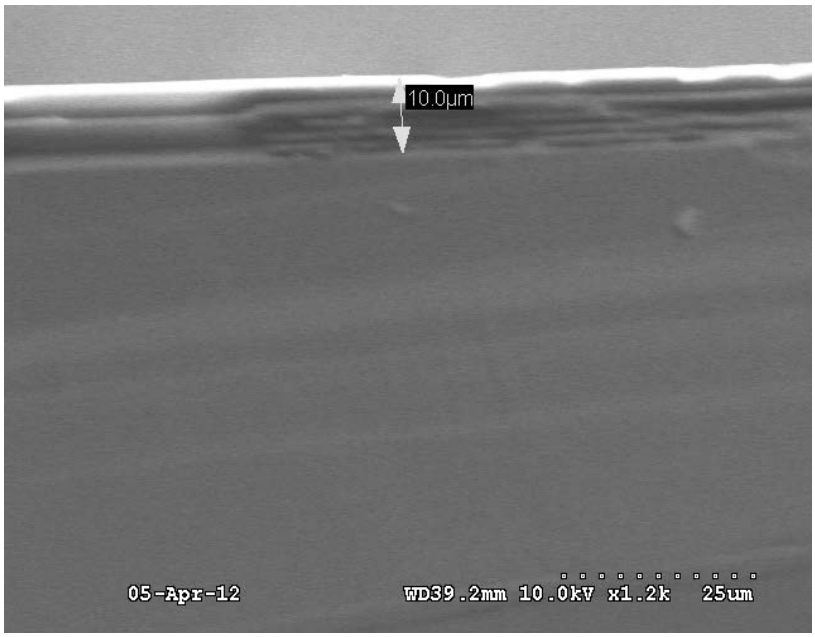


Figure 28: SEM showing the thickness of the ILD layer in the CMOS IC.

again.

Table 1: Plasma-Therm ICP Process Parameters

Parameters	Value
C_4F_8	15 sccm
CO_2	28 sccm
Ar	5 sccm
Pressure	5 mTorr
RF1	40 Watt
RF2	800 Watt

Side Wall Passivation Despite the simplicity of forming the side wall passivation layer using a thermal oxidation process, this process is performed in a high-temperature environment (greater than 1000 °C) and is not CMOS compatible. In this work, PECVD is used to deposit the silicon dioxide passivation layer at 250 °C.

Due to the poor conformal deposition that is possible with a PECVD tool inside deep trenches, the passivation layer on the side wall is deposited in multiple steps from both sides of the sample with piranha cleaning steps in between. First, 2-3 μm of

Figure 29: Back side of the sample showing 50 μm TSV holes patterned on NR5-8000P photoresist.

silicon dioxide is deposited on the front side. Second, 1-2 μm of silicon dioxide is deposited on the back side. Third, 0.5 μm of silicon nitride is deposited on the back side. Lastly, 0.5 μm of silicon nitride is deposited on the front side. Figure 32 shows that the mesh pattern remains open after the PECVD passivation step.

The remaining steps are performed in the same manner as described in the prior section on the TSV fabrication. Figure 33 shows the samples after the via hole filling processes. Chemically removing the seed-layer and the excess electroplated copper on the front side reveals the undamaged ILD surface (Figure 35). The undamaged ILD surface is critical for the subsequent fabrication of CMUT arrays on top.

2.5.3 Verification

The fabricated TSVs are tested electrically with no dielectric breakdown through the substrate up to 200 V DC, which is the operating voltage of the CMUT devices used in this work. To attain TSVs with low leakage current that is required for this application and to compensate for the relatively lower quality dielectric layer that

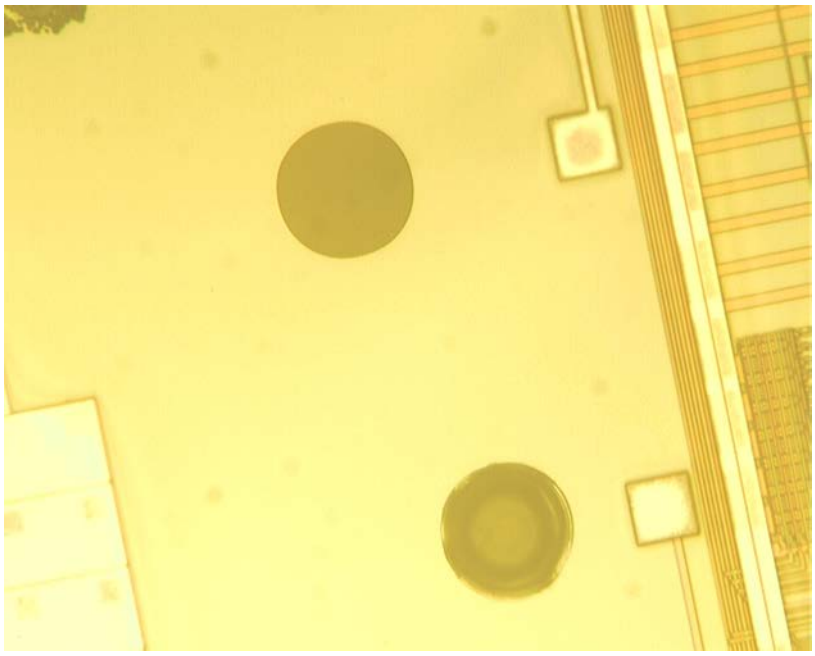


Figure 30: Microscope image from the front side of the wafer after the via holes have been etched.

is deposited by PECVD, the overall thickness of the deposited passivation layer is significantly increased compared to the TSVs in Figure 24. As a result, the leakage current between TSVs has been shown to be in the nano-ampere range at a 200 V bias, which is a sufficiently low for the CMUT system in this work (Figure 37). In addition, this result passes the failure criteria defined in [39]; failure is defined as having a leakage current above 1nA at 2V bias.

Figure 24 shows that a small amount of current flows (at 1pA/V) when the dielectric layer is probed directly. Unchanged results after multiple measurements indicate that breakdown of the dielectric layer is unlikely; instead, the leakage may be attributed to the imperfections such as poorly covered region around the edges of the via hole.

Finally, the testing of the CMOS electronics, measured after the TSV fabrication, shows that the current draws of the CMOS circuits are not changed across multiple samples. This verifies that the TSV process is compatible with CMOS processes.

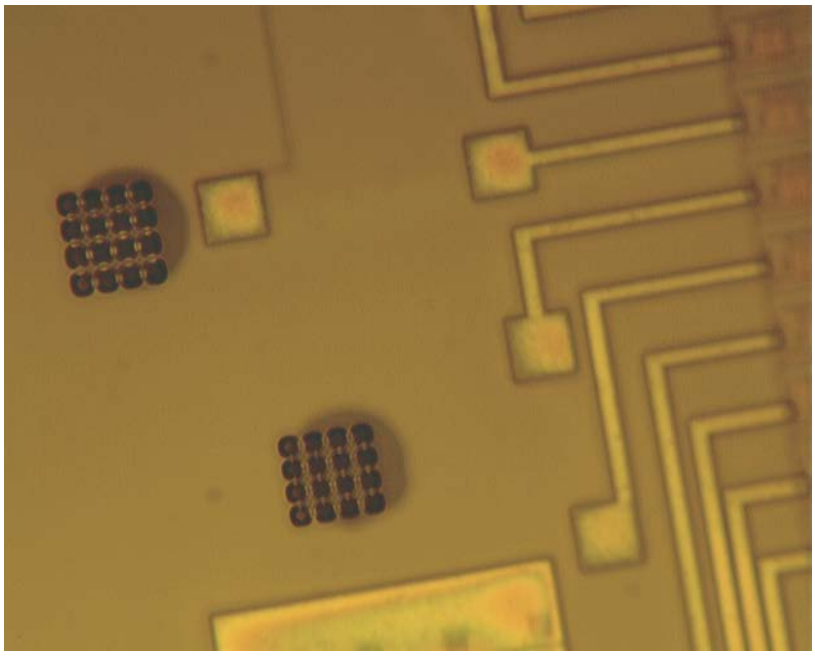


Figure 31: Mesh pattern is etched on top of the TSV hole.

2.6 Extended Work: Polymer-clad TSVs

The "mesh" TSV technology can be easily extended to form polymer-clad TSVs, as shown in the work by Professor Bakir's group at Georgia Tech's School of Electrical and Computer Engineering. This section demonstrates the versatility of the "mesh" TSV process. A detailed description of polymer-clad TSVs is provided in [40].

Polymer-clad TSVs are TSVs with a side wall passivation layer made of a thick polymer layer. Compared to a thin ($<1\ \mu m$) silicon dioxide layer, the thick polymer layer reduces thermo-mechanical stress. This is because the Young's modulus of the polymer is lower than the moduli of copper and silicon [41]. In addition, the thicker side wall passivation layer results in a reduced dielectric capacitance and a reduced high-frequency loss.

This work is of particular interest for silicon interposer applications because the aspect-ratio limited TSVs in thick silicon interposers are tall. This leads to an increase in TSV capacitance and RF losses [42, 43]. Moreover, the larger TSV diameter increases the likelihood and severity of thermo-mechanical stress-induced reliability

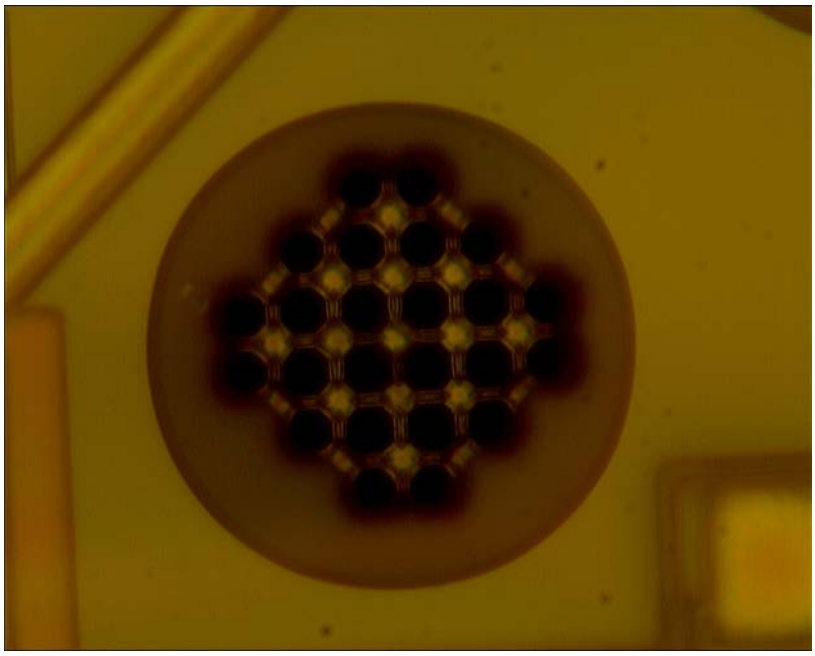


Figure 32: The mesh opening remains open after the PECVD passivation process step.

issues, such as cohesive cracks in silicon and interfacial delamination [44], compared to smaller TSVs in thinner substrates

The fabrication process for the polymer-clad TSVs is shown in Figure 38. The process begins on a blank wafer with a layer of silicon dioxide. SU-8 material is spin-coated and an optimized baking process is performed to ensure that the SU-8 material fills the etched via hole. The openings on the "mesh" oxide layer are critical in preventing air from becoming trapped inside the via-hole during this process.

The SU-8 material that fills the via holes is photolithographically defined and developed in an SU-8 developer solution. The exposure is performed from the "mesh" side of the wafer because of that side's smoother surface compared to the non-mesh side. Following the SU-8 cladding formation, the electroplating step is performed as described in the prior section describing the TSV fabrication. Completed polymer-clad TSVs are shown in Figure 38.

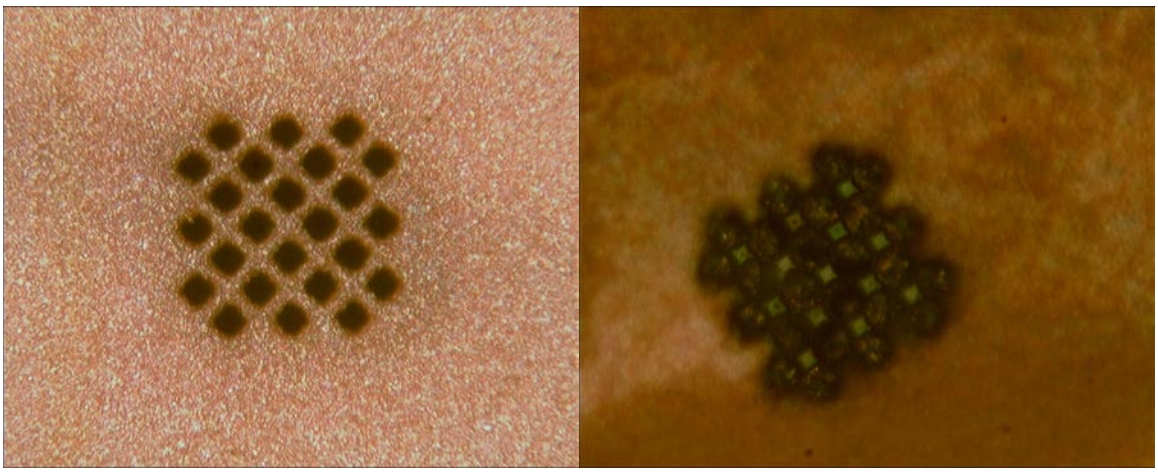


Figure 33: The left image shows the mesh holes after the seed layer deposition. The right image shows the closed mesh holes after the "pinch-off" process.

2.7 Conclusion

A novel TSV technology for thick silicon interposers is demonstrated. The "mesh" technique makes the seed-layer formation efficient, and the chemical-only planarization becomes possible by electroplating with two metals. The benefits of the developed TSV process are demonstrated in two ways. First, the CMOS compatibility of the process is demonstrated by fabricating the TSVs in TSMC 0.35 μm CMOS ICs. Second, the versatility of the "mesh" process is demonstrated by extending the technology to form polymer-clad TSVs.

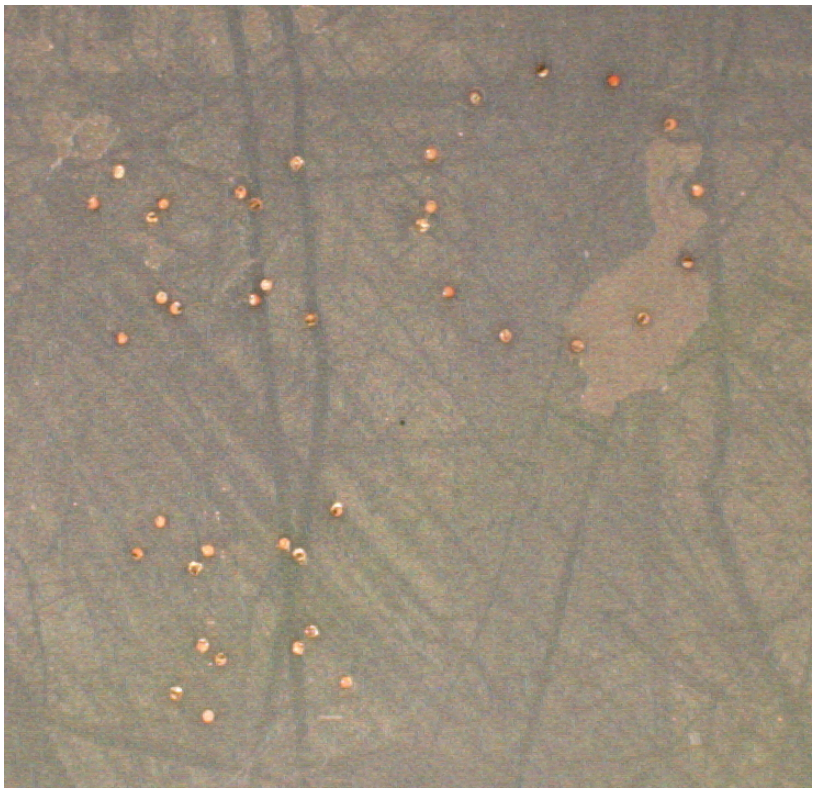


Figure 34: Microscope images from the back of the CMOS IC shows that TSVs are completely filled.

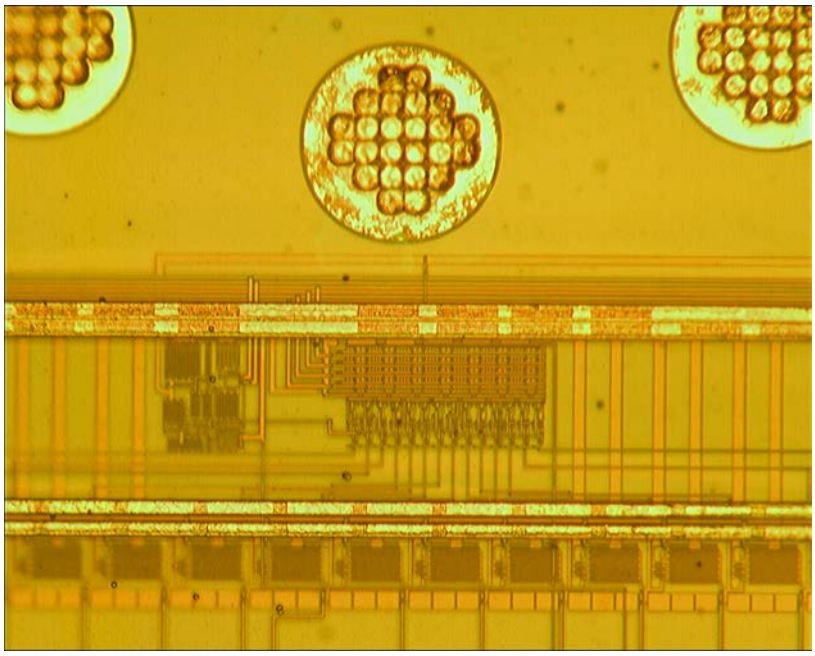


Figure 35: A microscope image showing the CMOS metallization layers and completed TSVs.

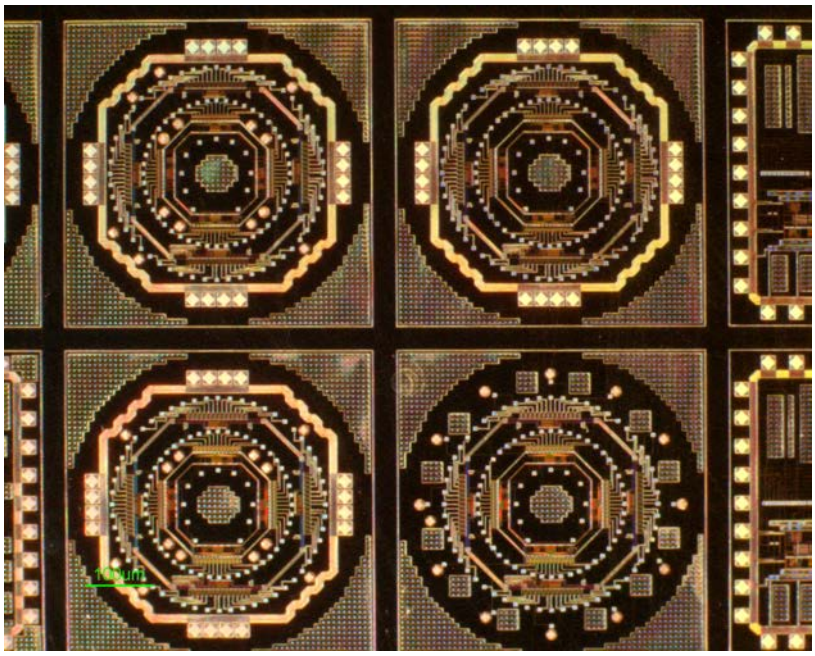


Figure 36: A microscope image showing CMUT arrays with TSVs.

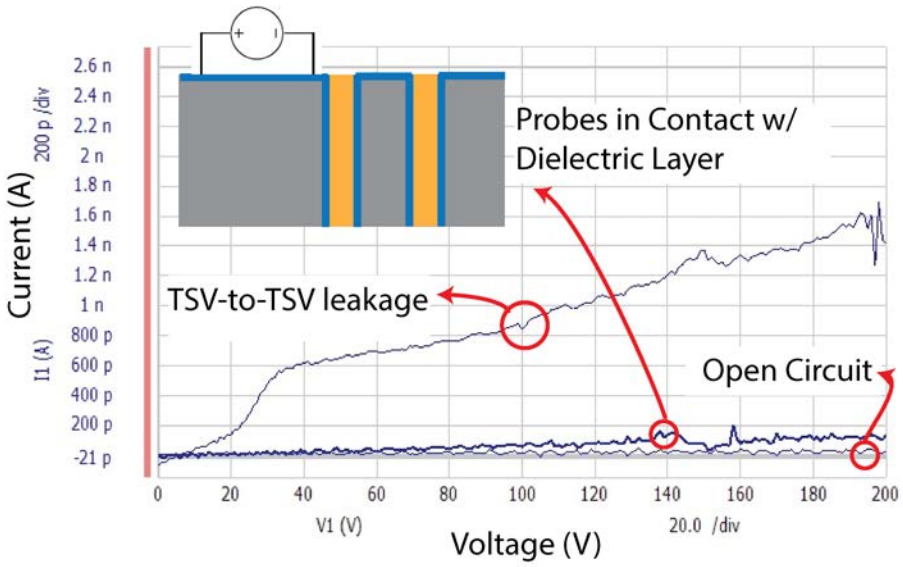


Figure 37: The level of leakage current between two TSVs in a TSMC wafer as a function of the bias voltage

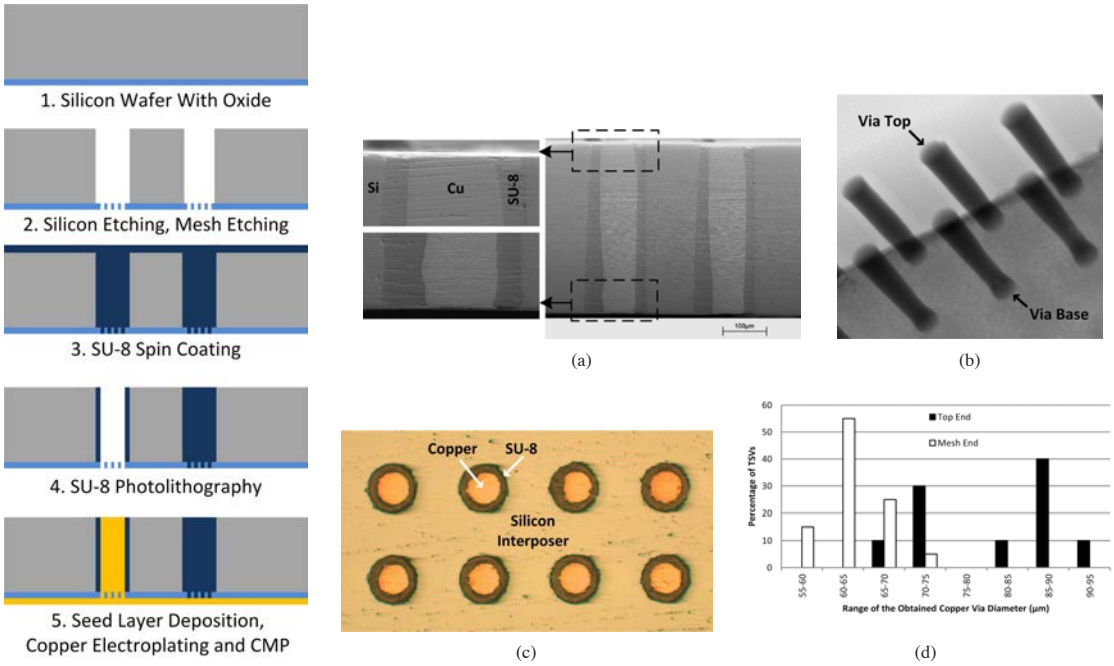


Figure 38: Fabrication process for simultaneous fabrication of photodefined polymer-clad and optical TSVs (left). Fabricated 390 μm tall SU-8-clad TSVs with $\sim$80 μm diameter copper vias surrounded by a 20 μm thick cladding on a 250 μm pitch: a) Cross section view, b) x-ray image showing void-free copper electroplating, c) Top view, and d) Distribution of the obtained copper via diameters of 20 measured polymer-clad TSVs [40].

CHAPTER 3

MECHANICALLY FLEXIBLE INTERCONNECTS (MFI)

3.1 Introduction

The concept of flexible structures as interconnects has been explored by a number of researchers. Beginning with multiple generations of works called Compliant Wafer Level Package (CWLP) and Sea-of-Leads (SoL) [45], these technologies initially aimed at mitigating thermo-mechanical stress issues by providing lateral compliance and lateral range-of-motion, and later works also included methods to provide a few microns of stand-off height by using aluminum as a sacrificial layer. G-Helix [46], FlexConnect [47, 48] and β-Helix [49] are additional examples of compliant interconnects. Other examples of compliant interconnects are discussed in [27].

Flexible interconnects can have significant advantages in interconnecting package substrates, interposer tiles, and bridges over conventional interconnects such as solder balls:

1. Flexible interconnects can be used to compensate for non-planar surfaces that may exist (Figure 39). Sources of non-planarity could come from the warped substrate, from buried features under the pad area, or be intrinsic to the material, such as FR4.

Figure 39: MFIs can be used to compensate for non-uniform surfaces.

2. Flexible interconnects can reduce the warpage that results from the CTE mismatch between underlying substrates (Figure 40); this warpage can be significantly worse for silicon interposer applications, where the substrate sizes are larger than conventional ICs.

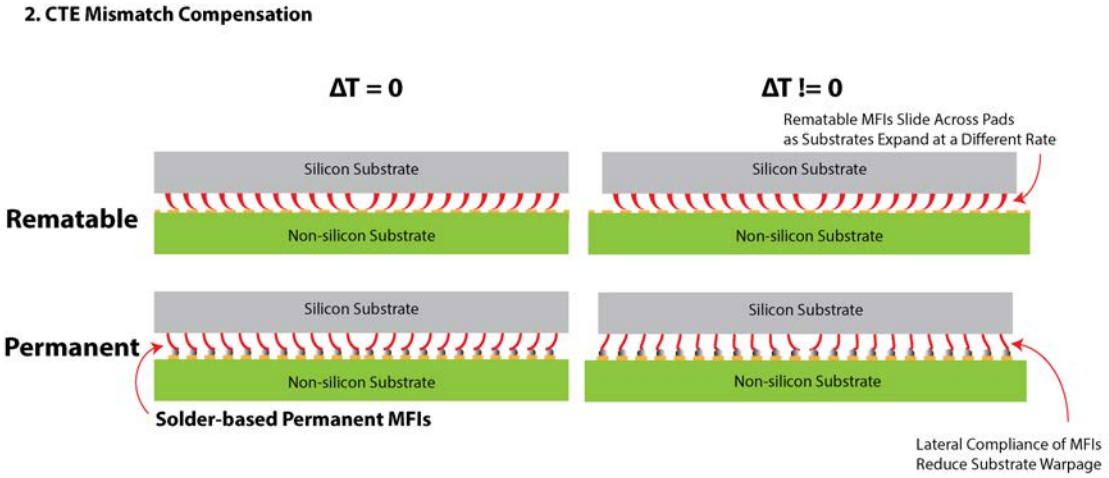


Figure 40: MFIs can be used to reduce the warpage resulting from the substrates' CTE mismatch.

3. Flexible interconnects enable the assembly of the package substrate, interposer tiles, and bridges without using permanent interconnects such as solder balls. This provides a simple means of replacing an individual interposer tile or a bridge even after initial assembly. For large integrated systems, the ability to replace defective tiles or bridges that are found after assembly can lower the cost of ownership and increase the life time of the system (Figure 41).

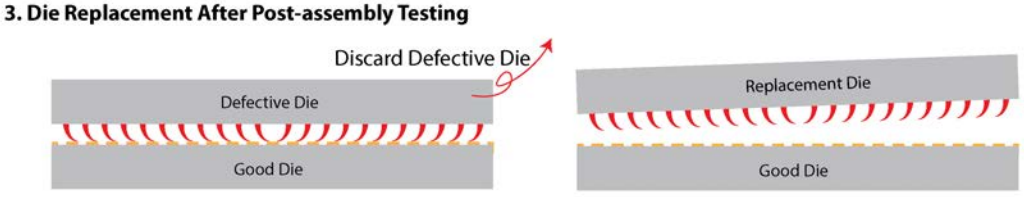


Figure 41: MFIs can be used to enable rematable assembly.

4. Flexible interconnects used on the bridges can make a reliable contact with two

tiles that may have a difference in height resulting from substrate thickness variations, misalignment, and/or features on the tiles (Figure 42).

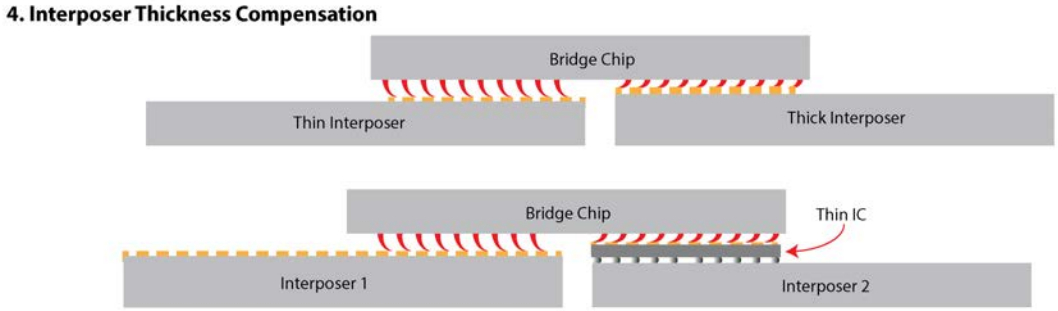


Figure 42: MFIs can be used to compensate for varying interposer heights.

However, to take advantage of flexible interconnects for the applications described above, the vertical deflection characteristics become increasingly important. The vertical range of motion directly affects the amount of topology variation and the warpage that can be compensated, and the vertical compliance is critical in enabling reliable rematable electrical interconnections. The bending profile is also critical in ensuring that the interconnects can be deflected vertically without obstruction.

Prior studies have mostly focused on the lateral deformation of the interconnects. Hence, the vertical deflection characteristics have not yet been studied extensively. In fact, a flexible interconnect with an elastic range of motion exceeding 5 μm + has not yet been demonstrated on non-stress-engineered flexible interconnects. As such, the focus in this work is in providing a vertical elastic range of motion that exceeds 20 μm.

3.2 1st Generation of MFIs: Fabrication and Mechanical Results

This section describes the design, fabrication, and testing of the 1st generation MFIs ('MFIv1'). The curved and the tapered designs are incorporated to reduce stress and increase range of motion. The stand-off height of the MFIv1 is 20 μm (Figure 47) and

copper is used as the structural material. The fabrication results are reported, and the MFI's mechanical characteristics are simulated and compared with the measurements.

3.2.1 MFI Shape

The shape of a flexible interconnect is a critical design consideration because it determines both the electrical and mechanical properties of the interconnect. In many instances, however, a geometrical variable has opposing effects on the mechanical and electrical performance, and a compromise is often required. In other cases, a desired geometry that could benefit both electrical and mechanical performance cannot be attained using conventional micro-fabrication techniques. The conflict between mechanical and electrical design requirements and the limitation of the shapes that can be attained using conventional micro-fabrication techniques are the two most challenging problems in the development of novel flexible interconnect technologies.

In its simplest form, a flexible interconnect has the shape shown in Figure 43; there are three defining characteristics of such a design:

1. A beam with uniform thickness and uniform width.

2. A beam that is straight and parallel to the substrate.

3. A beam with a single support at one end.

The simple design described above is a commonly used design for many flexible interconnects because only two electroplating process steps are needed to form a cantilever that is both constant in thickness and parallel to the substrate, and the single-support cantilever design produces less stress while being deformed vertically compared to a design with multiple supports.

However, the design has two critical issues. First, the maximum stress occurs in a very concentrated area near the support region, which can cause plastic deformation and/or a failure. Second, additional structures are required at the tip to increase the

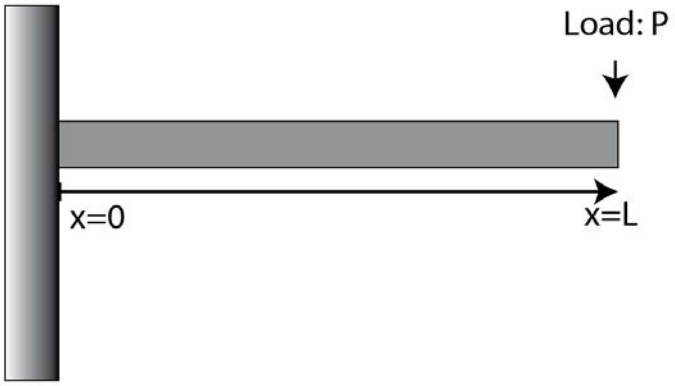


Figure 43: A simple beam with a single support at one end and force applied at the tip.

vertical range of motion. Figure 44 illustrates the problem associated with the simple flexible interconnect design.

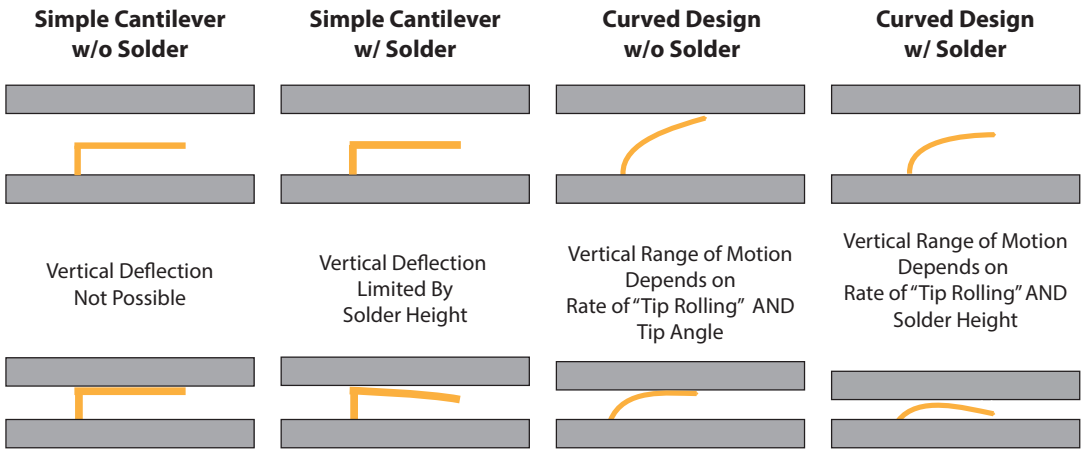


Figure 44: Conventional cantilevers have a limited vertical movement while curved cantilevers have the potential to increase the range of movement significantly.

Both issues can be addressed by modifying the geometry of the flexible interconnects. Two design features used by MFIs to address both issues are: the curved design and the tapering design. Each design is described in the sections below.

3.2.1.1 Curved Design

The simple cantilever design has a limited range of motion if it is used as an interconnect. This is because the tip is at the same height as the rest of the structure, and therefore the top substrate makes simultaneous contact with the entire flexible interconnect, including the tip.

This problem can be overcome by fabricating an extruding structure at the tip such as a solder ball or a copper pillar. However, the range of motion is still equal to the height of the structure on the tip and is independent of the stand-off height of the flexible interconnect. Also, additional photolithography steps are required to fabricate the solder ball or other structures on the tip.

A curved cantilever, as shown in Figure 44, addresses this issue. Even without a structure on the tip, the curved design has the potential to significantly increase the vertical range of motion over the simple design because the tip is initially higher than the rest of the interconnect structure, and the rest of the structure moves down as the tip is deflected downwards. Consequently, the range of motion is now determined by the initial curvature and the bending profile of the flexible interconnect.

3.2.1.2 Tapering Design

The maximum stress experienced by the structure during a deflection is an important consideration because this maximum stress determines the interconnect's elastic vertical range of motion. The elastic deformation is desirable as the plastic deformation of the flexible interconnect structure can negatively affect reliability. In the worst case scenario, it can also cause a catastrophic failure if the stress level exceeds the ultimate stress of the material. For rematable interconnect applications, the elastic deformation ensures that the flexible interconnect returns to its original position after a vertical deflection, which ensures that the tip of the flexible interconnect makes contact with the pads in subsequent assembly processes.

FEM studies and classical beam theory show that beam length, width, and thickness are the primary variables that affect the stress. Euler-Bernoulli classical beam theory shows that the bending stress of a symmetric rectangular beam at position x can be simplified and expressed as

$$\alpha(x) = \frac{M(x) \cdot c}{I_x} \tag{5}$$

where x is the distance from the tip end, *M(x)* is the bending moment at distance x, c is the distance from the neutral axis to the beam surface, and I is the moment of inertia of the beam cross-section [50].

Since the thickness is uniform, c is half of h, and for a cantilever with a single fixed point and force applied to the tip end, as shown in Figure 43, (5) simplifies to

$$\alpha(x) = \frac{6P(L-x)}{wt^2} \tag{6}$$

where L is the length of the beam.

Eq. 6 shows that if the width of the beam is constant, stress will vary throughout the beam as a function of x. The maximum stress is concentrated close to the fixed end (when x=0) and decreases toward the tip end (when x=K). Therefore, a constant width beam spreads the stress inefficiently.

There are two ways to distribute the stress more evenly. Either the thickness of the beam can be varied as a function of x, or the width of the beam can be varied as a function of x. Varying the width is the preferred method because the fabrication of a cantilever with a varying thickness is extremely challenging using micro-fabrication processes.

If the width of the beam is tapered linearly, Eq. (6) can be rewritten as shown

below:

$$w = C_1 \cdot (L - x) \tag{7}$$

$$\alpha(x) = \frac{6P}{C_1 t^2} \tag{8}$$

$$= constant \tag{9}$$

The resulting stress equation shows that the stress is constant throughout the length of the entire beam.

The tapered design and the straight design are modeled using the ANSYS finite element modeling (FEM) software and compared. The structures are modeled as an elastic material and constraints are applied identically to both structures.

When the tips of the two structures are displaced downwards by an identical amount (free in 2 lateral DOFs), the simulation results show that the tapered design has a lower maximum stress (Figure 45) compared to the straight design, and the stress is more equally distributed. As a result, the tapered design is capable of a larger vertical deflection compared to the straight design, which is otherwise identical.

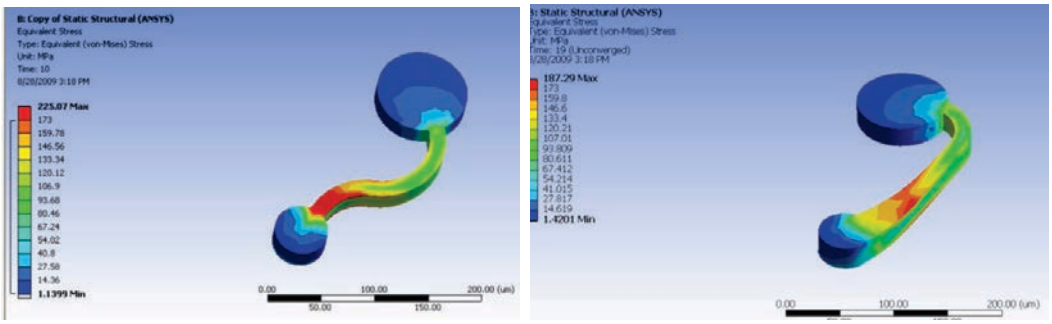


Figure 45: ANSYS FEM simulation showing that tapered design can be used to reduce the maximum stress experienced by the beam while deforming.

3.2.2 Fabrication of Curved MFIs

3.2.2.1 Process Overview

The fabrication of MFIs begins with a blank silicon wafer, although the process can be performed on any polished and planarized surface with devices or materials that

can withstand up to 30 minutes of total baking time at 200 °C or less. This also implies that the process is CMOS compatible. An overview of the process is shown in Figure 46. The resulting MFI structures are shown in Figure 47, and an array of MFIs fabricated using this process are shown in Figure 48. Subsequent sections describe key fabrication issues in detail.

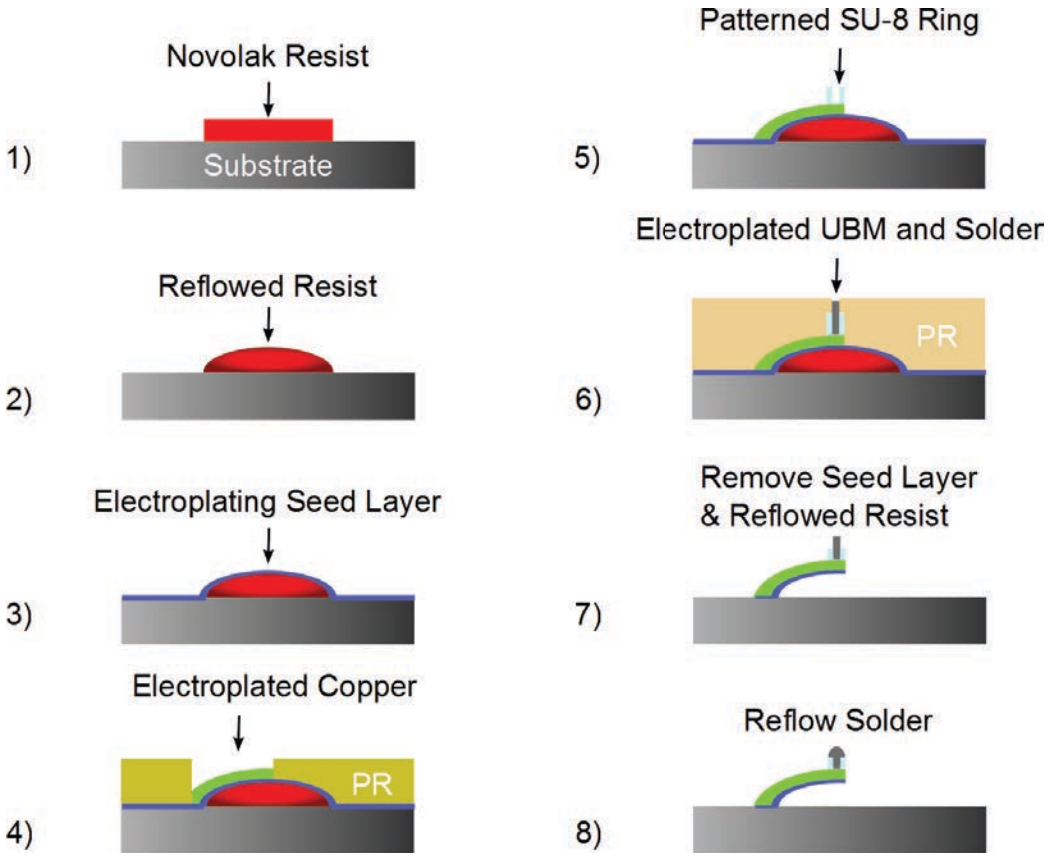


Figure 46: Fabrication process for MFIs with confined solder balls.

On the planar surface, a layer of Novolac-DNQ positive photoresist is spin coated, exposed, and developed. The resulting photoresist structure is reflowed and baked to form a curved surface (Figure 49). The baking procedure ensures that the photoresist structure does not reflow in subsequent processes and can still be removed chemically. The challenges in reflowing the photoresist are discussed in Section 3.2.2.2. A single layer of photoresist forms a curved surface with a height of approximately 20 μm at the center; the same process can be extended to form a taller curved surface using a

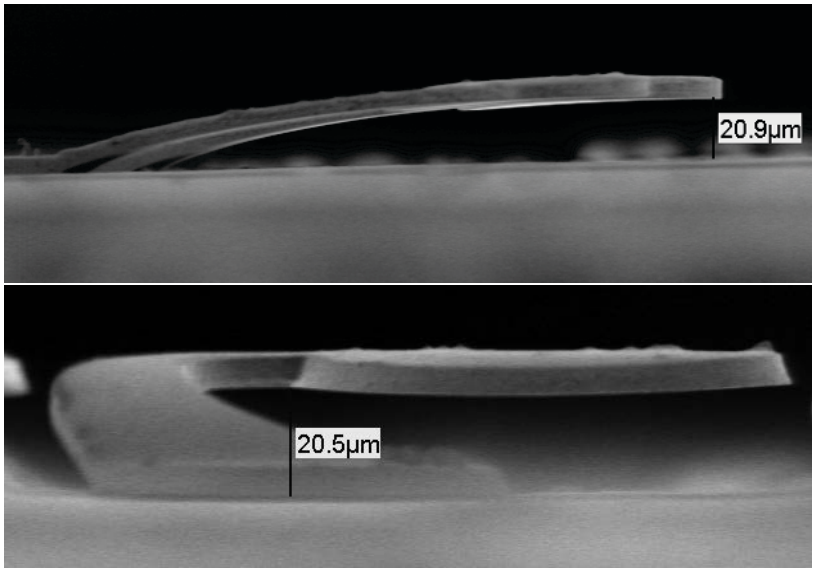


Figure 47: SEM image taken from the sides showing Cu MFIs with 20 μm gaps and the MFI's curved cantilever structure.

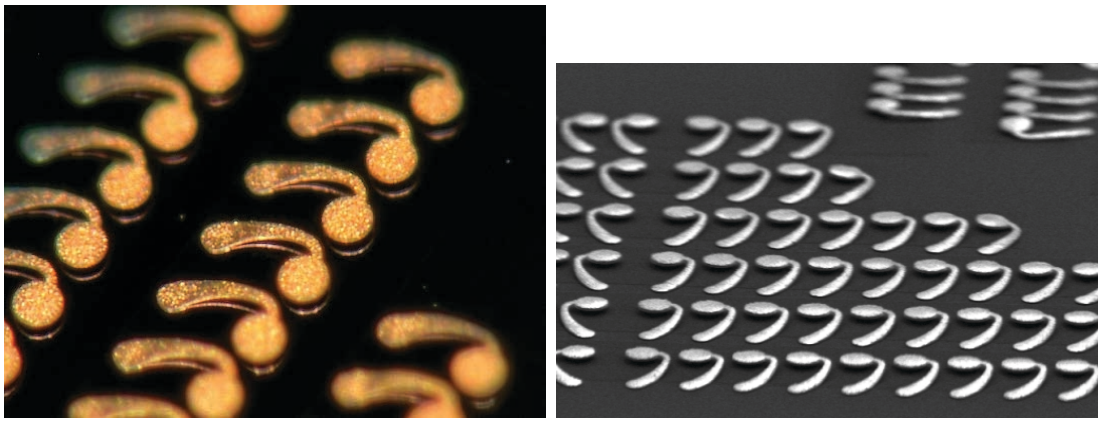


Figure 48: SEM (left) and optical microscope (right) images showing batch fabricated area array of MFIs.

double and a triple spin-coated layers, as shown in Figure 50.

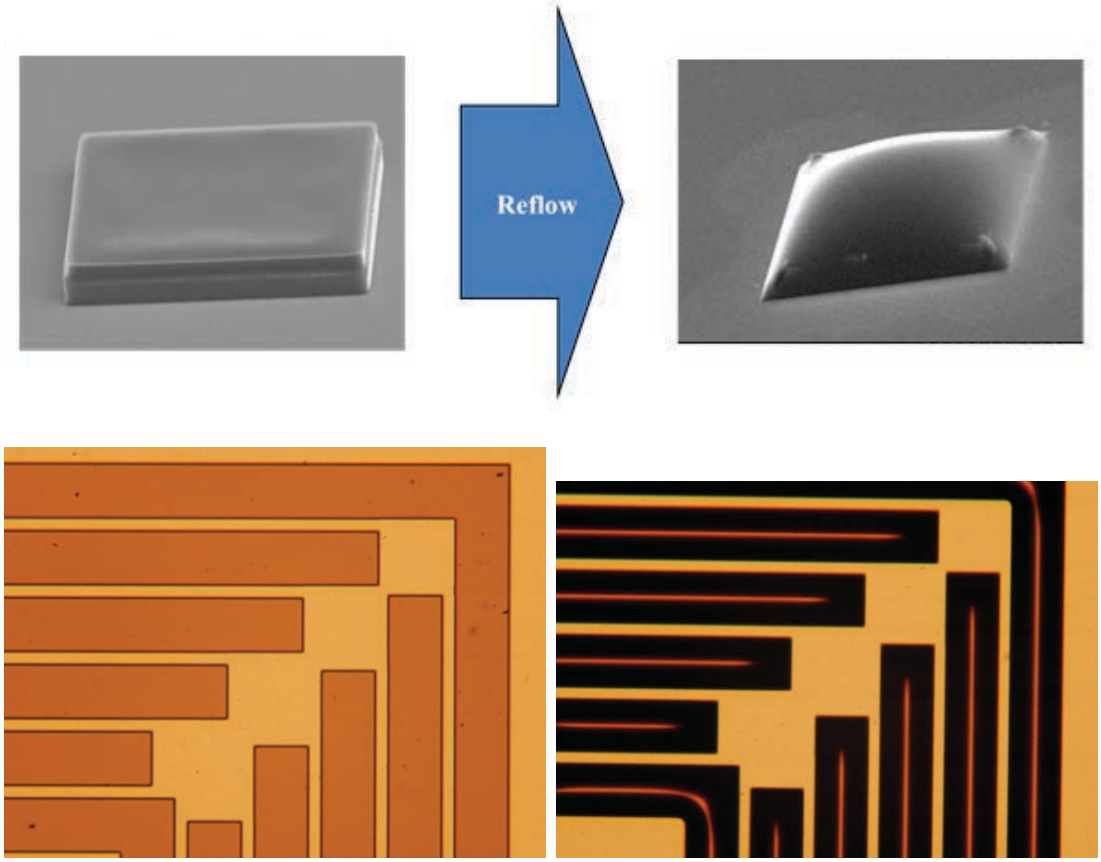


Figure 49: SEM (above) and optical microscope (below) images showing the patterned photoresist before and after the reflow.

An electroplating seed layer consisting of titanium, copper, and titanium (30nm / 300nm / 30nm) layers are deposited on top of the curved structures and the exposed substrate. A DC sputterer or an e-beam evaporation tool can be used for the deposition process.

A thick negative photoresist is spin coated on top of the seed layer to form an electroplating mold. The mold forms the tapered shape of the MFI. A buffered oxide etch (BOE) is used to remove the Ti layer under the mold openings, and copper or nickel tungsten is electroplated. The negative photoresist is then removed in acetone. The reflowed photoresist under the seed layer is unaffected by the acetone solution

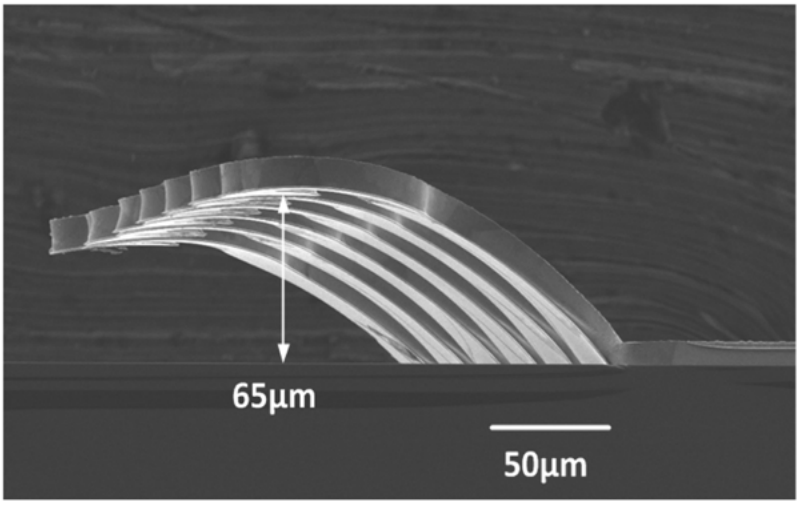


Figure 50: Double and triple coating of the photoresist can produce MFIs with 65 μm stand off height. The extended work is published in [51].

because of the seed layer that completely covers the structures. The challenges associated with forming the electroplating mold are described in Section 3.2.2.3.

To form solder balls on the tip of the MFIs, additional processes are required. To form solder balls, an SU-8 layer is spin coated, and a polymer dam is patterned and developed. Next, a layer of thick negative photoresist is spin coated, and only the area inside the polymer dam is patterned and developed away. 1-2 μm of nickel and 20-30 μm of solder are electroplated. The negative photoresist is removed using acetone. A detailed description of the solder ball fabrication is described in Section 3.2.2.5.

For both versions of MFIs with and without solder, the seed layer is removed using a BOE solution and a copper etchant. The reflowed photoresist is removed in an acetone bath and in a heated resist remover solution. The removal of the seed layer and the reflowed photoresist releases the electroplated MFI structures.

3.2.2.2 Sacrificial Reflowed Photoresist

Sacrificial reflowed photoresist (Novolac based) structures are critical in fabricating MFIs because they enable the curved surface described in the previous section. In addition, they enable 20 μm, and up to 60 μm with multiple spin coating, of vertical

gap using only two masking steps and a single electroplating step.

Even though reflowed photoresist structures have been widely used in microelectronics to form micro-lens structures, their use as a sacrificial layer and at the dimension required by MFIs is a first. As a result, the technique has many novel challenges yet to be addressed. These challenges are described in the sections below.

Complete Reflow without Deviation The first challenge is in determining the reflow and baking temperatures. Initially, a constant temperature on a hotplate was used, which yielded unsatisfactory results. At a lower temperature (130 °C), but still above the glass transition temperature (Tg), the reflow process stops prematurely, leaving a partially reflowed photoresist structure (Figure 51). It is suspected that this is because the Tg is raised above the baking temperature before the material has had a chance to reflow completely.

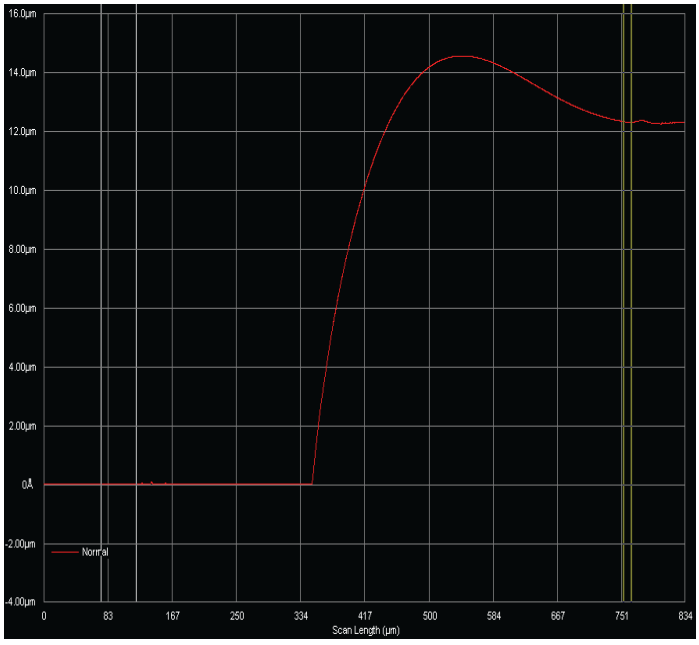


Figure 51: The profilometer result shows that the photoresist is partially reflowed at lower temperatures.

At a higher temperature (160 °C), the reflow is complete. However, the base of the resulting structure deviates from the pattern on the mask. In extreme cases,

the reflowed structures merged with adjacent structures as shown in Figure 52. The deviation is shown to be anisotropic. The deviation occurs because the photoresist is in a highly glassy state at high temperatures [52].

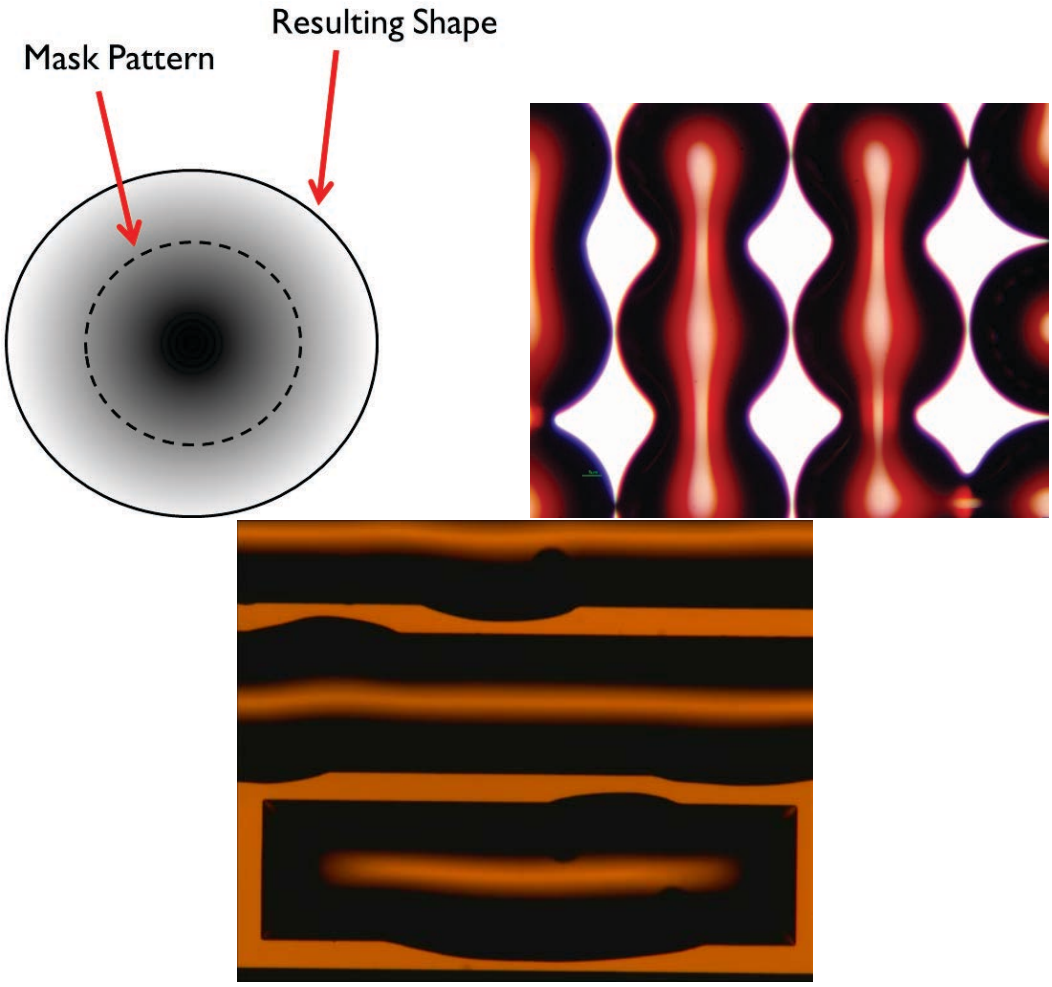


Figure 52: Reflowing at a constant high temperature results in final a shape that deviates from the original patterned shape. The optical microscope image on the right shows that despite having the same spacing in both of the lateral directions, the photoresist merged in only one direction, indicating that the flow is laterally anisotropic and needs to be minimized.

Hence, what is needed is a reflow and baking process that can completely reflow the photoresist and yet minimize deviation. However, experiments showed that an optimal temperature does not exist for a constant-temperature process; all temperatures (in 2 °C increments) between 130 °C and 160 °C either produced a partially

reflowed structure or a structure that had a visibly large deviation from the mask pattern.

The problem is resolved by using a reflow temperature profile that increases over time. The reflowed structures using a ramped temperature profile are shown to be completely reflowed and to have a significantly reduced amount of deviation, as shown in Figure 53. While the exact mechanism of the process is unknown, the following are observed:

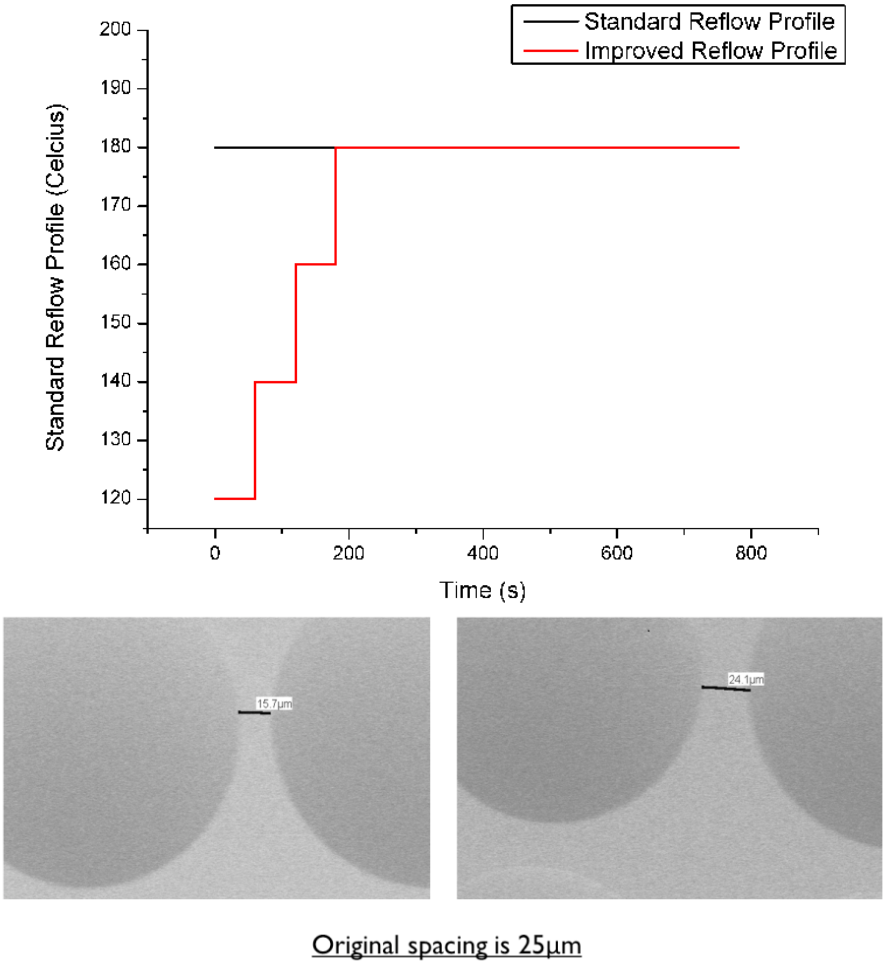


Figure 53: Comparison of the isothermal reflow process (left) and the ramped reflow process (right).

1. The difference between the bake temperature and the glass transition temperature (Tg) is inversely correlated to the viscosity of the glassy photoresist, and

a lower viscosity of the photoresist can be observed at a higher temperature.

2. The Tg is increased during the bake process. However, the resulting Tg does not increase significantly beyond the bake temperature. This is observed experimentally when a partially reflowed photoresist at 130 °C can be reflowed again at a slightly elevated temperature of 135 °C. A similar material that displays the same phenomena is described in [53].

One plausible explanation for the mechanism of the process is that by ramping up the temperature slowly, the baking temperature "follows" the increasing Tg of the photoresist material. In other words, the baking temperature is constantly raised above the Tg, however, the difference between the two temperatures is always minimized as the Tg is also raised simultaneously. This results in photoresist structures that are in a highly viscous glassy state throughout the entire reflow process, which in turn minimizes the deviation.

Outgassing and Reflow in Subsequent Processes The second challenge arises during the subsequent processes where multiple photolithography and deposition processes are performed on top of the reflowed photoresist structures. Many of these processes require a baking process (e.g. pre- and post-bake), which causes the reflowed photoresist structure to reflow once more and/or produce outgassing (Figure 54). Both challenges must be eliminated because they damage the metal seed layer that is deposited on top.

To determine the additional baking process required to eliminate both effects in subsequent processes, a thermogravimetric analysis (TGA) is performed. A temperature of 180 °C is selected as the TGA temperature as the subsequent processing steps involve the 150 °C baking processes. By performing the isothermal TGA at 180 °C, the baking time needed to eliminate the solvent evaporation and decomposition at a

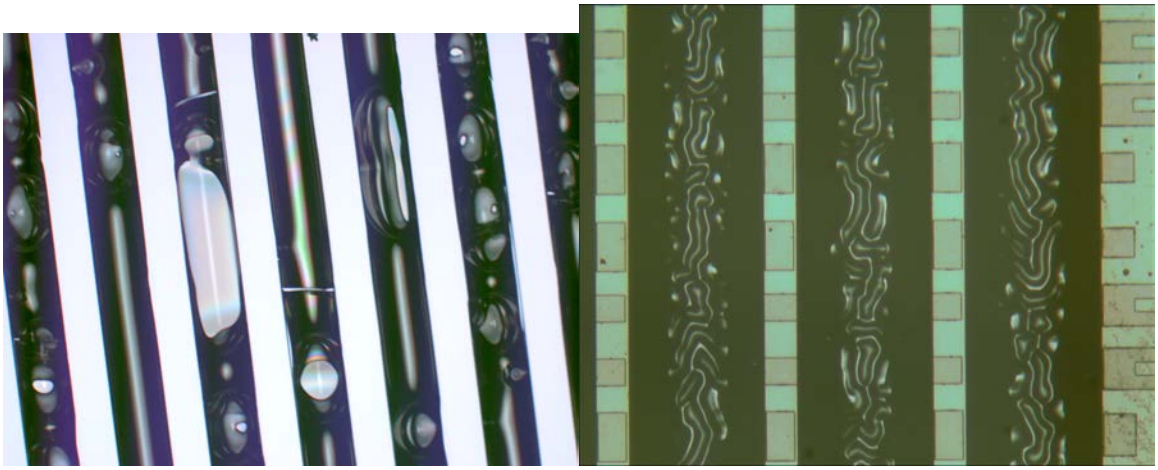


Figure 54: Damaged electroplating seed layer due to the outgassing (left) and the reflow (right).

temperature of 180 °C or less can be determined. The result of an isothermal TGA at 180 °C is shown in Figure 55.

The result shows that less than 5 minutes of baking at 180 °C is required for the photoresist to reach a stable weight. An experiment with the reflowed structure and the seed layer also shows that a baking duration of 5 minutes or longer at 180 °C is indeed sufficient to eliminate the breakage in seed layer due to outgassing. However, the warpage caused by the reflow is still not eliminated.

To eliminate the warpage due to the reflow, it is essential to raise the Tg of the photoresist to a temperature higher than 150 °C. A differential scanning calorimetry (DSC) analysis is performed to determine the length of the bake process required. The reflowed photoresist is divided into two samples, and the two samples are baked for 5 minutes and 10 minutes, respectively, at 180 °C. The photoresists from the two samples are then collected into two DSC containers, and the same DSC is performed on both samples. The DSC result for the 5-minute sample is inconclusive, but the 10-minute sample shows a clear increase in the Tg to 150 °C(Figure 56). A similar DSC result has been reported for other Novolac-epoxy systems, where the Tg of the resin is increased after an isothermal baking process [54]. Subsequent experimental

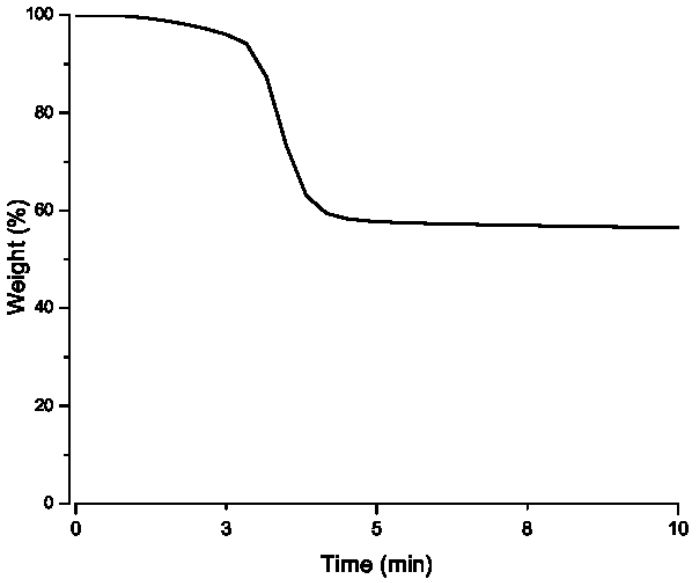


Figure 55: Isothermal Thermo-Gravimetric Analysis (TGA) performed at 180 °C.

verification shows that 10 minutes of baking at 180 °C after the ramped reflow process is sufficient to eliminate both the outgassing and the reflow effect.

3.2.2.3 Electroplating Mold Exposure Control

The need to spin-coat, pattern, and develop a thick negative photoresist on top of a reflowed photoresist is a significant challenge because of the large variation in the surface topology. The large variation produces regions where the thickness difference is as much as the height of the underlying reflowed structure (20 μm for a single spin-coated structure and 60+ μm for a triple spin-coated structure).

The varying photoresist thickness is a challenge because the required exposure dose varies with the thickness. It becomes impossible to have optimal exposure at all areas of the sample; if the optimal dosage for the thinnest region is used, the thickest regions will have an insufficient amount of exposure causing undercutting of the electroplating mold during the development process (Figure 57). On the other hand, if the exposure dose is increased to give the optimal dose to the thickest region, the resist on the curved region would not develop because the reflection of the light

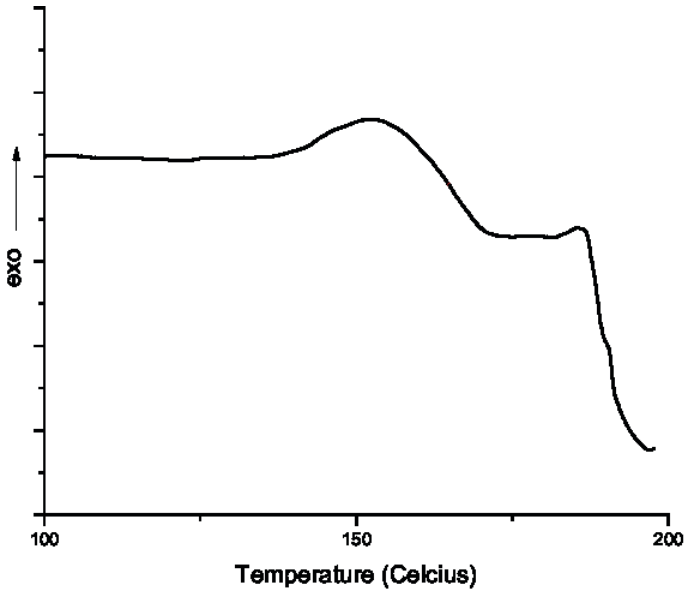


Figure 56: After curing the photoresist at 180 °C for 10 minutes, Differential Scanning Calorimetry (DSC) results show that the Tg has been raised above 150 °C.

on the curved region of the dome results in an inadvertent exposure of the masked (i.e., unexposed) region.

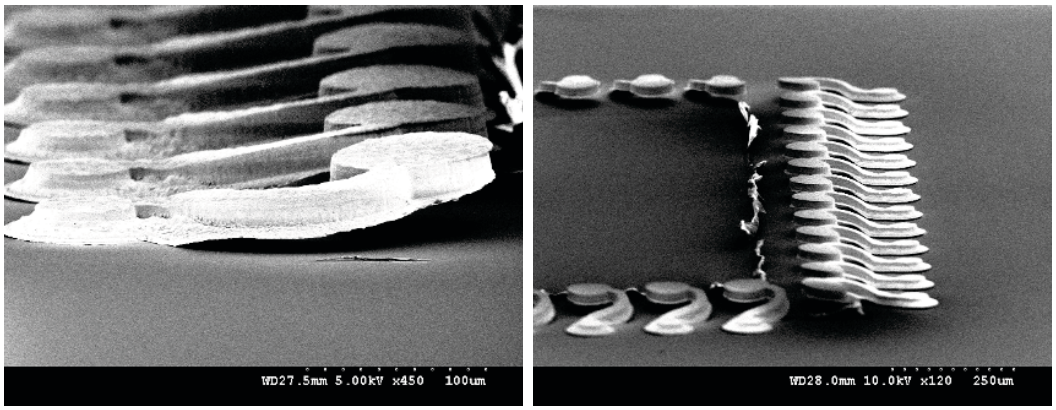


Figure 57: SEM images showing the result of electroplating with a mold that has an undercut.

After experimenting with various thick resists, a negative resist with a very wide sensitivity range is identified (Futurrex NR21-20000P). For the photoresist layer where the thickest region is 40 μm (with an optimal dose of 2200mJ) and the thinnest region is 20 μm (with an optimal dose of 920mJ), a dose of 1200mJ and a doubled post-exposure bake (PEB) time are used successfully.

3.2.2.4 Spray Coating

In an extended work by Professor Bakir's Research Group at Georgia Tech, the electroplating mold is produced using a spray-coating process instead of a spin-coating process [51]. The spray coating enables a photoresist layer with uniform thickness to be coated regardless of the surface topology. Figure 58 shows the two photoresist layers: one produced by the spin-coating process and another produced by the spray-coating process.

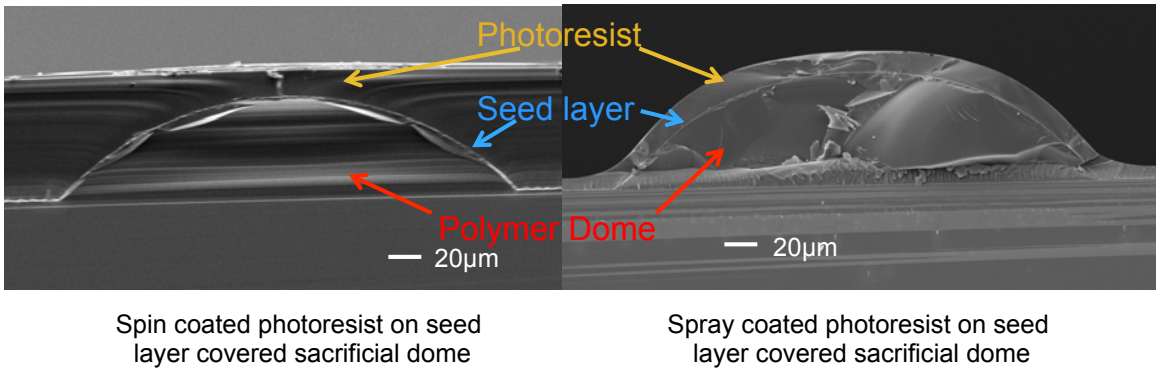


Figure 58: Cross-sectional SEM image shows that a more uniform photoresist layer is produced by the spray coating process compared to the spin coating process [51].

The spray coating enables the development of higher fidelity patterns on highly non-uniform surfaces, including the tops of curved surfaces with 60 μm heights. Figures 59 and 60 show the enhanced fidelity achieved using the spray-coating process compared to the spin-coating process.

3.2.2.5 Polymer Dome / Solder

As discussed in the previous section, additional processing steps are required to form solder balls on the tip of the MFIs. First, an SU-8 ring is formed around the pad area, and nickel and solder are electroplated inside the ring. The purpose of the SU-8 ring is to confine the solder during the reflow process and during the thermo-compression assembly process. The polymer dam is shown in Figure 61.

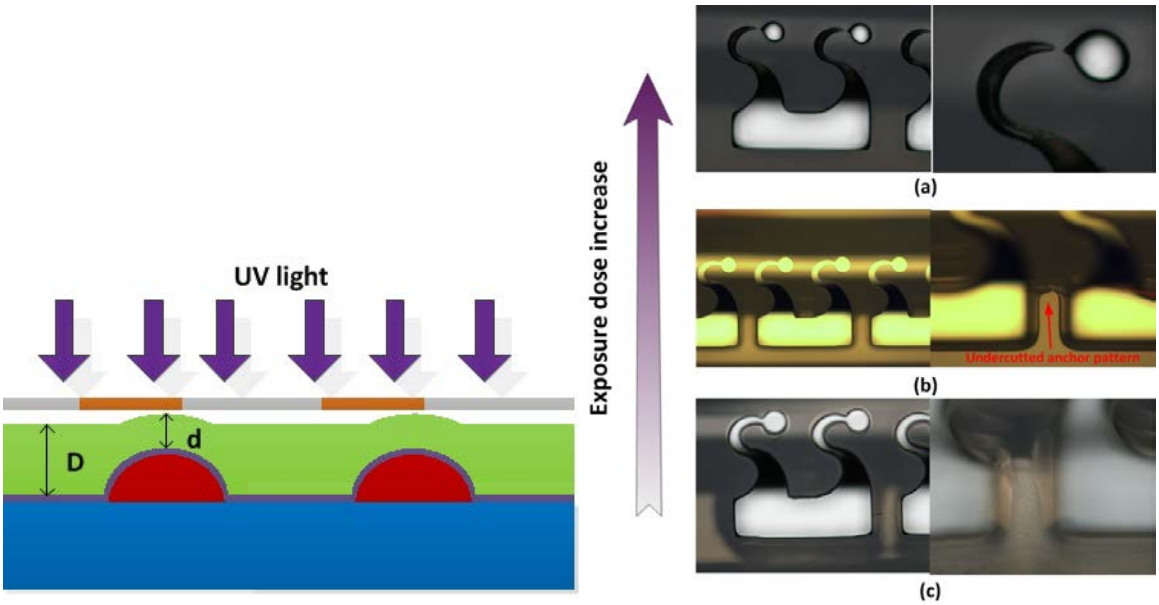


Figure 59: Optimization of the exposure dose is difficult with the spin coating process [51].

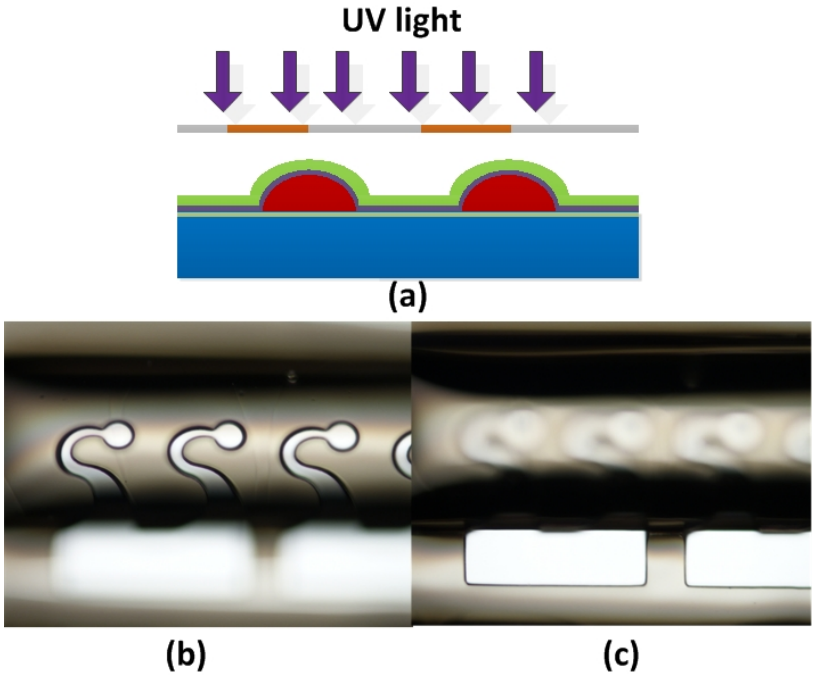


Figure 60: High fidelity patterning can be achieved with the spray coating process [51].

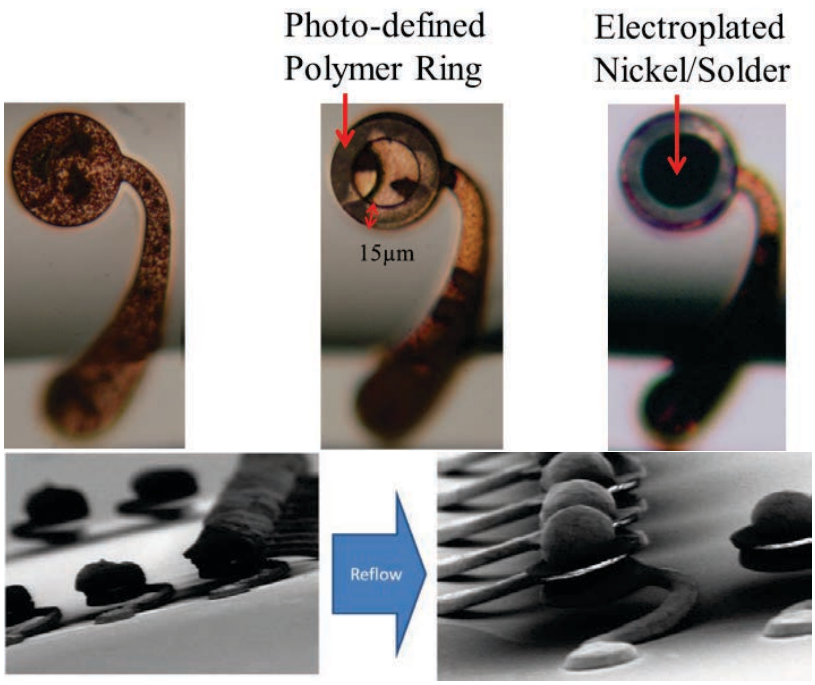


Figure 61: Electrodeposition of solder inside a polymer ring allows confinement of solder in MFIs.

After the assembly of the chips containing MFIs with solder balls with 2N of force, the top chip is removed and MFIs and the solder balls are examined under an SEM. The images show that solder balls are completely confined to the pad area even after the thermo-compression assembly process (Figure 62).

3.2.3 Mechanical Compliance FEM and Measurement

Compliance (the inverse of stiffness) is an important metric for flexible interconnects because it determines the force applied to pads during the assembly process. It is measured using a Hysitron Triboindenter, which can apply a vertical force on the tip area of the MFI and collect the force vs. displacement data. From this data, the slope is measured from the linear region, which corresponds to the compliance.

The compliance of MFIs with various thicknesses is measured and compared to the ANSYS FEM simulation results. Figure 63 shows the experiment setup, and Figure 64 shows the compliance as determined by the simulation and the indentation.

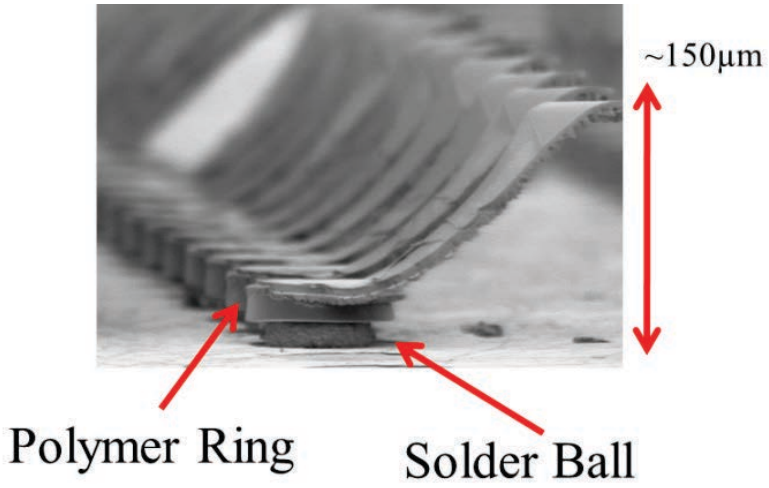


Figure 62: SEM image of the assembled MFIs after the substrate has been pulled off. The solder is confined using the SU8 ring and remains confined even after assembly.

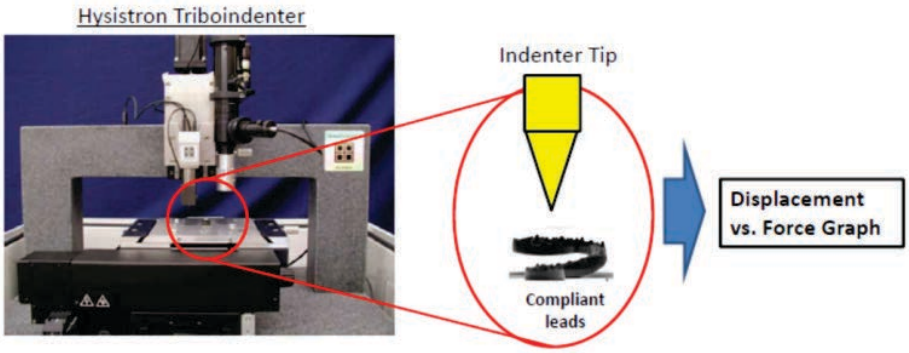


Figure 63: Mechanical characterization setup using the nano-indenter to measure the vertical compliance of MFIs.

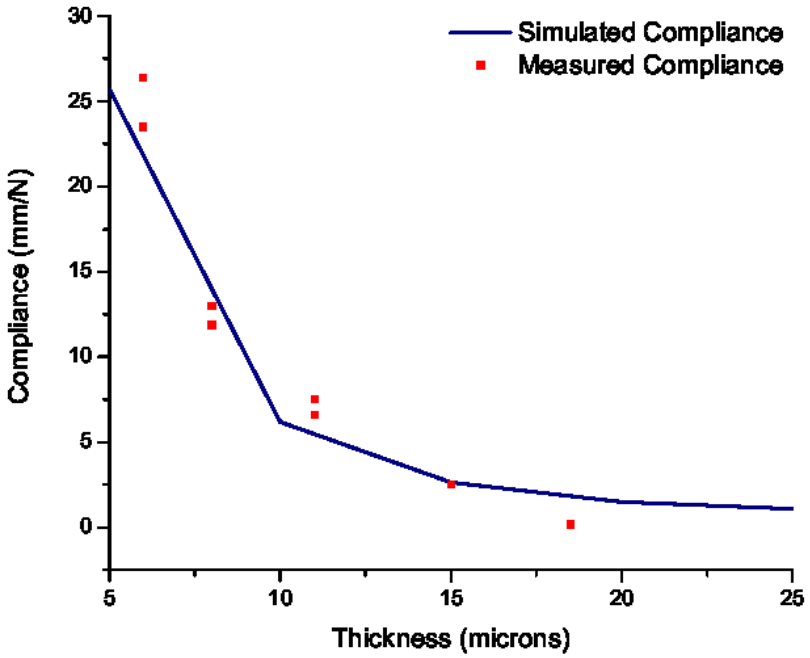


Figure 64: Simulation and indentation results showing the MFI's compliance as a function of thickness.

It is important to note that a wide range of compliance can be obtained just by varying the thicknesses of the MFIs. This is important because varying the thickness is a trivial process, since only the electroplating time needs to be changed. As a result, the compliance of the MFIs can be tailored to meet the requirements of various applications. For example, MFIs on a low-k surface might require a high compliance, while rematable interconnects require a relatively low compliance to ensure that sufficient force is applied to form low-resistance interconnections. The required compliance may also vary depending on the number and density of MFIs used in the application. For example, having the ability to change the compliance of individual MFIs allows one to achieve a predetermined spring constant between two substrates without adjusting the number of MFIs.

3.2.4 Elastic Range of Movement

A single MFI is indented twenty times to determine if plastic deformations have occurred. The tip is vertically displaced by 4.5 μm, and the force vs. displacement

data is collected. The results show that the first and the twentieth indentations have a linear force vs. displacement relationship, and the slope of the first and the twentieth indentations is almost identical. This indicates that the MFI experiences only a small amount of plastic deformation when vertically deflected up to 4.5 μm. The graph in Figure 65 also shows that the loading and the unloading profiles are closely matched, which confirms that little, if any, plastic deformation has occurred. The indentation is limited to 4.5 μm by the tool used in this experiment.

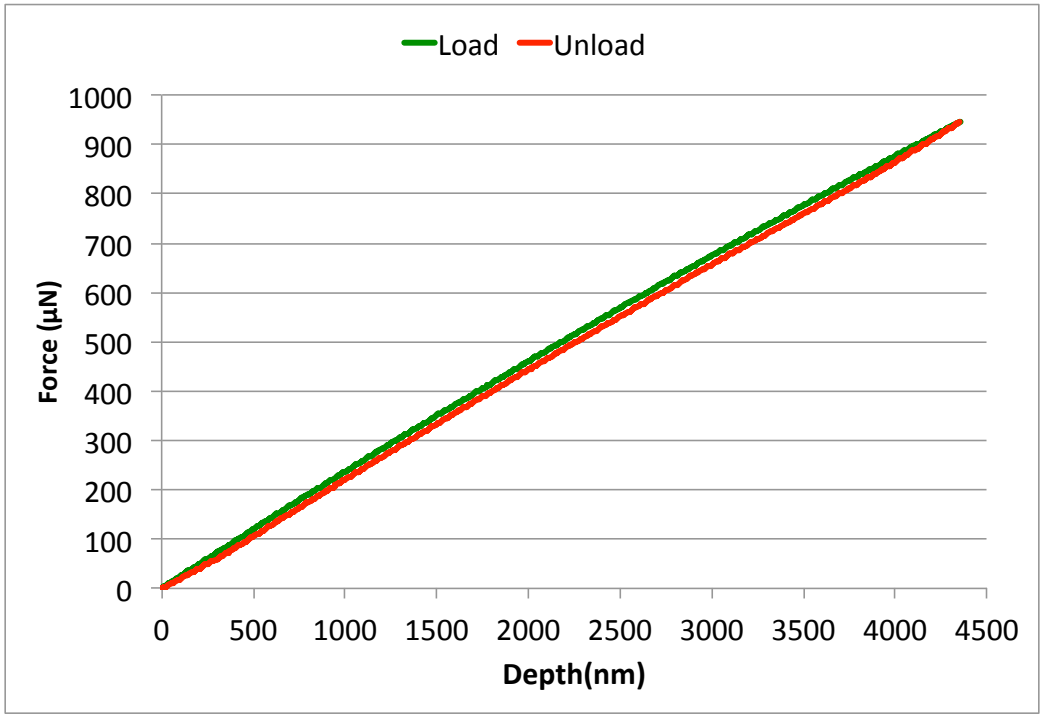
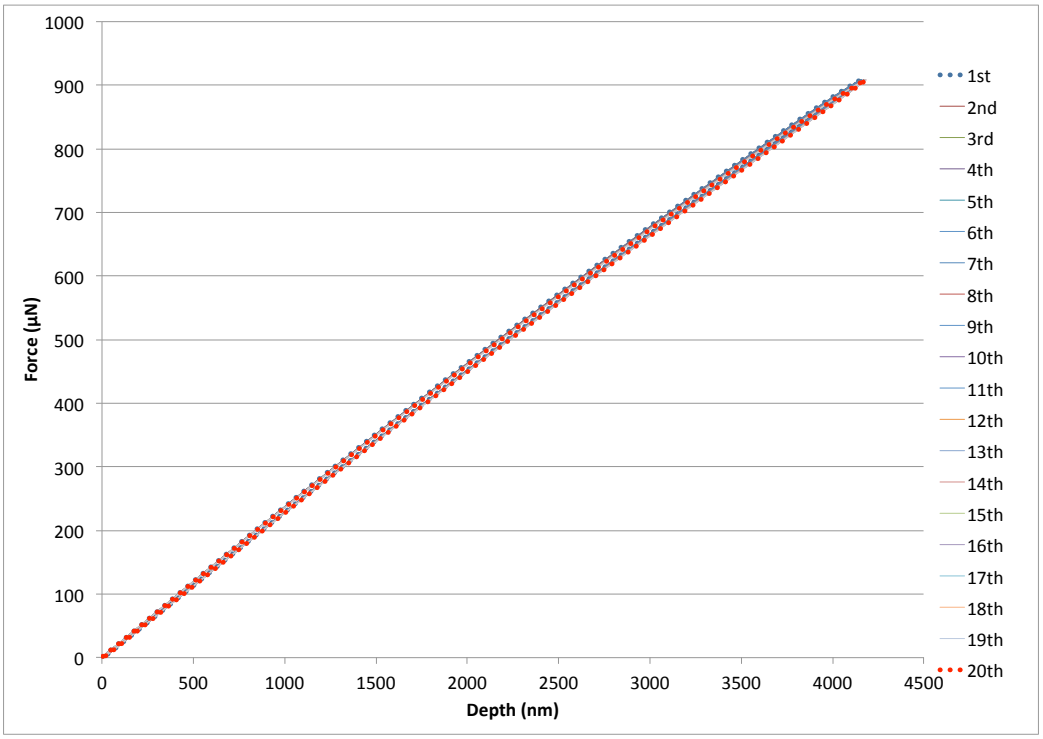


Figure 65: Loading and unloading profiles of an MFI.

To characterize the deformation beyond 4.5 μm, a high-force indenter is used to press on the tip of the MFI. The tip is pressed all the way so that the tip area makes contact with the substrate (Figure 67). The resulting structures are examined under an SEM. The captured images show that the MFI's stand-off height remains unchanged at 20 μm even after the full deformation, which again indicates a small amount of plastic deformation (Figure 68).



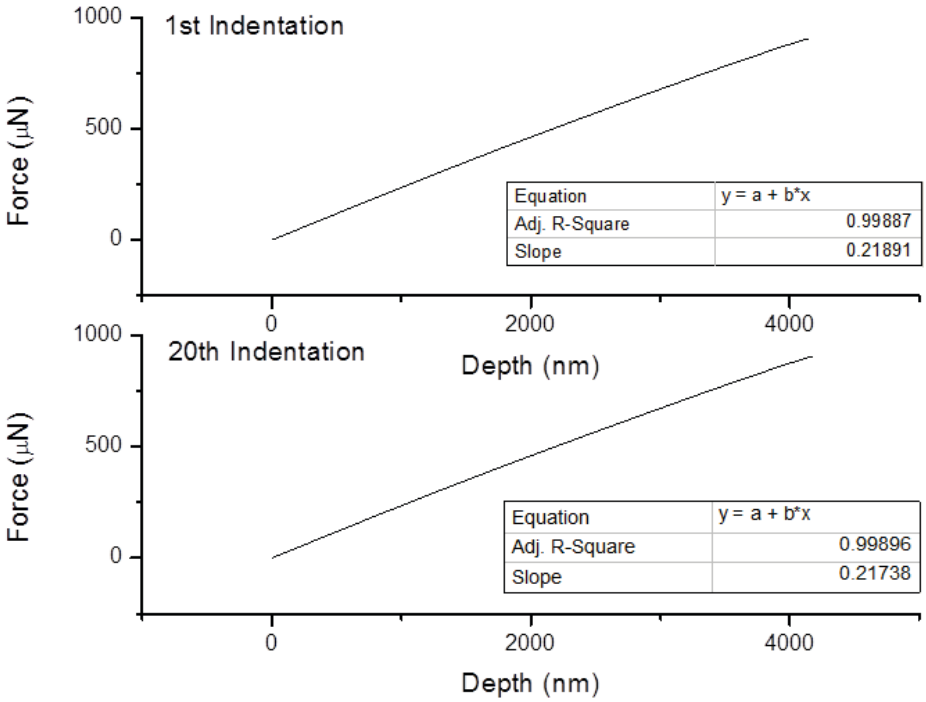


Figure 66: Top graph shows the force vs. displacement graph of the first indentation and the bottom shows after 20 indentations of the same MFI. Graph's linear and unchanged slope shows that minimal plastic deformation has occurred.

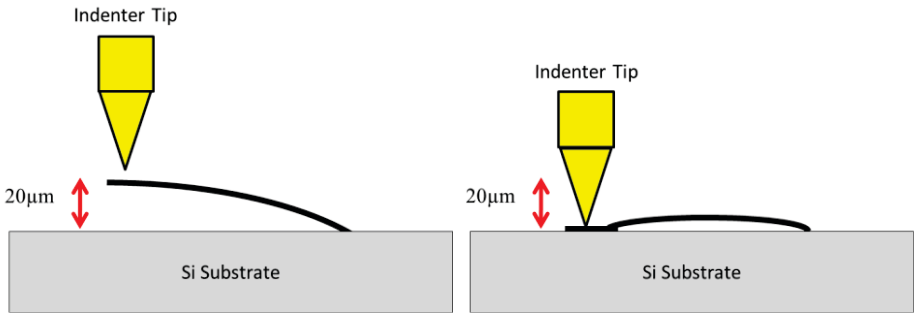


Figure 67: Indentation using high force head flattens the pad area flat against the substrate.

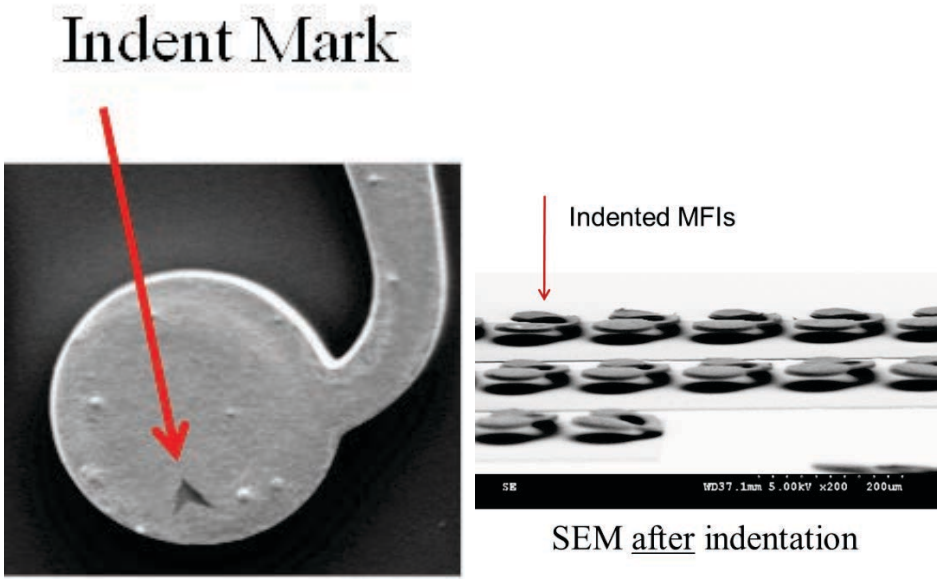


Figure 68: Even after the indenter presses the pad area flat against the substrate, the MFIs are returned to their original positions as shown in the SEM(right).

3.3 2nd Generation of MFIs: Rematable Tip, Mechanical, Electrical Results

This section describes the design, fabrication, and testing of the 2nd generation of MFIs ("MFIv2"). The fabrication process is slightly modified from the MFIv1's process; the modifications are made to 1) increase the stand-off height to 60 μm (Figure 47); 2) use nickel-tungsten, a material with a significantly higher tensile stress (1.9 GPa) than copper, as the structural material; and 3) to further optimize the shape in order to increase the elastic range of movement beyond 20 μm and enable rematable interconnections.

3.3.1 MFI Shape

For MFIv1, the tapered shape is used to equally distribute the stress and reduce the maximum stress. However, the tapered design has a serious side effect that limits the range of motion to what is demonstrated by MFIv1 (20 μm or the height of solder ball); the bending profile of a tapered MFI shows that the tip "rolls" during a vertical deflection, and the tip is eventually at the same height as the body parts of the MFI before the tip is completely deflected vertically. For MFIv1, the presence of solder balls at the tip ameliorated the problem, however, for MFIv2, where the stand-off height is significantly increased and the solder balls are not present (for rematable interconnections), the "rolling" effect must be minimized.

The rolling effect can be seen from classical beam theory. The bending profiles (or elastic curves) for the tapered, reverse-tapered, and straight cantilevers are derived in Appendix A.

3.3.2 Comparison of Designs

The derived bending profile formulas are plotted in Figure 69. It can be seen that the tapered design reaches a predefined slope at a much lower level of deflection compared to the straight or reverse-tapered tips. This means that the tapered design is much

more prone to rolling of the tip. In fact, the results suggest that the reverse taper has the optimal bending profile for flexible interconnect applications.

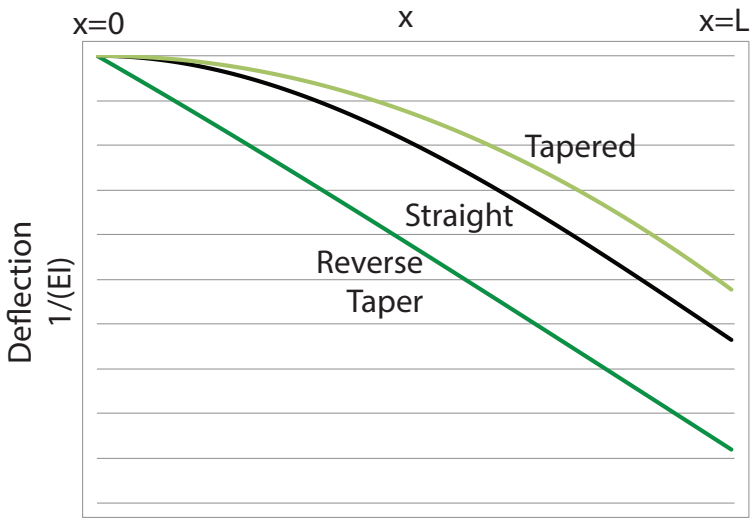


Figure 69: Test setup for four point probing resistances including contact resistance. The chip is mounted using PSAS to ensure consistent contact force.

Similar results can be seen from FEM simulations, where the initial stand-off height and the curved profile are taken into consideration (Figure 70). It is shown again that the tapered tip reaches a prescribed angle (i.e., becomes flat) before the straight design and MFIv2 design, which incorporates the reverse-taper design.

However, while the reverse taper design has the optimal bending profile, the stress resulting from its deflection is the highest of the three designs. What is needed is the stress profile of a tapered design and the bending profile of a reverse-tapered design. As a result, a new design ("MFIv2") that incorporates both the tapering design as well as the reverse-tapering design is developed. The stress distribution of the new design is compared with the tapered and the straight designs (Figure 71).

The MFIv2 design provides over 33% increase in the range of motion compared to the tapered shape and over 17% increase compared to the straight design. The FEM also shows that MFIv2 design moves laterally as it deforms. Such movement is beneficial for the rematable interfacing as it "scratches" the pads to potentially break

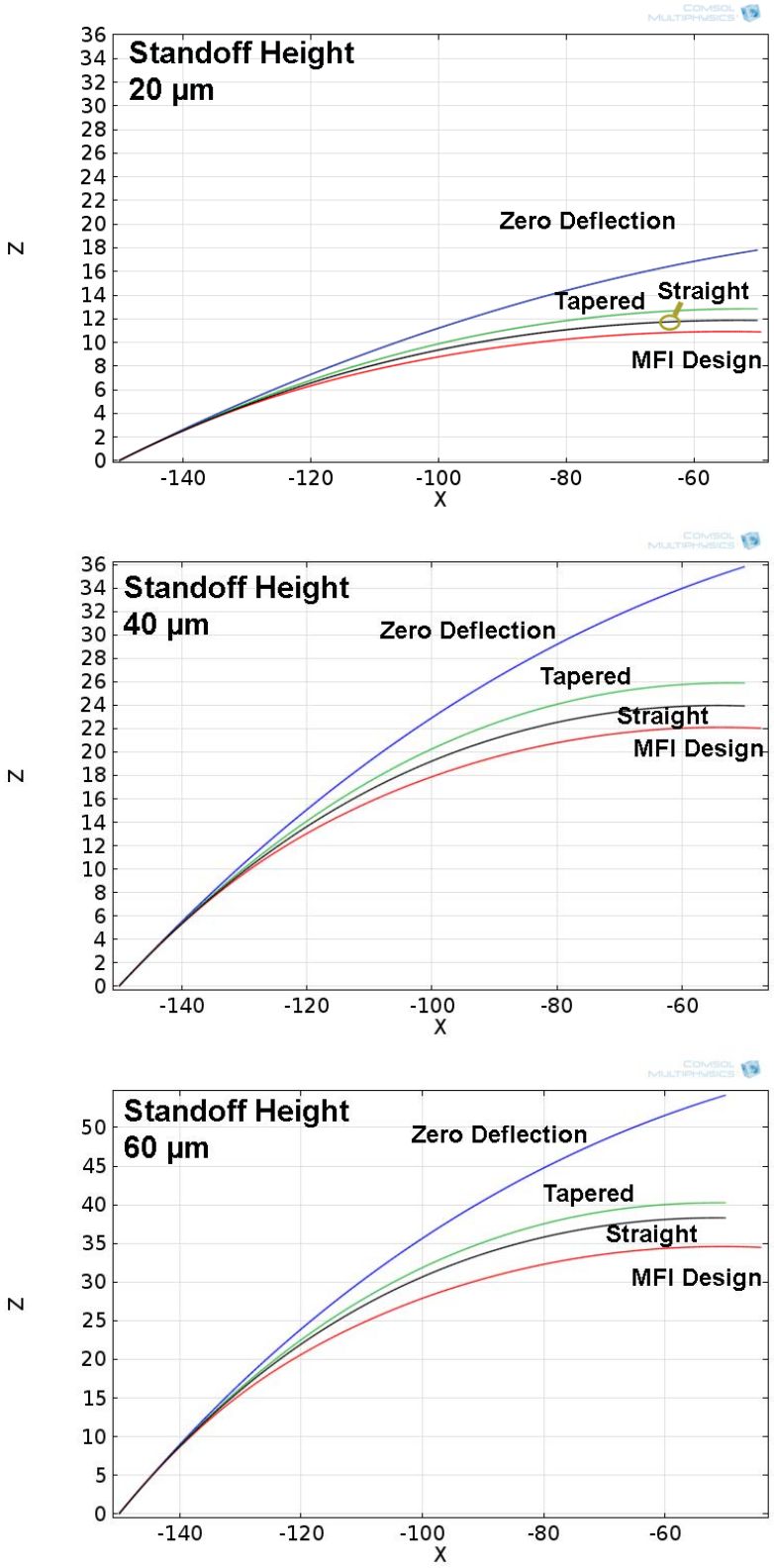


Figure 70: Bending profiles of constant-width, tapered, and t-MFI designs for varying stand-off heights (20 μm, 40 μm, and 60 μm).

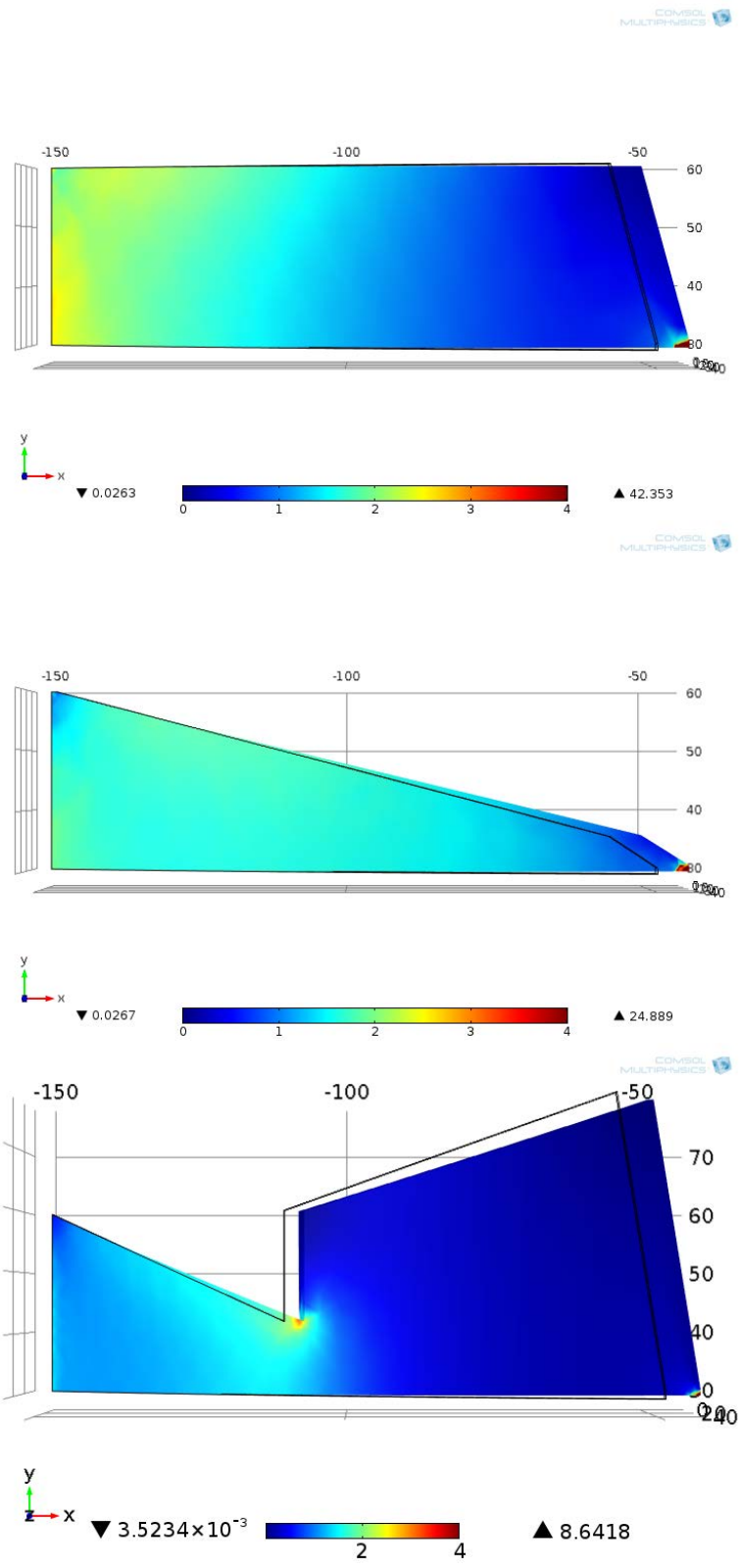


Figure 71: FEM simulated MFIs and corresponding stresses during 20 μm vertical deformation. Constant-width, tapered, and T-MFI designs are shown.

through the oxide layer and form a better electrical contact.

3.3.3 Pointy Tip Fabrication

Pointy tips are required to make a low contact resistance interface with pads. To form pointy tips, a non-flat angle of the curved surface is used, as shown in Figure 72. This configuration also decreases the pitch, as two MFIs can be formed on the same area needed to form a single MFIv1. Fabricated MFIs are shown in Figure 73.

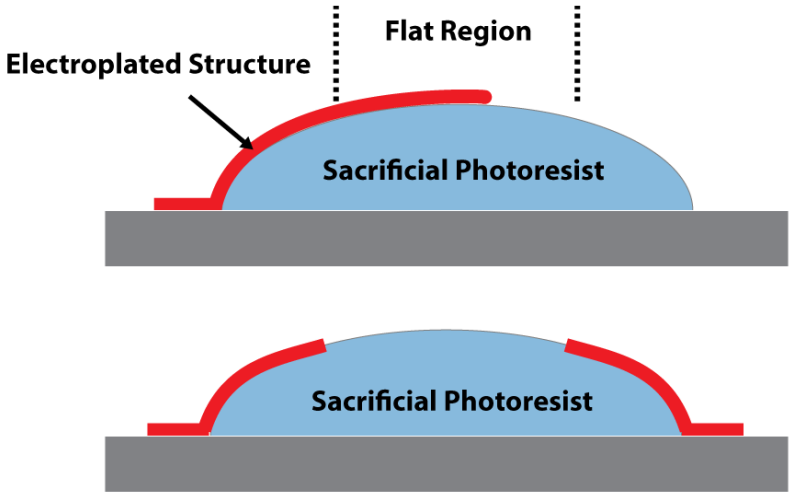


Figure 72: MFIs point upwards by not utilizing the flat region. It is also possible to increase pitch by using both sides of the sacrificial photoresist.

3.3.4 Electrical Results

A four point resistance measurement of a single MFIv2 (without contact resistance) is performed by directly probing an MFI on a four point probe station. In addition, the resistance, including contact resistance, is also measured using the setup shown in Figure 74. The resistance of a single MFIv2 is 48 $m\Omega$, and the resistance including the contact resistance on a pad coated with gold is 58 $m\Omega$. The resistance including the contact resistance on an aluminum pad without a gold layer is 298 $m\Omega$; the higher contact resistance may be caused by the native oxide that is formed on the aluminum pads.

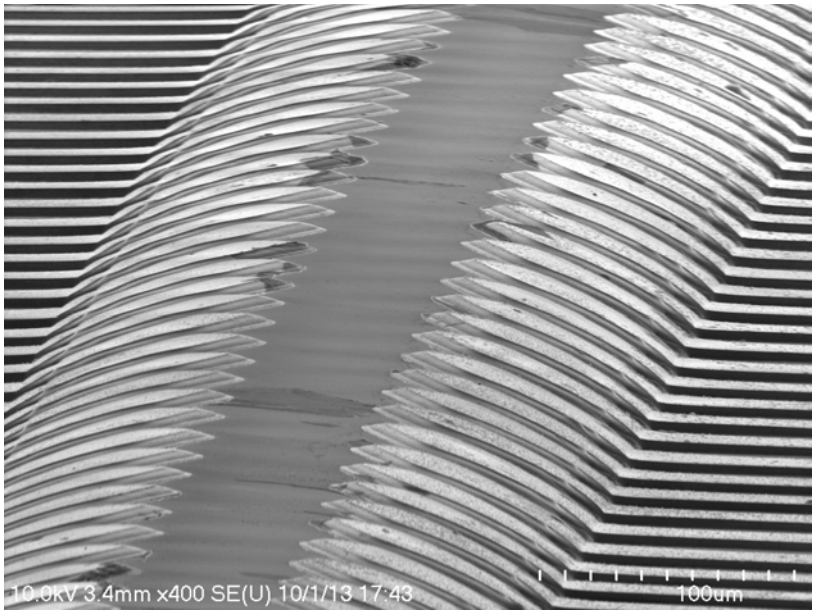


Figure 73: SEM of MFIs show pointy tip end of the structure.

3.4 Conclusion

A novel flexible interconnect technology called mechanically flexible interconnects (MFIs) is developed. The first generation of MFIs ("MFIv1") has a stand-off height of 20 μm and incorporates the tapered and the curved designs to increase the vertical elastic range of movement; a novel sacrificial reflowed photoresist process is developed to enable the fabrication of curved MFIs, and the benefit of the tapered design is analyzed. Mechanical FEM simulations and measurements are performed to verify that only a small amount of plastic deformation is experienced by MFIv1 when it is deflected 20 μm vertically. The fabrication process to form and confine solder balls at the tips of MFIs are also developed.

The second generation of MFIs ("MFIv2") has a stand-off height that is greater than 60 μm and incorporates both the reverse-tapered and the tapered design. The reverse-tapered region of the design produces a bending profile that allows the MFI's vertical range of motion to be increased significantly, while the tapered region of the design reduces the maximum stress to minimize plastic deformation. The pitch is

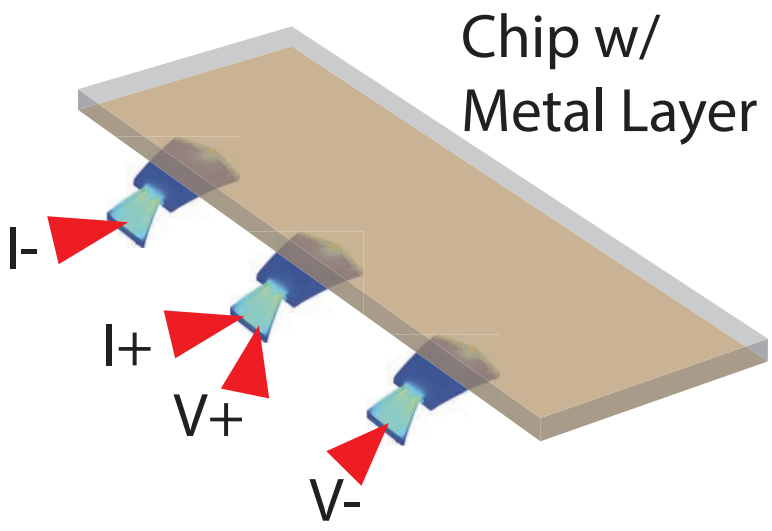


Figure 74: Test setup for four point probing resistances including contact resistance. The chip is mounted using PSAS to ensure consistent contact force.

doubled by forming MFIs on both sides of the curved surface, and pointy tips are produced by avoiding the flat region at the top of the sacrificial photoresist. The resistance of a single MFIv2, including the contact resistance with the pointy tip, is measured.

CHAPTER 4

POSITIVE SELF-ALIGNMENT STRUCTURES AND INVERTED PYRAMID PITS

4.1 Introduction

An accurate alignment is critical for the performance of interconnects between two substrates, so misalignment must be minimized. This chapter begins by outlining the effect of misalignment on the performance of electrical and optical interconnects between substrates. Then, a novel self-alignment technology utilizing positive self-alignment structures (PSAS) and inverted pyramid pits ("pits") is introduced and experimentally demonstrated.

4.1.1 Effect of Misalignment on Pitch

Typically, alignment accuracy between two vertically stacked substrates limits the minimum pitch of interconnects. However, there are also other factors that may affect the pitch. For electrical interconnects, the size of the solder bumps typically limits the pitch, not the wires; and for nanophotonics, the size of the optical devices and fibers limit the pitch, not the waveguide dimensions. However, these limits are not fundamental limits; there are significant efforts to reduce the electrical I/O pitch as demonstrated in sub-10 μm bumps [55, 56], and there are also efforts to reduce the size of the nanophotonic devices, such as micro-ring modulators [57, 58]. As these limiting technologies continue to scale, it becomes increasingly important to improve alignment accuracy.

4.1.2 Effect of Misalignment on Bandwidth

The pitch of the interconnects directly affect the bandwidth density, as is evident from the definitions of bandwidth density (β) given for electrical and nanophotonic I/Os below.

$$\beta_{optical} = \frac{kB}{p} \tag{10}$$

$$\beta_{electrical} = \frac{B}{p} \tag{11}$$

where k is the number of wavelength-division multiplexing channels; B is the bit rate for a single wire or a waveguide; and p is the wire or the waveguide pitch.

For nanophotonic waveguides, the minimum pitch is also governed by the cross-talk. For a given length of a waveguide (z), the minimum pitch required to keep the cross-talk above 3dB is given by [58, 59]:

$$p = 0.12 log_e\left(\frac{56.6z}{\pi}\right) \tag{12}$$

Thus, the bandwidth potential may not fully utilized if the pitch is increased beyond this limit due to the limitations of the alignment technology. Figure 75 shows that the bandwidth can theoretically be increased by 617% (from 31.25 Gbps$\cdot$ μm to 200 Gbps$\cdot\mu m$) if the misalignment is reduced from 5 μm to 0.5 μm (i.e. 10 μm pitch to 1 μm pitch); the theoretical system described in [58] is assumed to have 25 WDM channels, a bit rate of 12.5 Gbps, waveguide dimensions of 250 nm x 450 nm, and a waveguide length of 4 mm; however, a similar trend can be observed for state-of-the-art systems that have a less number of WDM channels.

4.1.3 Effect of Misalignment on Coupling Efficiency of I/Os

Alignment accuracy can also directly affect the coupling efficiency of the I/Os such as proximity I/Os (Figure 76) that link two substrates (Figure 77) in a stack. For example, the coupling loss in the proximity optical communication technology (Figure 78) is shown to be extremely sensitive to in-plane alignment [60], especially for

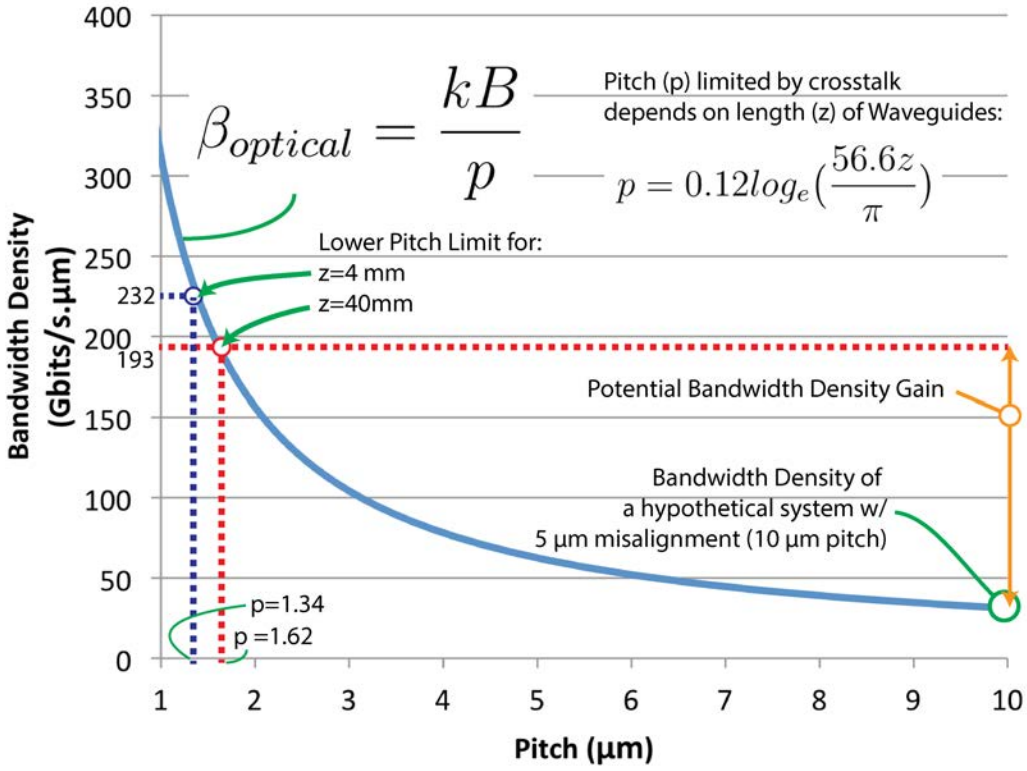


Figure 75: Bandwidth is plotted for various waveguide pitches. Twenty-five WDM channels (k) and a bit rate (B) of 12.5 Gbit/s are assumed. The cross-talk limited (maximum of 3dB coupling) minimum pitch and the maximum bandwidth are also plotted for 40 mm and 4 mm long 250 nm x 450 nm waveguides [58, 59].

micro-mirror couplers that are at a 54.7 °angle. For capacitive proximity communication, coupling capacitance decreases rapidly with increasing misalignment [16]; at the same time, cross-talk capacitance increases, resulting in an increased signal-to-noise ratio (SNR).

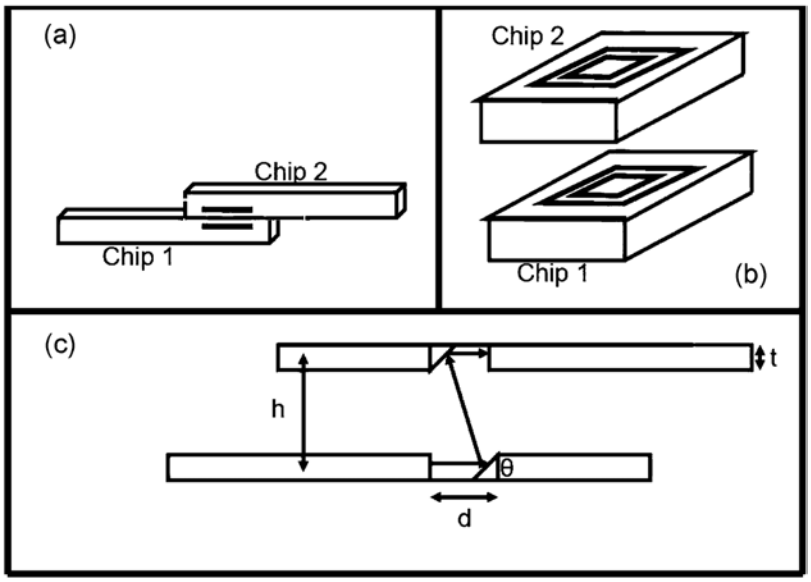


Figure 76: Capacitive (a), inductive (b), and optical (c) communication technologies are shown [16].

4.1.4 Cost of Accurate Alignment

Despite the benefits of accurately aligned tiles, bridges, and the package substrate, however, an accurate alignment is typically achieved at a steep cost when using conventional alignment techniques. For example, Panasonics's FCB3 with +/-3 μm accuracy is capable of placing chips at a speed of 1.8s/IC, while the same company's BM123 with +/-50 μm accuracy is capable of placing chips at a speed of 0.12s/IC [61, 62]. In sum, alignment accuracy requirement comes at a cost, and there is a significant manufacturing throughput benefit to a self-alignment technology that aligns chips to a <5 μm accuracy using a 50+ μm accuracy tool. In this chapter, a novel self-alignment technology is demonstrated, which allows a <5 μm accuracy alignment to be achieved with an initial coarse alignment of <150 μm. This technology is

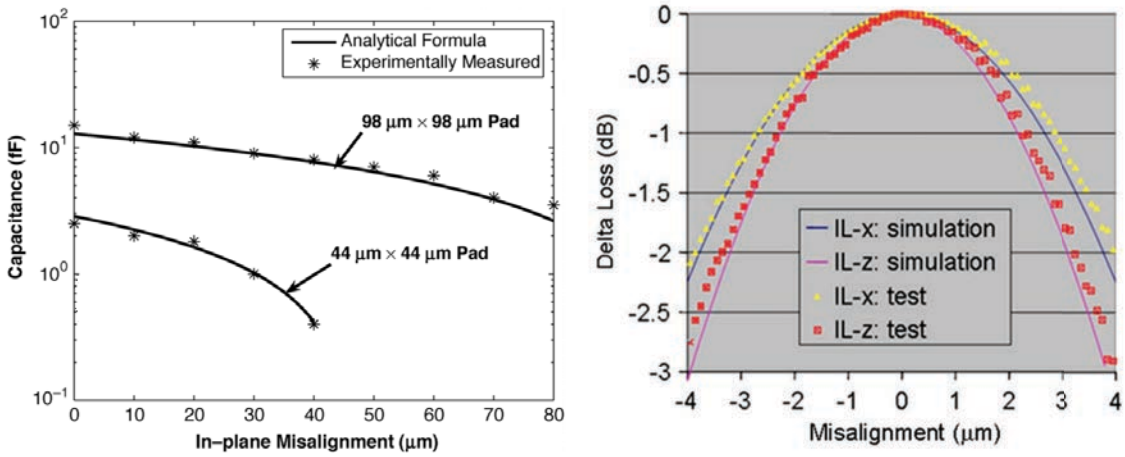


Figure 77: In-plane misalignment affects coupling efficiency. For example, coupling capacitance decreases with increased misalignment in capacitive proximity communication [16], while the coupling loss is increased with increased misalignment in optical proximity communication [60].

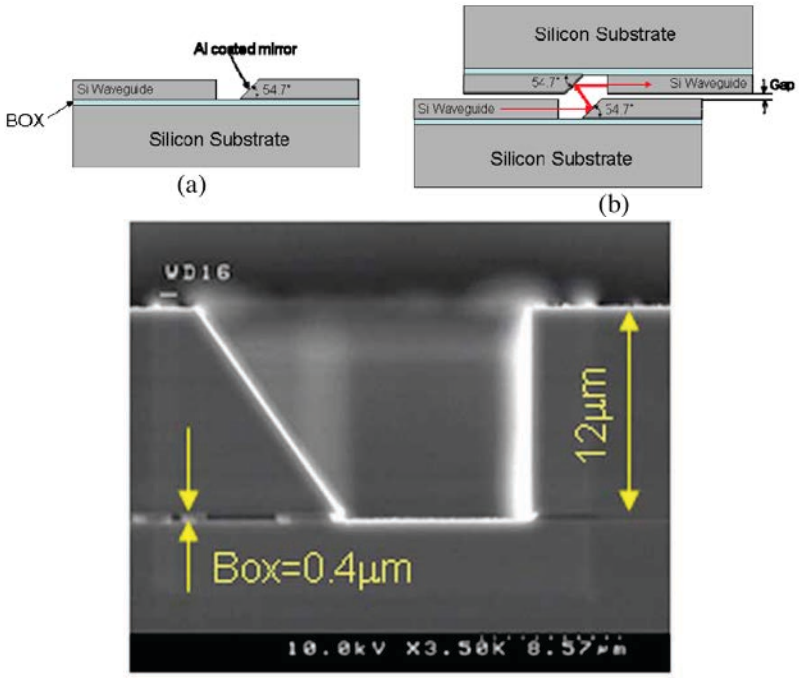


Figure 78: A reflective mirror used for optical proximity communication [63].

demonstrated on various substrates including silicon, FR4, and glass.

4.2 Self-alignment Mechanism

Two micro-fabricated structures are needed for the self-alignment technique described in this chapter: PSAS and pits. A PSAS and a pit are shown in Figure 79. PSAS are semi-sphere or truncated-sphere shaped structures that can be fabricated on any arbitrary planar substrate and are formed by reflowing cylindrical photoresist structures. Inverted pyramid pits are trench structures etched in <100> silicon substrates; the four sides are each at an angle of 54.7 °.

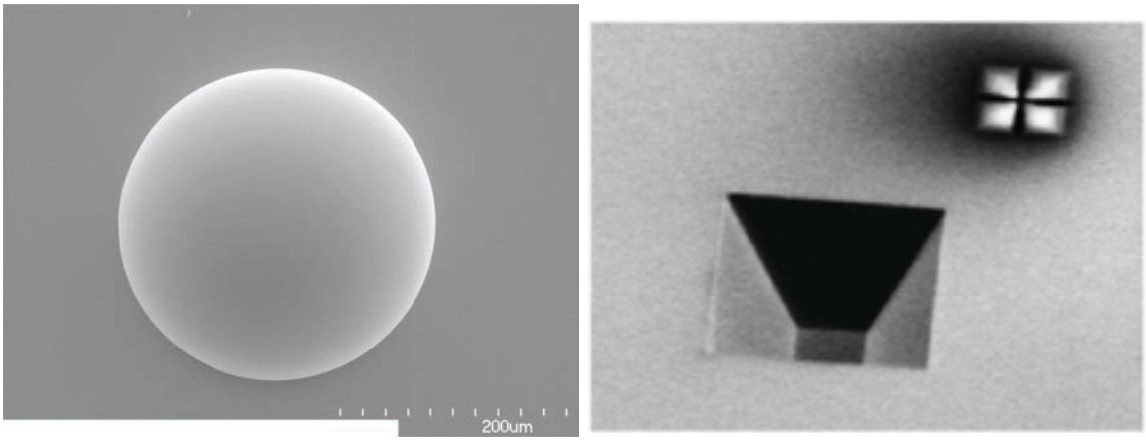


Figure 79: A PSAS (left) and a pit (right).

In the simplest configuration involving two substrates that need to be aligned, four PSAS are formed on the first substrate, and four pits are formed on the second substrate; the second substrate must be a <100> silicon substrate (Figure 80). The substrates are brought close together with a rough alignment. The large amount of misalignment tolerated by the mechanism (as much as the radius of PSAS, which is 150 μm) allows the assembly to be performed manually without a tool.

A small vertical pressure is applied to the top chip, which forces the four PSAS to slide along the sides of the pits. The four PSAS continue to slide until the center of each of the PSAS are aligned with the centers of the pits. At this point, a small "click" sound can be heard, which indicates that PSAS and pits have engaged; the

PSAS are in contact with all four sides of the pits, and the two substrates are locked in alignment as long as a continuous compression force is applied to keep the PSAS and pits engaged.

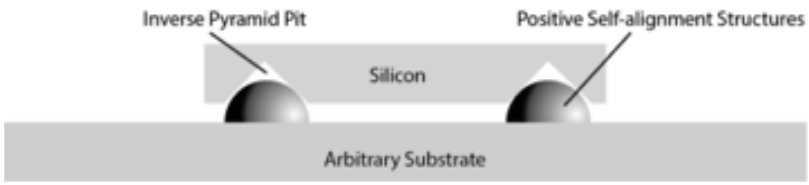


Figure 80: Simplest configuration involving PSAS and pits.

4.3 Other Self-alignment Technologies

There are many novel self-alignment technologies described in the literature because of the significant benefits associated with them. Most notably, the Ball-in-Pit technology by Oracle Labs [7] uses two inverted pyramid pits with a sapphire ball to align two substrates. While the alignment mechanism is similar and in fact helped inspire this research, there are several significant differences between this work and the Ball-in-Pit technique.

First, a PSAS can be fabricated on any surface in which photolithography can be performed. This implies that a PSAS can be fabricated not only on silicon wafers, but also on non-silicon substrates such as FR4 PWB and glass substrates. The alignment of a FR4 substrate with a silicon substrate using PSAS is demonstrated in this work [64].

Second, a PSAS does not damage the surface underneath it. This means that electronics can be located directly underneath a PSAS structure, and thus the active silicon area is not wasted.

Finally, a PSAS can be compressed at higher temperatures and removed. Therefore, a PSAS can be used to align substrates during a thermo-compression bonding

process, and it can also be removed after assembly to improve reliability. Thermo-compression bonding with a PSAS is demonstrated in a subsequent chapter.

There are also other self-alignment mechanisms that have been published recently. One method of self-alignment is to use the surface tension of the solder ball itself [65], as well as the surface tension of water [66] and flux [67]. While these techniques are good alternative self-alignment technologies, additional complications must be addressed to ensure an accurate alignment; clean dicing, chip leveling, and precise volume control are some examples of the factors that must be carefully controlled for these technologies. In addition, compared to these technologies, the combination of a positive structure and a negative structure used in this work allows one to minimize and control the gap between the substrates, which is essential for nanophotonics-enabled systems.

4.4 Fabrication

4.4.1 Fabrication of Positive Self-alignment Structures (PSAS)

PSAS fabrication begins by spin coating an AZ 40XT-11D photoresist layer. Next, the layer is patterned into circular patterns with diameters equal to the base of the PSAS. The photoresist is a chemically-amplified (CA) positive-tone thick resist designed for etching and electroplating applications. While CA photoresists are different from DNQ-based photoresists used for the MFIs, it is determined that the two types of photoresists have a very similar reflow characteristic; specifically, it is experimentally seen that the AZ 40XT photoresist reflows at 130 °C and that the Tg is raised during the baking process. Therefore, the ramped temperature profile developed in the previous chapter can be used to minimize the deviation during the reflow process.

4.4.2 Inverted Pyramid Pit Structures

Inverted pyramid pits are fabricated using a chemical wet etch process commonly used to make bulk micro-machined devices (Figure 79). A solution of KOH is used

to anisotropically etch the [100] silicon wafer. Alternatively, a TMAH-based etch solution can be used [68] for the CMOS process compatibility. In calculating the widths of the final pit structure, it is important to note that {111} is also etched, albeit much more slowly. This results in an undercut, which produces an opening that is slightly larger than the original pattern. Etching a 300 μm x 300 μm opening on a layer of silicon oxide deposited using an LPCVD tool results in an opening of 305 μm x 305 μm.

4.5 Geometrical Considerations

The shape of the PSAS and the pit structure determines the final relative position of the two substrates. In this section, the shape of the PSAS is characterized, and the relationship between various controllable dimensions and the size of the gap between two substrates are examined. Pit structures are not explored in this work as the process for fabricating such structures is already well documented in the MEMS related literature.

4.5.1 Approximating PSAS Shape

The PSAS is fabricated by reflowing a cylindrical photoresist structure. Consequently, the final shape can be determined using the same methods used to predict the shape of a reflowed solder ball; various methods for predicting the reflowed solder ball shape have been described in [69].

In this work, the reflowed structure is approximated as a truncated sphere. In order to verify that the approximation is accurate in describing the PSAS structure, the shape of the PSAS is measured using a confocal laser microscope capable of capturing the surface profile of a 3D structure. The captured profile of a PSAS is shown in Figure 81. The analysis of the captured data showed that:

- the profile of the PSAS surface through the center can be accurately approximated as a circular segment.

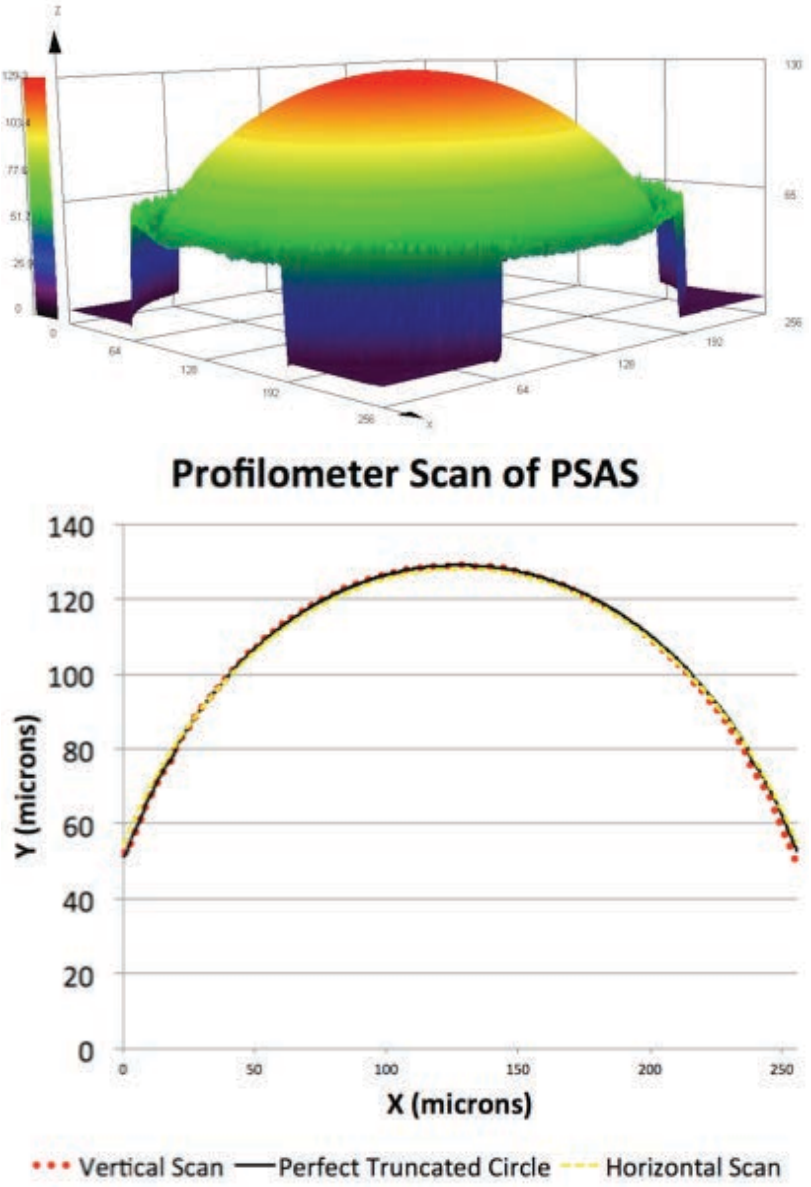


Figure 81: 3D image of a PSAS scanned by a confocal laser microscope, and a plot showing the measured profile of the PSAS through the center point. Also plotted is a perfect truncated circle with a radius of 148 μm.

- the PSAS surface is radially symmetric, evident from the identical horizontal and vertical profiles extracted from the captured data.

From the results, it is possible to conclude that the shape of the PSAS approximately represents a truncated sphere.

4.5.2 PSAS Diameter, Pit Opening Size, and Gap

The critical variables that can be easily controlled are the PSAS radius/diameter and the width of the pit openings. These two variables determine the final position of the PSAS inside the pit structure and can affect the relative positioning of the two substrates in all 6 degrees of freedom. However, if the shape and the distances between four PSAS/pit pairs are identical, only the resulting gaps between the substrates become sensitive to the shapes of the PSAS and pits.

In addition, the width of the pits also determines the maximum initial misalignment for the self-alignment mechanism to work. It can be seen that the initial coarse alignment tolerated is equal to half the width of the pit. Initial alignment within this range will place the centers of the PSAS inside the pit region, thereby causing them to slide and be guided into the centers of the pits.

In this work, the pit is fabricated with a 300 μm width, which allows up to 150 μm of initial misalignment. At these dimensions, it is possible to align two substrates using tweezers, without a placement tool. The next section will derive the quantitative relationships between the PSAS and the pit dimensions and the resulting gap.

4.5.3 Relationship between PSAS Radius, Pit Width, and Gap

Figure 82 shows the geometry involved in the self-alignment mechanism, and the gap between the substrates can be derived as shown below. The triangle represents the cross-section of the inverted pyramid pit; α, is the (111) plane in the silicon crystal, which is at an angle of 54.7° (β becomes 35.3°). The semi-circle and circle segments

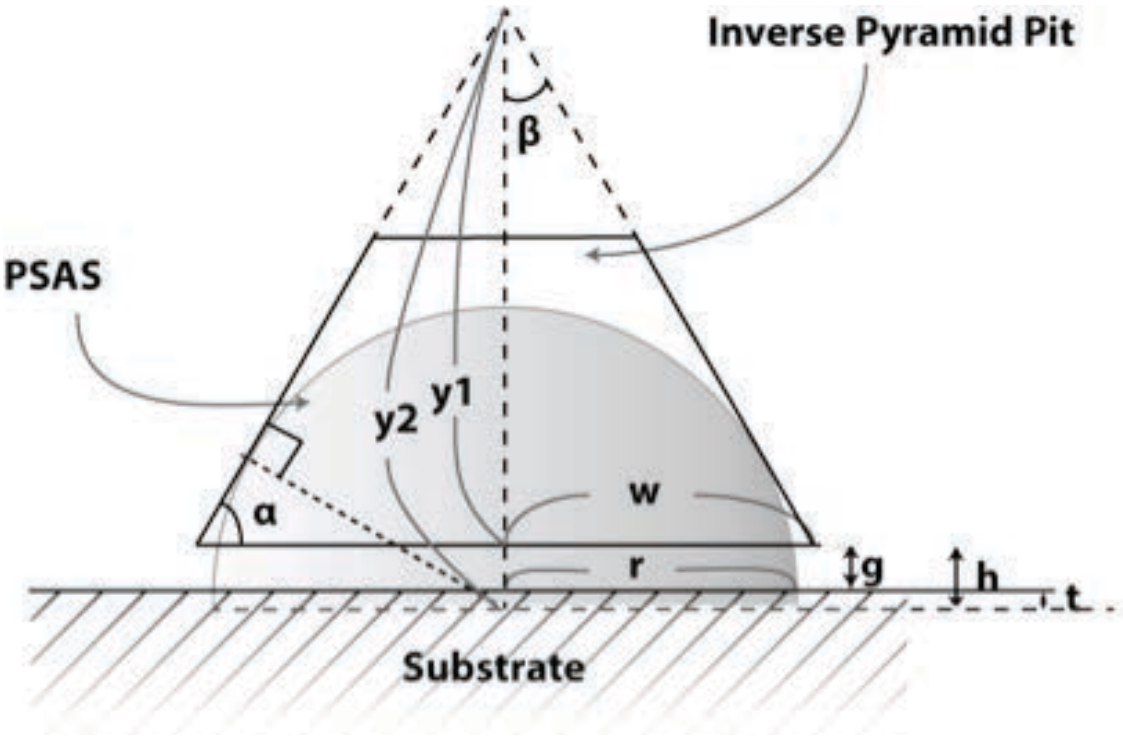


Figure 82: Geometry involved in the self-alignment mechanism.

represent the PSAS; g is the gap between the two chips, and h is the distance from the surface of the top chip to the imaginary center of the sphere. If the PSAS is a semi-sphere, then g will be identical to h; and t, which is the difference between h and g, would be zero.

The pit depth, y_1, can be calculated using simple geometry considerations, as shown below:

$$\begin{aligned} tan(\beta) &= \frac{w}{y_1} \\ y_1 &= \frac{w}{tan(\beta)} \end{aligned} \tag{13}$$

where w is half the side width of the pit.

Similarly, y_2 can be calculated as

$$\begin{aligned} sin(\beta) &= \frac{r}{y_2} \\ y_2 &= \frac{r}{sin(\beta)} \end{aligned} \tag{14}$$

As a result, h and g can be derived as

$$\begin{aligned} h &= y_2 - y_1 \\ h &= \frac{r}{sin(\beta)} - \frac{w}{tan(\beta)} \\ g &= h - t \\ g &= \frac{r}{sin(\beta)} - \frac{w}{tan(\beta)} - t \end{aligned} \tag{15}$$

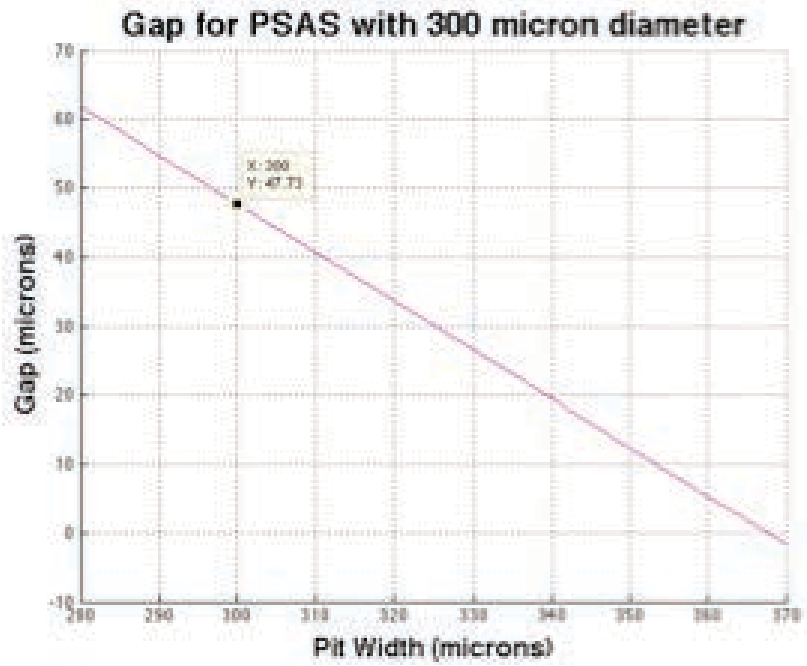


Figure 83: For a fixed PSAS diameter, the gap is dependent on the opening size of the pit. The graph is plotted for a semi-sphere PSAS (i.e., t=0).

Eq. 15 shows that the gap is dependent on both the pit width and the PSAS radius. Figure 83 illustrates the predicted gap as a function of the pit width.

Two versions of PSAS are developed. The first version is a semi-sphere PSAS with a base radius of 150 μm. It is fabricated by reflowing a photoresist cylinder that has a 150 μm base radius and is 90 μm tall. The expected gap with this PSAS is 48 μm, as shown in Figure 83. The second version is a truncated-sphere PSAS with t=20 μm. It has a base radius of 150 μm, and it is 130 μm tall. It is fabricated by reflowing a cylinder patterned photoresist that has a 150 μm base radius and is

95 μm tall. The expected gap with this PSAS is 28 μm .

4.6 Experimental Setup

The alignment capability of the PSAS and pits is demonstrated in two sets of experiments. The first experiment represents the simplest configuration involving two substrates. The pits are fabricated on a silicon substrate and aligned with a silicon substrate, an FR4 substrate, and a glass substrate with the PSAS. This demonstrates that the PSAS and pits can be used to align silicon interposer tiles to a wide range of substrates.

The second experiment aligns multiple silicon substrates in a 3D configuration. This demonstrates that the PSAS and pit can be used to align two or more layers of substrates. This is important because the silicon bridges are aligned on top of the silicon interposer tiles, which are also aligned with the PSAS and pit to an FR4 substrate. In other words, the silicon interposer configuration is essentially a 3D stack with three layers.

4.6.1 Vernier Patterns for Measuring Misalignment

Vernier patterns are used to measure alignment accuracy (Figure 84). The patterns include two separate scales that are aligned in the center, but have a different spacing between tick marks; when two substrates containing vernier patterns become misaligned relative to each other, the center tick marks become misaligned. However, because of the different spacings between the two scales, another set of tick marks away from the center becomes aligned instead. By determining which of the tick marks are aligned and the location of such tick marks relative to the center, it becomes possible to measure the misalignment with a resolution that is significantly smaller than the tick mark spacing.

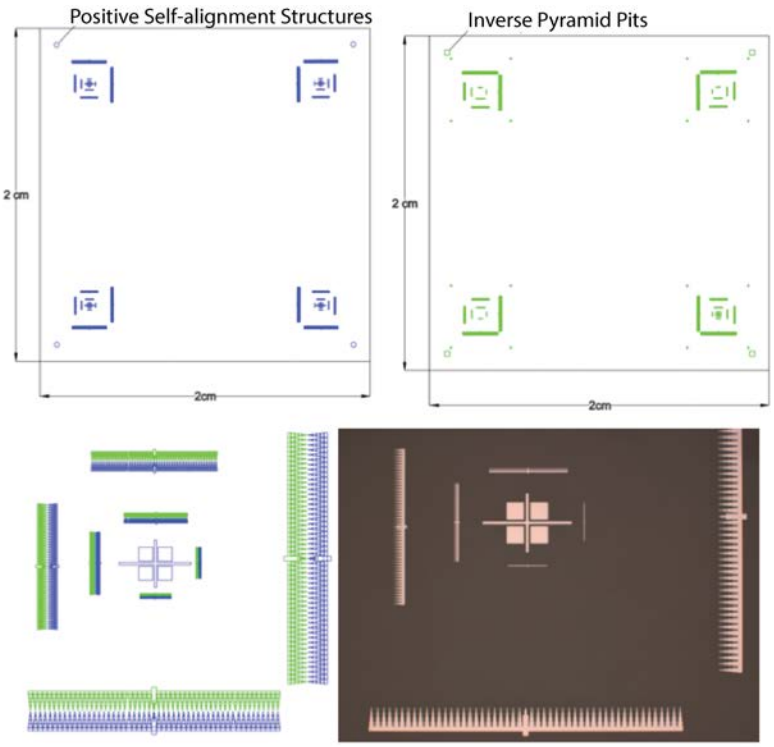


Figure 84: The mask layout used for the assembly experiment contains two sets of corresponding vernier scale patterns (one on each chip) designed to measure the relative alignment accuracy.

4.6.2 Fabrication of Vernier Patterns

Vernier patterns on the chip containing the PSAS are fabricated using a lift-off process. The process begins with a silicon dioxide layer deposited on a blank wafer using a PECVD tool. Next, a negative resist (NR71-3000PY) is patterned, which contains the vernier scale pattern as well as circles where PSAS is to be located. Next, 300 Å of titanium is deposited using an e-beam evaporator. Finally, the negative resist is removed by submerging the wafer in acetone placed inside an ultrasonic bath. A 300 Å thick titanium layer is sufficiently thick to be visible under an infrared microscope.

A vernier pattern on the chip containing the pits can be fabricated in two ways. It can be fabricated using the same lift-off process described above, or the pit and the vernier pattern can be fabricated simultaneously. To fabricate the pattern simultaneously, the silicon nitride mask layer for the pit fabrication is patterned with both the pit openings and vernier patterns. A subsequent KOH etching process creates the pits, and the areas under the vernier patterns are also etched to cause the teethmarks to become suspended, as shown in Figure 85. By fabricating the pit simultaneously with the vernier patterns, the lithography induced misalignment between the pit pattern and the vernier pattern can be eliminated.

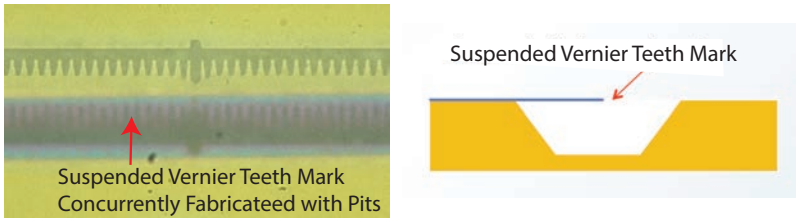


Figure 85: Suspended vernier teeth marks can be concurrently fabricated with the pits to eliminate the misalignment between the vernier pattern and the pit.

4.6.3 Factors Affecting Alignment Accuracy

There are two major sources of inaccuracy. The first factor is from the mask aligner (Karl Suss MA6). Even though the tool specification shows that a topside alignment (TSA) having an error as low as 0.5 μm is achievable, previous experiments have shown that the misalignment can be as large as +/-2 μm in many cases. In this work, PSAS (and pits if not fabricated simultaneously with the vernier patterns) are aligned to the vernier patterns using the mask aligner.

The second factor is human error. Using the vernier patterns require a person to subjectively decide which of the tick marks aligns the best, but in some cases this is very difficult to discern. In difficult cases, a set of three aligned vernier tick marks is identified instead of a single mark.

4.7 Alignment Results

Two PSAS demonstrations are needed to achieve the configuration described in Figure 2. The first is the demonstration of alignment accuracy for various substrate materials including silicon, glass, and FR4. This demonstrates that PSAS can be used to align interposer tiles directly on an FR4 package substrate. The second is the ability to align multiple layers and the ability to measure the misalignment at each interface. This is important because the proposed 2.5D platform, which involves the FR4 package substrate, interposer tiles and a bridge, is essentially a three-layer stack of substrates that need to be aligned using PSAS.

4.7.1 Alignment of Silicon to Silicon, Glass, and FR4

In this experiment, four inverted pyramid pits are fabricated on 2cm x 2cm silicon substrates, while four PSAS are fabricated on three different types of substrates: silicon, glass, and FR4 (Figure 86). The alignment is performed manually using PSAS and without the aid of a placement tool, and the alignment accuracy is measured by

visually observing the vernier patterns under an infrared (Figure 87) or an optical (Figure 88) microscope (for glass). Table 2 shows the results of the experiment.

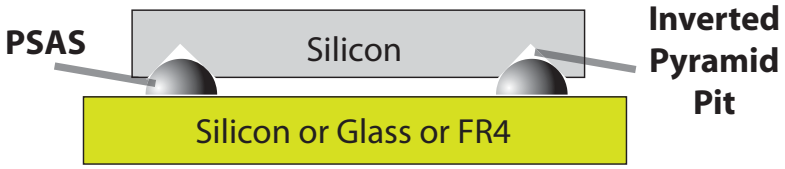


Figure 86: A silicon substrate with four inverted pyramid pits is aligned with three different types of substrates containing four PSAS on the surface.

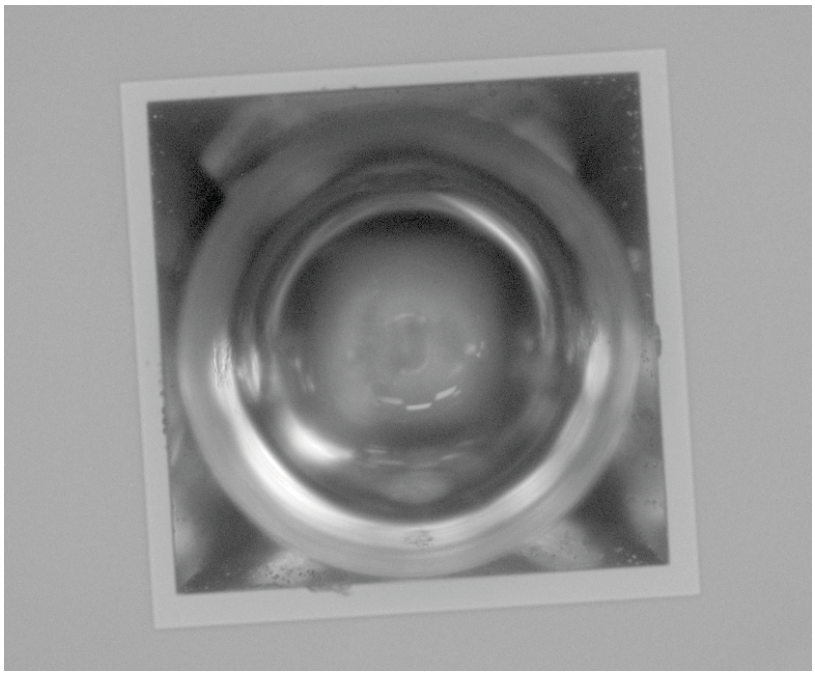


Figure 87: Infrared image showing a PSAS inside a pit.

To observe smaller vernier patterns, which can resolve much smaller misalignments, higher magnifications are needed. However, the limited depth of field and the gap between two substrates makes simultaneous focusing of the two patterns impossible. To address this, two sets of microscope images are captured each at a focal plane; the images are then merged in the post-processing, similar to the "focus stacking" technique. Figure 90 shows the infrared microscope images for silicon to FR4 alignment.

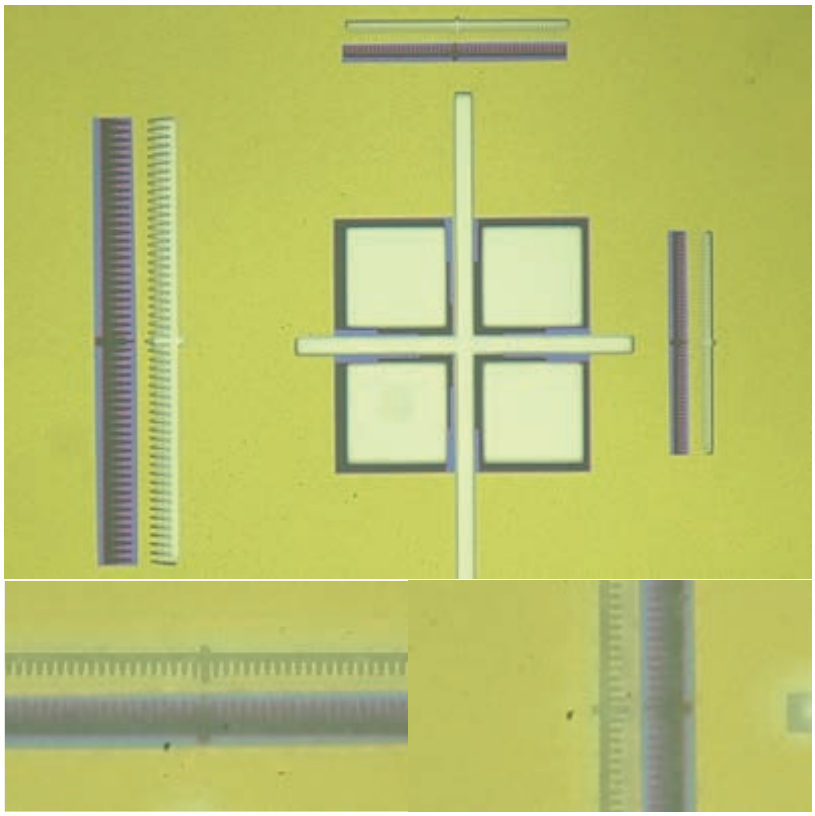


Figure 88: Optical microscope image showing the overlay of the two vernier scale patterns. The bottom images show high magnification images of the smallest vernier patterns.

Table 2: Misalignment in μm for Silicon to Silicon/Glass/FR4 Substrates

Regions	Glass		Polished Silicon		FR4	
	X	Y	X	Y	X	Y
	(μm)		(μm)		(μm)	
Bottom Left	>-1	+1	<+1	<+1	+4.4	+2.0
Bottom Right	-1	<+1	+1	+1	+3.2	-3.2
Top Right	+1	-5.8	<+1	+1	-1.6	-3.2
Top Left	+1	-5.6	<+1	<+1	-2.8	+2.4

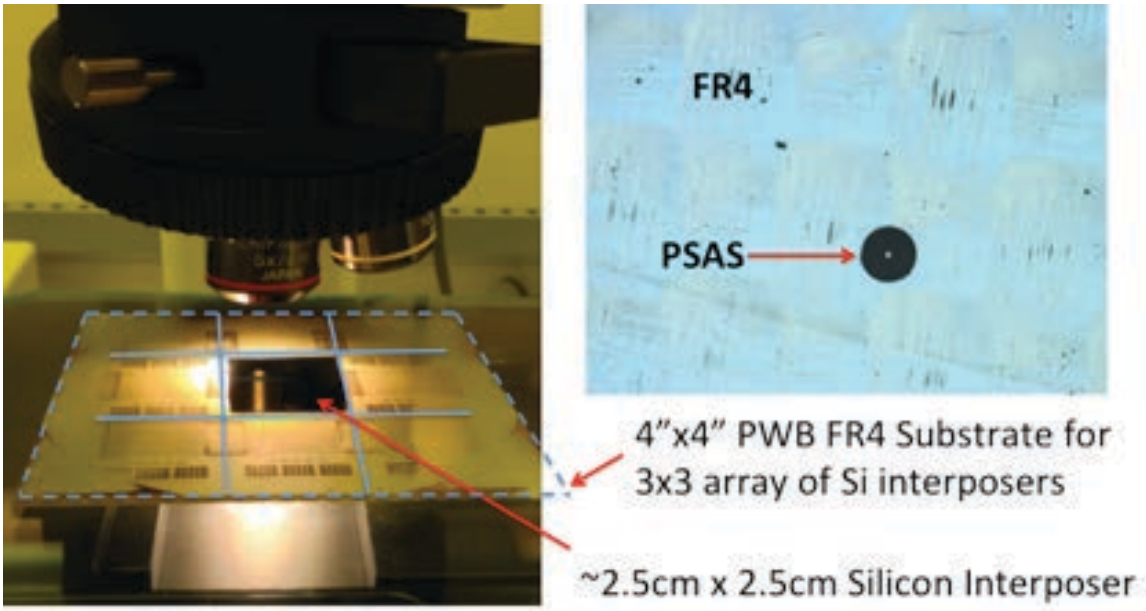


Figure 89: Image of misalignment between an interposer and an FR4 PWB being measured using infrared microscopy (left). Optical microscope image showing reflowed PSAS on the FR4 PWB (right).

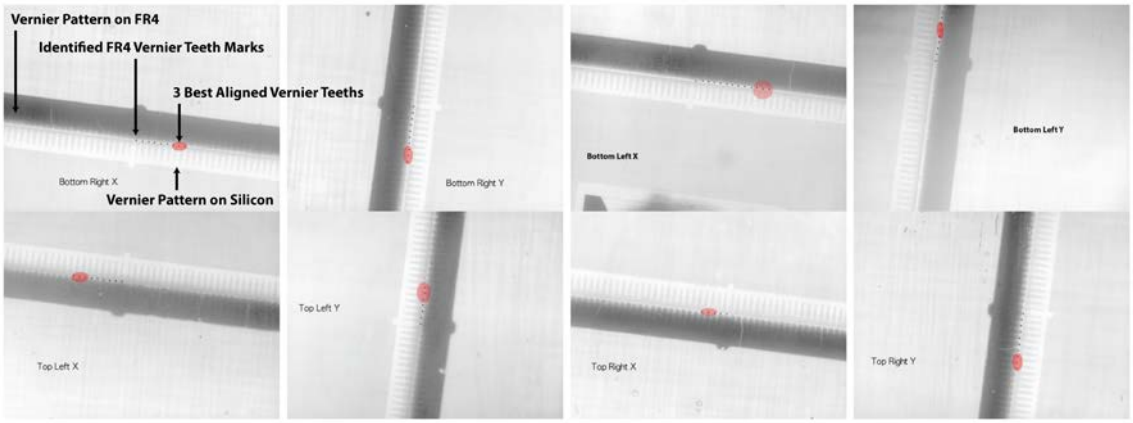


Figure 90: Silicon to FR4 misalignment measurement using infrared microscopy.

For the two silicon substrates, the misalignment could not be observed using the vernier patterns, which indicates that the misalignment is less than the resolution of both the vernier pattern and the mask (1 μm). For glass substrates, the measured misalignment was within the accuracy of the mask used except in the Y-axis of the top vernier patterns.

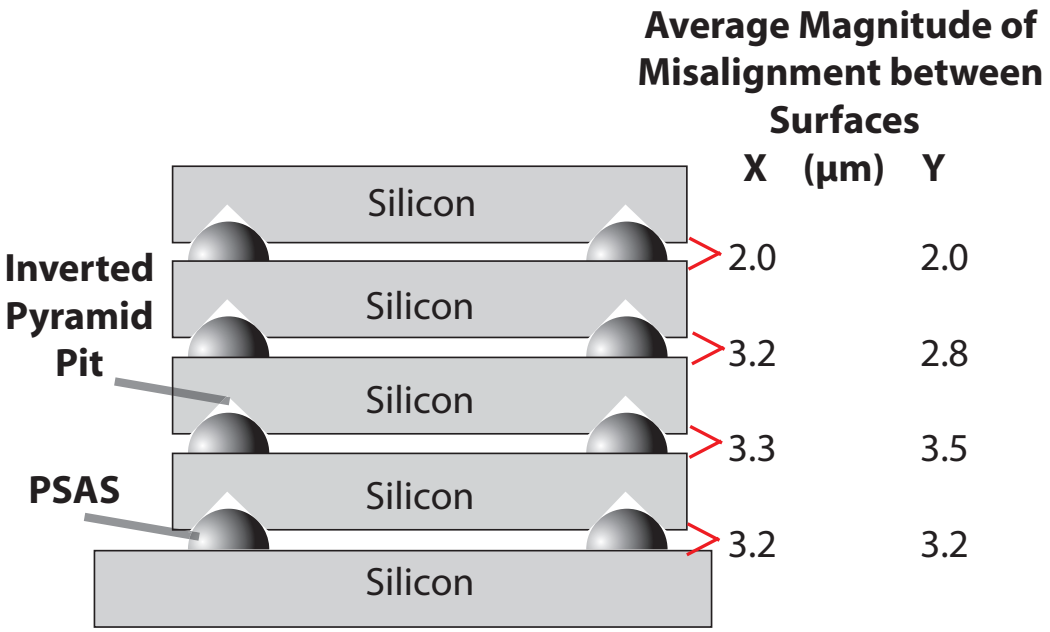


Figure 91: Five silicon substrates are aligned and stacked on top of each other. The average magnitude of misalignment at each interface is shown.

4.7.2 Alignment of Multiple Layers of Substrates

In this experiment, the PSAS' ability to align multiple layers of substrates, as well as our capability to measure misalignments at each interface, are demonstrated.

The experimental setup is shown in Figure 91; five 2cm x 2cm silicon substrates are aligned and stacked on top of each other without a placement tool. The PSAS and the inverted pyramid pits in the chips were fabricated similarly to the ones described in the previous section. However, the pits and the PSAS are fabricated on the two sides of the same wafer, and the front and back side vernier patterns are aligned using a back-side mask alignment tool.

The alignment accuracy between the different surfaces in each stack of five substrates is also measured using an infrared microscope. By focusing on different focal planes (i.e., surfaces of substrates), it is possible to determine the misalignment at each interface. As a result, the misalignment from the back side alignment does not affect the measurement.

One challenge during the measurement is the degrading image fidelity and contrast as the microscope focuses on the lower surfaces of the stack; though it is possible to see the vernier patterns clearly in the first three substrates, the last two substrates are not clear enough for measurements. To obtain results for the last two surfaces, the stack is flipped upside down and then measured.

The misalignments are measured at all four corners of the chip at each interface; Figure 91 shows the average of misalignment measured at each interface. The results show that an alignment accuracy better that 4 μm can be achieved consistently.

4.8 Conclusion

A novel self-alignment technology is fabricated, and the accuracy of the technology is experimentally demonstrated between a silicon substrate and silicon, glass, and FR4 substrates. A stack of silicon substrates is also aligned and its accuracy measured. The accuracy of <4 μm is consistently demonstrated between two silicon substrates (including in a 3D configuration), and <5 μm misalignment is demonstrated between a silicon substrate and an FR4 substrate.

CHAPTER 5

SILICON INTERPOSER TILES AND BRIDGES

5.1 Introduction

This chapter combines the MFI and PSAS technologies to demonstrate the novel large-scale silicon system integration platform described in Chapter 1. Three silicon interposer tiles are aligned and mounted on a PWB, and two silicon bridges are aligned and mounted on top of the three interposer tiles; each silicon bridge spans two interposer tiles. Four PSAS and four inverted pyramid pits self-align a tile to the PWB and a bridge to two tiles. MFIs form rematable electrical interconnections between the three interposer tiles and two silicon bridges; MFIs are fabricated on the interposer tiles. Pointy tips on the MFIs form low contact resistance with the pads on the silicon bridges. An alignment accuracy of less than 8 μm between a silicon bridge and two tiles is demonstrated on an FR4 substrate. Daisy chain and four-point resistance measurements are performed to verify electrical connections between three interposer tiles via MFIs and silicon bridges.

5.2 PSAS Geometry and Fabrication

Eq. 15 is used to derive the dimensions of the PSAS and pits and the resulting gap between substrates. A semi-sphere version of the PSAS with base diameters of 150 μm and pits with 305 μm sides are used to produce a theoretical gap of 47.7 μm. Therefore, the minimum depth of the pit required is 102.27 μm.

Figure 93 shows a diagram of a pit etched using KOH. To produce pits with 305 μm sides, mask openings with 300 μm sides are used; the additional 5 μm results from the etching of the (111) plane, albeit at a slower etch rate compared to the (100)

plane. Since the depth of the pit does not affect alignment accuracy, the etching is stopped once the undercut reaches 5 μm. The undercut length is observed under the microscope through the transparent silicon nitride mask layer every 10 minutes of etching beyond the initial 3 hours, and the slow rate of etching in the (111) plane allows the process to be controlled very accurately. The undercut length ($\delta/2$) can be evaluated with:

$$\frac{\delta}{2} = \frac{t \cdot R < 111 >}{sin(54.7\ ^\circ)} \tag{16}$$

where t is the etch time in hours and R<111>is the etch rate of the (111) plane.

The etching is performed in a temperature controlled bath set at 75 °C with a 45% KOH solution. The expected and the observed etch rate of the (100) plane is approximately 40 $\mu m/hr$ (Figure 92), and a (100) plane etch rate to (111) plane etch rate ratio (i.e. R<100>/ R<111>) of 30 to 35 is observed. Therefore, the 5 μm undercut is created with an etch time (t) between 3 and 3.5 hours, and the resulting depth ranges from 120 μm to 140 μm.

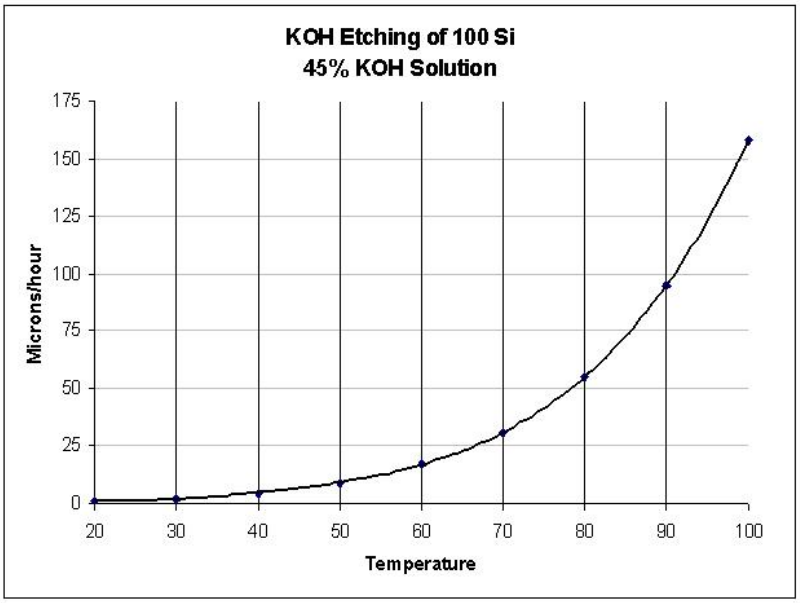


Figure 92: Etch rate of a <100>silicon wafer at various temperatures [70].

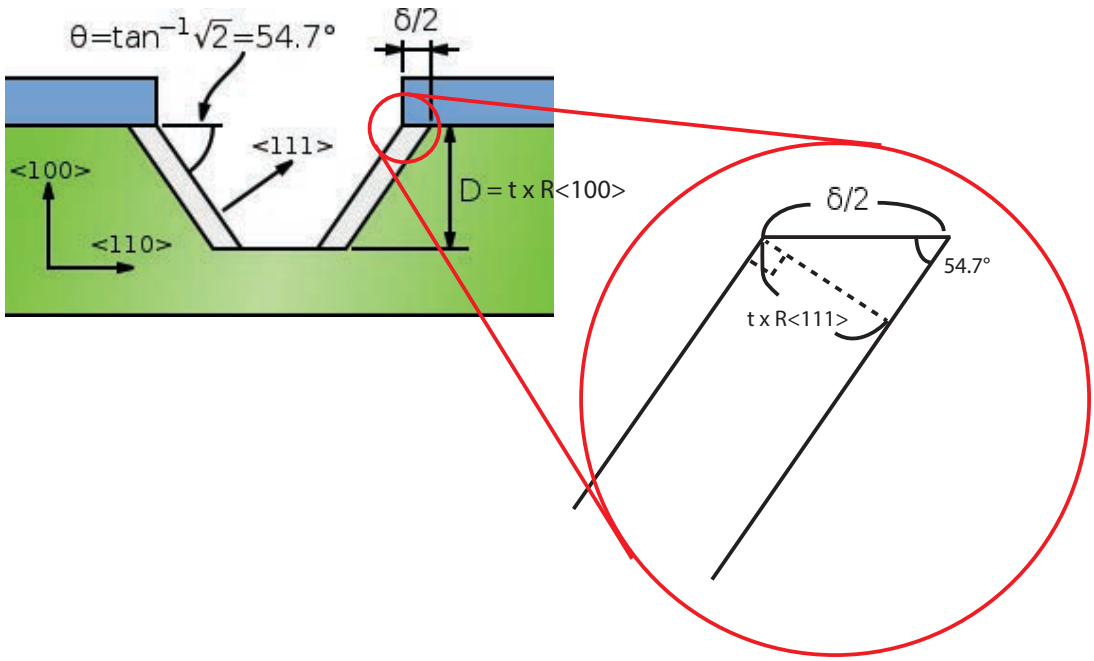


Figure 93: Calculating mask undercut during a KOH etch process.

Phosphorus doped (1-10$\Omega \cdot cm$) wafers are used for pit wafers since boron doping can affect anisotropic etch rates. In addition, prime wafers with the lowest available total thickness variation (TTV) (<5 μm) are used for maximum alignment accuracy. The wafers are also double side polished with a 525 μm thickness. Once the box of wafers is opened, the wafers are cleaned using a piranha solution, and 2 μm of LPCVD silicon nitride layers are deposited immediately thereafter. The silicon nitride layers are used as the mask material for the KOH etch and as the passivation layer for the traces.

5.3 MFI Optimization

The design of MFIs must be optimized for the expected gap of 48 μm produced by the PSAS and the pits. This means that the final height, including the MFI thickness, will be 48 μm, and the tip must remain the highest point and the stress must be below the yield stress of nickel tungsten (1.9 GPa) when the MFIs are deformed to the final

height of 48 μm. The initial MFI stand-off height must also be 5 μm above the 48 μm final height to compensate for the 5 μm TTV inherent in the wafer; however, an even greater initial MFI stand-off height is desired if it can be attained.

To satisfy these constraints, various parameters of the MFIv2 design are optimized using Comsol FEM software. Most importantly, the ratio of the tapered length to the reverse tapered length, the initial stand-off height, and the offset from the center that determines the initial tip angle, are defined as variables (Figure 94), and their relationships with relevant performance metrics are shown in Table 3. Increasing the tapered length distributes stress over a larger area, which reduces mechanical stress; at the same time, this reduces the reverse tapered length, which results in a worse bending profile (i.e., the tip is rolled more easily). Increasing the stand-off height allows larger surface variations to be compensated and produces MFIs at a greater slope because of the increased height of the sacrificial photoresist; however, the level of deflection is increased, which increases the stress. Increasing the offset from the center results in MFIs with a greater initial tip angle because the more sloped area of the sacrificial photoresist is utilized; as a result, the bending profile is improved but the increased offset from the center requires a taller sacrificial photoresist to be formed to maintain the same initial stand-off height, and the pitch is also increased due to the wasted flat region at the center. Other adjustable parameters include the MFI thickness, the reverse-taper width, the MFI length, and the tip shape. Figure 94 shows the stress and the bending profile of the optimized MFIs.

5.4 Interposer Tile Design and Fabrication

The interposer tiles contain pits on both sides of the wafer at the same four corners. Moreover, MFIs are fabricated on the top surface facing away from the motherboard. Copper wires are also fabricated on the top surface to connect the MFIs in a daisy chain configuration in conjunction with wires on the bridge chips. The dimensions of

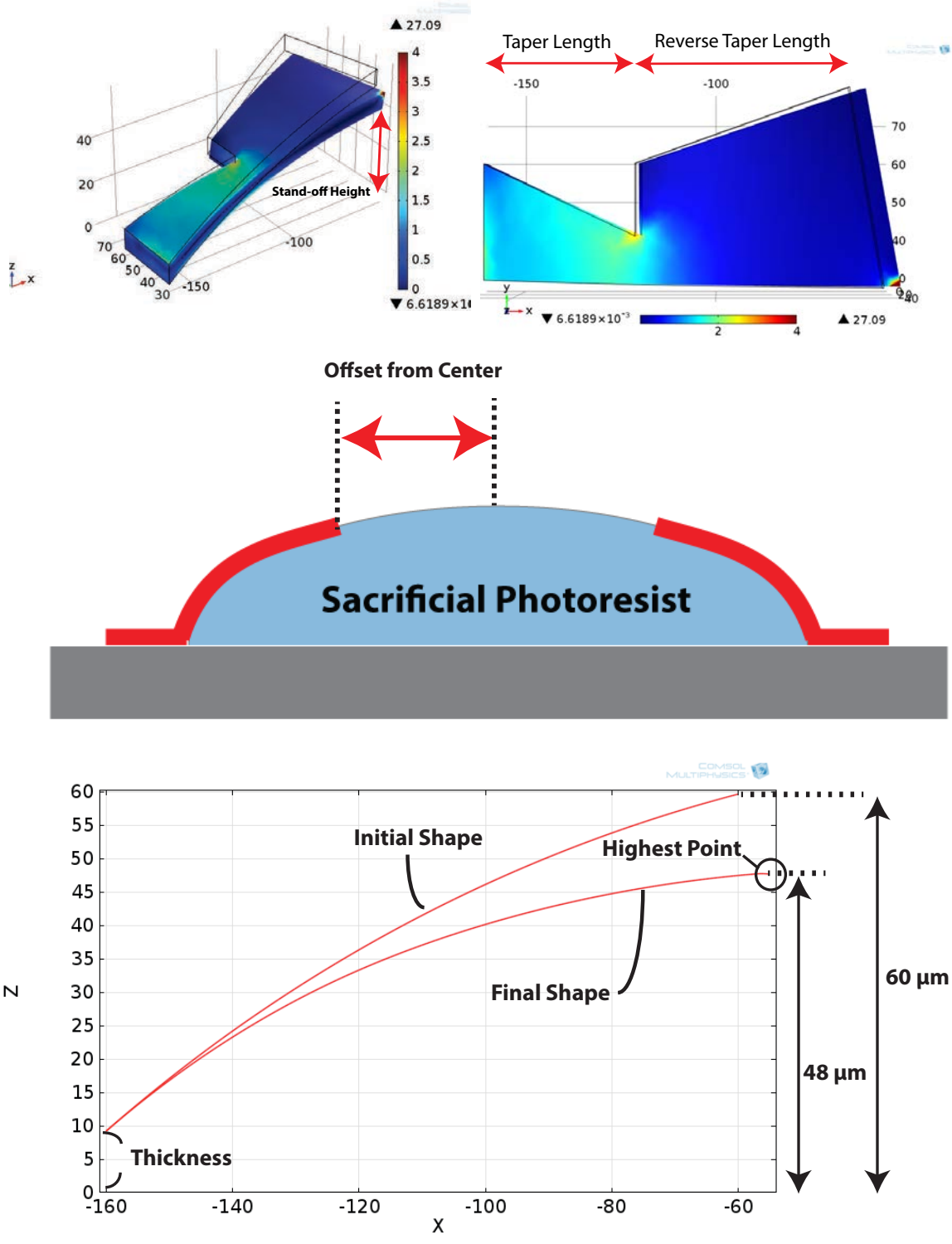


Figure 94: Optimized shape of MFIv2 shows that the maximum stress is in the elastic regime. The bending profile shows that the tip remains the highest point of the structure.

Table 3: The relationship between MFI parameters and performance metrics.

	Affected Metrics			
Increased Parameters	*Mechanical Stress at Final Height*	*Surface Variation Compensation*	*Initial Tip Angle*	*Bending Profile*
Taper to Reverse Taper Length	↑	–	–	↓
Initial Stand-off Height	↓	↑	↑	–
Offset from Center	–	–	↑↑	↑

a single interposer tile die are 2cm x 2cm, and thirteen interposers can be fabricated on a single 4-inch wafer.

Four masks are used to fabricate wafers containing interposer tiles. The first mask contains squares for pits ("pits mask"); the second mask contains rectangles for the sacrificial photoresist used in fabricating MFIs ("sacrificial PR mask"); the third mask contains an array of MFI geometry ("MFI mask"); and the forth mask contains wires, vernier patterns, and other alignment marks ("traces mask").

The pits on both sides of the wafer are fabricated first and concurrently. Using the pits mask, the squares are patterned on one side of the wafer, and a back side alignment (BSA) technique is used to pattern the back side of the wafer. The symmetric mask allows the same mask to be used to pattern both sides. An anisotropic etch in a KOH solution etches both sides of the wafer concurrently.

The traces mask is used to form the wires, vernier patterns, and other alignment features. A lift-off process is used to deposit titanium, copper, and titanium layers. The mask also contains squares with thick borders, as shown in Figure 95. These square patterns are used to align the trace mask to the pits that are formed first; the oxide openings of the pits fit inside the bordered squares.

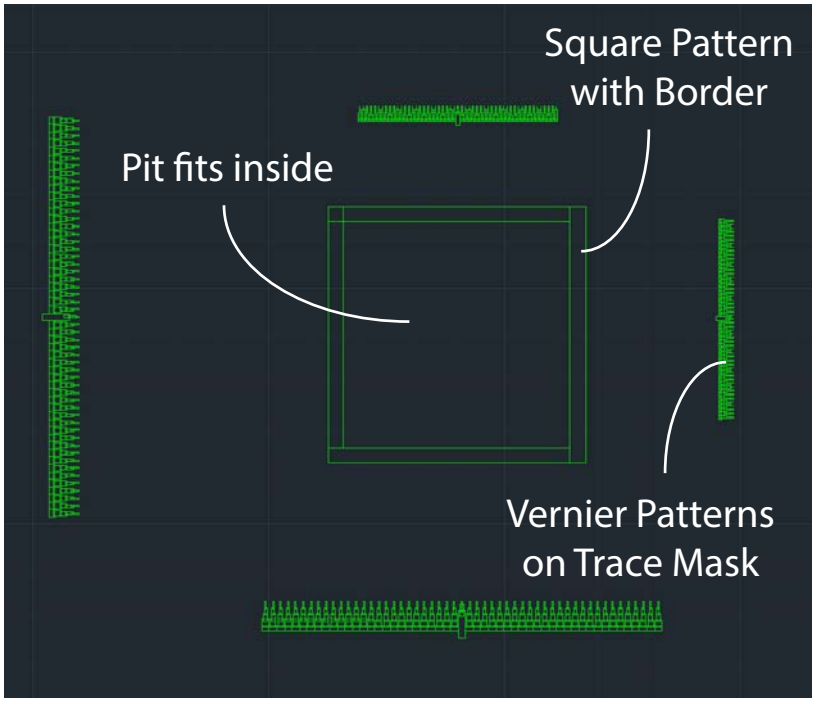


Figure 95: A square pattern with a thick border is used to align the traces mask to the pits.

Next, MFIs are fabricated by initially forming the sacrificial photoresist structures with the sacrificial PR mask. A feature-to-feature alignment technique is used, as shown in Figure 96, to align the sacrificial photoresist mask to the traces. Feature-to-feature alignment is necessary because the presence of alignment marks on the sacrificial photoresist mask reflows to form an arbitrary structure that may not be completely covered using the seed layer deposition method; an incomplete coverage by the seed layer causes the electroplating mold and the sacrificial photoresist to interact, which can cause catastrophic damage to the sample.

After the reflowing and baking of the photoresist, a seed layer is deposited on top, and the MFI mask is used to pattern the electroplating mold. Following the electrodeposition of nickel tungsten, the electroplating mold, seed layer, and sacrificial photoresist are removed. The wafer is then diced, and a gold layer is deposited on top of the traces and on the MFI surfaces using an electroless deposition process. The pits and the MFIs that are fabricated on the same wafer surface are shown in

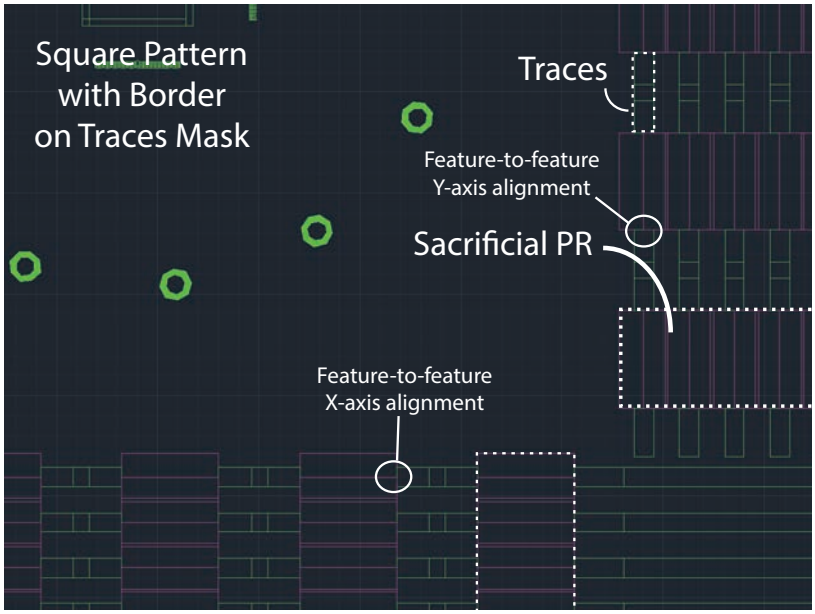


Figure 96: Feature-to-feature alignment of sacrificial PR mask to the traces.

Figure 97.

A single interposer tile is shown in Figure 98. The tile contains a 10x100 array of MFIs and 100 horizontal traces that connect to 5 MFIs on each side of the tile. As a result, for a three tile system, 40 MFIs are in a single daisy chain, and 100 such chains can be formed.

5.5 Bridge Design and Fabrication

The bridges contain the PSAS and traces that make contact with the tip of the MFIs. The trace mask also contains donut-shaped features at the PSAS sites so that the PSAS mask can be aligned accurately to the traces (Figure 99) and the vernier patterns. The dimensions of the bridge die are 0.6 cm x 2 cm.

The traces are fabricated first using a lift-off process on a blank silicon wafer with a 1 μm layer of silicon oxide; titanium, copper, and gold layers are then deposited using an e-beam evaporator. The bridge wafer is diced after the fabrication of the PSAS.

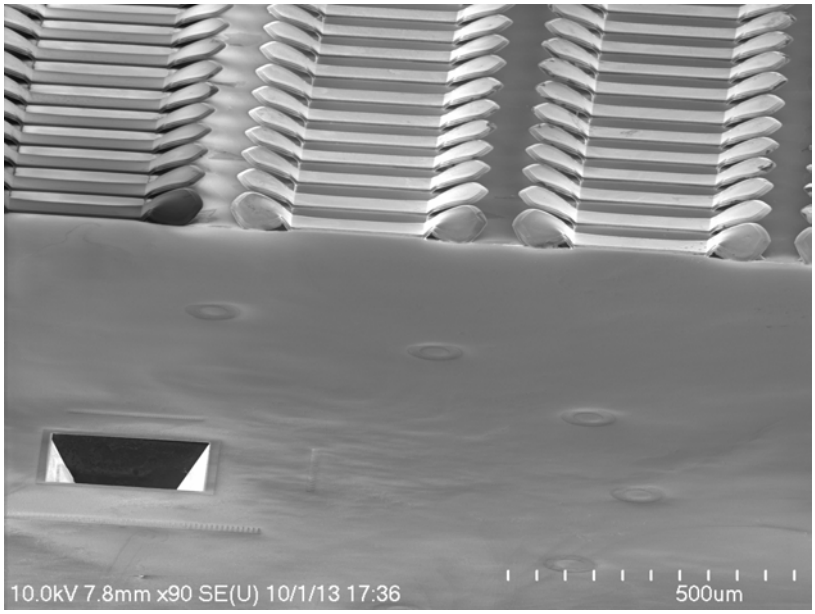


Figure 97: MFIs are fabricated on the same surface as the inverted pyramid pits.

5.6 Interposer Tiles and Silicon Bridges

The test setup is shown in Figure 100. Three interposer tiles and two silicon bridges are aligned and assembled using PSAS and inverted pyramid pits, and electrical connectivity between interposer tiles through MFIs is demonstrated. A summary of the system configuration is shown in Table 4.

5.6.1 Assembly of Interposer Tiles and Si Bridges

After the fabrication of the PSAS, pits, and MFIs, the interposer tiles are brought together and coarsely aligned to the FR4 PWB. Next, the interposer tiles are gently pushed downward and slightly moved around laterally until all PSAS and pit pairs engage and the interposer tiles become fixed. The height of the PSAS is greater than the height of the MFIs; this prevents damage to the MFIs during the assembly process when the PSAS are disengaged from the pits and are sliding across the substrate surface. The MFIs only make contact with the corresponding pads after the PSAS engage with the pits and the gap between the substrates is reduced. The silicon bridges are assembled in a similar manner.

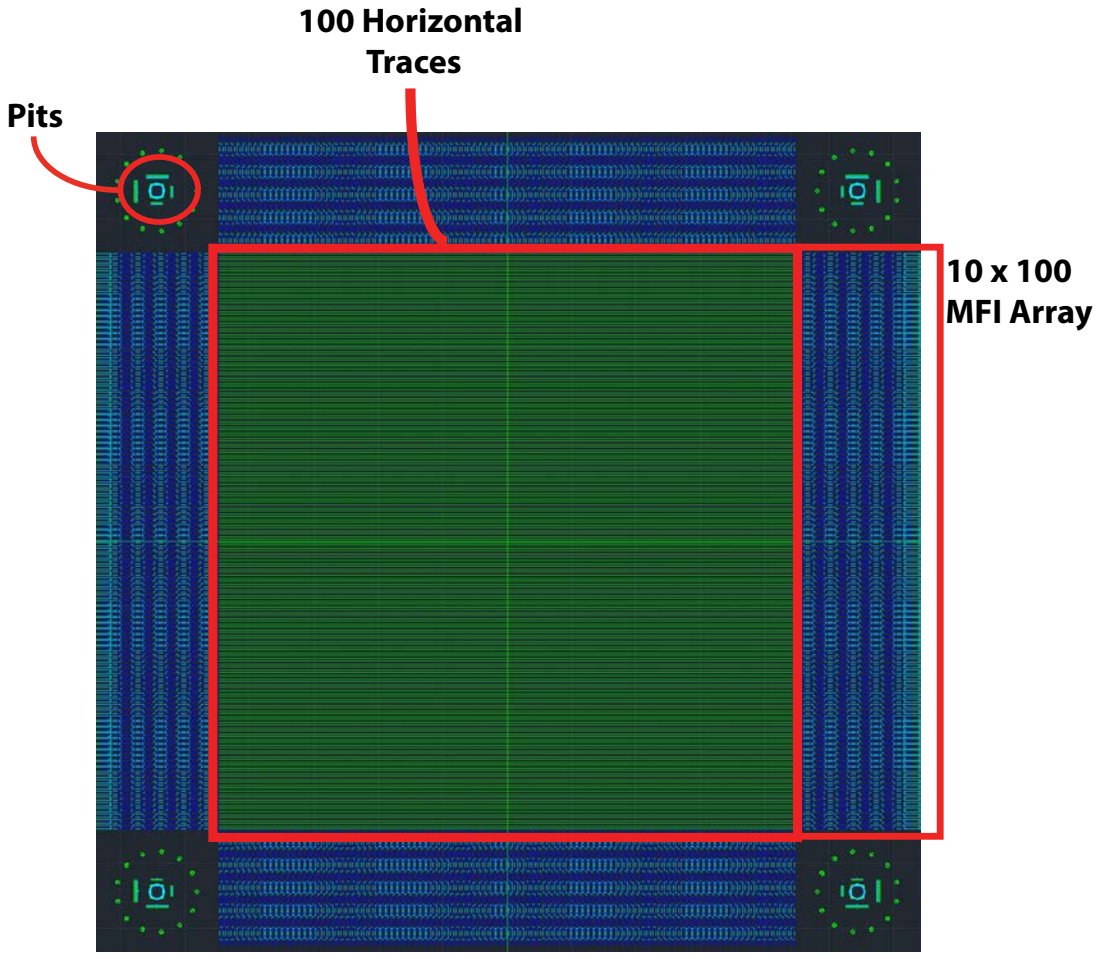


Figure 98: The mask design for the interposer tiles.

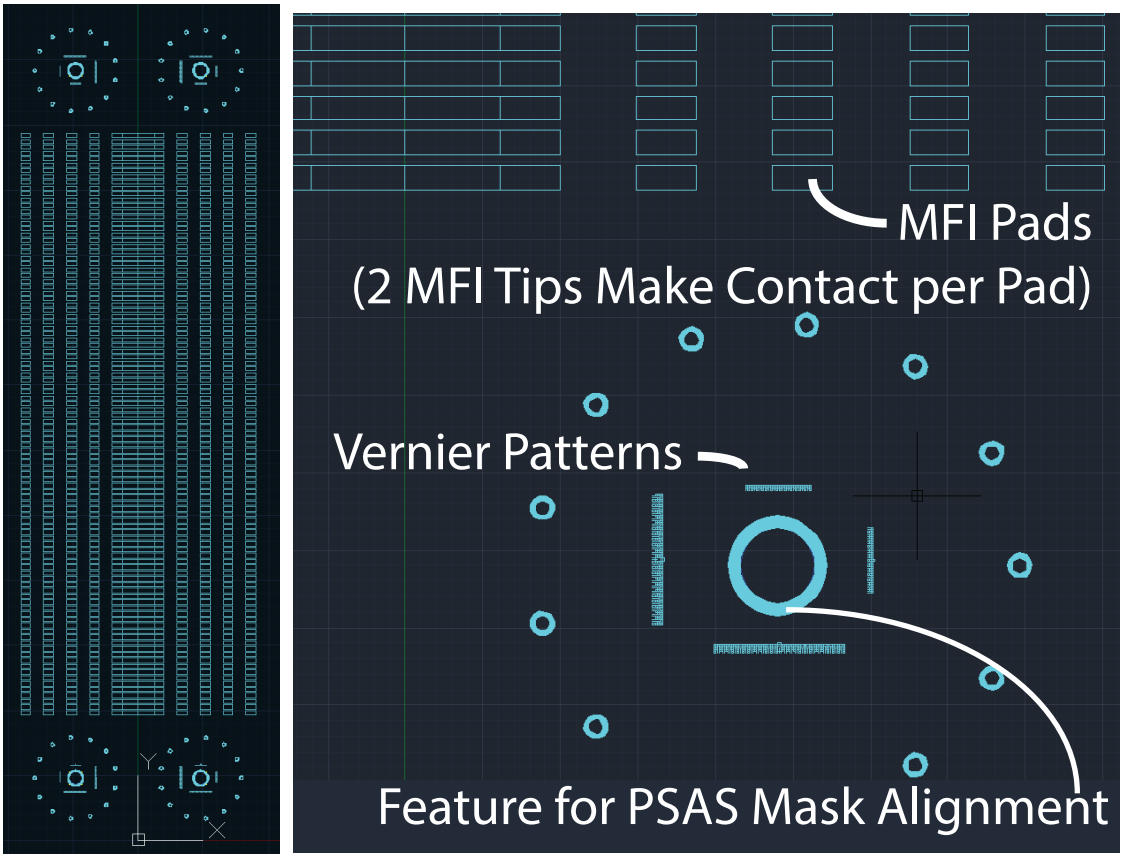


Figure 99: The bridge design is shown on the left. A magnified image of the design is shown on the right; MFI pads, the donut alignment mark (for alignment with the PSAS mask), and vernier patterns are identified.

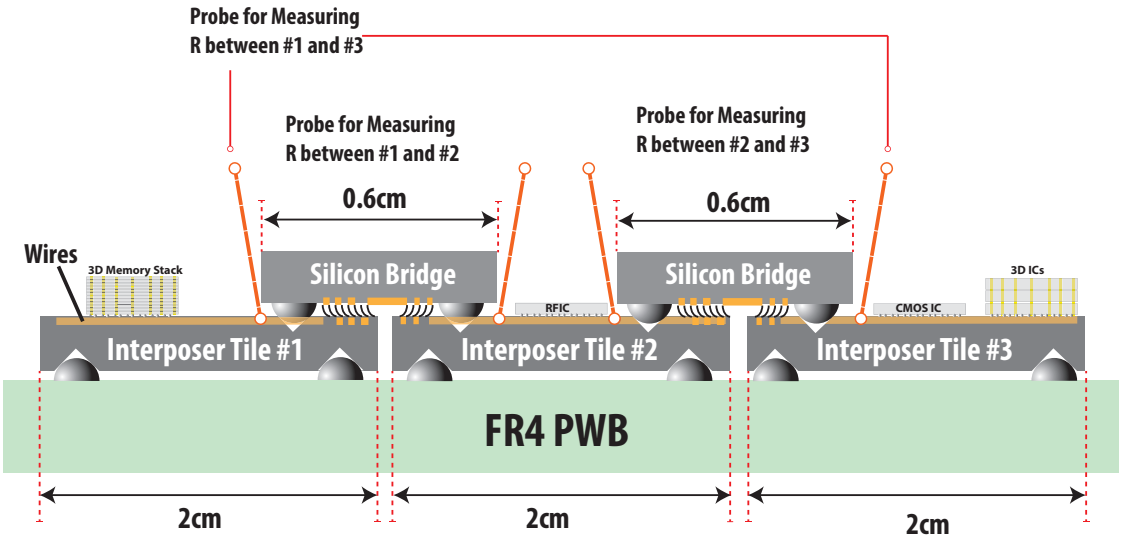


Figure 100: Multiple interposer tiles are interconnected via mechanically flexible interconnects and are aligned to the PWB and the silicon bridges using PSAS and pits. Probe locations for measuring the resistance between interposer tiles are identified in the figure.

For simplicity, an adhesive material is applied at the edges of the interposer tiles and the silicon bridges to hold the assembly. The assembled interposer tiles and silicon bridges are shown in Figure 101. The measurement of the alignment accuracy before and after the application of the adhesive material shows that the alignment is not affected.

It is worth noting that the adhesive material should be replaced with a more advanced clamping mechanism for future works. A clamping mechanism would enable precise control of the position as well as the magnitude of the clamping force to minimize tile warpage and ensure reliable operation of the MFIs. The ability to clamp and unclamp the tiles and bridges in conjunction with temporary interconnects, such as MFIs, and non-bonding alignment mechanisms, such as PSAS, would enable tiles and bridges to be replaced repeatedly. An example of the clamping mechanism is discussed in Chapter 6 and [17].

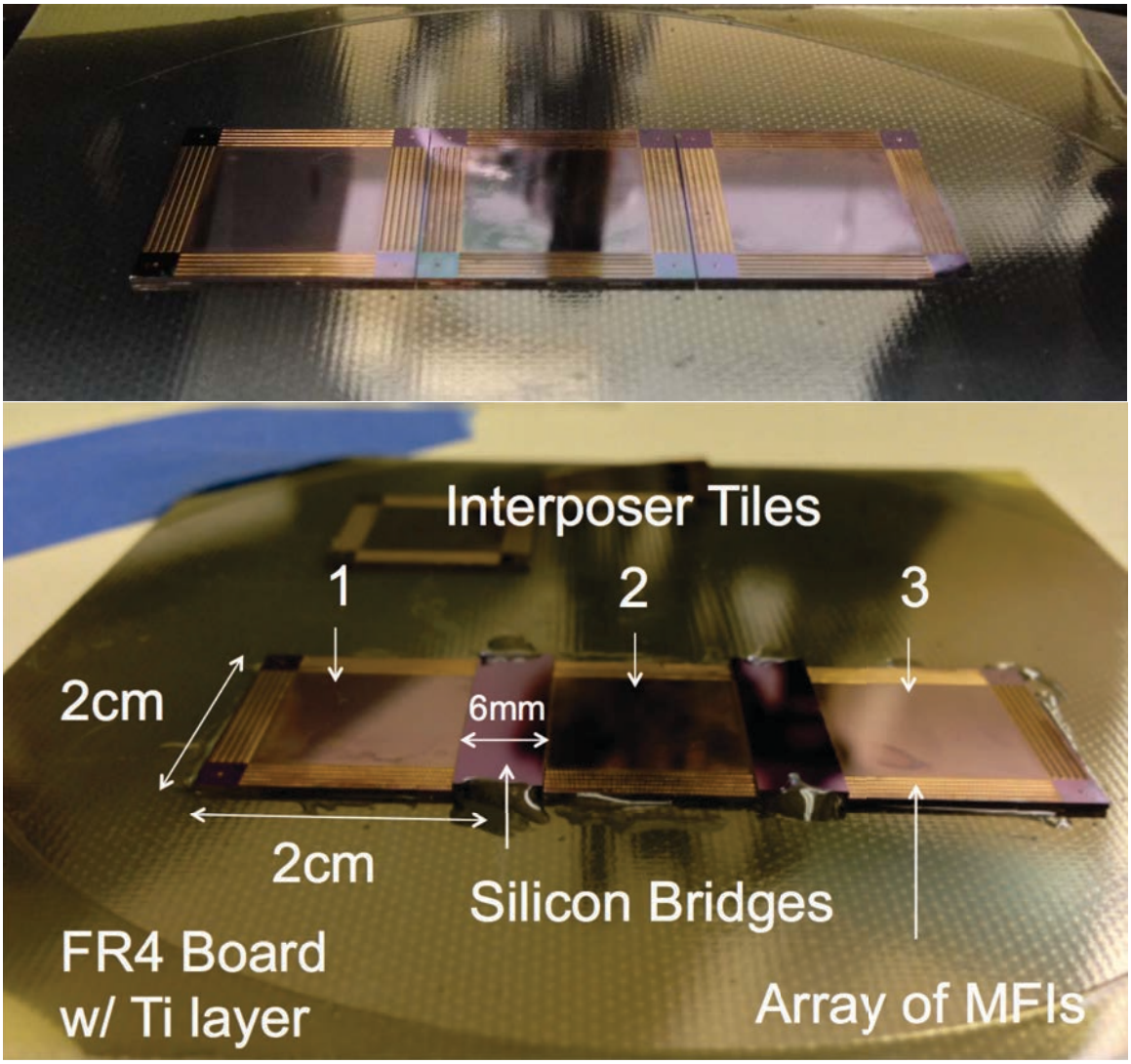


Figure 101: Image of the three interposer tiles mounted directly on FR4 and interconnected using silicon bridges and MFIs.

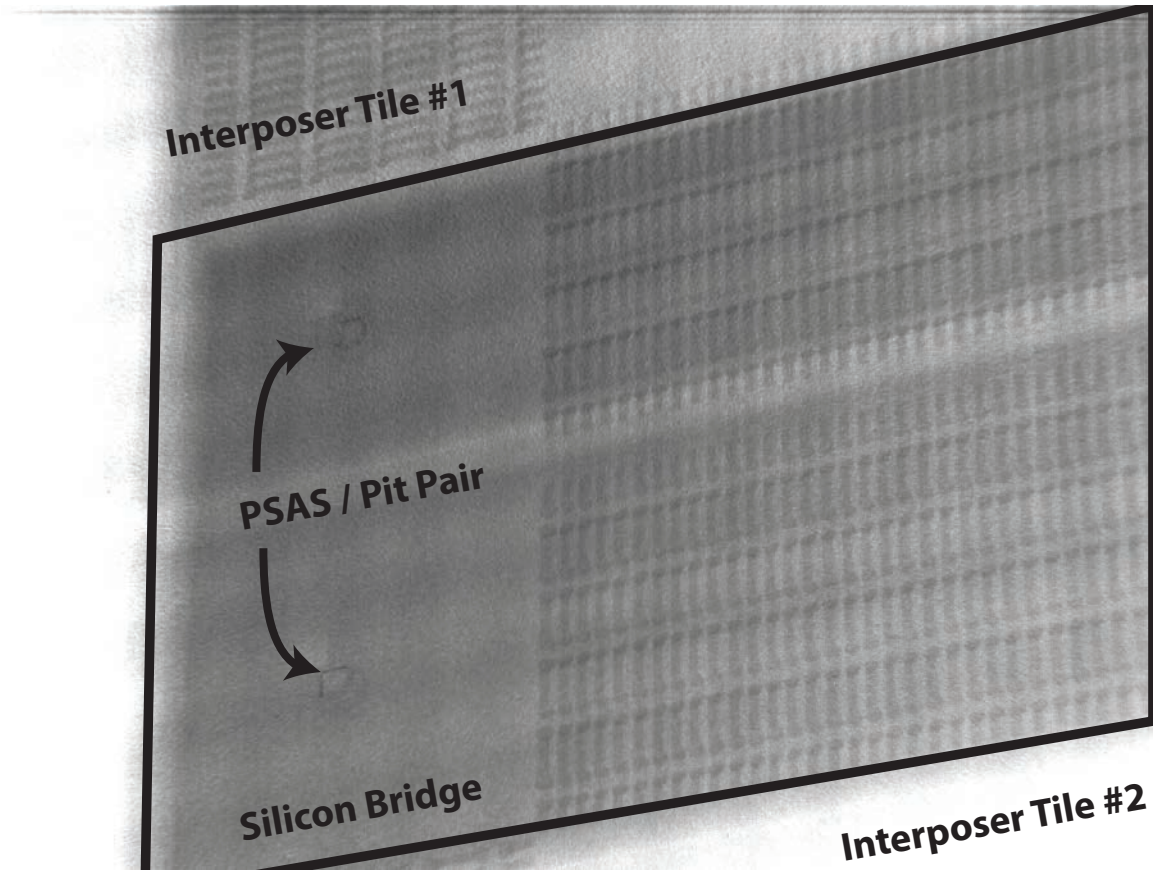


Figure 102: X-Ray image showing the two aligned Pit/PSAS pair, silicon bridge, and two interposer tiles. Array of MFIs as well as traces connecting them on both the interposer tiles and the silicon bridge are shown.

Table 4: Summary of Properties for Assembled Platform

Property	Value
Interposer Tile Area (cm^2)	4.0
No. of Interposer Tiles	3
Silicon Bridge Area(cm^2)	1.2
No. of Silicon Bridge	2
Tile/Bridge Thickness (μm)	500
Total Available Silicon Interposer Area (cm^2)	9.6

5.6.2 Alignment Accuracy Measurement

Since the silicon bridges are aligned to the interposer tiles on the assumption that the interposer tiles are aligned perfectly to the PWB, it is essential that the alignments between the PWB and interposer tiles are accurate even though nanophotonics and high-density I/Os do not exist between those two layers. The alignment accuracy is measured by observing vernier patterns fabricated on the silicon bridge and the interposer tiles via infrared microscopy. Results are summarized in Table 5.

Table 5: Misalignment between Silicon Bridge and Interposer Tiles

Regions	Silicon Bridge 1		Silicon Bridge 2	
	Horizontal (μm)	Vertical	Horizontal (μm)	Vertical
Bottom Left	-4.0	+4.6	-5.2	-5.0
Bottom Right	-5.4	-4.8	-5.0	-5.0
Top Right	+5.8	+3.2	-5.8	-5.2
Top Left	+6.0	-5.0	-7.6	-5.0

5.6.3 Electrical Measurements

Electrical resistance is measured between interposer tiles to verify electrical connectivity. Figure 100 shows the locations of the probes for measuring resistance. Table 6 summarizes the results. Expected values are calculated by taking into account the resistance of the MFIs measured using a four point electrical measurement as well as the gold-coated wire traces fabricated on the interposer tiles and silicon bridges. The

data shows that the resistance is within two standard deviations of the expected resistance. The major source of variation is the wire traces which are electroless plated; noticeable thickness variation is introduced after this process.

Table 6: Resistance Between Interposer Tiles

	Resistance between interposer tiles		
	1 and 2	2 and 3	1 and 3
Average (Ω)	1.51	1.60	4.98
Expected Value (Ω)	1.32	1.32	4.36
Standard Deviation (Ω)	0.138	0.140	0.363
No. of Samples	20	20	20
No. of MFIs in Chain	20	20	40

5.7 Conclusion

A novel large-scale silicon system platform with $9.6cm^2$ of active silicon area is demonstrated. The platform contains three interposer tiles and two silicon bridges, and an accurate alignment ($<8\ \mu m$) between silicon bridges and interposer tiles is achieved. The accurate alignment makes it possible to accommodate nanophotonics to enable a high bandwidth and low-energy system in the future. In addition, mechanically flexible interconnects and silicon bridges are used to provide electrical connections between interposer tiles without having to use motherboard-level interconnects.

CHAPTER 6

ELASTOMERIC BUMP INTERPOSER FOR PSAS PACKAGING

6.1 Introduction

A critical requirement for PSAS-enabled systems is a vertical compression force to "clamp" the multiple layers of substrates including an FR4, interposer tiles, and bridges. The compression force maintains the alignment by keeping the PSAS and pits engaged; it is determined that 1 lbf to 2 lbf is required to withstand the vibrations that exist in data centers and rack mounted server housings.

The distribution of the pressure on the substrates is also critical to control; specifically, the pressure must be symmetrically distributed around PSAS/pit sites. An asymmetric distribution may cause the substrates to warp, which can affect the reliability and the performance of the system. Reliability is affected because the substrates can be damaged physically, while performance is affected because the warpage may affect the coupling efficiency between layers and the device characteristics on warped substrates.

This chapter describes a component designed to address the challenges associated with applying an accurate amount of force with an accurate distribution of pressure. Elastomeric bump interposers are packaging components that can be placed between a clamping mechanism and a substrate aligned with a PSAS. A thick tungsten layer and precisely designed and placed PDMS domes deliver precise amounts of force at predetermined locations to minimize warpage. This research activity was done as part of an internship at Oracle and is published in [17].

6.2 Background

As integrated-circuit (IC) technology continues to scale to smaller critical dimensions, it is increasingly difficult for existing interconnection technologies to keep up with communication requirements such as high bandwidth, low power, reliability and low cost. Chip stacking in multi-chip modules (MCMs) is being investigated to address these challenges, and to enable future high-density, high-performance systems.

However, because MCMs by definition include multiple chips, it is all the more important to solve the so-called known-good die (KGD), problem. In particular, manufacturing yields can be improved and cost can be reduced by ensuring that only good semiconductor dies are included in an MCM. This can be achieved by increasing the amount of testing at the die level; because of cost and test-time limitations, this additional testing typically needs to be performed at the speed of the ICs at the wafer-level, which can be challenging.

Alternatively, an MCM can be assembled in a remateable fashion using Proximity Communication (PxC) signaling technology [71]; PxC is a type of coupled-data interconnect that allows one to wirelessly interconnect multiple chips into MCMs to form a single logical chip. Its wireless nature is a key feature as it allows for rework, allowing one to identify KGD and if necessary, replace non-functional die.

However, in order to achieve high-speed inter-chip signaling with PxC interconnects, accurate relative alignment of components in a multi-chip package using Proximity Communication (PxC) I/Os, capacitive [72] or optical [7], is absolutely critical. This is because the alignment accuracy correlates strongly with the coupling efficiency; for optimal performance, these chips assembled in a face-to-face configuration, must be aligned accurately in all six degrees-of-freedom and with a minimal separation between them. Typically, lateral misalignments of better than 8m and l m are desirable for capacitive and optical proximity interconnects, respectively.

One method for achieving these stringent alignment requirements is by using Ball-in-Pit self-alignment structures [73]. This technique requires inverse pyramidal pits to be fabricated at designated locations on the Si ICs that are to be aligned; a precision sapphire ball is then sandwiched within the two pits. By conforming the pyramidal pit etch process, a common Si anisotropic wet etch process in MEMS fabrication, to CMOS foundry standards, and using accurately sized sapphire balls, submicron alignment between ICs has been previously demonstrated [74].

In the simplest PxC package, two chips (islands), attached to a substrate, may be interconnected via a third chip (bridge) that attaches face-to-face with the islands (Figure 103). This bridge chip can be powered directly by the islands or independently with wire bonds but communicates off-chip solely via PxC. In order to keep chips engaged and aligned using Ball-in-Pit technology, an external clamping force must be applied between the chips. The island chips are assembled to the package substrate using standard C4 bumps and require freedom-of-movement in all directions during the flip-chip bonding process. Once the islands are attached via reflow soldering, they provide a reference mechanical plane against which the clamping force can be applied. The bridge chip is placed face-up on the substrate and has some face-to-face overlap with the island chips, where the PxC interconnects and ball-in-pit structures are situated. When assembled, this bridge chip must push up against the island chips for the ball-in-pit structures to engage and remain aligned.

For a PxC package described above, what one needs is a packaging mechanism that allows the bridge chip to be disengaged from the islands during industry standard reflow processes, but post-reflow returns the bridge chip to the correct position. In addition, it would keep the chips aligned by applying the needed force to the back of the ball-pit sites.

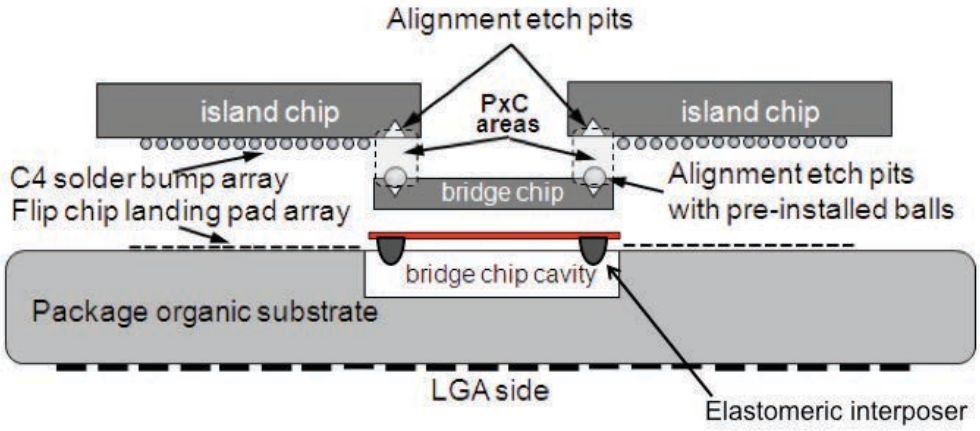


Figure 103: Three-chip MCM package with elastomeric bump interposer.

6.3 Package Assembly

Previous work approached this through the use of underfill and vacuum tools [75]; the bridge chip is placed at the bottom of the substrate cavity during the island chips solder reflow process with the ball-and-pit disengaged. Then, using a vacuum tool, the chip is raised and underfill material is used to fill the bottom of the chip that is keeping the ball-and-pit sites securely engaged. Though this method showed that chips may be aligned to 8 μm lateral accuracy, it is difficult to precisely engineer the force distribution on the bottom of the bridge chip. Rework may also be difficult since removing the underfill material is not a trivial task. In this work, we introduce an alternative method of assembly using a mechanical interposer containing elastomeric structures whose shapes and locations can be precisely engineered. As a result, by placing this interposer inside the package cavity, it is now possible to control the amount of force applied to the bridge chip as well as the distribution of force. Moreover, this method eliminates the need for vacuum tools and allows for simple pick-and-place type assembly chips. Additionally, with the right fixturing, multiple bridge chips in a large-array multi-chip package could be aligned and locked in place simultaneously. The proposed assembly process using the elastomeric bump

interposer is shown in Figure 104.

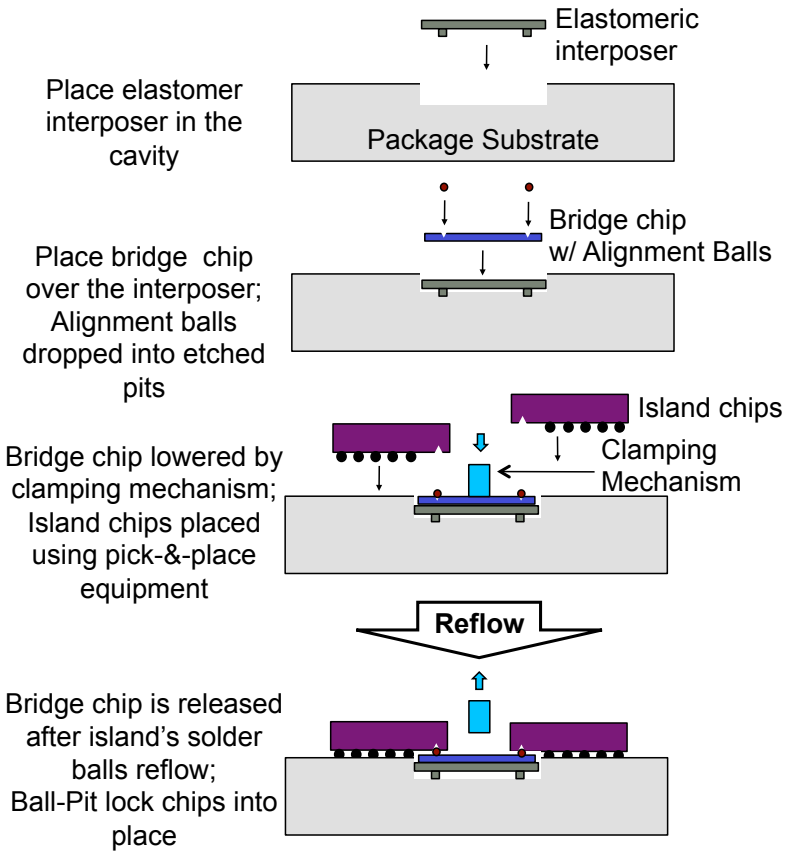


Figure 104: MCM Assembly Process using an elastomeric bump interposer.

For pushing down the chip during the reflow process, a fixture (Figure 105) can be used. It consists of an arm with a narrow center section, which is designed to fit between two island chips, on top of the exposed center section of the face- up bridge chip. The tool presses on the exposed bridge chip to lower it while the island chips are reflowed.

This tool can be extended to push down multiple bridge chips at once in the case of a system with multiple bridge chips. This can increase assembly throughput significantly as it allows simultaneous assembly of every chip in the system, regardless of size.

The interposer designed and fabricated in this work consists of an array of elastomeric structures on a thin, but stiff substrate. The design targets for this interposer

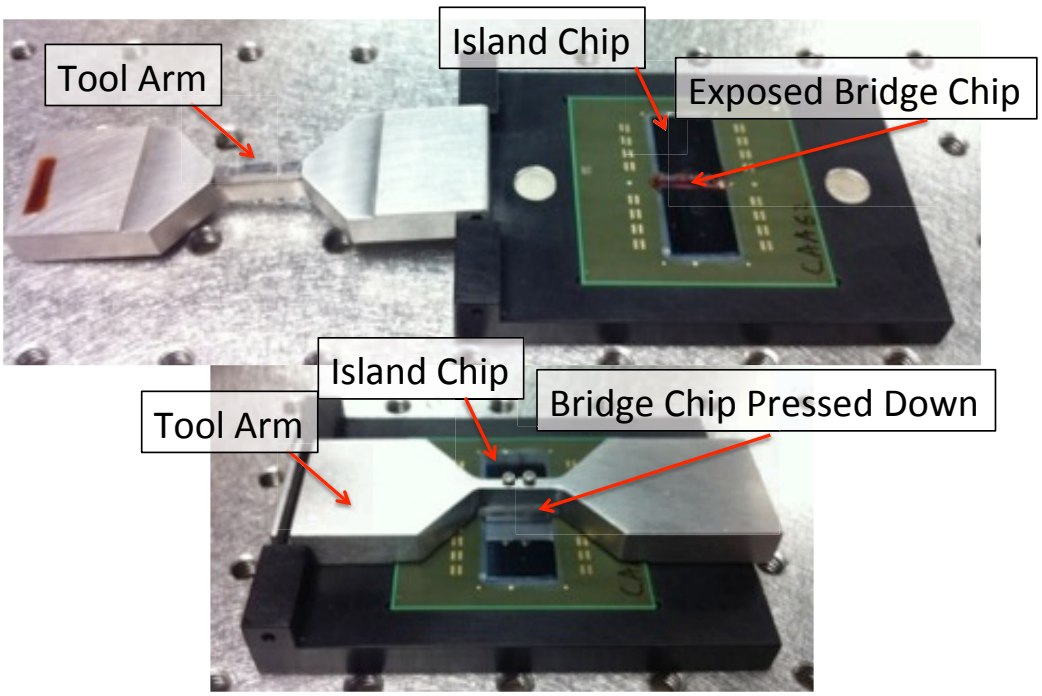


Figure 105: Tool/Fixture for pushing down the bridge chip.

include the ability to provide as much as 1 lbf per ball-pit site in the engaged mode and to be compressed sufficiently to disengage from the island chips sufficiently (by applying greater than 1 lbf/site) to allow them to move freely during the solder reflow process. The interposer also requires an ultrathin form factor to fit into the package cavity, which is 300 μm deep. Considering that the solder ball diameter on the island chips used in this work is 80 μm, one can safely assume that the maximum lateral freedom of movement required for the solder ball self-alignment is half of the solder ball diameter, 40 μm. Using simple trigonometry, we can determine that the ball-pit sites need to be lowered by 25 μm from the engaged state in order to allow for such lateral movement (Figure 106). FEA using ANSYS was performed to determine exactly how much force is required to compress the interposers by 25 μm, as well as to determine the shape of the elastomer needed. The elastomer was modeled as an Ogden hyper-elastic material [76].

Unfortunately, finding the amount of force required to do this is not trivial due

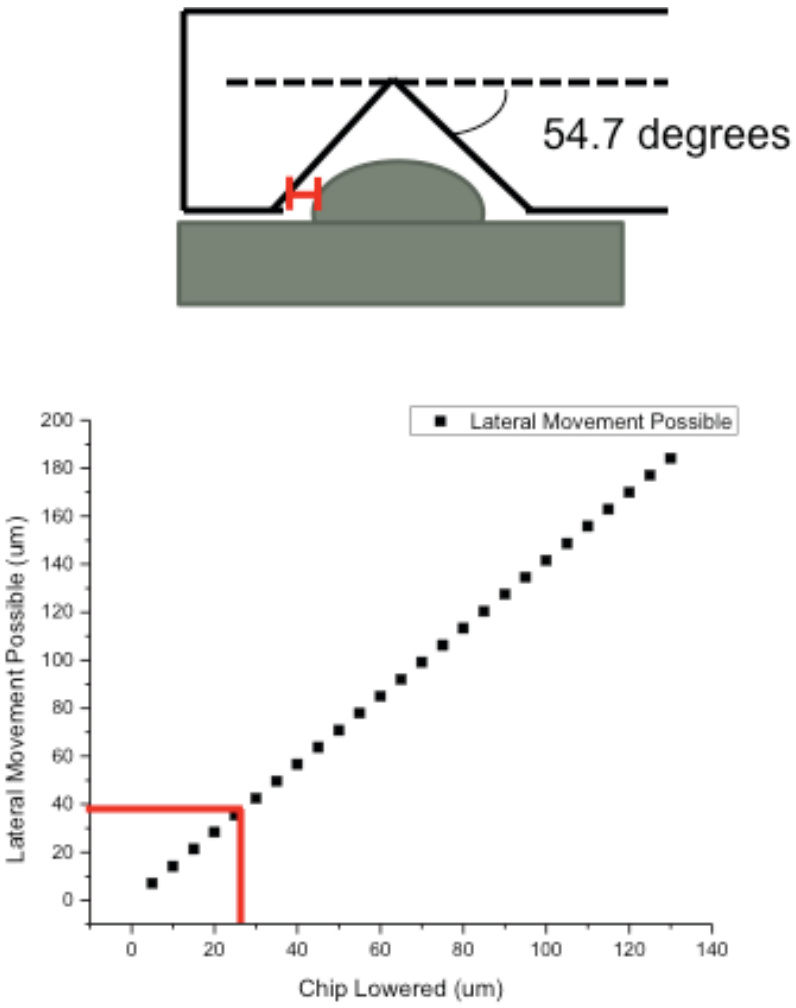


Figure 106: Ball-pit sites must be lowered 25 μm to allow for the lateral movement required in solder ball self alignment. This is due to the 54.7 degrees angled pits etched in the Si substrate.

to the location in which the downward force is applied (the center of the bridge chip) that produces warpage of the bridge chip. At first, an interposer made entirely out of elastomeric materials was examined, however, as shown in Figure 107, warpage of the bridge chip, as measured by the vertical height difference between the ball-pit site and the center of the chip ("Edge2Center"), can exceed the depth of the cavity and cause the bridge to bottom out before the ball-pit sites can be successfully disengaged. In fact, what was determined during the first design iteration is that the interposer must also act as a stiffening layer to reduce warpage, and eliminate the bottoming-out effect.

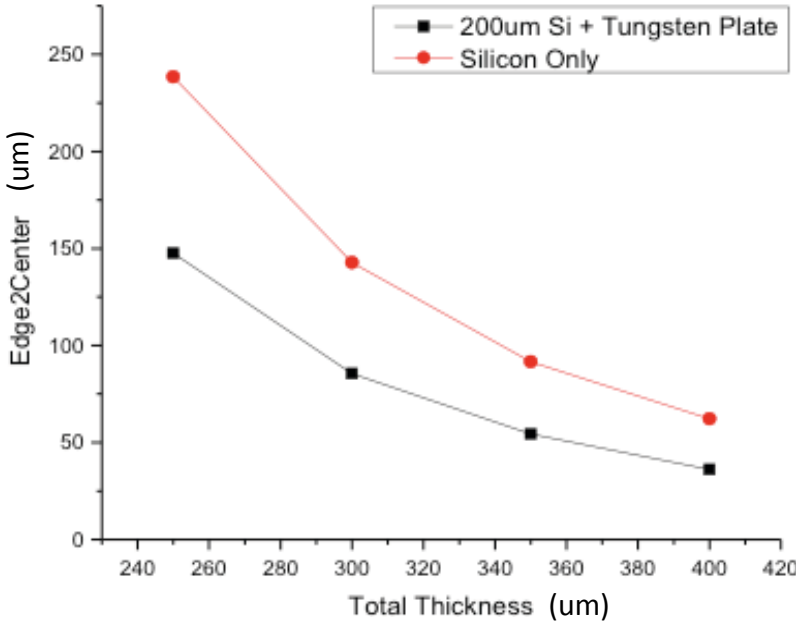


Figure 107: Edge2Center (warpage) vs. total thickness of the chip + stiffener stack.

With a stiffening layer (tungsten in this work), the warpage is significantly reduced. A stiffening layer also provides additional benefits; by fabricating elastomers directly to it, we can precisely position the elastomers and ensure that the elastomer bumps are right under the ball-pit sites. It also makes it easy to place the elastomers inside the package substrate; without the tungsten layer, one would have to position each individual elastomer inside the package substrate.

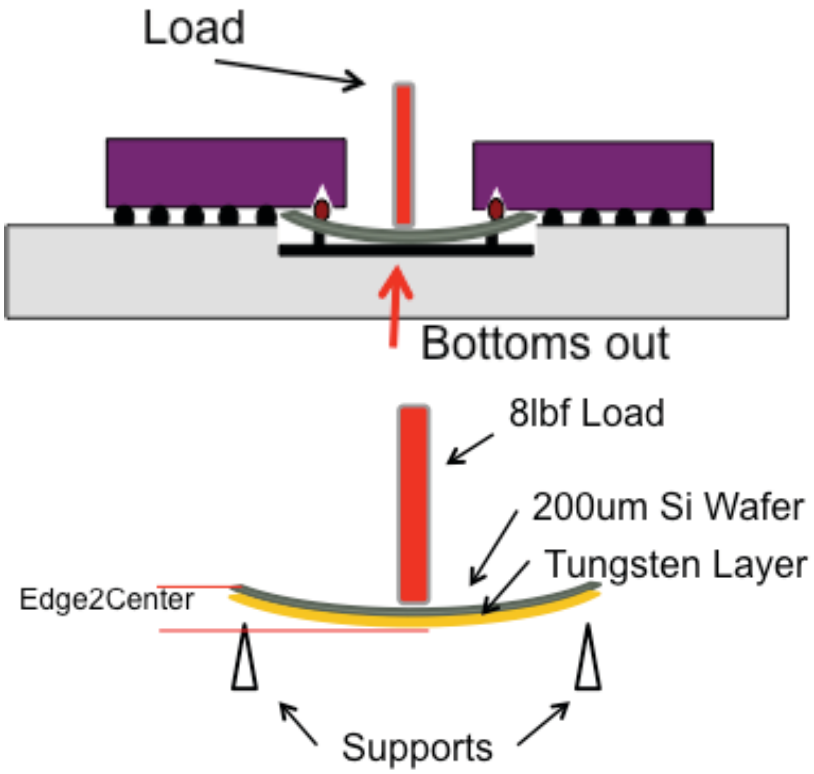


Figure 108: The bridge chip is warped as the tool pushes it down to disengage the ball-and-pit sites. Too much warpage can cause the chip to bottom out before successful disengagement.

Even the stiffening layer, however, was not enough to prevent bottoming out of the bridge due to warpage, so another method was devised. One can further reduce the warpage of the bridge chip without reduction in the reaction force by using multiple smaller elastomer bumps instead of a single large structure. In Figure 109, the warpage vs. force of two different elastomer bump distributions is compared. One has a single large dome and other has four smaller bumps symmetrically distributed around the ball-pit sites. The result shows a significant reduction in warpage at identical levels of reaction force. The main reason for this is the fact that elastomers are placed closer to the center of the chip, effectively shortening the distances between support structures.

Using the four elastomer bump configuration as well as the tungsten stiffening layer, optimal bump dimensions were found. In the designed elastomeric bump interposer, 1 lbf is applied at each ball-pit site in the engaged state while 3 lbf is required per site to lower the bridge by 25 μm and disengage it sufficiently from the islands during reflow. At the 3 lbf/sites, a 70 μm gap exists between the bridge chips and the bottoms of cavities, meaning that the bottoming-out effect does not occur.

It is worth noting that for this work where ball-in-pit is used for alignment between island chips and a bridge chip, it is vital that the force applied to the ball-pit sites be symmetrically distributed. Asymmetric force distribution will result in chip warpage.

6.4 Fabrication

6.4.1 Overview

For the interposer, a fabrication process was developed with cost control being an important consideration. Specifically, a stamping process is developed that lends itself to batch processing not only at the wafer level but also at the panel level. In addition, the stamping mold is reusable and was demonstrated to stamp out several elastomeric bump interposers. The fabrication process can be divided into three

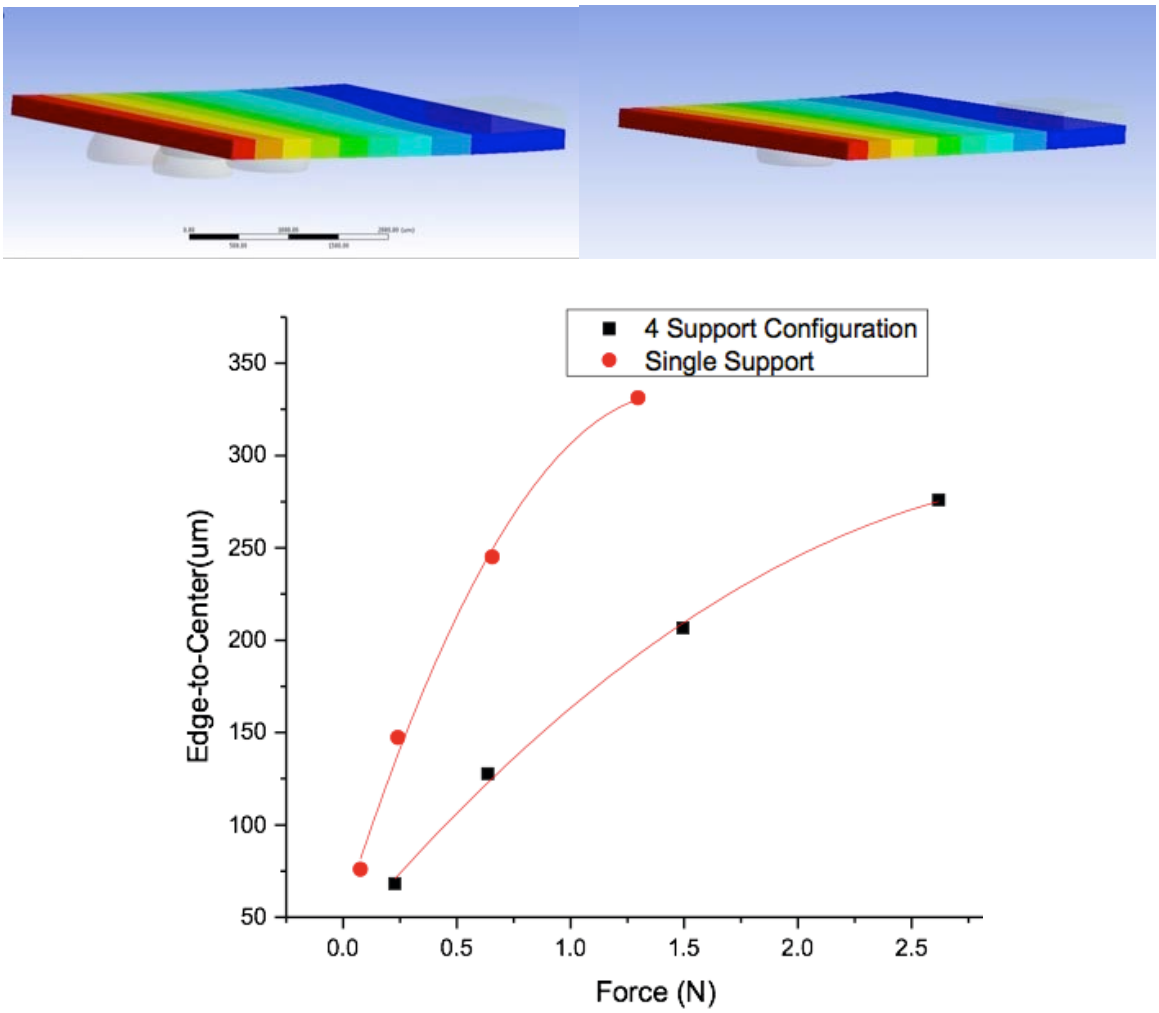


Figure 109: Using four smaller elastomer bumps instead of one larger one can reduce the warpage of the chip at the same level of reaction force.

major steps.

1. Positive dome fabrication using photoresist reflow
2. Negative dome SU-8 mold fabrication
3. Positive silicone dome stamping using the SU-8 mold

6.4.2 Dome Fabrication

Dome fabrication is the step where the shape of the final elastomer is determined, as negative and positive copies of it are made in subsequent steps. Although a truncated sphere shape is used for our application, there are various other shapes that can be used and have been considered. For example, a cylindrical pillar is an example of a different shape that can be used.

The shape of a truncated sphere, however, has many advantages in the fabrication and the operation of the package compared to other shapes. First, the dome does not have sharp edges that can be damaged when trying to separate the newly formed mold. Second, its smaller surface area makes it easier to separate the mold from it without the structure detaching and getting stuck in the mold. Third, its dome shape allows a higher vertical range-of-movement for the same target load force. Fourth, the dome shape eliminates the possibility of buckling.

The truncated sphere is fabricated by reflowing a photoresist structure. This technique is commonly used for creating micro-lens structures; however, in this application, the size and volume of the photoresist that needs to be reflowed is significantly larger than what is typically used in a micro-lens process making it more complex.

The main challenge is in reflowing large structures due to the fact that most photoresists have a limited time in which they can remain in a glassy state. The glass transition temperature is continually increasing as it is being reflowed, and eventually it is raised beyond the decomposition temperature or beyond the maximum allowable

process temperature. As a result, the available time in the glassy state for a particular photoresist may not be sufficient to completely reflow a structure as wide and tall as the elastomeric dome needed per the design (180 μm). Both the photoresist and reflow process have to be carefully chosen to ensure that the photoresist is reflowed completely and consistently. In order to preserve the patterning accuracy of the domes, the reflow technique introduced in the previous section and in [77] are used. The resulting dome structures are 180 μm tall and are shown in Figure 110.

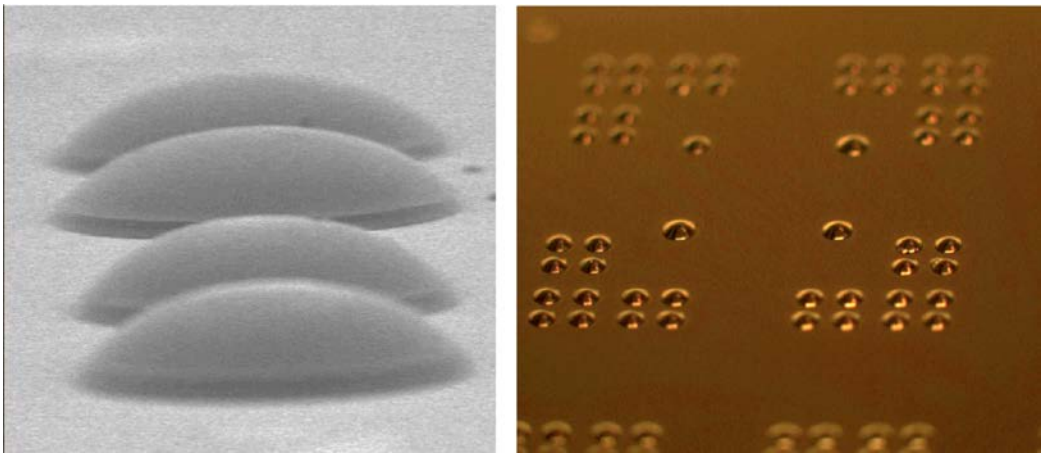


Figure 110: Reflowed photoresist to form truncated sphere structures that are 180 μm tall.

6.4.3 Mold Fabrication

The next step in the fabrication process is to create a negative mold of the reflowed structure using SU-8. However, SU-8's excellent adhesion to the photoresist structures, it is necessary to place an intermediary material in between so that the negative SU-8 mold can be detached from the positive structure without damage. Unfortunately, SU-8 also has excellent adhesion to many compatible intermediary materials that were considered. The solution is to use a sacrificial layer; rather than looking for materials with poor adhesion to SU-8, a material that can later be softened and removed was employed.

There are three layers involved in making this sacrificial process work. In addition

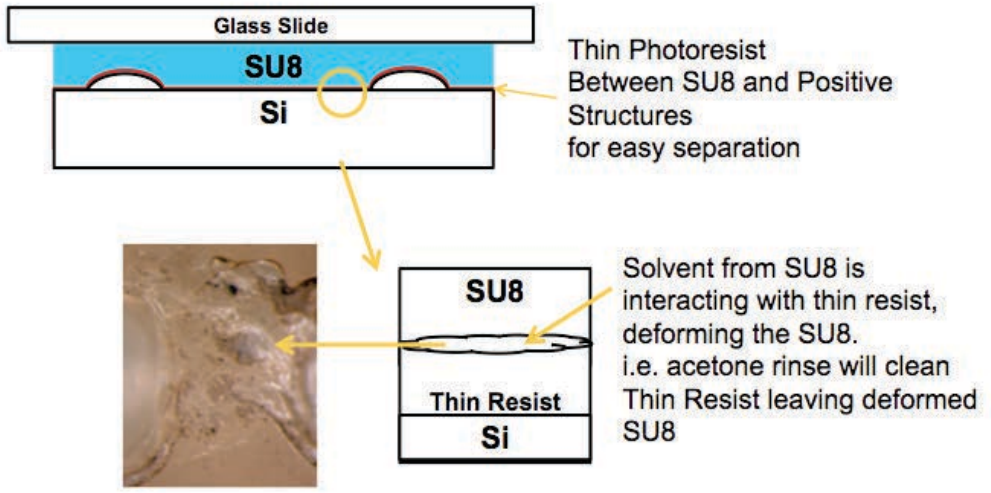


Figure 111: Metal layers used to prevent SU-8 interaction with the sacrificial layer.

to the sacrificial material, two metal layers are used to prevent interaction between the sacrificial material, the reflowed photoresist and the SU-8, as shown in Figure 111. The first metal layer is sputtered on top of the reflowed photoresist structures and the sacrificial material (a thin photoresist layer) is spin coated above it. The sacrificial resist is then flood exposed and baked before the second layer of metal is sputtered on top.

For this application, the sacrificial material used is a negative resist. However, any material that is easily removed and softens or even decomposes when heated above 100 °C is adequate for this application. The material must not be affected at temperatures below 100 °C (the SU-8 PEB temperature)

Once the sacrificial layer and two metal layers are deposited, SU-8 is poured over the positive dome structure and a glass substrate is placed over the SU-8. Then, the SU-8 is cross linked by exposing it in a flood UV light through the glass slide and placing it in the oven (90 °C) post-exposure bake.

Once the SU-8 mold is fully crosslinked, it can be separated by placing for a few seconds on the hot plate, which has been heated to 150 °C; the sacrificial layer will

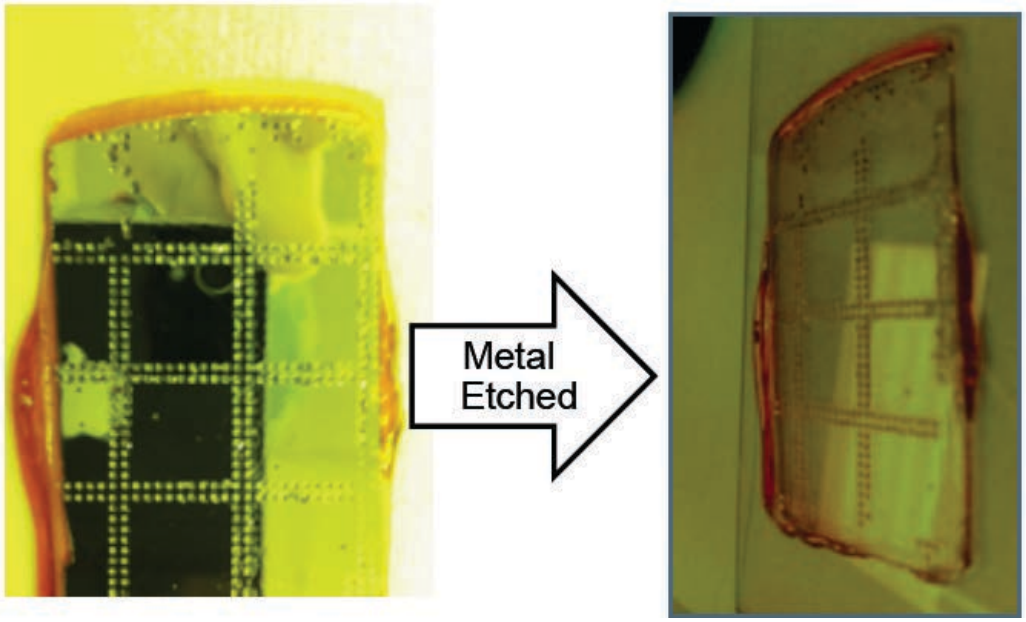


Figure 112: Negative SU-8 mold after the separation; the mold has a metal layer that can be removed using a wet etch process.

soften, and it becomes easy to separate the mold. Any remaining sacrificial photoresist on both sides can be easily removed using solvents. The SU-8 mold is then placed in wet etchants to remove the metals, leaving behind only the SU-8 negative mold. An image of the resulting SU-8 mold is shown in Figure 113.

6.4.4 Silicone Stamping

Once the mold is created, a silicone material is poured over the mold and a tungsten foil plate is placed on top. While the negative features in the SU-8 drive the shape of the bumps, the pressure applied on the tungsten during the stamping process determines the thickness of the elastomer film in the "field". It is vital that the force applied during this process be uniform. The resulting film thickness is targeted to be 10-30 μm thick. In this work, precision weights are used. With the pressure still applied, the whole stack, including the weight, is placed in an oven to cure. Once cured and cooled to room temperature, one can separate the tungsten plate with elastomer structures quite easily from the SU-8 mold.

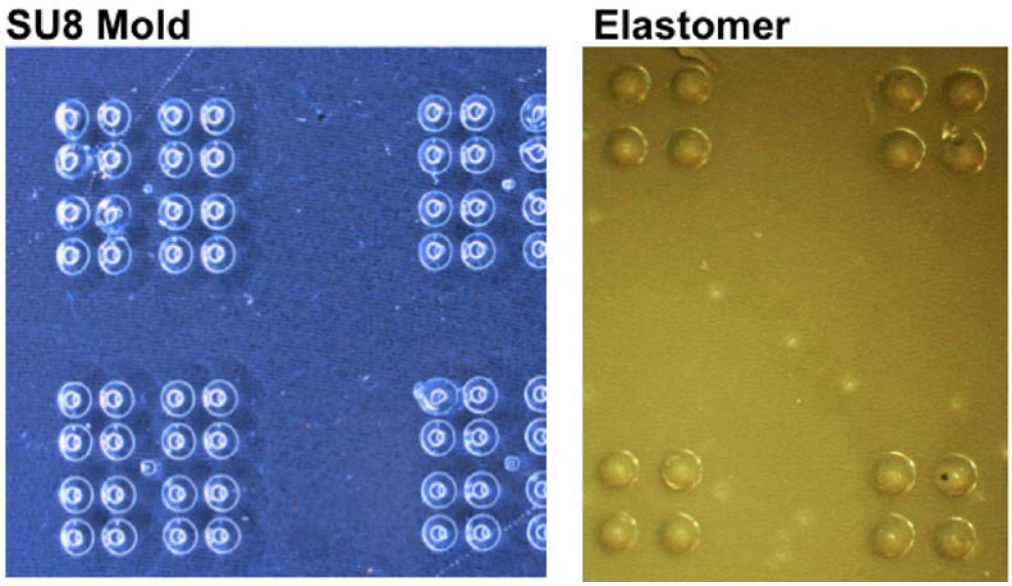


Figure 113: On the left is an optical microscope image of the SU-8 mold and on the right is an optical microscope image of the resulting stamped elastomer structure.

Finally, the tungsten film with elastomer domes are cut into package-cavity sized pieces. Dicing is the method of choice for cutting the interposer since other methods, including shearing, resulted in warpage and splitting of the tungsten plate.

6.5 Mechanical Characterization

To ensure that the elastomer dome structures perform as designed, mechanical characterization was performed. A uniaxial compression tool from MTS is used to determine the compliance of the elastomer structure. This instrument is able to measure vertical deflection to a resolution of one-tenth of a micron. Figure 115 shows the result of the uniaxial compression test performed on four elastomer domes (one ball-pit site), compared to the simulation results. When the interposer is compressed by $\sim 60\ \mu m$, 1 lbf of reaction force is measured.

To make sure that the interposer structure does not change its properties during the high temperature reflow process, the interposer was subjected to the reflow condition, and its compliance measured again. The results are also shown in Figure 115;

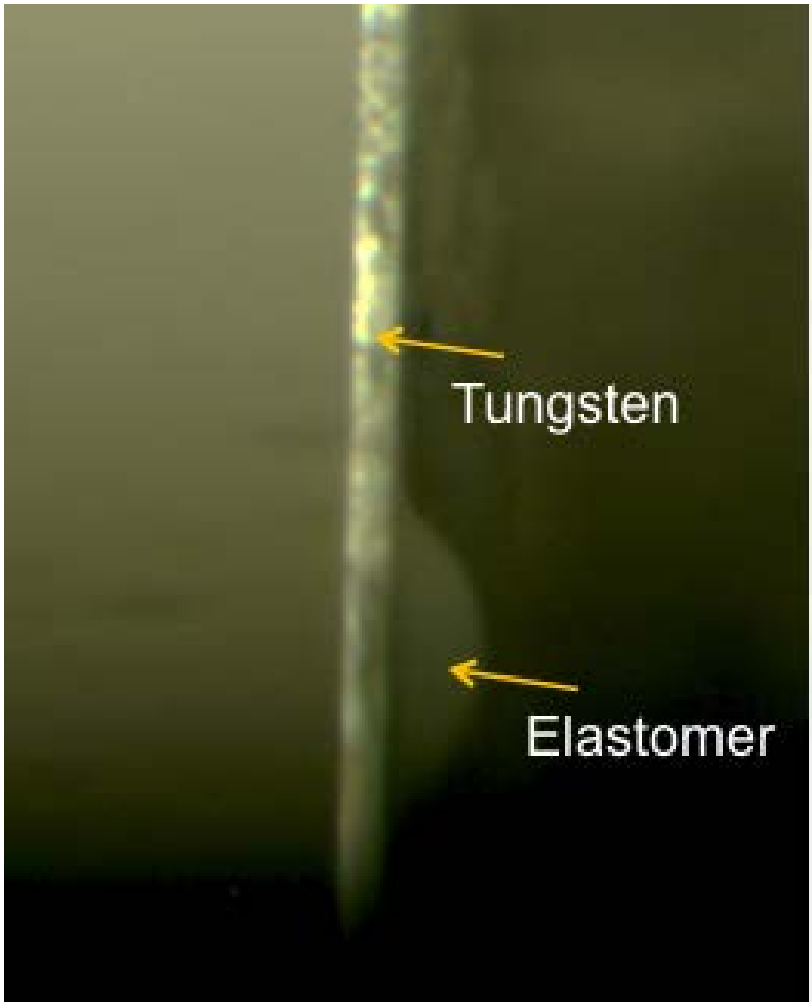


Figure 114: Cross section image showing the silicone dome as well as the tungsten layer.

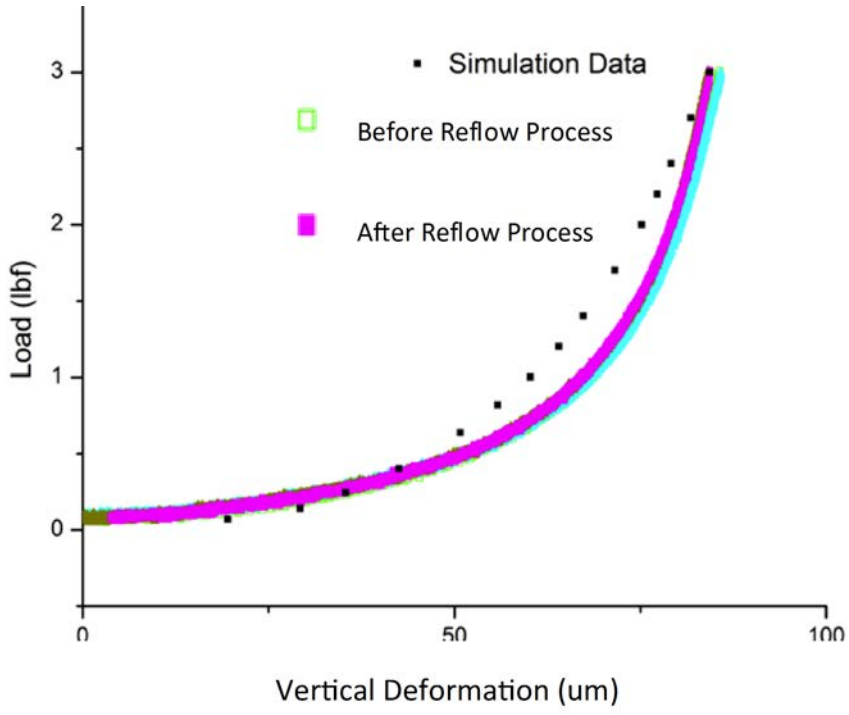


Figure 115: Uniaxial compression measurement compared to the simulation results.

the mechanical characteristics of the interposer do not significantly change after the reflow process.

6.6 Conclusion

A low-cost interposer with elastomeric structures was designed and fabricated for use in batch assembly and alignment of proximity communication enabled multi-chip packages. These interposers are carefully designed to minimize the warpage of the bridge chip during the assembly process by using multiple elastomeric bumps, and also by using stiffening Tungsten layers. At the same time the interposer also provides adequate force to keep the Ball-in-Pit reliably secured. Future work in this project will involve tests at the package level including verification that good alignment can be achieved, enabling high efficiency PxC.

CHAPTER 7

SACRIFICIAL PSAS FOR FLIP-CHIP BOND ASSEMBLY

7.1 Introduction

In Chapter 5, the PSAS' compatibility with rematable MFIs is demonstrated; it is shown that a low resistance contact can be formed using MFIs that have been aligned using PSAS. In this chapter, the PSAS' compatibility with a non-flexible interconnect is described. Permanent interconnects pose a a greater challenge for PSAS compared to MFIs because the bonding process involves thermo-compression. The bonding technology also often requires an underfill, and the PSAS needs to be removed to prevent interaction between the underfill and the photoresist-based PSAS material.

The PSAS' compatibility with the thermo-compression bonding is important because this compatibility allows for a wider range of system configurations involving interposer tiles and bridges. For example, in the multi-chip package configuration described in Chapter 6 and Figure 103, the island chips are bonded with solder balls using a thermo-compression bonding process. The techniques described in this chapter can eliminate the need for placement tools entirely even in such configurations.

There are also situations where flexible interconnects may not be appropriate. For example, mobile applications in which the system experiences frequent shock and movements may cause flexible interconnects to become disconnected from pads. The work in this chapter aims to increase the range of applications and system configurations that are possible with PSAS.

7.2 Flip-chip Bonding

Flip-chip bonding is a high-performance assembly technique that enables area-array interconnections between a chip and a substrate. The technique typically involves an array of solder balls and a matching array of pads, and it also requires a flipchip bonder to align, apply heat, and provide compression for bonding.

In this chapter, a novel enhancement of the flip-chip assembly technique is presented through the use of two novel structures: sacrificial positive self-alignment structures (PSAS) and inverted pyramid pits ("pits"); using this technique, an array of solder balls can be manually aligned and bonded without using an expensive, large placement tool. An overview of the process is shown in Figure 116. Features of the technique include:

1. Cost of assembly is reduced as the need for an accurate flip-chip bonder and additional tools are eliminated.

2. Assembly throughput can be increased because applications requiring high-accuracy alignment can be performed with high-speed but low-accuracy placement tools.

3. Ability to correct large initial misalignments enables the end user to perform the assembly with minimal packaging capability.

7.3 Background

7.3.1 Flip-chip Bonding

In a typical flip-chip assembly process, a flip-chip bonder tool picks up a chip containing an area-array of solder balls facing downward. The chip is then aligned and placed on top of a substrate with a corresponding area-array of pads. A survey of commercially available placement tool specifications shows that there is an inverse

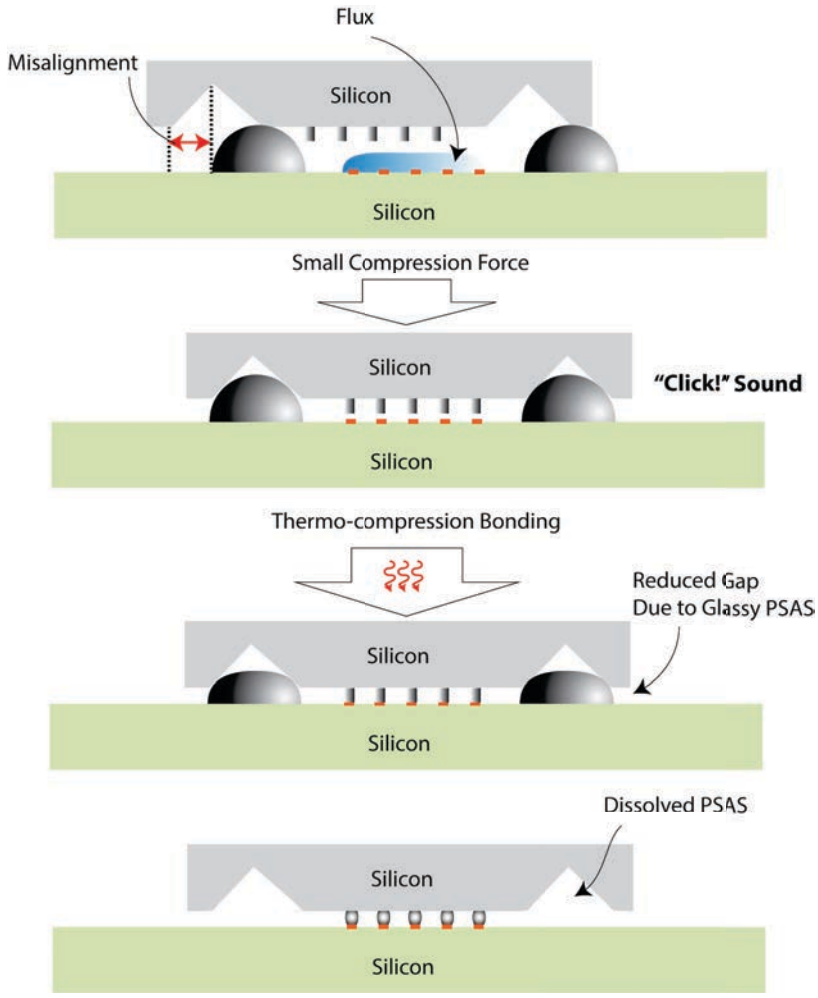


Figure 116: Brief overview of the tool-less self-alignment bonding process.

relationship between alignment accuracy and speed of alignment. For example, a flipchip bonder from Panasonic (Model FCB3) is capable of aligning a chip to a substrate with +/-3 μm accuracy in 1.8s. On the other hand, a different model from the same company (Model BM123) with a much lower accuracy of +/-50 μm can align a chip to a substrate in 0.12 s [61, 62]. Thus, it is possible to see that the alignment accuracy requirement comes at a cost, and there is a significant manufacturing throughput advantage to being able to place chips to a less than 5 μm accuracy using a 50+ μm accuracy tool.

Once the chip and the substrate are aligned, the flip-chip bonder mounts the chip on the substrate so that the solder balls and pads come into contact. The reflowing of

the solder physically bonds and electrically interconnects the chip and the substrate. Application of flux to the solder is essential for high quality bonds.

The alignment accuracy required for the flip-chip process depends on the interconnect technology used; for arrays of solder balls, the misalignment must be smaller than the radius of the solder interconnects (self-aligned through molten solder's surface tension), while optical interconnects require an alignment accuracy better than 1 μm for optimal performance [14, 15, 16]. It has been shown that for an optical system with grating couplers, less than 2 μm misalignment is needed to achieve less than 1dB excess loss [15]. As the interconnect density increases, and as the industry looks towards optical interconnects, highly accurate alignment will become critical for future system assembly needs.

7.3.2 Other Self-alignment Techniques

A number of self-alignment techniques compatible with flip-chip bonding have been published previously. Most notably, the surface tensions of flux [67] and water [66] have been exploited to provide the self-alignment between the chip and substrate. However, there are several challenges associated with such techniques, which warrants alternative techniques such as the one described in this work. Challenges include:

- Alignment accuracy of the self-alignment technique using the entire die surface is limited by the dicing precision, which is limited to +/- 15 to 25 microns [66].

- For the self-alignment technique that exploits pad areas, the magnitude of correctable misalignment is dependent on pad size; large pads (i.e., large pitches) are required to correct large initial misalignments.

- For the self-alignment technique that exploit water or flux surface tension, the ability to dispense a small volume of water is essential [78]. In addition, leveled surfaces are required [79].

In another study, sapphire balls and inverted pyramid pits are used to provide self-alignment [65]. However, such mechanisms lack the ability to be compressed during the assembly process. Another paper presented an alignment using a precisely patterned template and DRIE etched chip edges, but this approach can be costly, and errors may be introduced when holding the chip in the corner position of the template [80].

The technique presented in this work can correct large misalignments independent of the sizes and pitches of the I/Os used, and its alignment performance is independent of dicing accuracy. Also, additional or specialized tools are not required.

7.4 Sacrificial Self-alignment Technology

PSAS and pits (Figure 79) are used for the alignment. PSAS are reflowed photoresist dome-like structures; depending on the initial heights of the cylinder-shaped structures that are reflowed, truncated spheres or semi-spheres can be formed [81].

The use of photoresist material is suitable for this application because it enables compression of the PSAS during the thermo-compression bonding process, and it can also be removed chemically once the bonding process is complete.

7.4.1 Geometrical Considerations

The width of the pit, in conjunction with the diameter of the base of the PSAS, plays an important role in determining the gap between the chip and the substrate. The resulting gap, which is greater than the solder height, is critical because premature contact between the solder and the bonding surface could halt the self-alignment process before completion.

For the process to be successful, the height of the solder used must be less than the final gap determined by the PSAS and pit sizes. The formula to calculate the resulting gap has been derived in Chapter 4 and in [82].

In this work, the resulting gap between the chip and the substrate is calculated to

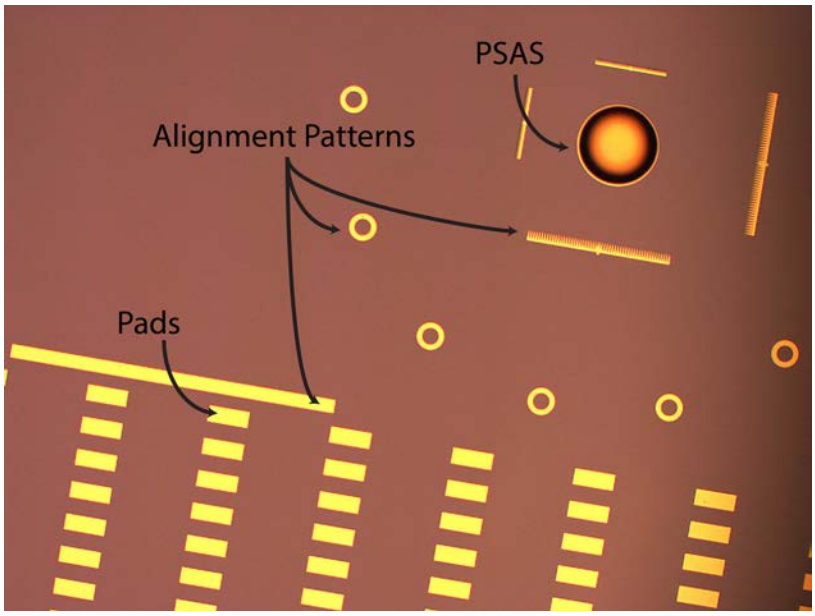


Figure 117: Microscope image showing a PSAS and pads.

be 28 μm. The height of the solder is 18 μm. As a result, a compression of at least 10 μm is required for the bonding process to be successful. A smaller gap is desired to prevent lateral shifts during the thermo-compression process, but a smaller gap also requires that the height of the solders and the accuracy of the gap produced by the PSAS and pits to be controlled precisely.

The width of the pit is also important because it determines the maximum initial misalignment that the self-alignment mechanism can tolerate. If the initial alignment is less than half the width of the pit, the center of the PSAS will be located within the square region of the PSAS. This causes the PSAS to slide into the center of the pit when pressure is applied.

To enable one to align without a placement tool, it is advantageous to make the coarse alignment tolerance as large as possible. The pits in this work are fabricated with 300 μm sides, which are large enough for assembly without an advanced placement tool.

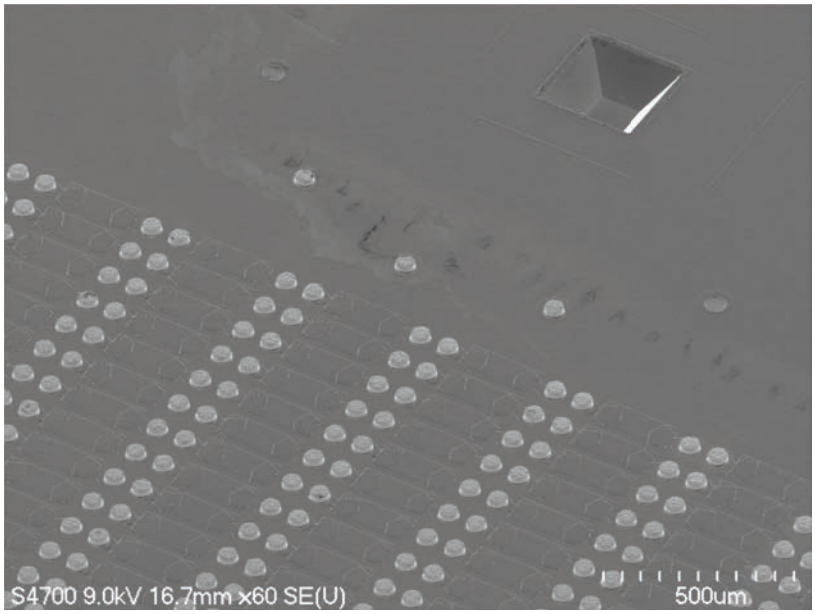


Figure 118: SEM image showing a pit, solder balls, and traces.

7.4.2 Assembly Process

The complete process flow is shown in Figure 119.

7.4.2.1 Intentional Misalignment and Placement (Steps 1 and 2)

The process assumes that misalignment less than half the width of the pits exists during placement. Flux is applied to the solder array, and the chip and the substrate are brought into contact.

7.4.2.2 Inducing Self-alignment (Step 3)

Once the chip and the substrate are in contact, a small amount of vertical compression force is required to initiate the self-alignment process. A "click" sound is heard as the PSAS slide into the pits, and the chip and the substrate become aligned. At this stage, the solder balls are not in contact with the pads.

7.4.2.3 Thermo-compression Bonding (Step 4)

Thermo-compression bonding is performed using a conventional flip-chip bonding reflow profile. Glassy PSAS become compressed during the reflow process, and the

gap between the chip and substrate decreases. This causes the solder array to make contact with the corresponding pads.

7.4.2.4 Flux/PSAS Removal via Water and Acetone Bath w/ Agitation (Step 5)

The bonded sample is submerged in a warm water bath and agitated. The water-soluble flux residue is removed during this process. Next, the sample is submerged in an acetone bath and agitated. The photoresist-based PSAS are dissolved.

7.5 Method and Results

The objective of this work is to demonstrate that self-alignment structures can be used *sacrificially* and that the technique can be applied in thermo-compression bonding of a solder ball array. Experiment details are outlined in Table 7. The technique is demonstrated in three parts:

1. The ability to correct misalignments beyond what is possible with conventional solder ball assembly techniques is verified; a lateral misalignment as large as 150 μm (five times the radius of the solder balls) is intentionally induced during chip placement. After applying a small compression force to induce the self-alignment mechanism, the relative positions of the substrates are determined using an x-ray tool, and the self-alignment process is verified (Steps 1-3 in Figure 119).

2. Compatibility with a thermo-compression bonding process is verified; three self-aligned chips (from the first set of experiments) and the electrical connectivity between the chip and the substrate are verified using daisy chain structures and four point measurements (Step 4 in Figure 119).

3. The ability to use the PSAS sacrificially is verified; the assembled samples are submerged in a resist remover solution to ensure that PSAS can be removed after

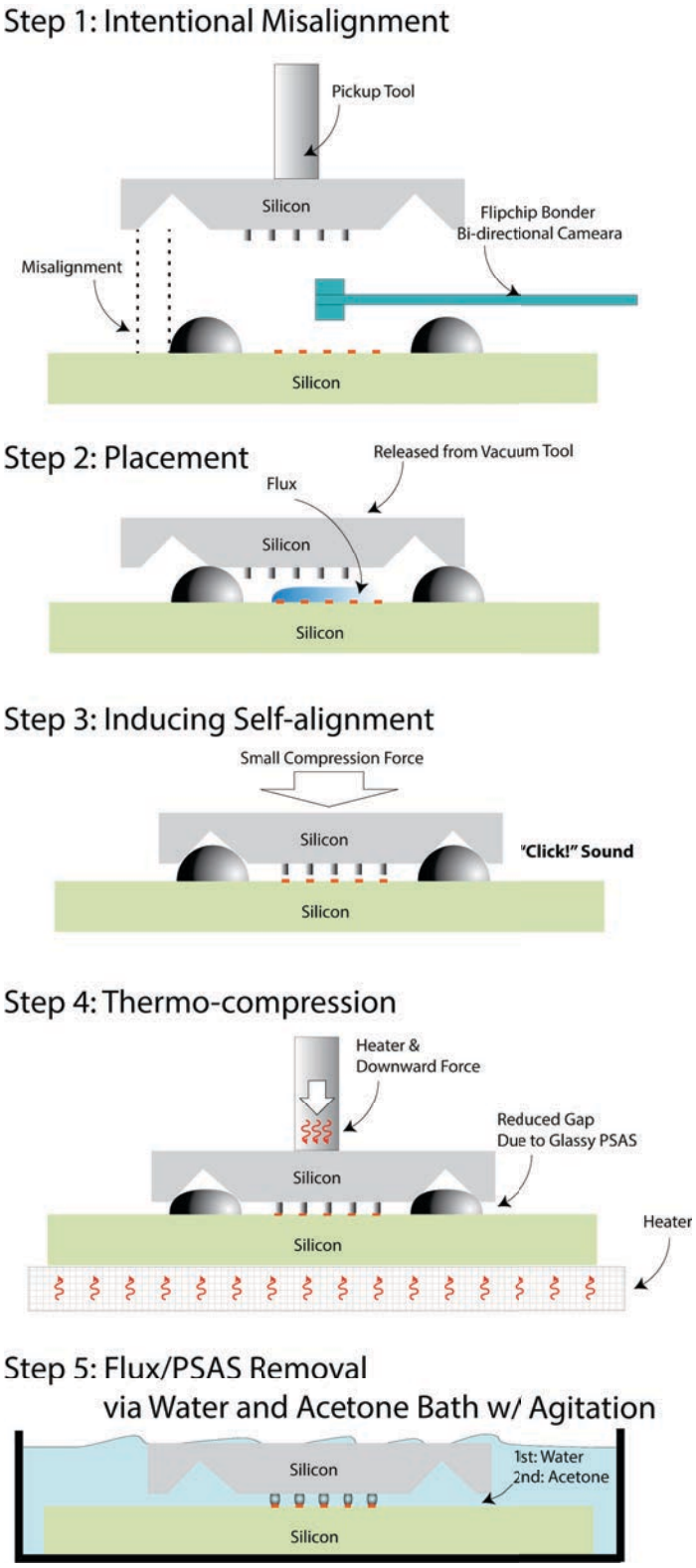


Figure 119: Experiment to verify the self-alignment capability.

Table 7: Experiment Details

Chip Parameters	
Top Chip Dimensions	1.8 cm x 1.6 cm
Bottom Chip Dimensions	2.7 cm x 2.7 cm
Chip Thicknesses	500 μm
Silicon Wafer Type	<100> n-type doped
Solder Parameters	
Solder Type	$Sn_{60}Pb_{40}$
Solder Deposition Method	Electroplating
Solder Diameter	60 μm
Solder Height (Pre-reflow)	18 μm
Array Size (row x col = total)	130 x 84 = 10920
Pad Parameters	
Top Chip UBM	
(Below Solder)	1-2 μm of Ni
	1 μm of Cu
(Above Si Nitride)	50 nm of Ti
Bottom Chip Pad Materials	
(Top Exposed Layer)	30 nm of Au
	1-2 μm of Ni
	1 μm of Cu
(Above Si Nitride)	50 nm of Ti
Assembly Parameters	
Pre-bonding Gap	28 μm
Bonding Force	4 N
Flux	Indium Corporation FC-NC-HT-A1

the assembly process. The assembled samples are separated and microscopically examined (Step 5 in Figure 119).

7.5.1 Misalignment Correction

The objective of this section is to verify that the PSAS and pits can correct initial misalignments larger than the self-alignment capabilities of a solder ball array. Typically, solder ball arrays can correct misalignments that are equal to or less than the radius of the largest solder balls used during the bonding process, and a highly accurate alignment accuracy can be achieved if the process is optimized [83]. However, it is often desirable to have smaller solder balls with small pitches, while attaining the

alignment capability of larger solder balls. For example, an application may require a dense array of solders with 30 μm diameters as well as a self-alignment capability that can correct up to 150 μm of misalignment. Using the conventional process, only up to 15 μm of misalignment can be corrected in such case, and a misalignment greater than 15 μm may result in solder balls becoming assembled with wrong pads.

Using the PSAS and pits, it is possible to decouple these two requirements. To demonstrate this, three samples are aligned with an intentional misalignment of 60 μm (2x r_{solder}), 120 μm (4x r_{solder}), and 150 μm (5x r_{solder}). The r_{solder} represents the radius of the solder balls, which is 30 μm. The intentional misalignment is induced using a flip-chip bonder and the images captured using the bonder's bi-directional camera before the chip placement are shown in Figure 122. For easy comparison, Figure 120 shows the mask design with the perfect alignment, and Figure 121 shows the perfectly aligned image captured by the bi-directional camera.

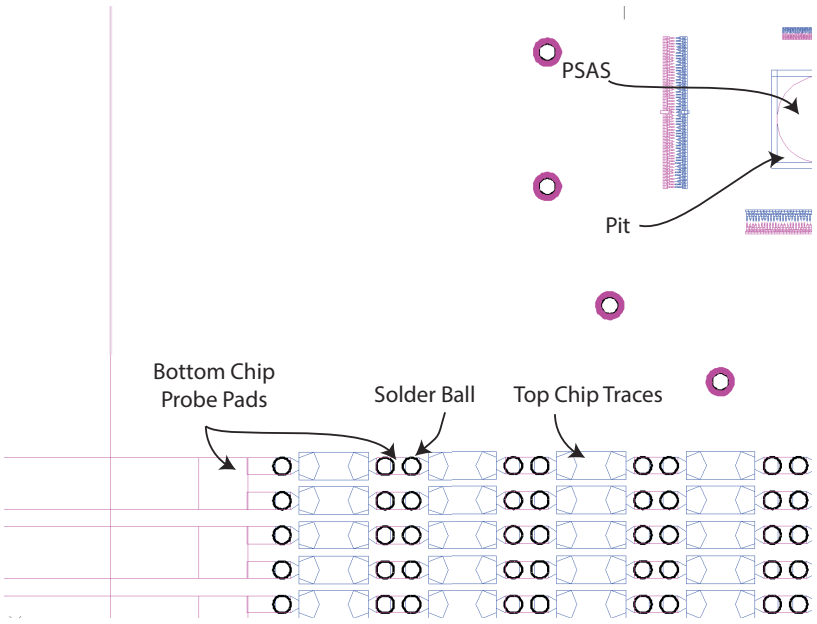


Figure 120: The mask design of the chips used to show the perfectly aligned features on two substrates.

Each chip is released from the vacuum tool after being placed on top of a pad array with the intentional misalignment. Next, a small weight is applied to the top

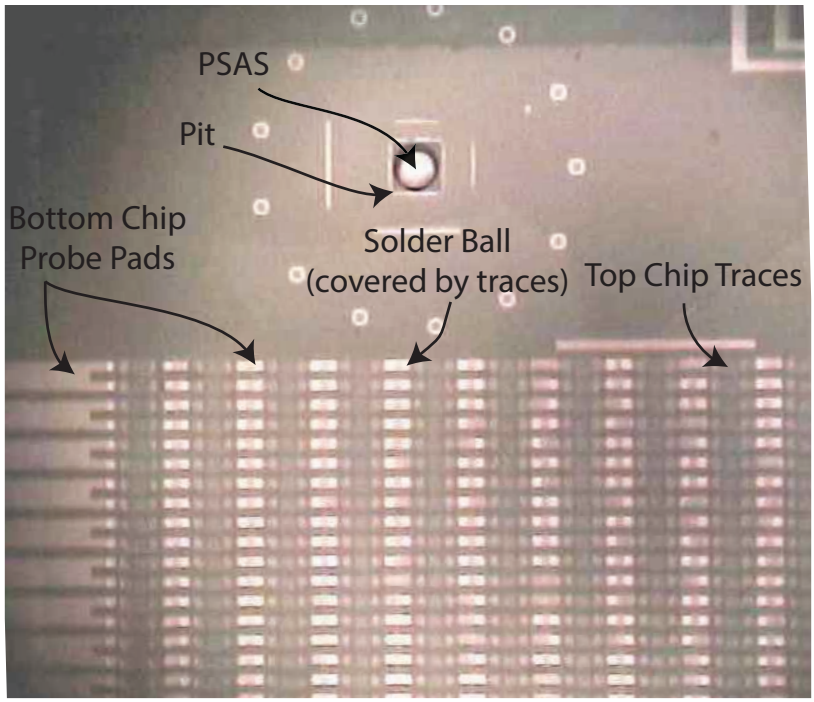


Figure 121: The overlay captured by the flip-chip bonder's bi-directional camera show substrates that are perfectly aligned.

chip until a "click" sound is heard. At this point, the chip becomes locked in position and cannot be moved laterally.

Figure 122 show images captured before and after the bonding process with various initial misalignments that are intentionally introduced. In all three cases, the x-ray images show that solder balls are placed and bonded to the intended pads despite large misalignments. Figure 123 shows the bonded chip on the substrate.

7.5.2 Thermo-compression Assembly and Electrical Connectivity

The objective of this section is to verify that the PSAS and pits are compatible with the thermo-compression bonding process; the bonding quality (i.e., resistance) of the solder balls and the yield are measured. Using the three samples from the first set of experiments, thermo-compression bonding is performed. A constant compression force (4 N) was used, and the reflow temperature profile used is shown in Figure 124.

Two types of electrical structures are built-in to the chips and substrates:

1. Daisy chain structures are used to verify that the bonding process provides high yield. Daisy chain sizes ranging from 84 solder balls to 10,920 solder balls are designed in the layout.

2. Four point resistance measurement structures are used to verify that high-quality bonds have been formed.

The electrical measurements are shown in Table 8. The results show that high quality solder bonds are formed, and that the yields calculated from the daisy chain measurements are 100 %. Subsequent detaching of the chip and substrate shows that 100 % of the solder balls (including the pads underneath) are transferred from the top chip to the bottom chip, which indicates that the newly formed bonds are stronger than the adhesion strength of the evaporated titanium and copper on a silicon nitride surface.

Table 8: Resistance Measurements and Bonding Yield

Sample 1 w/ 60 μm of Initial Misalignment	
$R_{solderball} + R_{contact}$	8.92 $m\Omega$
Standard Deviation	1.50 $m\Omega$
Yield calculated from Daisy Chain	100%
Sample 2 w/ 120 μm of Initial Misalignment	
$R_{solderball} + R_{contact}$	8.42 $m\Omega$
Standard Deviation	0.96 $m\Omega$
Yield calculated from Daisy Chain	100%
Sample 3 w/ 150 μm of Initial Misalignment	
$R_{solderball} + R_{contact}$	8.42 $m\Omega$
Standard Deviation	0.96 $m\Omega$
Yield calculated from Daisy Chain	100%

7.5.3 PSAS Removal

The objective of this section is to verify that the PSAS can be removed after thermo-compression assembly. Since PSAS are made of photoresist, the structures' presence beyond the assembly process can cause reliability issues, and they must be removed. However, while photoresists can typically be removed easily, there are two factors that

may affect the ability to remove PSAS: the temperature of the bonding process and the gap between the chip and the substrate. As such, the removal process warrants verification.

Flux is removed prior to the removal of the PSAS. Solder flux from the Indium Corporation is used and can be removed by a warm water bath with a gentle agitation. To remove the PSAS, the bonded samples are submerged in resist remover solvent. Figure 126 shows an image of detached chips that underwent the PSAS removal process. The image shows that the PSAS are completely removed.

7.6 Conclusions

A thermo-compression bonding of a solder ball array is demonstrated using sacrificial positive self-alignment structures and inverted pyramid pits. By intentionally introducing a lateral misalignment greater than what is correctable with the surface tension of solder balls, the ability to correct up to 150 μm of misalignment using PSAS and pits is experimentally verified. In addition, high-quality bonding is also verified through electrical measurements, and the ability to remove the PSAS after the bonding process is visually verified.

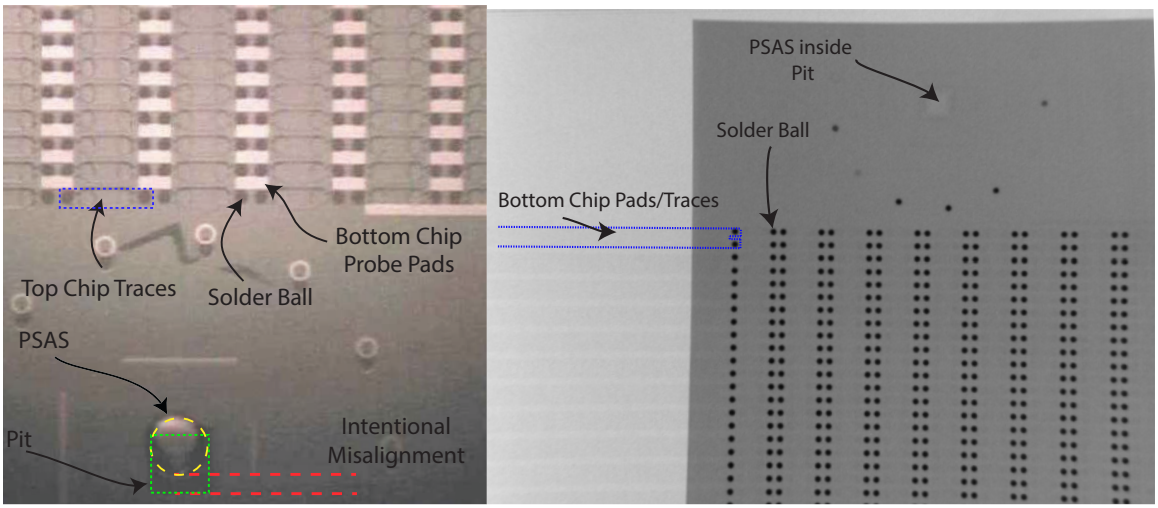


Image showing 60 μm (two times the solder ball radius) of intentional misalignment.

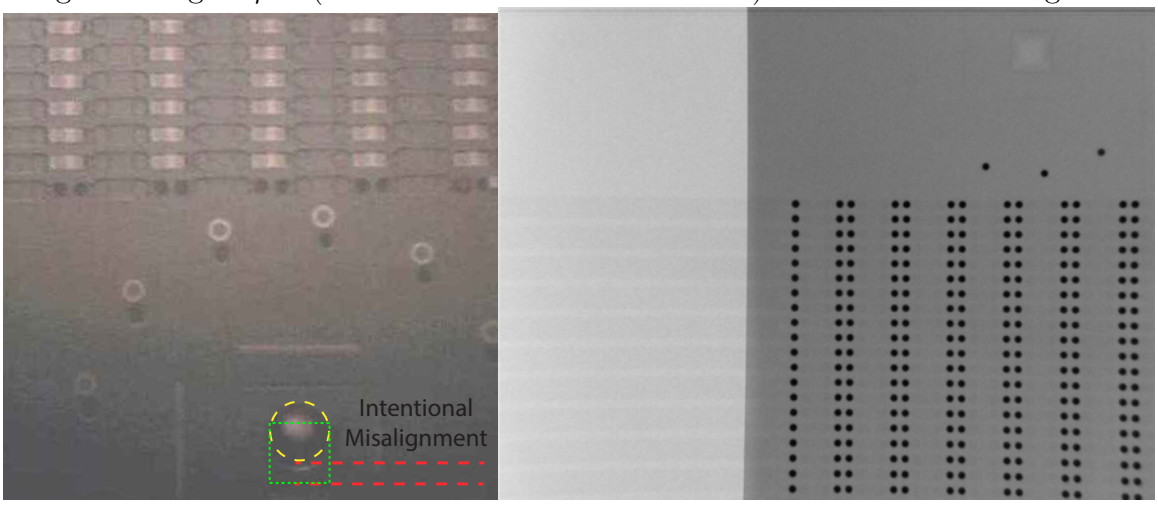


Image showing 120 μm (four times the solder ball radius) of intentional misalignment.

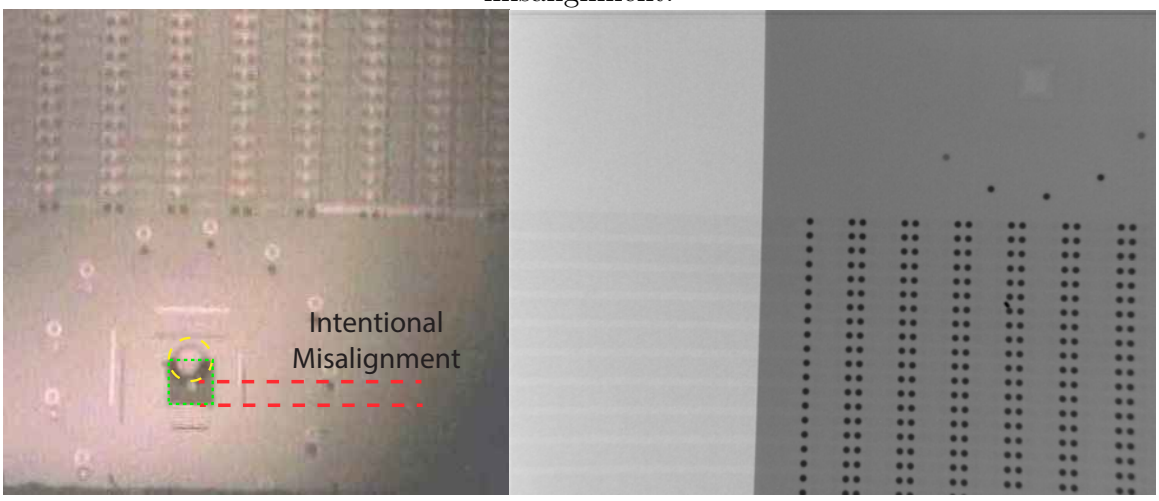


Image showing 150 μm (five times the solder ball radius) of intentional misalignment.

Figure 122: Images showing the misalignment correction.

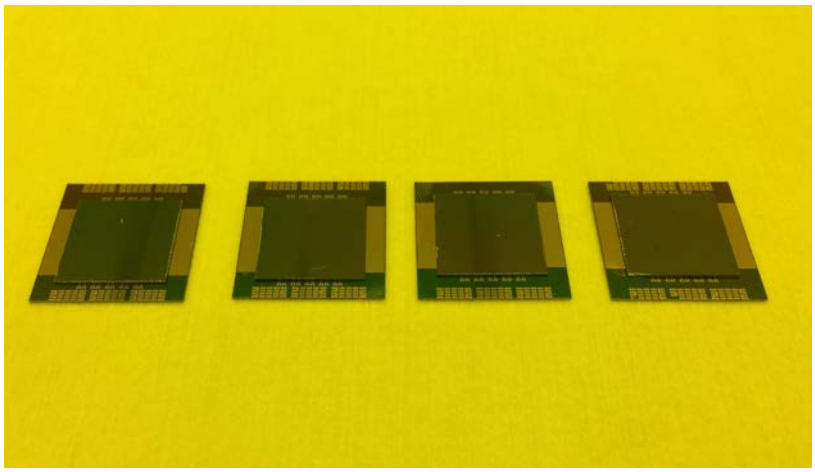


Figure 123: Photo showing four pairs of bonded chips.

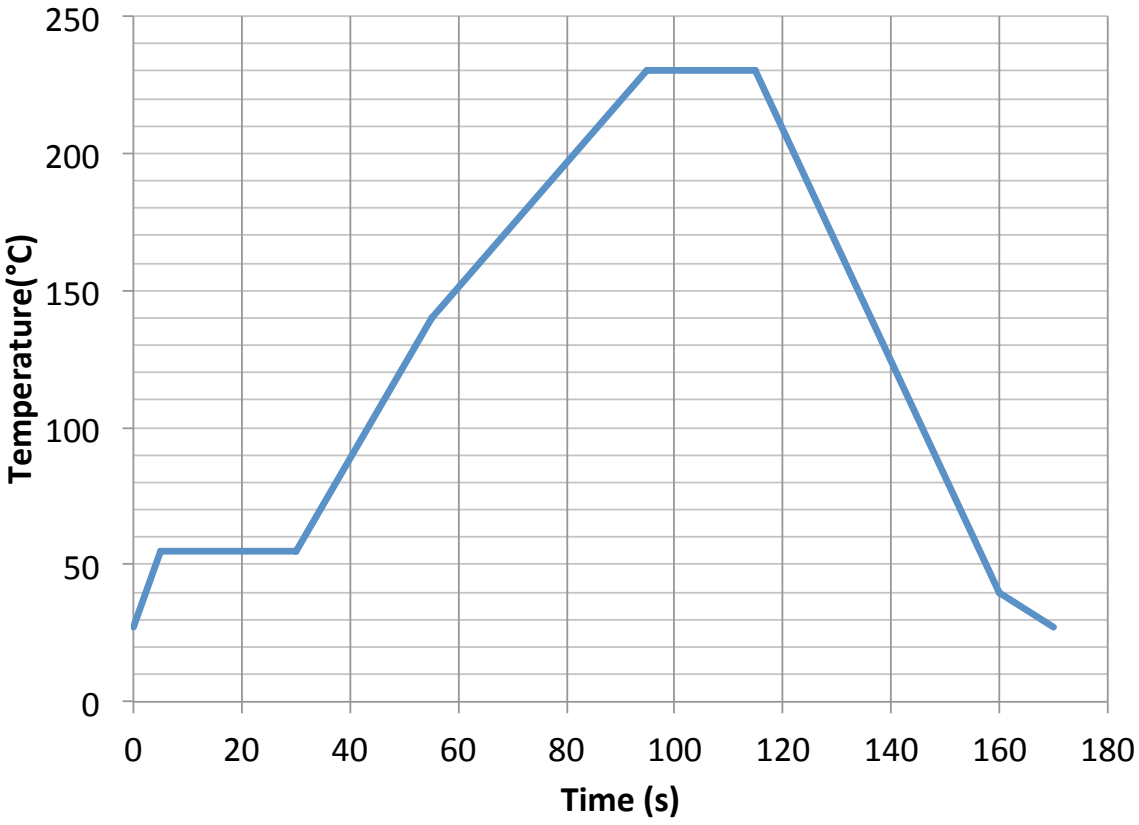


Figure 124: Reflow profile used for the assembly process.

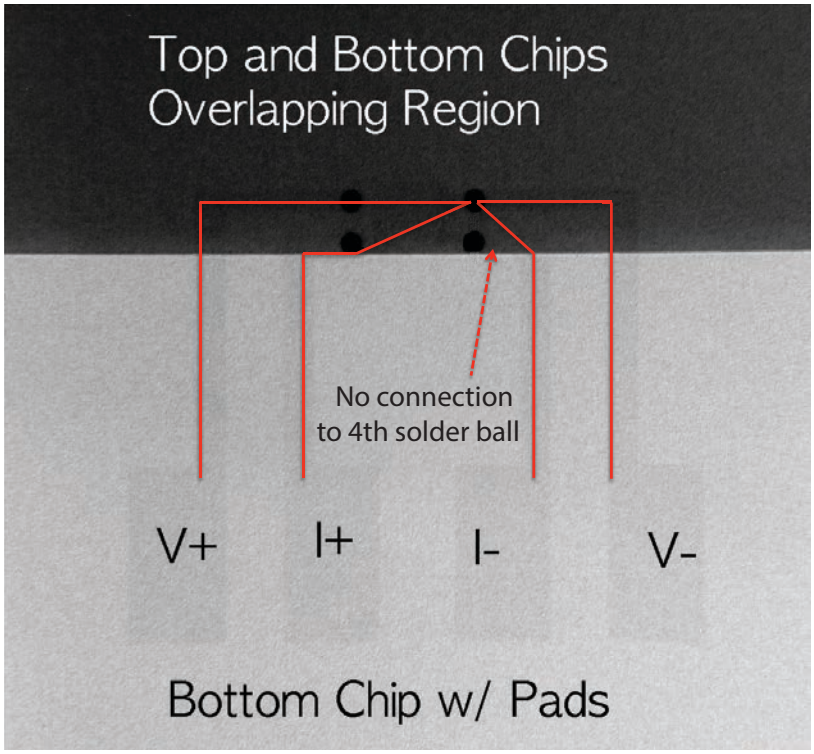


Figure 125: X-ray image showing four point probe structures to measure the resistance of a single solder ball including the contact resistance.

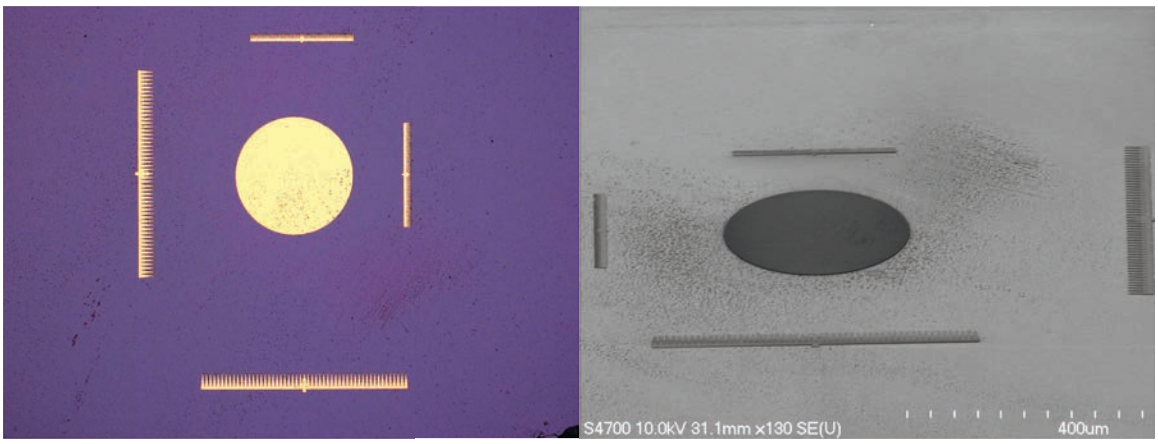


Figure 126: SEM and microscope images of detached chips show that the PSAS are completely removed.

CHAPTER 8

FUTURE WORKS

This chapter describes opportunities for advancing the technologies in this dissertation. In the first section, opportunities to advance MFIs and PSAS are described. In the second section, opportunities to advance the platform are described.

8.1 Silicon Interposer Tiles and Bridges Platform

8.1.1 Co-fabrication of PSAS and MFI

For the demonstration in this work, MFIs and pits are fabricated on the same side of the interposer tiles. This is partially due to the difficulty of forming PSAS and MFIs at the same time; when PSAS are formed after the MFIs have been released, the photoresists trapped under the MFIs (Figure 127) become impossible to remove without damaging the PSAS.

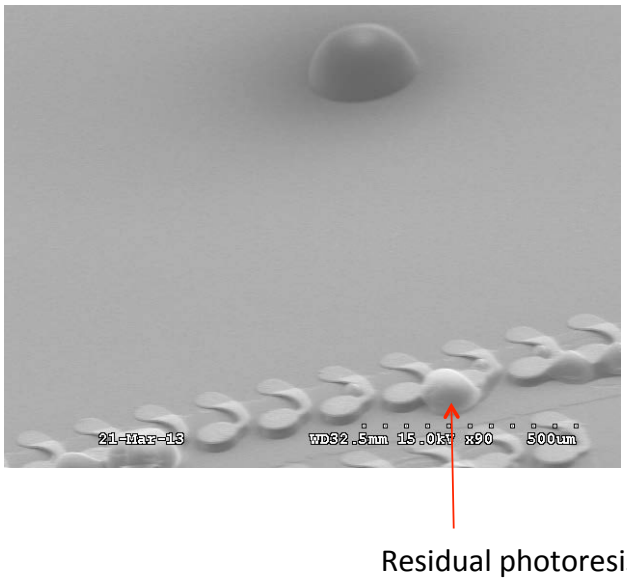


Figure 127: A trapped photoresist under an MFI during the co-fabrication process.

There are several significant advantages to being able to form PSAS and MFIs

on the same wafer side. First, since the motherboard can only contain PSAS and not pits, this is the first step in being able to fabricate MFIs on an FR4 substrate. Second, the configuration can become more versatile, and a stacking of 3 or more substrates becomes possible without having to fabricate PSAS and/or MFIs on both sides of a single substrate.

8.1.2 Nanophotonics Integration

The alignment and electrical interconnectivity have been demonstrated on the bridged platform. To demonstrate the platform's advantage over conventional systems, nanophotonics must be integrated into the interposer tiles and bridges. Once nanophotonics are integrated, the performance should be benchmarked against electrical interconnects for systems with varying numbers of interposer tiles.

8.1.3 RF Characterization of Electrical Interconnects

The RF characteristics of MFIs on silicon interposer tiles and bridges must be investigated. The design of the current MFIs focuses on mechanical performance, and its high frequency characteristics may require a significant modification to its geometry. A testing setup, as shown in Figure 128, may be used.

Also, the benefit of silicon bridges may be quantified by comparing the performance of the electrical path through the silicon bridge with the electrical path through the motherboard via TSVs and motherboard traces.

8.1.4 Micro-fluidic Cooling on Silicon Interposer Tiles

A large system containing multiple silicon interposer tiles may be challenging to cool using conventional air heat sinks. Therefore, micro-fluidic heat sinks may need to be integrated into silicon interposers.

Solder-based microfluidic I/Os have been reported [84], in which a thermo-compression bonding process is used to form fluidic pipes between two substrates. The technique

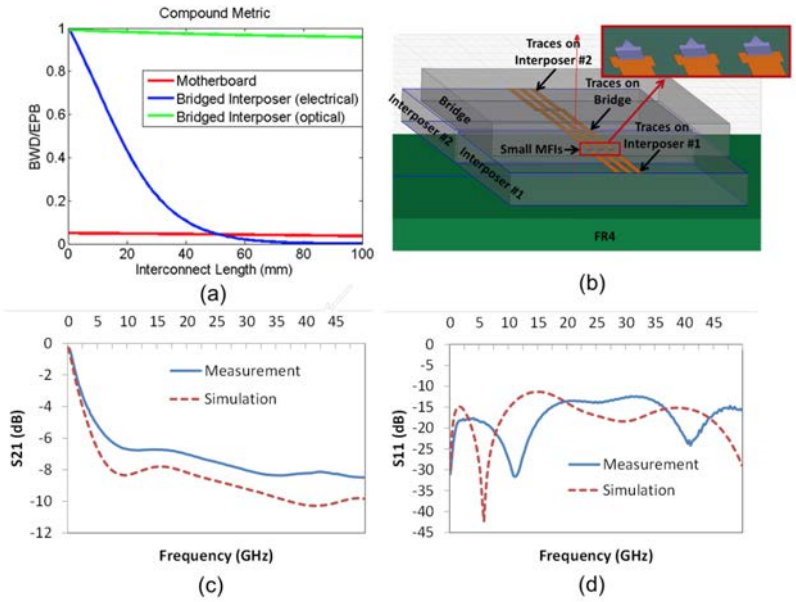


Figure 128: An RF testing setup for the bridged silicon system.

developed in Chapter 8, in which PSAS are used for a thermo-compression bonding, may prove to be useful if such technology is integrated into silicon interposer tiles.

8.1.5 Elongated Pits and PSAS for Thermo-mechanical Compliance

While the PSAS and pits provide an accurate alignment at a given temperature, undesired changes may occur when the temperature changes. Four modes of such changes are described in Figure 129. To address this, elongated pits may be formed instead of pits. Elongated pits would allow the PSAS to move in only one degree of freedom, and if positioned appropriately, would allow the assembled substrates to expand freely without warping or being lifted in an uncontrolled manner due to the CTE match (Figure 130).

8.2 MFI

8.2.1 MFI Scaling

This work demonstrated a novel process for forming a flexible interconnect with the focus being on vertical deflection. This technique must be scaled down to provide the

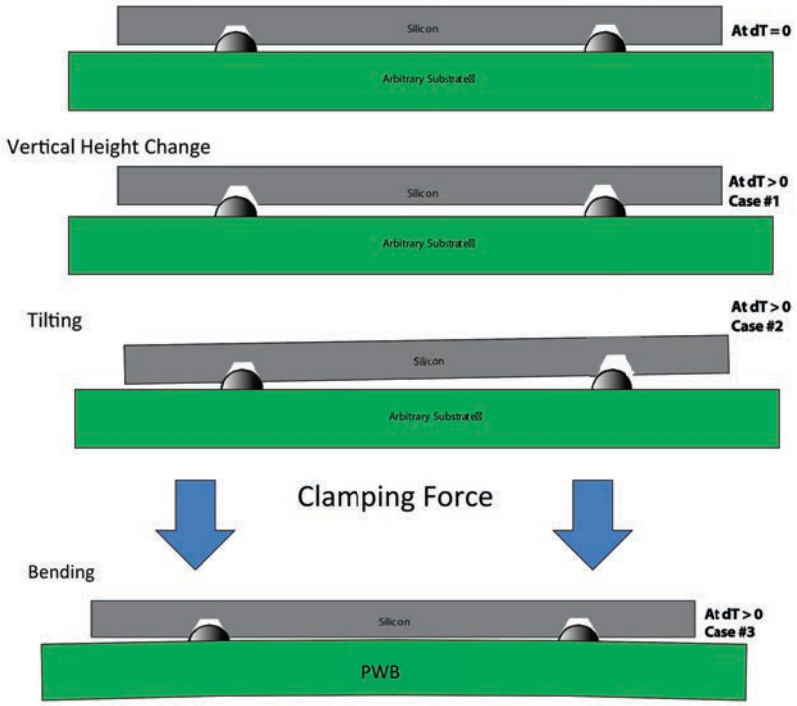


Figure 129: The CTE mismatch between the silicon and FR4 substrate causes undesirable effects.

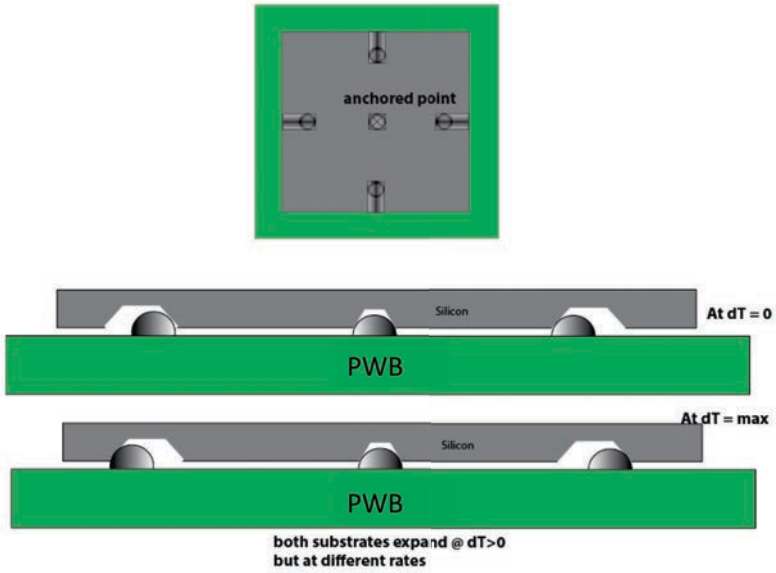


Figure 130: Elongated pits can completely eliminate the effect of the CTE mismatch.

pitch and the bandwidth required for high-performance systems.

There are several potential challenges. First, smaller MFIs may not be able to provide the same amount of elastic vertical deflection range; instead, the vertical stand-off height and the thickness may also need to be scaled down. Second, patterning MFIs on a curved surface may be difficult since the dimensions of the MFIs are reduced; alternative methods, such as spray coating may be required. Finally, electro-deposition may be difficult because of the small openings on the electroplating mold; plasma deposition methods such as sputtering must be explored, which can also provide more uniform mechanical characteristics throughout the wafer.

8.2.2 Vertical Pads

The mechanical characteristics of conventional flexible interconnect structures have conflicting requirements. While it is desirable to have a high vertical compliance and high vertical elastic range of motion to reduce the internal stress on the flexible interconnect structure, it is also desirable to have a low compliance to make sure the contact resistance between the interconnect and the pad is minimized. By fabricating the pads as shown in Figure 131, the problem of these conflicting requirements can be resolved.

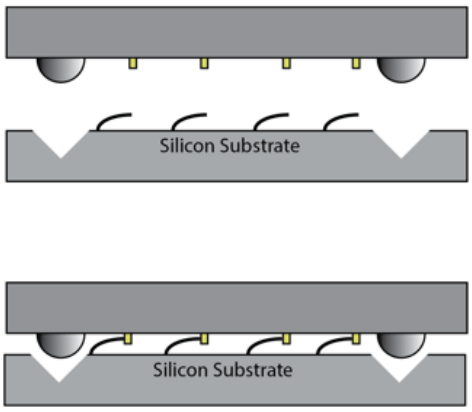


Figure 131: MFIs make contact with the sides of the pads. The lateral compliance determines the contact resistance, while the vertical compliance can be increased to reduce stress.

The key component in this process is the presence of tall pads; instead of flexible interconnects making contact with the top/bottom planes of the pads, the contacts occur on the side of the pads. This means that the contact resistance (which is inversely proportional to the contact force) between the pads and the flexible interconnects is determined by the in-plane compliance of the flexible interconnect, while the vertical compliance is still responsible for overcoming the non-uniform surface. This is significant because the vertical compliance is mainly affected by thickness, while the lateral compliance is affected by the width of the flexible interconnect; by designing the flexible interconnects to have a wide but thin structure, a high vertical elastic range-of-motion and low contact resistance can be achieved.

In their simplest form, the pads can be tall pillar like structures. However, by shaping the pads as shown in Figure 132, they can also be used to hold two chips together. In the latter configuration, MFIs may also bend upwards, increasing the elastic range-of-motion after assembly.

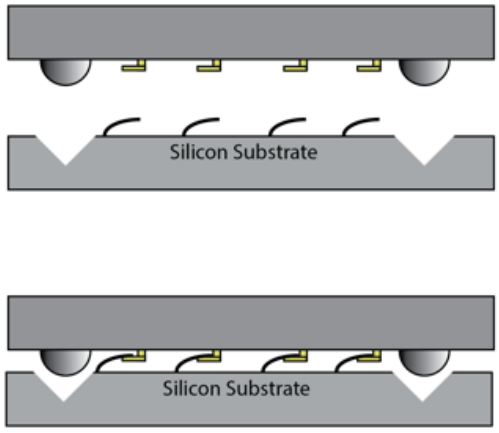


Figure 132: Clamping pads provide the benefits of vertical pads and also prevents MFIs from being disconnected unintentionally.

Vertical pads also addresses the inherent challenges in designing MFIs; as MFIs become taller, it becomes difficult to assure that the tip is the highest point during most of its deformation. By using tall vertical pads, the tip no longer needs to be the

tallest part during the deformation process to ensure a good electrical contact.

8.3 PSAS

8.3.1 Gap Measurement

The gap between two substrates is a critical parameter for silicon nanophotonics. While this work has demonstrated that PSAS can accurately align two substrates laterally, additional work is necessary to measure and control the gap that is produced by the PSAS and pit technology.

This work should begin by developing a novel method of measuring gaps between substrates. A conventional method, such as examining a cross-sectional image of the assembled substrates, is not adequate because the angle of the cut affects the result significantly. Instead, a highly precise method is required.

Next, the uniformity of the PSAS must be controlled to improve the control over the gap. While the precision of the lateral alignment accuracy is quite insensitive to the uniformity of the photoresist layer, the gap is highly affected; the 10% variation in the thickness would be translated into a significant variation in the gap that is produced by the PSAS-pit pairs in a single wafer. A novel photoresist deposition method, such as spray-coating, may be used.

8.3.2 Alignment Accuracy Measurement Improvement

Improving the lateral alignment accuracy of the PSAS technology is also desirable. One major source of inaccuracy is from the misalignment introduced during the feature-to-feature alignment of the pits or PSAS to the traces containing the vernier patterns. This can be improved by using a more advanced mask aligner; however, because of the large PSAS thickness, it is impossible to focus on both the mask and the traces, which makes the accurate alignment difficult.

8.3.3 Metal-based PSAS

While photoresist-based PSAS have advantages, such as compressibility and removability, it may be desirable to have PSAS that are more reliable under elevated temperatures and other operating conditions. A metal-based PSAS is ideal in such situations.

However, forming a metal-based PSAS is challenging because electroplating is the only viable process for forming such a large metal-based structure. Electroplating, however, is an inherently non-uniform process, and extraordinary measures are required to ensure that the resulting structure is exactly as intended. Below, two potential methods of fabricating accurate metal-based PSAS are described.

8.3.3.1 Metal PSAS via Inner Plating

The first method begins with the photoresist-based PSAS fabricated on top of a seed layer (Ti/Cu/Ti). After the reflow, the PSAS is exposed, which makes the entire structure removable using a developer solution. A glass layer is evaporated or sputtered, and a thick photoresist layer is spin-coated. A small hole is patterned on the photoresist to reveal the glass layer on PSAS. An RIE process is used to etch away the glass layer, which exposes the PSAS photoresist. The sample is then submerged in a developer to remove the photoresist PSAS. The sample is electroplated using the newly exposed seed layer. The process flow is shown in Figure 133.

8.3.3.2 Metal PSAS via Double Exposure

The second method begins with a photoresist-based PSAS (unexposed). A mask with a small hole is used to expose the center of the PSAS, and the developed center is developed way. The resulting structure is shown in Figure 134. A metal seed layer and a glass layer are evaporated under a high pressure environment to minimize the deposition on the side wall of the hole. Acetone is used to remove the PSAS and results in the suspended metal and glass layers. Electroplating the sample begins

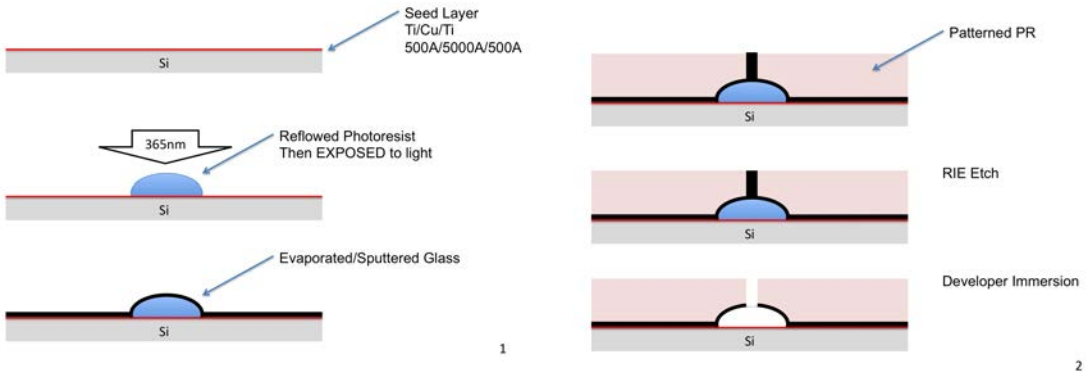


Figure 133: Process flow for forming metal PSAS via inner plating.

forming metal from the suspended layers, which results in a smooth PSAS surface. The process flow is shown in Figure 135.

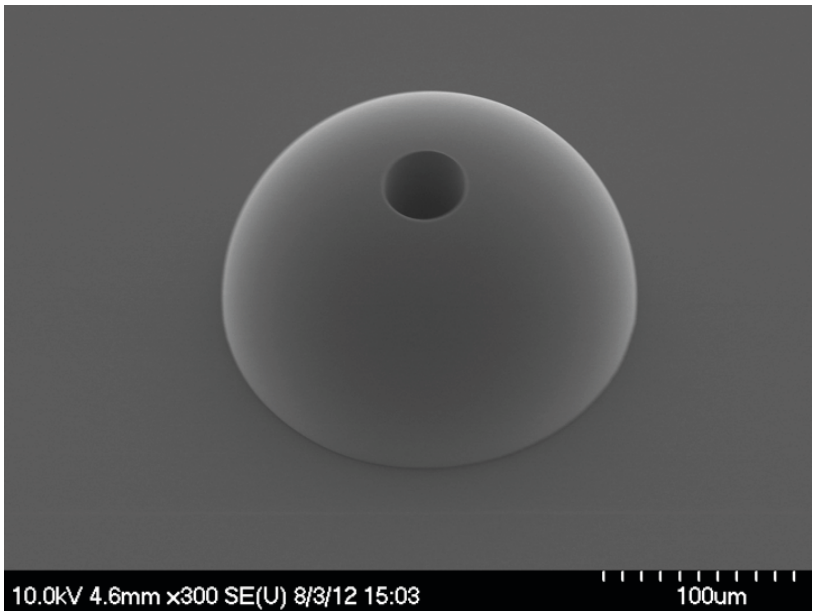


Figure 134: Double exposed PSAS with a center hole.

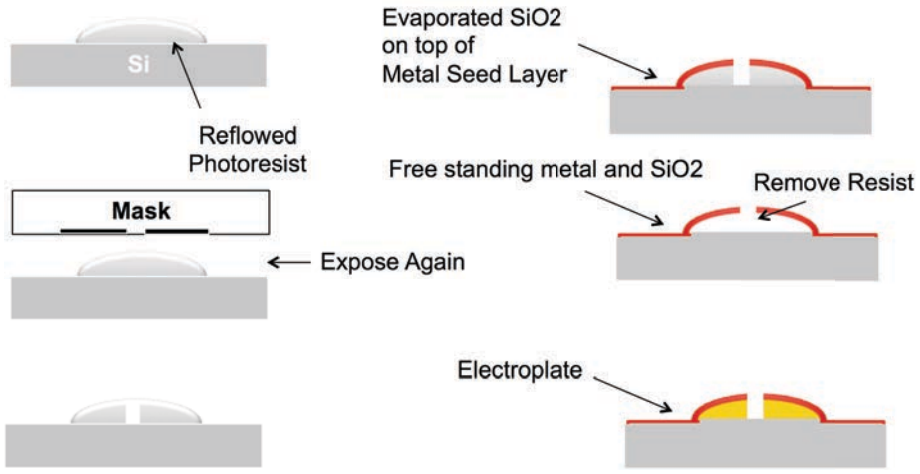


Figure 135: On the left is an optical microscope image of the SU8 mold and on the right is an optical microscope image of the resulting stamped elastomer structure.

CHAPTER 9

CONCLUSION AND CHAPTER SUMMARIES

9.1 Conclusion of the Thesis

A novel large-scale silicon system platform with 9.6 cm^2 of active silicon interposer area is demonstrated. The platform contains three interposer tiles and two silicon bridges, and a novel self-alignment technology and a novel flexible interconnect technology are developed and used to align and interconnect tiles and bridges on an FR4 substrate. An accurate alignment (<8 μm) between the silicon bridges and interposer tiles makes it possible (with additional improvements) to accommodate nanophotonics to enable a high-bandwidth, low-energy system in the future. In addition, mechanically flexible interconnects and silicon bridges are used to provide electrical connections between interposer tiles without having to use motherboard-level interconnects.

Finally, an elastomeric bump interposer is developed to enable the packaging of PSAS-enabled silicon systems, and PSAS' compatibility with a thermo-compression bonding process is demonstrated to enable a wide range of system configurations involving interposer tiles and bridges, including the multi-chip package configuration used with the elastomeric bump interposers.

9.2 Chapter Summaries

In addition to the platform demonstration (Chapter 5), the following novel interconnect and packaging components are developed:

9.2.1 Through-silicon Via (TSV)

In Chapter 2, a novel TSV technology for silicon interposers is demonstrated. The "mesh" technique makes the seed-layer formation efficient, and the chemical-only planarization becomes possible by electroplating with two metals. The benefits of this TSV process are demonstrated in two ways. First, the CMOS compatibility of the process is demonstrated by fabricating the TSVs in TSMC 0.35 μm CMOS ICs. Second, the versatility of the "mesh" process is demonstrated by extending the technology to form polymer-cladded TSVs.

9.2.2 Mechanically Flexible Interconnects

In Chapter 3, a novel flexible interconnect technology called mechanically flexible interconnects (MFIs) is developed. The first generation of MFIs ("MFIv1") has a stand-off height of 20 μm and incorporates the tapered and curved designs to increase the vertical elastic range of movement; a novel sacrificial reflowed photoresist process is developed to enable the fabrication of curved MFIs, and the benefit of the tapered design is analyzed. Mechanical FEM simulations and measurements are performed to verify that only a small amount of plastic deformation is experienced by MFIv1 when it is deflected 20 μm vertically. The fabrication process to form and confine solder balls at the tips of MFIs is also developed.

The second generation of MFIs ("MFIv2") has a stand-off height that is greater than 60 μm and incorporates both the reverse-tapered and tapered designs. The reverse-tapered region of the design produces a bending profile that allows the vertical range of motion to be increased significantly, while the tapered region of the design reduces the maximum stress to minimize plastic deformation. The pitch is doubled by forming MFIs on both sides of the curved surface, and pointy tips are produced by avoiding the flat regions at the top of the sacrificial photoresist. The resistance of a single MFIv2, including the contact resistance with the pointy tip, is measured.

9.2.3 Positive self-alignment Structures

In Chapter 4, a novel self-alignment technology is fabricated, and the accuracy of the technology is experimentally demonstrated between a silicon substrate and silicon, glass, and FR4 substrates. A stack of silicon substrates is also aligned and its accuracy measured. An accuracy of $<4\ \mu m$ is consistently demonstrated between two silicon substrates (including in a 3D configuration), and $<5\ \mu m$ of misalignment is demonstrated between a silicon substrate and an FR4 substrate.

In Chapter 7, thermo-compression bonding of a solder ball array is demonstrated using sacrificial positive self-alignment structures (PSAS) and inverted pyramid pits. By intentionally inducing a lateral misalignment greater than the self-alignment capability of the solder joints, the ability to correct up to 150 μm of misalignment using PSAS and pits is experimentally demonstrated. In addition, the high quality bonding is verified through electrical measurements, and the ability to remove the PSAS after the bonding process is visually verified.

9.2.4 Elastomeric Bump Interposer

In Chapter 6, a low-cost elastomeric bump interposer that minimizes the warpage of substrates aligned using PSAS is designed, fabricated, and tested. These interposers apply a precise amount of force at precise locations to keep the PSAS and pits reliably engaged and to enable a batch assembly and alignment of PSAS-enabled multi-chip packages. The design of the interposers is optimized using FEM, and multiple elastomeric bumps and stiffening tungsten layers are used to further minimize the substrate warpage.

APPENDIX A

DERIVATION OF BENDING PROFILES

A.1 Straight Cantilever

This section derives the elastic curve of a cantilever with a constant width and a constant thickness.

$$M(x) = -P(L - x) \tag{17}$$

$$I(x) = I_0 \tag{18}$$

$$\frac{d^2y}{dx^2} = \frac{M(x)}{EI(x)} \tag{19}$$

$$= \frac{-P(L - x)}{EI_0} \tag{20}$$

$$\frac{dy}{dx} = -\frac{PLx}{EI_0} + \frac{Px^2}{2EI_0} + C1 \tag{21}$$

$$x = 0, \frac{dy}{dx} = 0, C1 = 0 \tag{22}$$

$$y(x) = -\frac{PLx^2}{2EI_0} + \frac{Px^3}{6EI_0} + C2 \tag{23}$$

$$x = 0, y = 0, C2 = 0 \tag{24}$$

$$y(x) = -\frac{PLx^2}{2EI_0} + \frac{Px^3}{6EI_0} \tag{25}$$

A.2 Tapered Cantilever

This section derives the elastic curve of a cantilever with a linearly tapering width and a constant thickness.

$$M(x) = -P(L-x) \tag{26}$$

$$I(x) = fracI_0(L-x)L \tag{27}$$

$$\frac{d^2y}{dx^2} = \frac{M(x)}{EI(x)} \tag{28}$$

$$= \frac{-P(L-x)L}{EI_0(L-x)} \tag{29}$$

$$\frac{dy}{dx} = -\frac{PLx}{EI_0} + C1 \tag{30}$$

$$x = 0, \frac{dy}{dx} = 0, C1 = 0 \tag{31}$$

$$y(x) = -\frac{PLx^2}{2EI_0} + C2 \tag{32}$$

$$x = 0, y = 0, C2 = 0 \tag{33}$$

$$y(x) = -\frac{PLx^2}{2EI_0} \tag{34}$$

A.3 Reverse Tapered Cantilever

This section derives the elastic curve of a cantilever with a linearly increasing width (from anchor to tip) and a constant thickness.

$$M(x) = -P(L-x) \tag{35}$$

$$I(x) = \frac{I_0(L+x)}{L} \tag{36}$$

$$\frac{d^2y}{dx^2} = \frac{M(x)}{EI(x)} \tag{37}$$

$$= \frac{-P(L-x)L}{EI_0(L+x)} \tag{38}$$

$$\frac{dy}{dx} = -\frac{PL}{EI_0}\left[2L \cdot ln(x+L) - x\right] + C1 \tag{39}$$

$$x = 0, \frac{dy}{dx} = 0, \tag{40}$$

$$C1 = L - 2L \cdot ln(L) \tag{41}$$

$$\frac{dy}{dx} = -\frac{PL}{EI_0}\Bigg\{ \left[2L \cdot ln(x+L) - x\right] \tag{42}$$

$$+ \left[L - 2L \cdot ln(L)\right] \Bigg\} \tag{43}$$

$$\frac{dy}{dx} = -\frac{PL}{EI_0}\Bigg\{2L \cdot \left[(x+L) \cdot ln(x+L) - x - L\right] - \frac{x^2}{2} \tag{44}$$

$$+ \left[L - 2L \cdot ln(L)\right] x + C2\Bigg\} \tag{45}$$

$$x = 0, y = 0, \tag{46}$$

$$C2 = -2L(L \cdot ln(L) - L^2) \tag{47}$$

$$\frac{dy}{dx} = -\frac{PL}{EI_0}\Bigg\{2L \cdot \left[(x+L) \cdot ln(x+L) - x - L\right] - \frac{x^2}{2} \tag{48}$$

$$+ \left[L - 2L \cdot ln(L)\right] x \tag{49}$$

$$- 2L(L \cdot ln(L) - L^2)\Bigg\} \tag{50}$$

REFERENCES

[1] Meindl, J., "Low power microelectronics: retrospect and prospect," *Proceedings of the IEEE*, vol. 83, pp. 619–635, Apr 1995.

[2] Knickerbocker, J., Andry, P., Buchwalter, L. P., Colgan, E., Cotte, J., Gan, H., Horton, R., Sri-Jayantha, S., Magerlein, J., Manzer, D., McVicker, G., Patel, C. S., Polastre, R., Sprogis, E. S., Tsang, C. K., Webb, B., and Wright, S., "System-on-package (sop) technology, characterization and applications," in *IEEE Proceedings of 56th Electronic Components and Technology Conference (ECTC)*, pp. 7 pp.–, 2006.

[3] Dickson, T., Liu, Y., Rylov, S., Dang, B., Tsang, C., Andry, P., Bulzacchelli, J., Ainspan, H., Gu, X., Turlapati, L., Beakes, M., Parker, B., Knickerbocker, J., and Friedman, D., "An 8x10-gb/s source-synchronous I/O system based on high-density silicon carrier interconnects," *IEEE Journal of Solid-State Circuits*, vol. 47, pp. 884–896, Apr. 2012.

[4] Dorsey, P., "Xilinx stacked silicon interconnect technology delivers breakthrough fpga capacity, bandwidth, and power efficiency," *Xilinx White Paper: Virtex-7 FPGAs*, pp. 1–10, 2010.

[5] Rahman, A., Schulz, J., Grenier, R., Chanda, K., Lee, M., Ratakonda, D., Shi, H., Li, Z., Chandrasekar, K., Xie, J., and Ibbotson, D., "Interconnection requirements and multi-die integration for fpgas," in *IEEE 2013 International Interconnect Technology Conference (IITC)*, pp. 1–3, June 2013.

[6] Shubin, I., Chow, E., Chow, A., De Bruyker, D., Thacker, H., Fujimoto, K., Raj, K., Krishnamoorthy, A., Mitchell, J., and Cunningham, J., "Package demonstration of an interposer with integrated tsvs and flexible compliant interconnects," in *IEEE Proceedings of 63rd Electronic Components and Technology Conference (ECTC)*, (Las Vegas, NV, USA), May 2013.

[7] Krishnamoorthy, A., Ho, R., Zheng, X., Schwetman, H., Lexau, J., Koka, P., Li, G., Shubin, I., and Cunningham, J., "Computer systems based on silicon photonic interconnects," *Proceedings of the IEEE*, vol. 97, pp. 1337–1361, July 2009.

[8] Polka, L. A., "Package technology to address the memory bandwidth challenge for terascale computing," *Intel Technology Journal*, vol. 11, Aug. 2007.

[9] Bowman, K., Alameldeen, A., Srinivasan, S., and Wilkerson, C., "Impact of die-to-die and within-die parameter variations on the clock frequency and

throughput of multi-core processors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, pp. 1679–1690, Dec. 2009.

[10] Zhang, C., Zia, M., Thadesar, P., Yang, H., and Bakir, M., "Fabrication and characterization of bridged multi-interposer system featuring double-sided mechanically flexible interconnects, through silicon vias and positive self alignment structures." Submitted to IEEE International Electron Device Meeting (IEDM) 2014, 2014.

[11] Cho, H., Kapur, P., and Saraswat, K., "Power comparison between high-speed electrical and optical interconnects for inter-chip communication," in *Interconnect Technology Conference, 2004. Proceedings of the IEEE 2004 International*, pp. 116–118, June 2004.

[12] Thacker, H., Shubin, I., Luo, Y., Costa, J., Lexau, J., Zheng, X., Li, G., Yao, J., Li, J., Patil, D., Liu, F., Ho, R., Feng, D., Asghari, M., Pinguet, T., Raj, K., Mitchell, J., Krishnamoorthy, A., and Cunningham, J., "Hybrid integration of silicon nanophotonics with 40nm-cmos vlsi drivers and receivers," in *IEEE Proceedings of 61st Electronic Components and Technology Conference (ECTC)*, pp. 829–835, 2011.

[13] Li, G., Zheng, X., Lexau, J., Luo, Y., Thacker, H., Pinguet, T., Dong, P., Feng, D., Liao, S., Shafiiha, R., Asghari, M., Yao, J., Shi, J., Shubin, I. N., Patil, D., Liu, F., Raj, K., Ho, R., Cunningham, J. E., and Krishnamoorthy, A. V., "Ultralow-power silicon photonic interconnect for high-performance computing systems," in *Proceedings of SPIE*, vol. 7607, pp. 760703–760703–15, 2010.

[14] Zheng, X., Liu, F. Y., Lexau, J., Patil, D., Li, G., Luo, Y., Thacker, H. D., Shubin, I., Yao, J., and Raj, K., "Ultralow power 80 Gb/s arrayed CMOS silicon photonic transceivers for WDM optical links," *Journal of Lightwave Technology*, vol. 30, no. 4, pp. 641–650, 2012.

[15] Yao, J., Zheng, X., Li, G., Shubin, I., Thacker, H., Luo, Y., Raj, K., Cunningham, J., and Krishnamoorthy, A., "Grating-coupler based low-loss optical interlayer coupling," in *IEEE 8th International Conference on Group IV Photonics (GFP)*, pp. 383–385, September 2011.

[16] Majumdar, A., Cunningham, J. E., and Krishnamoorthy, A. V., "Alignment and performance considerations for capacitive, inductive, and optical proximity communication," *IEEE Transactions on Advanced Packaging*, vol. 33, no. 3, pp. 690–701, 2010.

[17] Yang, H. S., Thacker, H., Shubin, I., Cunningham, J., and Mitchell, J., "Assembly and alignment of proximity communication enabled multi-chip packages using elastomeric bump interposers," in *IEEE Proceedings of 62nd Electronic Components and Technology Conference (ECTC)*, pp. 2029–2035, May 2012.

[18] Wu, J., Del Alamo, J., and Jenkins, K., "A high aspect-ratio silicon substrate-via technology and applications: through-wafer interconnects for power and ground and faraday cages for soc isolation," in *IEEE International Electron Device Meeting (IEDM)*, pp. 477–480, Dec 2000.

[19] Neysmith, J. and Baldwin, D., "Modular, device-scale, direct-chip-attach packaging for microsystems," *IEEE Transactions on Components and Packaging Technologies*, vol. 24, pp. 631–634, Dec 2001.

[20] Chow, E., Chandrasekaran, V., Partridge, A., Nishida, T., Sheplak, M., Quate, C. F., and Kenny, T., "Process compatible polysilicon-based electrical through-wafer interconnects in silicon substrates," *Journal of Microelectromechanical Systems*, vol. 11, pp. 631–640, Dec 2002.

[21] Mehra, A., Zhang, X., Ayón, A. A., Waitz, I. A., and Schmidt, M. A., "Through-wafer electrical interconnect for multilevel microelectromechanical system devices," *Journal of Vacuum Science and Technology B*, vol. 18, no. 5, pp. 2583–2589, 2000.

[22] Tsang, C. K., Andry, P. S., Sprogis, E. J., Patel, C. S., Webb, B. C., Manzer, D. G., and Knickerbocker, J. U., "CMOS-compatible through silicon vias for 3-D process integration," in *Materials Research Society Symposium Proceedings*, vol. 970, p. 145, 2007.

[23] Patel, C. S., Tsang, C. K., Schuster, C., Doany, F. E., Nyikal, H., Baks, C. W., Budd, R., Buchwalter, L. P., Andry, P. S., Canaperi, D. F., and others, "Silicon carrier with deep through-vias, fine pitch wiring and through cavity for parallel optical transceiver," in *IEEE Proceedings of 55th Electronic Components and Technology Conference (ECTC)*, pp. 1318–1324, 2005.

[24] Schaper, L., Burkett, S., Spiesshoefer, S., Vangara, G., Rahman, Z., and Polamreddy, S., "Architectural implications and process development of 3-D VLSI z-axis interconnects using through silicon vias," *IEEE Transactions on Advanced Packaging*, vol. 28, pp. 356–366, Aug. 2005.

[25] Song, C., Wang, Z., Chen, Q., Cai, J., and Liu, L., "High aspect ratio copper through-silicon-vias for 3D integration," *Microelectronic Engineering*, vol. 85, no. 10, pp. 1952–1956, 2008.

[26] Sunohara, M., Sakaguchi, H., Takano, A., Arai, R., Murayama, K., and Higashi, M., "Studies on electrical performance and thermal stress of a silicon interposer with TSVs," in *IEEE Proceedings of 60th Electronic Components and Technology Conference (ECTC)*, (Las Vegas, NV, USA), pp. 1088–1093, June 2010.

[27] Bakir, M. S. and Meindl, J. D., *Integrated interconnect technologies for 3D nanoelectronic systems*. Artech House Publishers, 1 ed., Nov. 2008.

[28] Tang, G. Y., Tan, S. P., Khan, N., Pinjala, D., Lau, J., Yu, A. B., Vaidyanathan, K., and Toh, K. C., "Integrated liquid cooling systems for 3-d stacked TSV modules," *IEEE Transactions on Components and Packaging Technologies*, vol. 33, pp. 184–195, Mar. 2010.

[29] Ayazi, F., Chen, H. H., Kocer, F., He, G., and Najafi, K., "A high aspect-ratio polysilicon vibrating ring gyroscope," in *Proceedings of Solid-state Sensor and Actuator Workshop*, pp. 4–8, 2000.

[30] Lishchynska, M., O'Mahony, C., Slattery, O., Wittler, O., and Walter, H., "Evaluation of packaging effect on MEMS performance: simulation and experimental study," *IEEE Transactions on Advanced Packaging*, vol. 30, pp. 629–635, Nov. 2007.

[31] Jueping, C., Peng, J., Lei, Y., Yue, H., and Zan, L., "Through-silicon via (tsv) capacitance modeling for 3d noc energy consumption estimation," in *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, pp. 815–817, Nov 2010.

[32] Bandyopadhyay, T., Han, K. J., Chung, D., Chatterjee, R., Swaminathan, M., and Tummala, R., "Rigorous electrical modeling of through silicon vias (tsvs) with mos capacitance effects," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 1, pp. 893–903, June 2011.

[33] Leung, L. and Chen, K., "Microwave characterization and modeling of high aspect ratio through-wafer interconnect vias in silicon substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 2472–2480, Aug. 2005.

[34] Thacker, H., *Probe modules for wafer-level testing of gigascale chips with electrical and optical I/O interconnects*. PhD Thesis, Georgia Institute of Technology, 2006.

[35] Lai, J. H., Yang, H. S., Chen, H., King, C. R., Zaveri, J., Ravindran, R., and Bakir, M. S., "A 'mesh' seed layer for improved through-silicon-via fabrication," *Journal of Micromechanics and Microengineering*, vol. 20, p. 025016, Feb. 2010.

[36] Cheramy, S., Charbonnier, J., Henry, D., Astier, A., Chausse, P., Neyret, M., Brunet-Manquat, C., Verrun, S., Sillon, N., Bonnot, L., Gagnard, X., and Vittu, J., "3d integration process flow for set-top box application: description of technology and electrical results," in *European Microelectronics and Packaging Conference (EMPC)*, pp. 1–6, June 2009.

[37] Zahorian, J., *Fabrication technology and design for CMUTs on cmos for IVUS catheters*. PhD Thesis, Georgia Institute of Technology, 2013.

[38] Nikoozadeh, A., Oralkan, O., Gencel, M., Choe, J. W., Stephens, D., de la Rama, A., Chen, P., Lin, F., Dentinger, A., Wildes, D., Thomenius, K., Shivkumar, K., Mahajan, A., Seo, C. H., O'Donnell, M., Truong, U., Sahn, D., and Khuri-Yakub, P., "Forward-looking intracardiac imaging catheters using fully integrated cmut arrays," in *IEEE Ultrasonics Symposium (IUS)*, pp. 770–773, Oct 2010.

[39] Stucchi, M., Perry, D., Katti, G., and Dehaene, W., "Test structures for characterization of through silicon vias," in *Microelectronic Test Structures (ICMTS), 2010 IEEE International Conference on*, pp. 130–134, March 2010.

[40] Thadesar, P. and Bakir, M., "Novel photo-defined polymer-enhanced through-silicon vias for silicon interposers," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 3, pp. 1130–1137, July 2013.

[41] Campo, A. d. and Greiner, C., "SU-8: a photoresist for high-aspect-ratio and 3D submicron lithography," *Journal of Micromechanics and Microengineering*, vol. 17, pp. R81–R95, May 2007.

[42] Zhang, Y., King, C., Zaveri, J., Kim, Y., Sahu, V., Joshi, Y., and Bakir, M., "Coupled electrical and thermal 3D IC centric microfluidic heat sink design and technology," in *IEEE Proceedings of 61st Electronic Components and Technology Conference (ECTC)*, pp. 2037–2044, 2011.

[43] Pak, J. S., Ryu, C., and Kim, J., "Electrical characterization of through silicon via (TSV) depending on structural and material parameters based on 3D full wave simulation," in *Proceedings of International Conference on Electronic Materials and Packaging (EMAP)*, (Daejeon, South Korea), pp. 1–6, Nov. 2007.

[44] Liu, X., Chen, Q., Sundaram, V., Simmons-Matthews, M., Wachtler, K., Tummala, R., and Sitaraman, S., "Thermo-mechanical behavior of through silicon vias in a 3D integrated package with inter-chip microbumps," in *IEEE Proceedings of 61st Electronic Components and Technology Conference (ECTC)*, pp. 1190–1195, 2011.

[45] Reed, H. A., Bakir, M. S., Patel, C. S., Martin, K. P., Meindl, J. D., and Kohl, P. A., "Compliant wafer level package (CWLP) with embedded air-gaps for sea of leads (SoL) interconnections," in *IEEE 2001 International Interconnect Technology Conference (IITC)*, pp. 151–153, June 2001.

[46] Kacker, K., Lo, G. C., and Sitaraman, S. K., "Low-k dielectric compatible wafer-level compliant chip-to-substrate interconnects," *IEEE Transactions on Advanced Packaging*, vol. 31, no. 1, pp. 22–32, 2008.

[47] Kacker, K. and Sitaraman, S. K., "Design and fabrication of FlexConnects: a cost-effective implementation of compliant chip-to-substrate interconnects," *IEEE Transactions on Components and Packaging Technologies*, vol. 31, pp. 816–823, Dec. 2008.

[48] Kacker, K. and Sitaraman, S., "Electrical/mechanical modeling, reliability assessment, and fabrication of flexconnects: a MEMS-based compliant chip-to-substrate interconnect," *Journal of Microelectromechanical Systems*, vol. 18, pp. 322–331, Apr. 2009.

[49] Zhu, Q., Ma, L., and Sitaraman, S., "Beta-helix: a lithography-based compliant off-chip interconnect," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, pp. 582 – 590, sept. 2003.

[50] Gere, J. M., *Mechanics of materials*. Toronto: Cengage Learning,, 7th ed. ed., 2009.

[51] Zhang, C., Yang, H. S., and Bakir, M. S., "Mechanically flexible interconnects (mfis) with highly scalable pitch," *Journal of Micromechanics and Microengineering*, vol. 24, no. 5, p. 055024, 2014.

[52] Schift, H., Spreu, C., Schleunitz, A., and Lee, J., "Shape control of polymer reflow structures fabricated by nanoimprint lithography," *Microelectronic Engineering*, vol. 88, pp. 87–92, Jan. 2011.

[53] Fadda, E., "Bake mechanisms in novolak-based photoresist films: investigation by contact angle measurements," in *Proceedings of SPIE*, (Santa Clara, CA, USA), pp. 460–468, 1996.

[54] Hale, A., Macosko, C. W., and Bair, H. E., "Glass transition temperature as a function of conversion in thermosetting polymers," *Macromolecules*, vol. 24, no. 9, pp. 2610–2621, 1991.

[55] Sueoka, K., Kohara, S., Horibe, A., Yamada, F., Mori, H., and Orii, Y., "Fine-pitch solder joining for high density interconnection," in *International Conference on Electronics Packaging (ICEP)*, pp. 600–603, April 2014.

[56] Ohyama, M., Mizuno, J., Shoji, S., Nimura, M., Nonaka, T., Shinba, Y., and Shigetou, A., "Fine-pitch hybrid bonding with cu/sn microbumps and adhesive for high density 3d integration," in *International Conference on Electronics Packaging (ICEP)*, pp. 604–607, April 2014.

[57] Timurdogan, E., Sorace-Agaskar, C. M., Hosseini, E. S., and Watts, M. R., "An interior-ridge silicon microring modulator," *Journal of Lightwave Technology*, vol. 31, pp. 3907–3914, Dec 2013.

[58] Manipatruni, S., Chen, L., and Lipson, M., "Ultra high bandwidth wdm using silicon microring modulators," *Optics Express*, vol. 18, pp. 16858–16867, Aug 2010.

[59] Manipatruni, S., Lipson, M., and Young, I., "Device scaling considerations for nanophotonic cmos global interconnects," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, pp. 8200109–8200109, March 2013.

[60] Krishnamoorthy, A., Cunningham, J., Zheng, X., Shubin, I., Simons, J., Feng, D., Liang, H., Kung, C.-C., and Asghari, M., "Optical proximity communication with passively aligned silicon photonic chips," *IEEE Journal of Quantum Electronics*, vol. 45, pp. 409–414, April 2009.

[61] Panasonic Corporation of North America, *Panasonic BM123-133 Flyer*. [Online document], http://www.panasonicfa.com/pdfs/BM123-133.pdf, 2012.

[62] Panasonic Corporation of North America, *Panasonic FCB3 Flyer*. [Online document], http://www.panasonicfa.com/pdfs/FCB3.pdf, 2012.

[63] Zheng, X., Cunningham, J. E., Shubin, I., Simons, J., Asghari, M., Feng, D., Lei, H., Zheng, D., Liang, H., chih Kung, C., Luff, J., Sze, T., Cohen, D., and Krishnamoorthy, A. V., "Optical proximity communication using reflective mirrors," *Optics Express*, vol. 16, pp. 15052–15058, Sep 2008.

[64] Krishnamoorthy, A., Stephen, C., Cunningham, J., and Mitchell, J., "Chip package with reinforced positive alignment features," Feb. 25 2014. US Patent 8,659,161.

[65] Shubin, I., Chow, A., Popovic, D., Thacker, H., Giere, M., Hopkins, R., Krishnamoorthy, A. V., Mitchell, J. G., and Cunningham, J. E., "A novel MCM package enabling proximity communication IO," in *IEEE Proceedings of 61st Electronic Components and Technology Conference (ECTC)*, pp. 224–229, 2011.

[66] Sun, F., Leblebici, Y., and Brunschwiler, T., "Surface-tension-driven multi-chip self-alignment techniques for heterogeneous 3D integration," in *IEEE Proceedings of 61st Electronic Components and Technology Conference (ECTC)*, pp. 1153–1159, 2011.

[67] Ito, Y., Fukushima, T., Lee, K. W., and Choki, K., "Flux-assisted self-assembly with microbump bonding for 3D heterogeneous integration," in *IEEE Proceedings of 63rd Electronic Components and Technology Conference (ECTC)*, May 2013.

[68] Cunningham, J. E., Krishnamoorthy, A. V., Ho, R., Shubin, I., Thacker, H., Lexau, J., Lee, D. C., Feng, D., Chow, E., and Luo, Y., "Integration and packaging of a macrochip with silicon nanophotonic links," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 17, no. 3, pp. 546–558, 2011.

[69] Chiang, K. N. and Yuan, C. A., "An overview of solder bump shape prediction algorithms with validations," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 158–162, 2001.

[70] Brigham Young University, *KOH etching of silicon 100 45% KOH Solution.* [Online document], http://www.cleanroom.byu.edu/KOH.phtml.

[71] Drost, R., Hopkins, R., Ho, R., and Sutherland, I., "Proximity communication," *Solid-State Circuits, IEEE Journal of*, vol. 39, pp. 1529–1535, Sept 2004.

[72] Sze, T., Giere, M., Guenin, B., Nettleton, N., Popovic, D., Shi, J., Bezuk, S., Ho, R., Drost, R., and Douglas, D., "Proximity communication flip-chip package with micron chip-to-chip alignment tolerances," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, pp. 966–971, May 2009.

[73] Cunningham, J., Krishnamoorthy, A., Shubin, I., Zheng, X., Asghari, M., Feng, D., and Mitchell, J., "Aligning chips face-to-face for dense capacitive and optical communication," *Advanced Packaging, IEEE Transactions on*, vol. 33, pp. 389–397, May 2010.

[74] Krishnamoorthy, A., Goossen, K., Jan, W., Zheng, X., Ho, R., Li, G., Rozier, R., Liu, F., Patil, D., Lexau, J., Schwetman, H., Feng, D., Asghari, M., Pinguet, T., and Cunningham, J., "Progress in low-power switched optical interconnects," *Selected Topics in Quantum Electronics, IEEE Journal of*, vol. 17, pp. 357–376, March 2011.

[75] Shubin, I., Chow, E., Cunningham, J., De Bruyker, D., Chua, C., Cheng, B., Knights, J. C., Sahasrabuddhe, K., Luo, Y., Chow, A., Simons, J., Krishnamoorthy, A., Hopkins, R., Drost, R., Ho, R., Douglas, D., and Mitchell, J., "Novel packaging with rematable spring interconnect chips for mcm," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, pp. 1053–1058, May 2009.

[76] Doyle, B. J., Corbett, T. J., Cloonan, A. J., O'Donnell, M. R., Walsh, M. T., Vorp, D. A., and McGloughlin, T. M., "Experimental modelling of aortic aneurysms: Novel applications of silicone rubbers," *Medical Engineering & Physics*, vol. 31, no. 8, pp. 1002 – 1012, 2009.

[77] Yang, H. S. and Bakir, M. S., "Design, fabrication, and characterization of freestanding mechanically flexible interconnects using curved sacrificial layer," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2012.

[78] Lee, K.-W., Kanno, S., Kiyoyama, K., Fukushima, T., Tanaka, T., and Koyanagi, M., "A cavity chip interconnection technology for thick mems chip integration in mems-lsi multichip module," *Microelectromechanical Systems, Journal of*, vol. 19, pp. 1284–1291, Dec 2010.

[79] Fukushima, T., Iwata, E., Konno, T., Bea, J.-C., Lee, K.-W., Tanaka, T., and Koyanagi, M., "Surface tension-driven chip self-assembly with load-free hydrogen fluoride-assisted direct bonding at room temperature for three-dimensional integrated circuits," *Applied Physics Letters*, vol. 96, no. 15, pp. –, 2010.

[80] Chen, Q., Zhang, D., Xu, Z., Beece, A., Patti, R., Tan, Z., Wang, Z., Liu, L., and Lu, J.-Q., "A novel chip-to-wafer (c2w) three-dimensional (3d) integration approach using a template for precise alignment," *Microelectronic Engineering*, vol. 92, no. 0, pp. 15 – 18, 2012. 27th Annual Advanced Metallization Conference 2010 27th Annual Advanced Metallization Conference 2010.

[81] Yang, H. S., Zhang, C., and Bakir, M. S., "Self-aligned silicon interposers tiles and silicon bridges using positive self alignment structures and rematable mechanically flexible interconnects," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 2014.

[82] Yang, H. S., Zhang, C., and Bakir, M. S., "Self-alignment structures for heterogeneous 3D integration," in *IEEE Proceedings of 63rd Electronic Components and Technology Conference (ECTC)*, May 2013.

[83] Thacker, H., Luo, Y., Shi, J., Shubin, I., Lexau, J., Zheng, X., Li, G., Yao, J., Costa, J., Pinguet, T., Mekis, A., Dong, P., Liao, S., Feng, D., Asghari, M., Ho, R., Raj, K., Mitchell, J., Krishnamoorthy, A., and Cunningham, J., "Flip-chip integrated silicon photonic bridge chips for sub-picojoule per bit optical links," in *IEEE Proceedings of 60th Electronic Components and Technology Conference (ECTC)*, pp. 240–246, June 2010.

[84] Bakir, M. S., Thadesar, P. A., King, C., Zaveri, J., Yang, H. S., Zhang, C., and Zhang, Y., "Revolutionary innovation in system interconnection: a new era for the IC," in *Proceedings of SPIE* (Garcia-Blanco, S. and Ramesham, R., eds.), vol. 7928, p. 792803, SPIE, 2011.