SILICON MICROSYSTEM PLATFORM WITH INTEGRATED MICROFLUIDIC COOLING AND LOW-LOSS THROUGH-SILICON VIAS

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Hanju Oh

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SILICON MICROSYSTEM PLATFORM WITH INTEGRATED MICROFLUIDIC COOLING AND LOW-LOSS THROUGH-SILICON VIAS

Approved by:

Dr. Muhannad S. Bakir, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Madhavan Swaminathan
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Gary S. May, Co-advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Hua Wang
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Suresh K. Sitaraman
The George W. Woodruff School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: March 28, 2017

Dedicated to my parents, Jin Hwa Lee and Kwang Je Oh,

and brother, Soong Ju Oh,

for their endless love and support.

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LIST OF SYMBOLS AND ABBREVIATIONS

ABF	Ajinomoto build-up film
ADS	Advanced Design System
ARDE	Aspect-Ratio-Dependent-Etching
BEOL	Back-End-Of-Line
CMP	Chemical Mechanical Polishing
CIS	CMOS Image Sensor
CPW	Coplanar Waveguide
DRIE	Deep Reactive Ion Etching
FEOL	Front-End-Of-Line
FPGA	Field-Programmable Gate Array
GS	Ground-Signal
GSG	Ground-Signal-Ground
HBM	High Bandwidth Memory
HFSS	High-Frequency Structure Simulator
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors

PVD	Physical Vapor Deposition
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PPC	Propylenecarbonate
RF	Radio-Frequency
RDL	Redistribution Layers
RLCG	Resistance, Inductance, Capacitance, and Conductance
SACVD	Sub-Atomic Chemical Vapor Deposition
TSV	Through-Silicon Via

SUMMARY

Microfluidic cooling technology is a promising thermal solution for high-performance three-dimensional (3-D) microsystems. However, the integration of microfluidic cooling into 3-D microsystems inevitably impacts tier-to-tier through-silicon vias (TSVs) by increasing their length and diameter (for a fixed aspect ratio). To address this challenge, we present the fabrication of very high-aspect ratio (23:1) TSVs within a microfluidic pin-fin heat sink using two types of silicon etch masks. Void-free TSVs are electrically characterized using X-ray inspection and four-point resistance measurements. Moreover, the impact of liquid cooling on the electrical characteristics of TSVs is analyzed using a microfluidic cooling testbed containing TSVs. The micro-fabrication of TSVs in a silicon micropin-fin heat sink is presented, and the high-frequency characterization of TSVs within deionized water is performed from 10 MHz to 20 GHz. TSV capacitance and conductance are extracted from measurements; TSVs within deionized water have larger capacitances and conductances than TSVs in silicon due to the lossy characteristics of deionized water at high frequencies.

To reduce high-frequency losses in silicon interposers, an air-isolated TSV technique is proposed. A testbed containing air-isolated and conventional TSVs is fabricated and characterized from 10 MHz to 20 GHz with an L-2L de-embedding technique. The proposed air-isolated TSV technique yields 46.7% lower insertion loss compared to conventional TSVs at 20 GHz from 3D full-wave simulations and measurements. Moreover, the impact of the air-isolation region width between TSVs on capacitance and conductance is quantified.

CHAPTER 1

BACKGROUND AND INTRODUCTION TO 3-D MICROSYSTEMS AND MICROFLUIDIC COOLING

1.1 Motivation

Demand for high-bandwidth communication with low energy consumption continues to grow in modern computing systems [1],[2]. Through innovations in materials, processes, and structures, integrated circuit (IC) technology has rapidly evolved – transistor count has increased by a factor of 16,000, and gate speed has increased by a factor of 100 since the mid-1980s [2],[3], as illustrated in Figure 1. Along with such efforts, the need for revolutionary innovation in system integration has become necessary to overcome the limitations of traditional packaging [4]. Moreover, chip-to-chip communication has emerged as a key bottleneck that limits total system performance. To address these needs, heterogeneous integrated microsystems in which multiple (and differing) dice are integrated within a single package have been proposed [5],[6]. Some of the proposed integrated microsystems include the vertical stacking of dice, i.e., 3-D integration, and the side-by-side bonding of chips on a substrate with dense interconnects, termed 2.5-D integration.

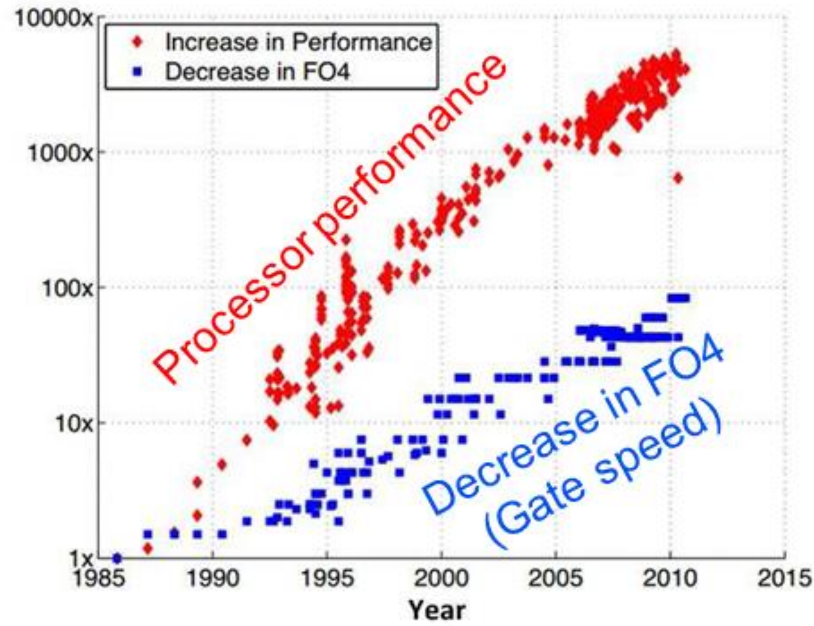
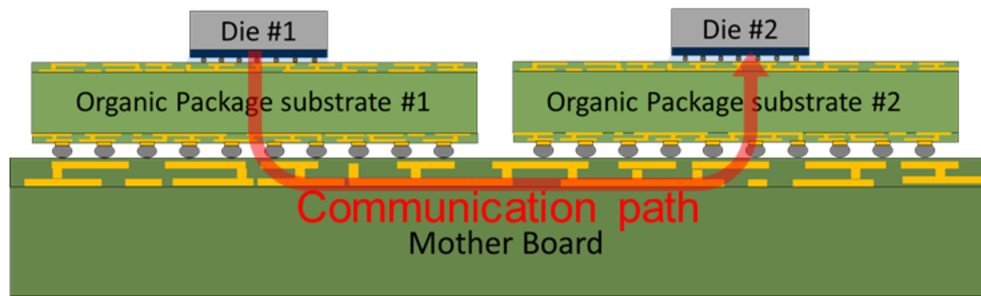


Figure 1. Semiconductor advances in processor performance and gate speed [2].

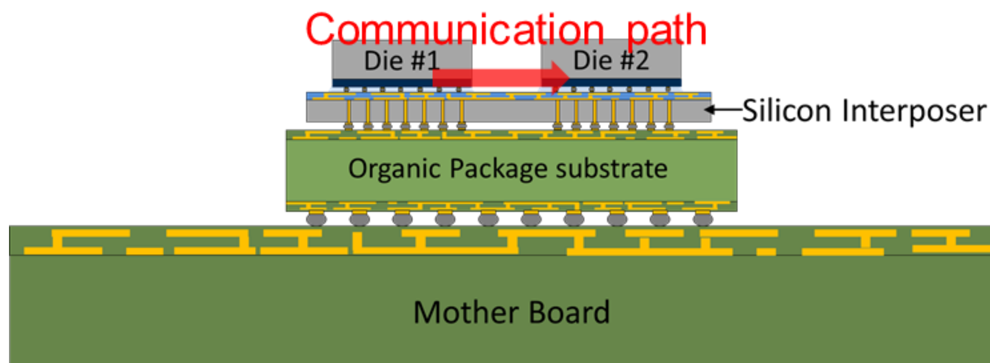
1.1.1 Demand for High-Bandwidth Off-Chip Communication

As IC technology has continued to advance in the past few decades, off-chip communication, or chip-to-chip interconnets, have become a key limiting factor to system performance and energy dissipation [4]. To address this challenge, silicon interposers with high-density interconnects have been widely explored to obtain high-bandwidth chip-to-chip communication [7],[8]. Figure 2 illustrates chip-to-chip communication paths using a conventional package (Figure 2a) and using a silicon interposer (Figure 2b). Moreover, the advantages of silicon interposers include the integration of heterogeneous technologies such as logic, memory, field-programmable gate array (FPGA), and passives yielding compact high-performance systems. Silicon interposers enable the fabrication of denser lateral metallization between stacked chips on the interposer compared to conventional substrates, such as organic or ceramic materials

[4]. Xilinx has demonstrated two or more FPGA chips stacked on a silicon interposer using TSMC 65 nm process with TSVs [8]. Altera and TSMC announced a 3-D microsystem test vehicle using silicon interposers for high-bandwidth and low-power intra-package chip-to-chip interfaces [9]. IBM demonstrated a silicon interposer with stacked transceivers with the characterization of an 8 × 10 Gb/s synchronous communication [10].



(a)



(b)

Figure 2. Chip-to-chip communication path using (a) a conventional package and (b) a silicon interposer.

1.1.2 Through-Silicon Via Technology for Heterogeneous Integrated Microsystems

A through-silicon via (TSV) is a vertical interconnect that transfers electrical signals from one side of a silicon substrate to another for 3-D microsystems [11], [12]. Figure 3 illustrates the basic concept of 3-D microsystem with TSVs; each tier consists of conductive material surrounded by an insulator within a silicon substrate. In general, the fabrication of a TSV begins by etching a silicon substrate. Next, the etched via holes are filled with a conductive material such as copper, tungsten or conductive paste. The side walls of the via holes are then covered with a dielectric, such as silicon dioxide, polymer or multiple dielectrics. Despite the simple structure of a TSV, there are significant numbers of variables including silicon resistivity, conductive material, liner material, and TSV dimensions (diameter, pitch, and height) that must be properly chosen to meet desired electrical characteristics.

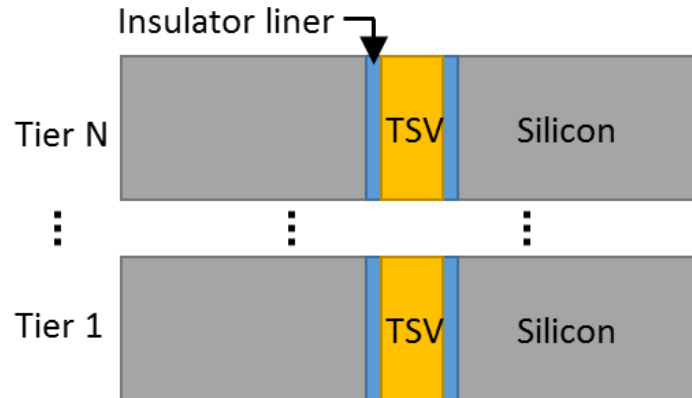


Figure 3. Schematic of stacked silicon dice using through-silicon vias (TSVs) for 3-D microsystem applications.

According to the International Technology Roadmap for Semiconductors (ITRS), depending on the order of TSV fabrication with respect to IC fabrication, TSV fabrication can be categorized in three ways: TSV-first, TSV-middle, and TSV-last processes [13]. As the names indicate, the TSV-first process begins with the fabrication of TSVs prior to the IC fabrication. The TSV-middle process fabricates TSVs after the front-end-of-line (FEOL) step and before the back-end-of-line (BEOL) step of IC fabrication. The TSV-last process firstly fabricates the FEOL and BEOL devices, followed by TSV fabrication.

The advantages of TSVs include high-bandwidth communication with greatly reduced routing lengths between dice. Moreover, they contribute to system miniaturization by geometrically integrating dice within the same footprint. For these reasons, TSV technology has been adopted in a number of applications that include CMOS image sensors (CIS), which are a representative high volume-manufactured application [14],[15]. In 2009, Samsung announced 3D DDR3 DRAM stacking using TSV technology [16]. In their paper, 300 TSVs are fabricated within 10.9 x 9.0 mm^2 dice using two TSV pitches of 40 and 60 µm, respectively. SK Hynix announced the production of high bandwidth memory (HBM) DRAM chip modules using 3D TSV technology. Xilinx has demonstrated and produced two or more FPGA chips side-by-side on a silicon interposer using the TSMC 65 nm process with TSVs.

1.1.3 Silicon Microsystems with Integrated Microfluidic Cooling

From the above discussion, it is clear that TSV technology has been the focus of significant recent research, including studies that seek to improve the electrical and/or thermomechanical performance of TSVs by including atypical materials in a CMOS process flow or atypical configurations. In this work, we refer to such TSVs as non-

traditional TSVs. First, the integration of microfluidic cooling with TSVs has been proposed for various heterogeneous integrated microsystems [17]-[24]. Thermal management is one of the critical issues for 3-D integrated microsystems because they can exhibit relatively large heat flux [25]. With its effective cooling capability, microfluidic cooling has been explored as a promising solution to heat rejection. Recently, the monolithic integration of microfluidic cooling on the back side of an FPGA has been demonstrated, and measurements suggest improved performance compared to air cooling [18].

Figure 4 illustrates three heterogeneous integrated microsystems with two cooling technologies (air and microfluidic). In Figure 4(a), the logic and the memory dice are bonded side-by-side in a 2.5-D configuration with an air-cooled heat sink. Figure 4 (b) illustrates the integration of microfluidic cooling within a silicon interposer. Because microfluidic cooling offers a number of benefits compared to air cooling, significant reduction in junction temperature is expected in such systems. Figure 4 (c) illustrates a heterogeneous 3-D microsystem in which logic and memory dice are stacked on top of each other, with integrated microfluidic cooling. Such a 3-D stack can further improve bandwidth, latency, and I/O power because it provides the shortest interconnect lengths between chips. However, the 3-D stack has the highest integration complexity among the microsystems in the figure.

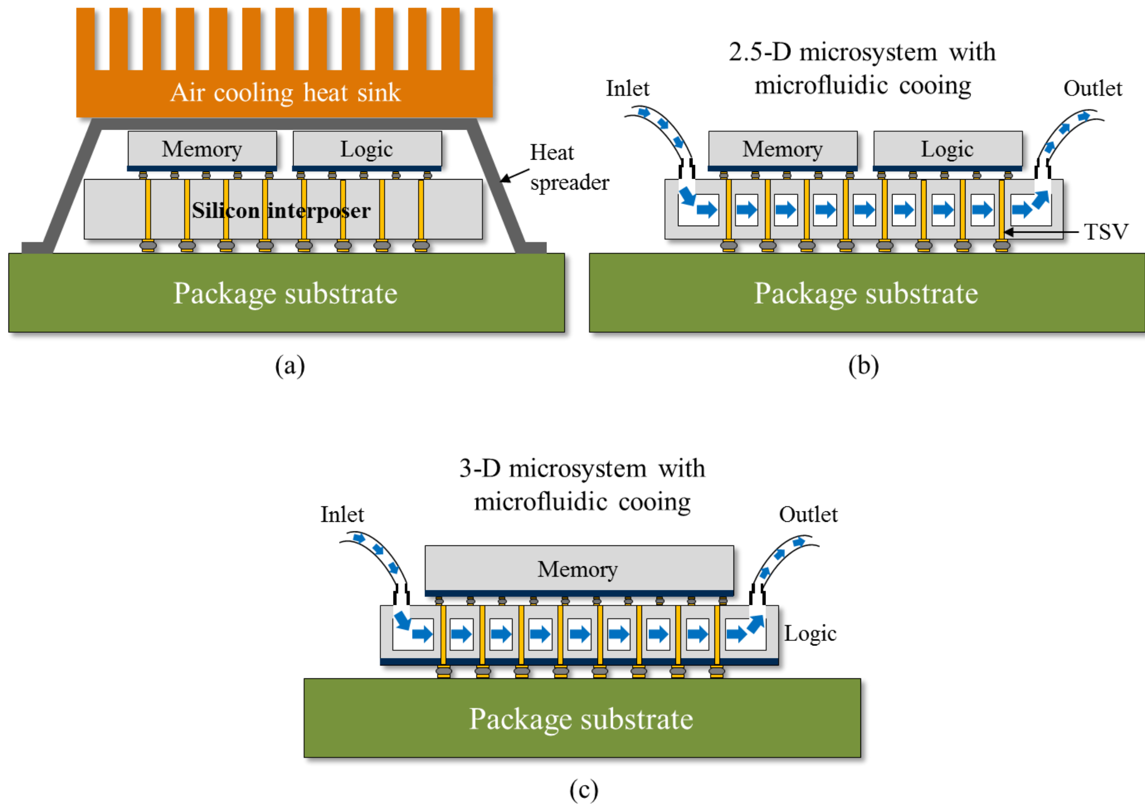


Figure 4. Three types of heterogeneous integrated microsystems: (a) 2.5-D integration using silicon interposer with conventional air cooling technology, (b) 2.5-D integration using silicon interposer with embedded microfluidic cooling technology, and (c) 3-D integration with embedded microfluidic cooling technology.

Due to advancements in microfabrication, more 'complex' microstructures for improved heat sink performance have been fabricated and these may outshine the performance of the plain microchannels proposed in [26]. Examples of more complex microfluidic heat sink structures include enhanced microchannels [27], in-line micropin-fins [28],[29], staggered micropin-fins [30], and pearl chains [28] etc. Among the various heat sink designs, the micropin-fin heat sink design has been of interest since it offers a large contact area with the coolant compared to other heat sink structures. Table 1

summarizes some of the micropin-fin heat sink designs used in the literature along with their performance. However, none of the aforementioned designs take into account the electrical and microfabrication constraints that TSVs impose on microfluidic cooling.

Table 1. Geometry and specification of a micropin-fin heat sink used in the literature.

Literature	Heat sink diameter [μm]	Heat sink height [μm]	Thermal resistance* [K/W]	Pressure drop [kPa]
Peles et al. [31]	100 / 243	243	5 ~ 6	14.7
Kosar et al. [30]	50 / 100	100	N/A	80 / 20
Liu et al. [32]	445 / 559	3000	0.88 / 1.16	3.8 / 2.6
Brunschwiler et al. [28]	50 / 100 / 200	97 / 189	0.29**	18**
Wan et al. [33]	17	176	0.538	N/A
Prasher et al. [34]	55 / 125***	155 / 310	0.1	7 / 3
This work	150	270	0.33 / 0.28	28.4 / 44.6

* Normalized thermal resistance to the 1 cm^2 area.

** In-line micropin-fin with a pitch of 200 μm and a height of 200 μm at a flow rate of 100 mL/min.

*** Round staggered micriopin-fins of RP1 and RP3 at a flow rate of 100 mL/min.

One general challenge of such TSV integration is that it necessitates TSVs being fabricated inside a microfluidic heat sink, and this introduces several fabrication challenges. From a cooling perspective, a relatively 'thick' die is preferred since the height of a microfluidic heat sink is related to its cooling capability, such as thermal resistance and pressure drop [35]. However, this inevitably requires TSVs to be relatively

tall (typically, TSV height is the same as wafer thickness). On the other hand, from an electrical point of view, it is desired to have as small an allocation of copper as possible for TSVs in a silicon substrate. This is because the area allocated to copper TSVs directly consumes active circuit area. Moreover, as the diameter of TSVs increases, not only does electrical TSV capacitance increase, but thermomechanical stress also increases [36]. However, it should be noted that the diameter of TSVs cannot be boundlessly reduced, since this will dramatically increase fabrication complexity, such as silicon etching and copper filling. Thus, it is critical to maximize the aspect ratio of TSVs without increasing fabrication complexity to satisfy both electrical and cooling metrics.

1.2 Research Objective and Contribution

The objective of this research is to provide electrical and thermal solutions to achieve high bandwidth communication with low energy consumption for advanced 3-D microsystems. More specifically, this research focuses on the modeling, fabrication, and characterization of high-aspect ratio TSVs embedded in a microfluidic heat sink that exhibit low electrical TSV loss for high-performance 3D microsystem applications. To complete the research objectives, the contribution of this research includes the fabrication and characterization of high-aspect ratio TSVs embedded in a micropin-fin heat sink and low-loss TSVs using partial air isolation between signal and ground TSVs. The developed technologies in this research are described as follows.

- High-aspect ratio TSVs embedded in a micropin-fin heat sink: for silicon dice with embedded microfluidic cooling, it is necessary to develop highly scaled TSVs in tall micropin-fins to address both the electrical and thermal constraints. This not only improves the electrical performance of TSVs, such as TSV capacitance and electrical loss, but also maintains an acceptable chip junction temperature under large power dissipation.
- Coaxially shielded TSVs in a micropin-fin heat sink: in such a silicon microsystem with embedded cooling, the existence of coolant between signal and ground TSVs will affect electrical signals propagating through a signal TSV, which impacts on TSV performance, such as loss, signal integrity and crosstalk. The coaxially shielded TSV structures are designed and fabricated to eliminate such unwanted effects of coolant on the TSV parasitics.

- Air-isolated TSVs for low-loss silicon interposers: air-isolated TSVs are proposed to reduce high-frequency TSV loss for silicon interposer applications. This research demonstrates the fabrication and characterization of copper TSVs with air isolation by partially etching silicon between TSVs. Since TSVs are partially isolated by air, TSV loss and TSV capacitance are significantly reduced.
- Modeling of TSVs embedded in a silicon microfluidic pin-fin heat sink with the presence of the deionized water: this chapter provides the electrical circuit model of TSVs in a silicon/water-mixed substrate based on transmission line theory using two-dielectric coaxial lines. More specifically, this chapter focuses on the extraction of capacitance and conductance and the correlation of the derived models with measurements.

1.3 Organization of the Thesis

The dissertation is organized as follows:

- Chapter 2: The fabrication and characterization of TSVs inside a silicon microfluidic pin-fin heat sink are demonstrated. Moreover, the four-point resistance measurements and X-ray inspection are also demonstrated.
- Chapter 3: The high-frequency characterization of TSVs in a microfluidic pin-fin heat sink with the presence of deionized water is presented.
- Chapter 4: The fabrication and characterization of air-isolated TSVs are demonstrated by partially isolating copper TSVs with air.

- Chapter 5: The electrical circuit model of TSVs in a microfluidic pin-fin heat sink is presented using coaxial-line formulas based on transmission line theory.
- Chapter 6: A summary is given and potential future work for the demonstrated technologies is described.

CHAPTER 2

HIGH-ASPECT RATIO TSVS INTEGRATED WITH MICROFLUIDIC COOLING FOR HIGH-PERFORMANCE 3-D MICROSYSTEMS

This chapter describes the fabrication of fully-isolated TSVs with an aspect ratio of 23:1 and investigates the integration of high-aspect ratio TSVs within a microfluidic heat sink using various fabrication processes. Moreover, void-free TSVs are validated using four-point resistance measurements and X-ray imaging.

2.1 Introduction: Thermal and Electrical Co-Design for High-Performance 3-D microsystems

Figure 5 illustrates a potential 3-D microsystem in which two logic dice and a memory cube are stacked on an interposer substrate. Each logic die consists of a micropin-fin heat sink with integrated TSVs for electrical connectivity. Fluidic vias are also formed in the dice to enable coolant delivery in and out of the dice. In 3-D microsystems, the thickness of the silicon must be greater than the height of the micropin-fin heat sink. In general, micropin fins of a relatively large height are required in order to maintain an acceptable chip junction temperature under large power dissipation since the surface area of a heat sink increases as the heat sink height increases [35]. Moreover, it increases the hydraulic diameter of the heat sink and thus reduces the

pressure drop. However, from an electrical perspective, this increased die thickness results in increased TSV dimensions (diameter and height) for a fixed aspect ratio TSV, as illustrated in Figure 6.

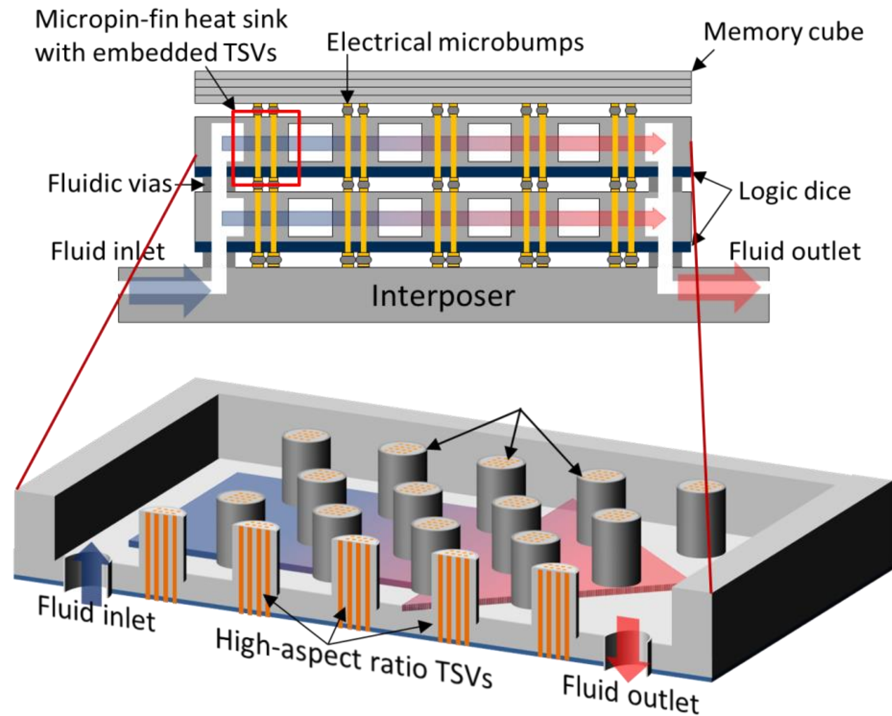


Figure 5. Schematic of the proposed 3D system with embedded microfluidic cooling.

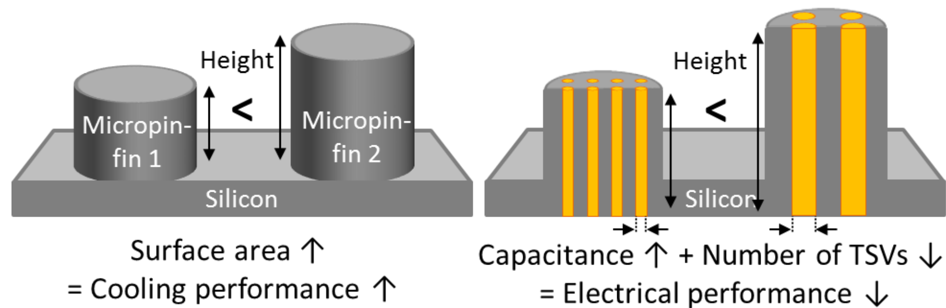


Figure 6. Trade-off exists between electrical and thermal performances with respect to the height of silicon micropin-fins.

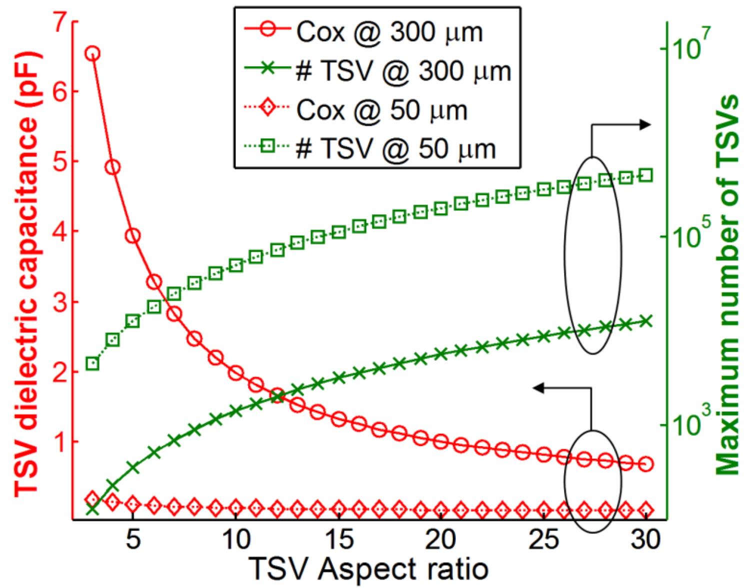


Figure 7. TSV dielectric capacitance and maximum number of TSVs as a function of aspect ratio and die thickness.

This in turn exacerbates the capacitance of the TSVs. Figure 7 illustrates TSV capacitance and the maximum number of TSVs as a function of TSV aspect ratio for two die thicknesses (50 and 300 μm), assuming only 1% of the die area is allocated for TSVs. For the thinner (50 μm) die, which is in-line with conventional 3-D microsystems, increasing the TSV aspect ratio does not significantly improve TSV capacitance. However, for thicker (300 μm) die, which is in-line with the thickness needed for dice with embedded microfluidic cooling, the TSV aspect ratio plays a critical role in the electrical performance. If we increase the TSV aspect ratio from 5:1 to 20:1, the TSV capacitance decreases from 3.94 pF to 1 pF (an approximately 75% reduction). At the same time, assuming only 1% of the die area is allocated to TSVs, the maximum number of TSVs in the die increases from 353 to 5,658. Thus, for silicon die with embedded microfluidic cooing, it is important to develop high-aspect ratio TSVs to lower the

capacitance and increase the number of interconnections between the tiers. This is missing in the literature and the focus of this chapter. The following section describes our proposed high-aspect ratio TSV processes and their integration with the silicon micropin-fin heat sink.

2.2 Literature Survey

2.2.1 Through-Silicon Vias Embedded in a Microfluidic Heat Sink

Table 2 summarizes the specifications of TSVs integrated with microfluidic cooling technologies in the literature. One prior study has demonstrated the integration of TSVs with micropin-fins [35]. However, it demonstrated only a single TSV per micropin-fin due to the large TSV diameter. Given the thickness of silicon dice with embedded microfluidic cooling, high-aspect ratio (i.e. high height-to-diameter ratio) TSVs become necessary in such 3-D microsystems. Prior work [37] showed preliminary progress in the integration of multiple TSVs in a microfluidic heat sink; however, the TSVs were not electrically isolated and were not completely etched through the wafer due to innate difficulty in high-aspect ratio silicon etching and copper filling in a thick silicon substrate. To address this, this research focuses on the fabrication of fully isolated TSVs with an aspect ratio of 23:1 and investigates the integration of high-aspect ratio TSVs within a microfluidic heat sink using various fabrication processes. Moreover, this research qualitatively investigates the co-design of the electrical and microfabrication constraints that TSVs impose on microfluidic cooling.

Table 2. Comparison of TSVs integrated with microfluidic cooling technology.

Parameters	C. R. King et al. [38]	Y. Madhour et al. [39]	N. Khan et al. [22]	Y. Zhang et al. [35]	H. Oh et al. [24]
TSV diameter	50 μm	60 μm	150 μm	13 μm	13 μm
TSV height	~300 μm	380 μm	400 μm	300 μm	320 μm
TSV pitch	200 μm	~200 μm	500 μm	24 μm	200 μm
Heat sink type	Channel	Channel	Channel	Pin-fin	Pin-fin
Heat sink width (or diameter)	100 μm	100 μm	50 μm	150 μm (diameter)	50, 100, 150 μm (diameter)
Heat sink height	200 μm	100 μm	175 μm*	200 μm	220 μm
Note	Long microchannel used	Vertical stack of 5 chips using solder bond	TSVs are not fabricated inside a heat sink	16 TSVs fabricated in each micropin-fin	TSV pitch is fixed for all diameters

*Two wafers are face-to-face bonded, so it gives a total height of 350 μm.

2.2.2 High-aspect ratio Through-Silicon Vias

Numerous studies in the literature have proposed high-aspect ratio TSVs to achieve high-density 3D interconnects as well as to reduce TSV parasitics [40]-[43]. In general, the main limiting steps to achieving high-aspect ratio TSVs are at the silicon etching and copper filling steps. First, high-aspect silicon etching is generally performed using the deep reactive ion etching (DRIE) process [44]. However, this process suffers from two limiting factors: the RIE-lag effect [45] and the aspect-ratio-dependent-etching (ARDE) effect [46]. The former refers to the fact that the etch rate is dependent on the total mask opening size. The latter indicates that the etch rate decreases as the aspect ratio increases. In addition to the DRIE process, various wet etching processes have also been proposed, for example photo-assisted electrochemical etching [47] and metal-assisted chemical etching [48]. Second, high-aspect ratio copper filling can be achieved using 'bottom up' electroplating [49]. Moreover, different approaches have been proposed using nickel wires or wire bonds [43], [50].

2.3 Fabrication of High-Aspect Ratio TSVs Integrated within a Micropin-fin Heat Sink

Figure 8 illustrates the overall fabrication steps for high-aspect ratio TSVs in micropin-fins. Figure 8 (a) illustrates a high-aspect ratio silicon via etching step using two etch masks (either by an oxide mask or a photoresist mask), and Figure 8 (b) presents the fabrication processes following silicon via etching.

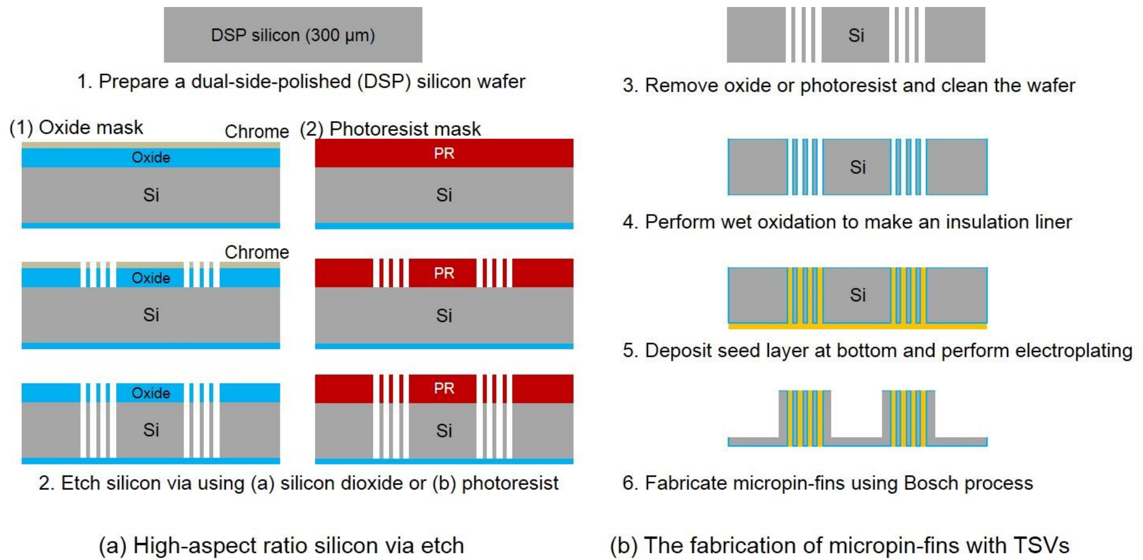


Figure 8: An overview of the fabrication process of high-aspect ratio TSVs in a micropin-fin heat sink.

2.3.1 High-Aspect Ratio Silicon Via Etch Using Two Etch Masks

The first step of the process is to etch narrow and tall silicon vias using the Bosch process, which alternates between passivation (C_4F_8) and etching (SF_6). This process step requires a precise procedure because the total area of vias to be etched is extremely small (e.g., 0.32%), which leads to a dramatic increase in the duration of etching, referred to as "RIE-lag effect" [45]. In addition, the time it takes to etch a silicon via does not proportionally increase as the via becomes deeper; rather, it becomes significantly prolonged for substantially deep vias. This effect occurs because the Bosch process is an aspect-ratio-dependent etch, so the etch rate decreases dramatically for narrow and tall vias [44],[46]. This increased etch time results in the depletion of etch mask during the long etch process, and thus we need robust etch masks that can endure in such long etch

processes. In this work, two types of etch masks (one hard mask and one soft mask) are demonstrated as follows.

- **Hard mask (silicon dioxide)**

To etch such deep vias with a small opening, we first optimized the Bosch process by increasing the coil power from 800 W to 2,000 W, as summarized in Table 3. While this process dramatically decreases the silicon etch time, it requires the etch mask to be sufficiently robust to endure such high coil power. Thus, we use silicon dioxide as an etch mask, which has a higher selectivity than polymer-based masks [51]. At such a high coil power, the oxide mask exhibits high selectivity to silicon (> 30:1), which indicates that we must deposit more than 10 µm of silicon oxide to etch a 300 µm thick silicon wafer. In order to pattern the silicon dioxide, we use a thin metal film as an etch mask instead of a polymer-based photoresist for two reasons: First, the metal film can be very thin (less than a micron) because of its high selectivity to silicon dioxide, while a photoresist mask is required to be as thick as the oxide (~10 µm). Second, the thin metal mask does not exhibit any sloped sidewalls as may occur in polymer-based etch masks.

Table 3. Summary of the fabrication parameters used for silicon etching.

Coil power	2,000 W (high)		800 W (low)
Mask	Oxide	Photoresist	Photoresist
Process	Complex	Simple	Simple
Etch rate	1.79 µm/min	N/A	0.92 µm/min
Selectivity	> 30 : 1	Too low	~ 16 : 1

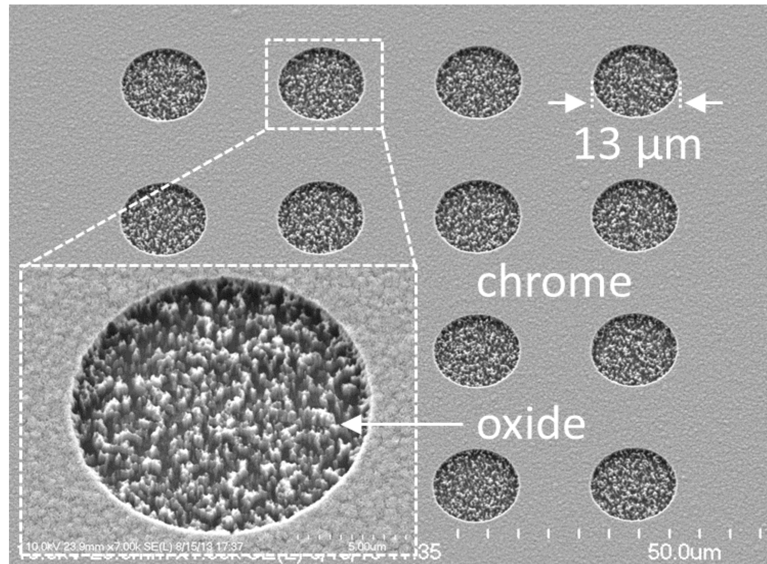


Figure 9. Pattern of a chrome mask on silicon dioxide (oxide less than a micron is etched to distinguish the thin chrome layer from the oxide layer).

To fabricate high-aspect ratio silicon vias, we follow the process steps summarized in Figure 8 (a). First, we deposited a thick (~10 µm) silicon dioxide film using plasma-enhanced chemical vapor deposition (PECVD). Next, we sputter a thin (5,000 Å) chrome film using physical vapor deposition (PVD) on the silicon dioxide followed by etching chrome using the CR-7S chrome etchant. Figure 9 shows an SEM image of the chrome-mask on the silicon dioxide.

Using the patterned chrome as an etch mask, the silicon dioxide was etched by an anisotropic dry etch using the SPTS advanced oxide etch system. In this step, a coil power of 1,800 W and a platen power of 180 W were set while the platen temperature was set to 60 ºC, which helps increase the sidewall angle. Figure 10 shows a cross-sectional view of the oxide mask after dry etching. Following the oxide etch, the silicon was etched using the SPTS Pegasus system with the optimization of etching parameters. During this step, as we continue to etch into the via, we slightly increase the etch duration

from 2.5 to 3 seconds per cycle and increase the platen power from 75 to 85 W at 380 kHz to obtain a vertical sidewall profile. The coil power, which is one of the most critical parameters for etch rate, was increased to 2,000 W. Etched silicon vias with a depth of 300 μm are shown in Figure 10.

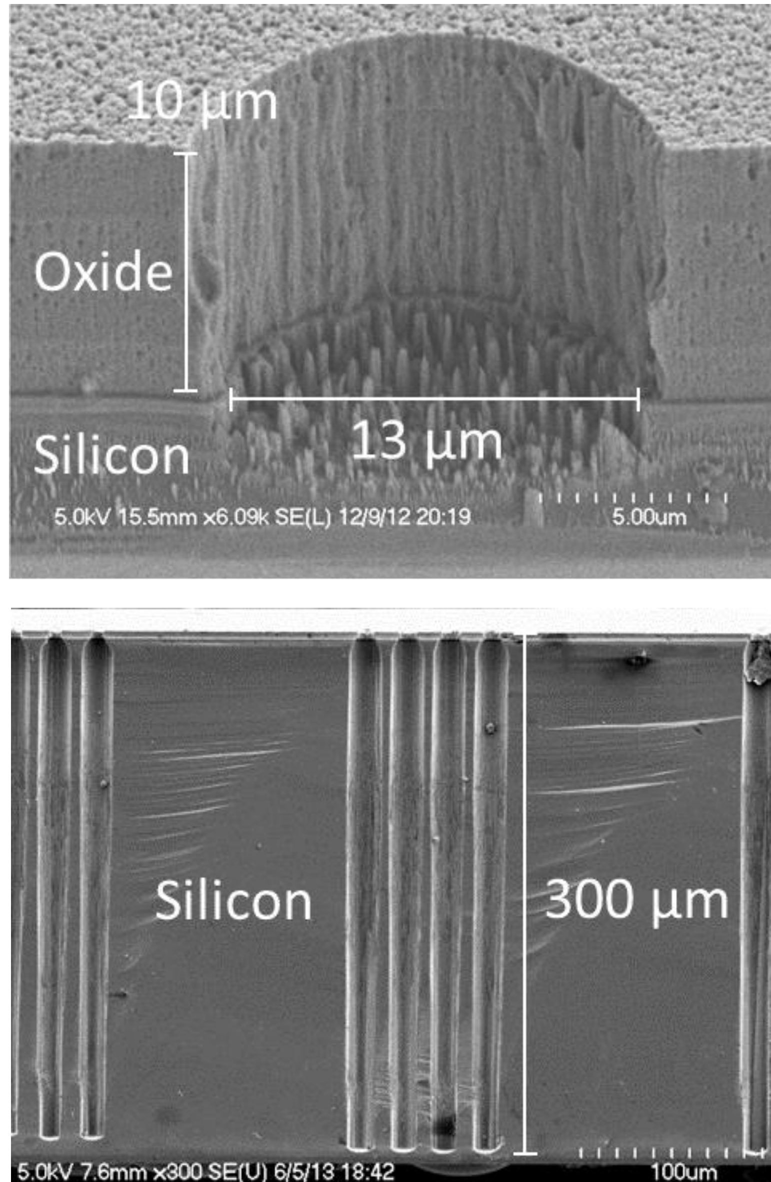
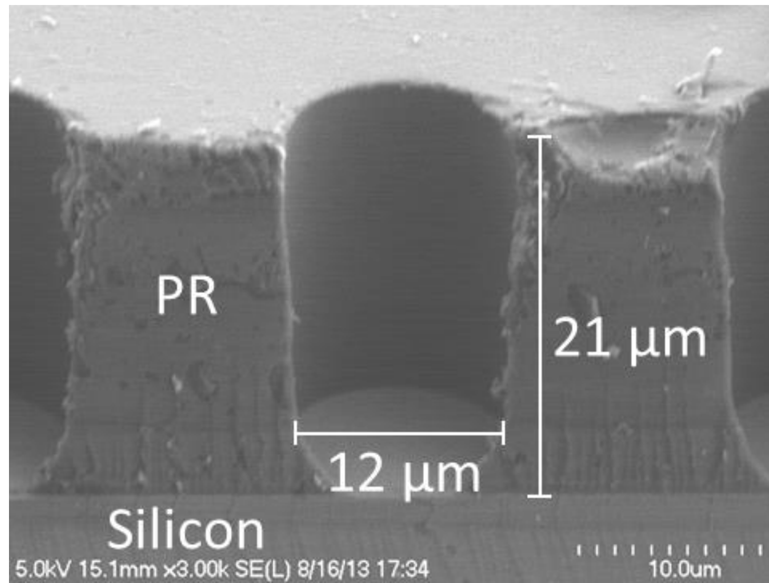


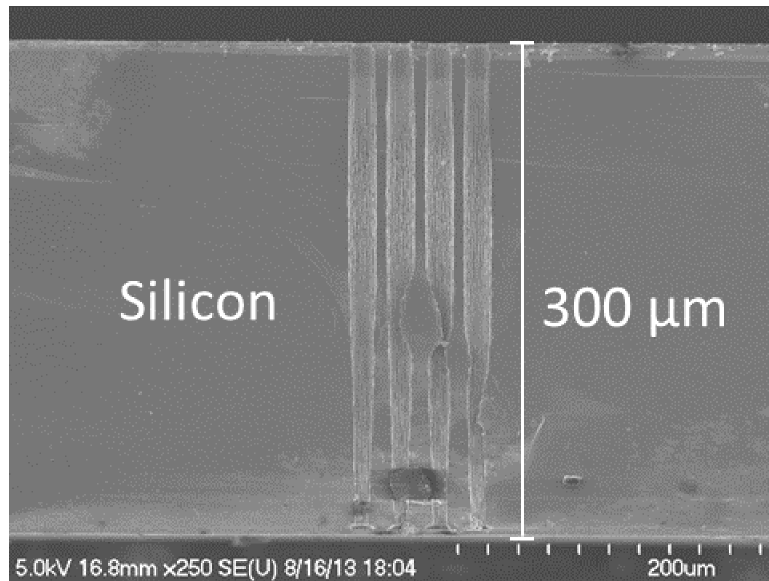
Figure 10. SEM images of Cross-section of the etched oxide (top) and the etched silicon using the oxide mask (bottom).

- **Soft mask (photoresist)**

To simplify the fabrication process of the high-aspect ratio silicon via etching, we also investigated silicon via fabrication using a chemically amplified photoresist, AZ-40XT (i-line positive photoresist) that can endure the total etch time. Figure 11 (a) exhibits a cross-sectional view of a 21 μm deep, 12 μm wide (aspect ratio of ~ 2:1) photoresist film. However, one limitation of using this photoresist is that it is not suitable for the high-power Bosch process (coil power of 2,000 W). This is because the process consumes the photoresist so rapidly that the photoresist becomes depleted during the process. For this reason, we lowered the coil power to 800 W with a platen power of 17 W, which consumes less photoresist but also slows down silicon etching considerably. Figure 11 (b) illustrates successful silicon via etching to a depth of 250 μm using a photoresist mask.



(a)

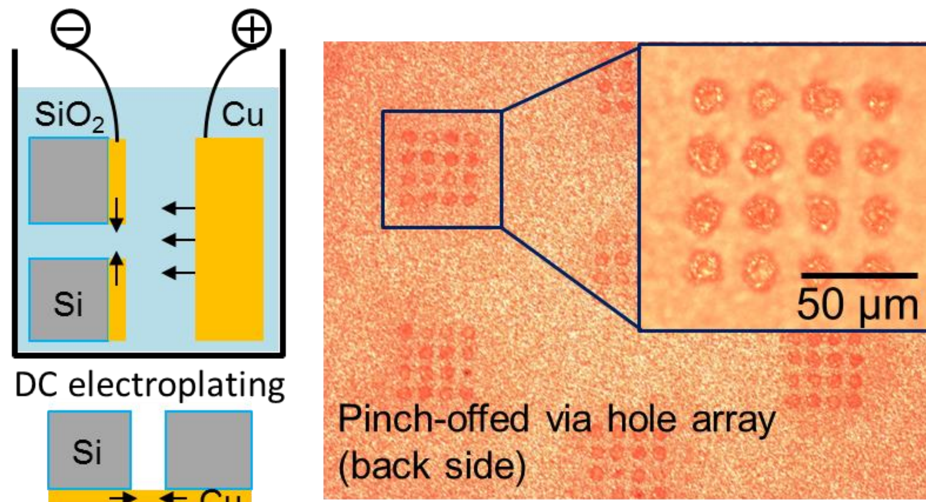


(b)

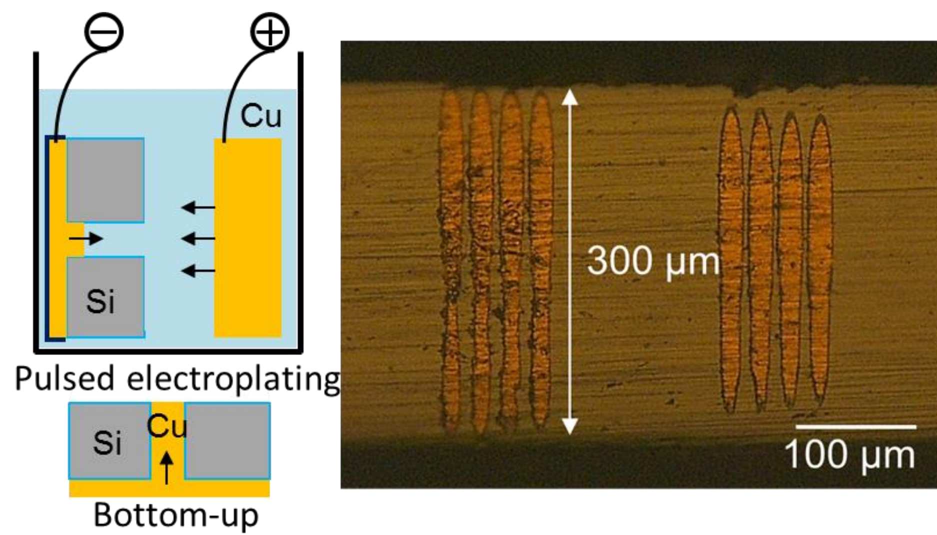
Figure 11. SEM images of (a) Cross-section of the photoresist mask and (b) etched silicon using the photoresist mask.

2.3.2 Fabrication of a Micropin-fin heat Sink with Embedded TSVs

After the removal of the remaining oxide on the wafer, the second fabrication step begins with thermal oxidation to form an insulation liner for TSVs (~0.5 μm). Metal layers, titanium and copper, are deposited using an e-beam evaporator on the back side of the wafer for copper electroplating; titanium acts as an adhesion layer between the oxide and the copper. To pinch the etched holes, DC copper electroplating is performed with a current level of 10 mA on the back side of the wafer to form a seed layer, as shown in Figure 12 (a). Next, to fill the holes with copper, bottom-up copper electroplating is performed on the newly formed seed layer using Enthone MICROFAB® DVF electroplating solution. Bottom-up electroplating is useful to fill very high-aspect ratio vias [40]. In this process, pulsed-plating (60:40 on-and-off ratio) with a current level of 7 mA is performed to fill the vias without voids, which will be addressed at the next section. To remove over-electroplated and seed copper after electroplating, chemical mechanical polishing (CMP) was performed on both sides of the wafer. Figure 12 (b) illustrates the cross-sectional view of fabricated TSVs with the dimensions of 13 μm in diameter and 300 μm in height, which yields an aspect ratio of 23:1. Following polishing, the micropin-fin structure is fabricated using the Bosch process with a standard negative photoresist. The angled and cross-sectional images of the fabricated TSVs in a 270 μm tall micropin-fin are shown in Figure 13.

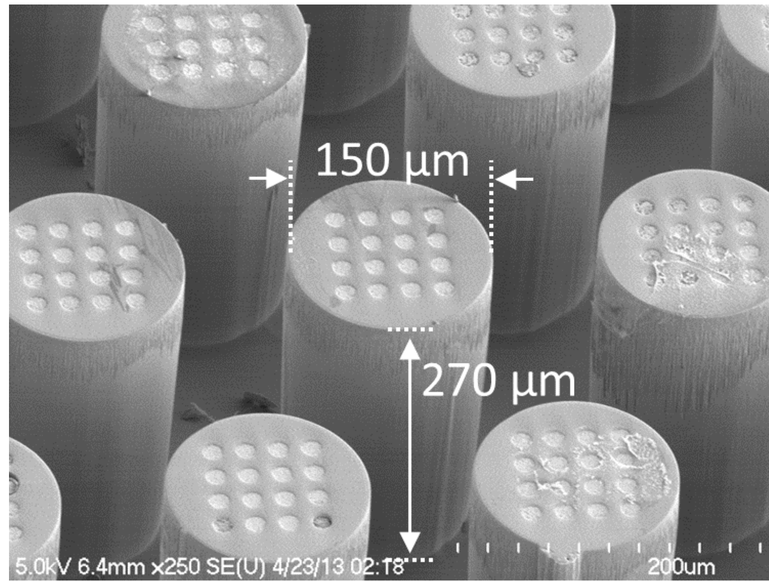


(a)



(b)

Figure 12. (a) Pinch-off via hole array by DC copper electroplating at the back side of the wafer and (b) cross-sectional view of TSVs after 'bottom-up' copper electroplating.



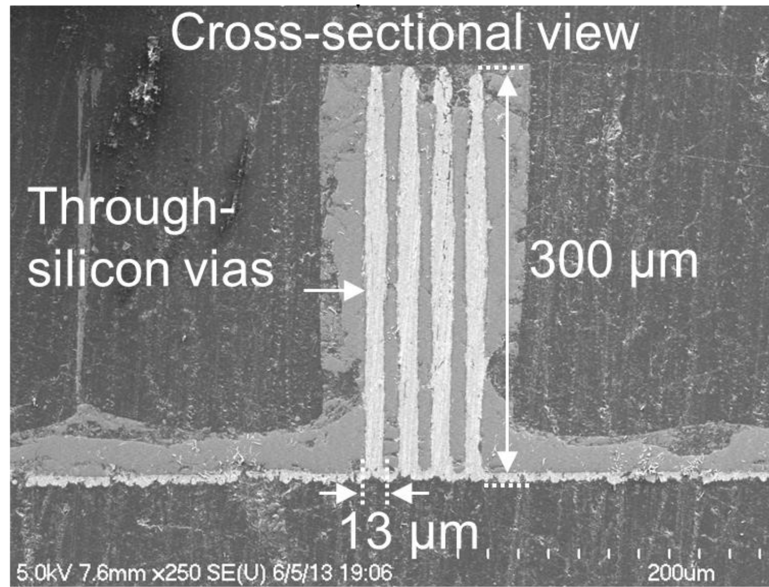


Figure 13: SEM images showing an array of micropin-fins with embedded TSVs from a bird's eye view (top) and a cross-sectional view (bottom).

2.4 TSV Validation: DC Resistance and X-ray Inspection

To verify void-free electroplating, we performed X-ray imaging. Figure 14 illustrates top and angled view X-ray images of a single micropin-fin containing 16 TSVs (4 × 4 array). The X-ray image was taken from the top side of the sample to identify if voids were formed inside of TSVs during fabrication. On the left figure, the large dark gray circle is the micropin-fin, and the sixteen black circles are the TSVs in a 4 × 4 array. We first set the boundaries on the TSV regions (the solid borders surrounding TSVs in the figure), and we increased the voltage of the tool to 130 kV. If the TSVs contained voids, a white hole would appear in the TSV region. In addition, the resistance of the fabricated TSVs is measured using a Signatone probe station with the four-point Kelvin technique. To facilitate probing, we fabricated 50 μm × 20 μm metal (titanium/copper/gold) pads by PVD above the TSVs, as shown in Figure 15. The final gold film was used to prevent the probing pads from being oxidized. The average measured resistance of a single TSV is 31.33 mΩ, with a standard deviation of 2.72 mΩ. Two methods (X-ray imaging and resistance measurements) verify the successful fabrication of void-free TSVs within the micropin-fin heat sink.

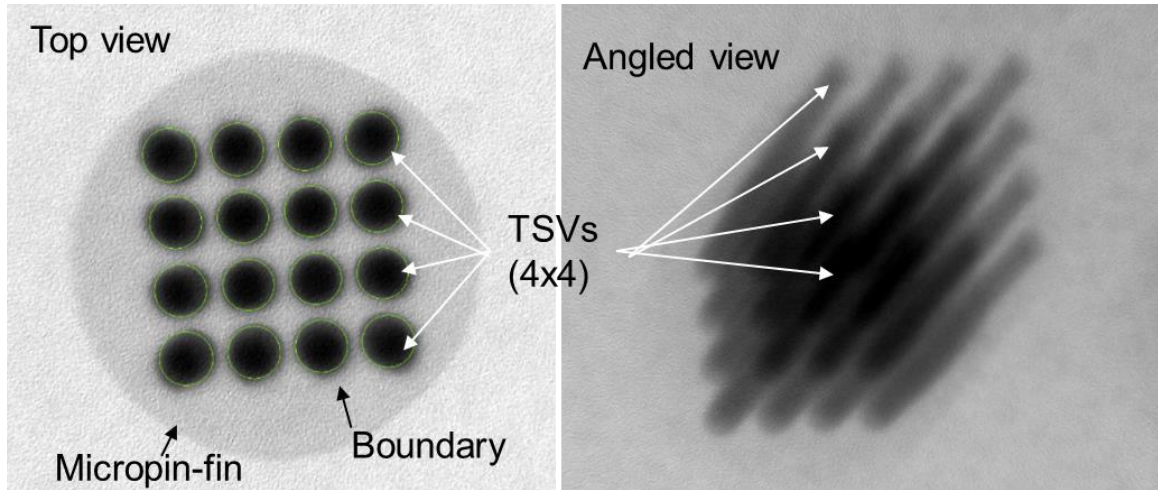


Figure 14. X-ray image of the TSVs in a micropin-fin from (a) a top view and (b) an angled view.

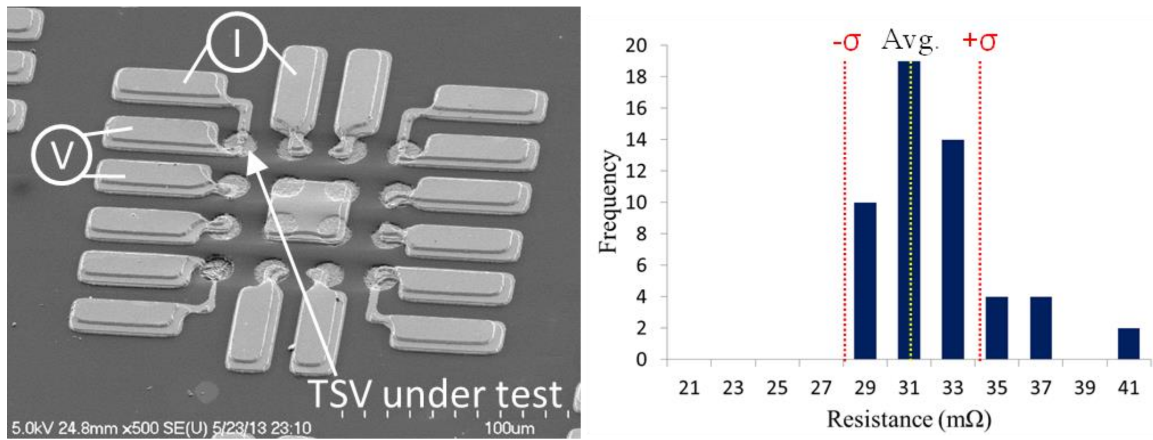


Figure 15. SEM image of TSVs with fabricated pads for TSV resistance measurements and resistant results.

2.5 Chapter Conclusion

This chapter demonstrates the integration of high-aspect ratio (aspect ratio of 23:1) TSVs in a micropin-fin heat sink. We successfully fabricated TSVs within a micropin-fin heat sink using two different silicon etch masks. The benefits of hard mask (silicon dioxide) over soft mask (photoresist) are increased selectivity, which allows a thinner etch mask, and reduced silicon etch time due to higher platen and coil powers, though this comes at the expense of more demanding lithography process. Moreover, we verified void-free TSVs using X-ray inspection and four-point resistance measurements. These TSVs promise to reduce the capacitance of the TSVs as well as to increase their density for fixed total footprint for the applications requiring microfluidic cooling.

CHAPTER 3

HIGH-FREQUENCY PERFORMANCE ANALYSIS OF TSVS WITH MICROFLUIDIC COOLING

This chapter describes the impact of deionized water on the electrical performance of TSVs by extracting the capacitance and conductance of TSVs within deionized water. The microfabrication of a testbed containing TSVs in silicon micropin-fins is presented, and the electrical performance of TSVs within deionized water is compared with conventional TSVs in silicon. Moreover, a coaxial-like TSV configuration is proposed as a possible solution to minimize the impact of coolant properties on the TSVs.

3.1 Introduction: Impact of Microfluidic Cooling on the Electronic Microsystems

As the need for microfluidic cooling in some applications increases, there have been various studies to understand the frequency dependent electrical characteristics of coolants used in microfluidic cooling. It is well known that the permittivity of deionized water changes significantly with frequency [52], [53]. The complex permittivity (real and imaginary permittivity) of deionized water has been characterized as a function of frequency using microwave spectroscopy [54]. Additionally, microwave platforms, such as ring resonators and RF sensing devices, have been developed to measure the permittivity of deionized water [55], [56]. Moreover, this frequency dependent

permittivity behavior of deionized water has been purposely utilized in various microwave components. For example, an L-band filter was integrated with microfluidic cooling to demonstrate a tunable corner frequency of the filter with respect to its dielectric constant [57]. In a similar manner, a high-sensitivity tunable sensor with conductor-backed coplanar waveguide (CPW) configuration was integrated with deionized water and a methanol-water solution [58]. A wideband differential detector was presented for the quantitative extraction of the frequency-dependent dielectric properties of different liquids [59]. One research study presented a shielded CPW on a liquid crystal polymer substrate with embedded deionized water to demonstrate the RF isolation of the CPW from the water [60]. However, no prior study has analyzed the impact of liquid cooling on the signal propagation of TSVs. The impact of the coolant on the electrical signaling should be analyzed, especially for liquid-cooled microsystems, because in such systems the liquid coolant surrounds the TSVs within a microfluidic heat sink [61]. The presence of coolant between signal and ground TSVs will impact electrical signal propagation, including loss, signal integrity and crosstalk [62]. To address this, this research analyzes the impact of deionized water on the electrical performance of TSVs, such as TSV capacitance and conductance, for liquid-cooled microsystems.

3.2 Design Challenges of TSVs Integrated with Microfluidic Cooling

Figure 16 compares the real permittivity and the effective conductivity of silicon and deionized water, respectively [53]. It can be seen that the effective conductivity of deionized water exceeds the conductivity of silicon at frequencies greater than 6.7 GHz, while the real permittivity of deionized water is unceasingly higher than that of silicon. Figure 17 illustrates the equivalent circuit models of: (a) conventional TSVs in a silicon

substrate from [63] and (b) TSVs in a micropin-fin heat sink within deionized water. It should be noted that, for the TSVs within deionized water, TSV capacitance and conductance are formed through not only silicon but also deionized water, as shown in Figure 17 (b); the capacitance and conductance consists of both silicon and deionized water between signal and ground TSVs (i.e., the canal region). If the width of the canal region (w_{canal}) increases, or equivalently the width of the micropin-fin (w_{pin}) decreases, at a fixed TSV pitch, the amount of water between TSVs increases. From an electrical perspective, this would increase the overall TSV capacitance and conductance because deionized water has higher permittivity and conductivity than silicon at high frequencies. Thus, when a liquid-cooled microsystem is designed, the microfluidic heat sink dimensions should be co-designed with respect to the TSVs, which will be analyzed in next sections.

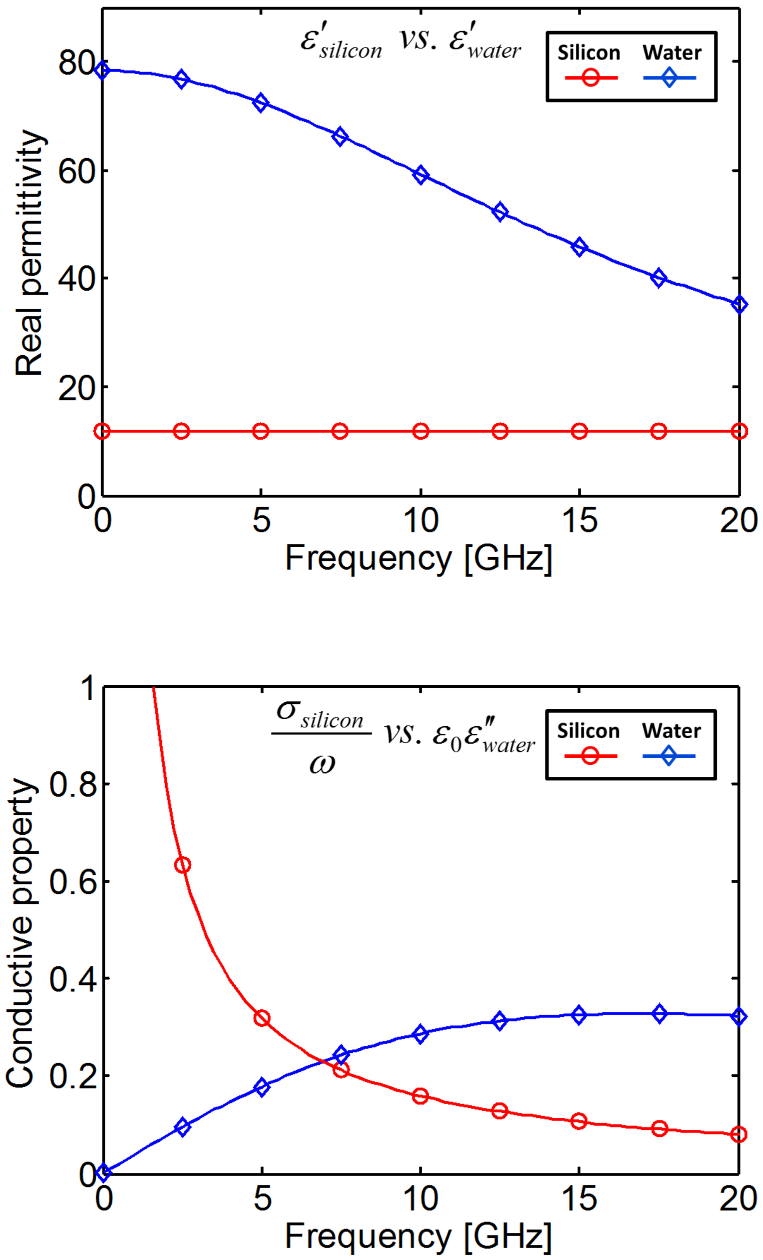
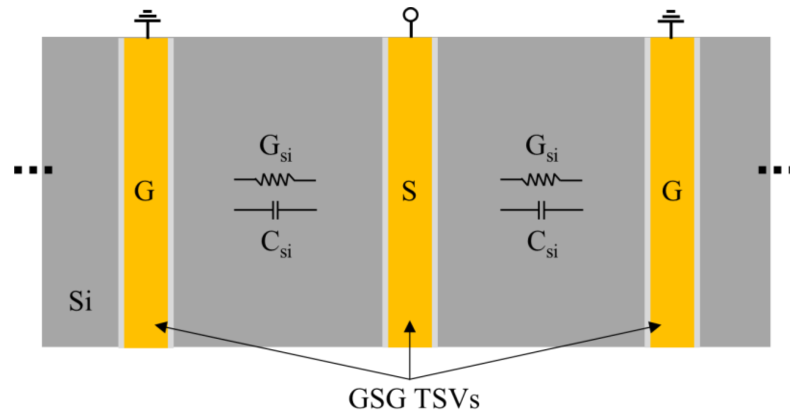
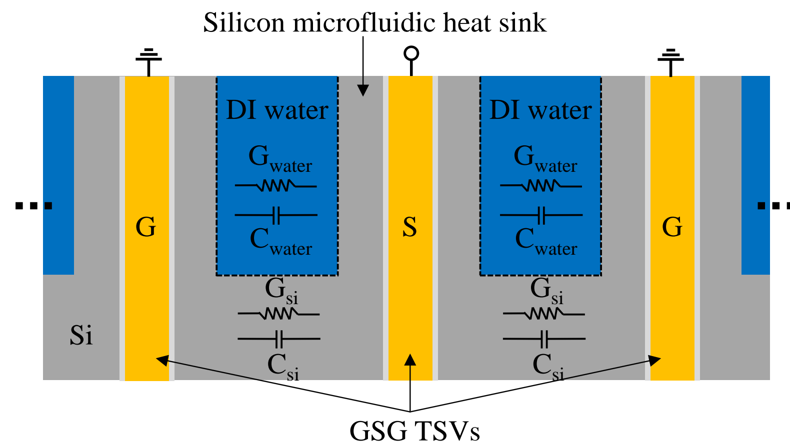


Figure 16. The real permittivity and the conductive property of silicon and deionized water as a function of frequency [53].



(a)



(b)

Figure 17. Simplified equivalent circuit models for (a) conventional TSVs in a silicon substrate and (b) TSVs in a micropin-fin heat sink within deionized water.

3.3 Fabrication and Assembly of TSVs within Deionized water

This section presents the microfabrication of TSVs embedded in three sets of micropin-fins for the high-frequency characterizion of TSVs. Figure 18 illustrates the overall fabrication process of the TSVs in a micropin-fin heat sink. The fabrication begins with the deposition of silicon dioxide (~9 μm) followed by the deposition of metal

using an e-beam evaporator. In this process, a thin layer of chrome (~0.5 µm) is chosen as an etch mask [Figure 18 (b)] since it has significantly high selectivity over silicon dioxide [44]. After etching the silicon dioxide layer through the chrome mask, the remaining chrome is removed using CR-7S chrome etchant. Using the resulting silicon dioxide as an etch mask, the high-aspect ratio Bosch process [51] is performed to etch via holes through the silicon wafer [Figure 18 (c)]. Following the removal of any remaining silicon dioxide etch mask, wet oxidation is performed to isolate the vias from the the silicon substrate [Figure 18 (d)]. Next, titanium and copper (30 nm / 500 nm) seed layers are deposited using an e-beam evaporator on the back side of the wafer. To pinch-off the etched openings, copper electroplating is performed at the back side using DC bias. Next, bottom-up copper electroplating is performed from the front side of the wafer with pulsed mode power supply (60:40 duty cycle). To remove the over-burdeon copper after electroplating, chemical mechanical polishing (CMP) is performed on both sides of the wafer [Figure 18 (e)]. Lastly, the Bosch process is performed to fabricate a silicon micropin-fin heat sink structure around the TSVs [Figure 18 (f)]. Figure 19 shows SEM images of three diameters (50, 100, and 150 µm) of micropin-fins each with a single TSV. The micropin-fin height and the base thickness of the micropin-fins are 230 µm and 100 µm, respectively. TSV diameter, pitch, and height are 13 µm, 200 µm, and 330 µm, respectively. Lastly, the fabricated sample is assembled to a glass slide with fluidic inlet/outlets (I/Os) for fluid delivery [Figure 18 (g)].

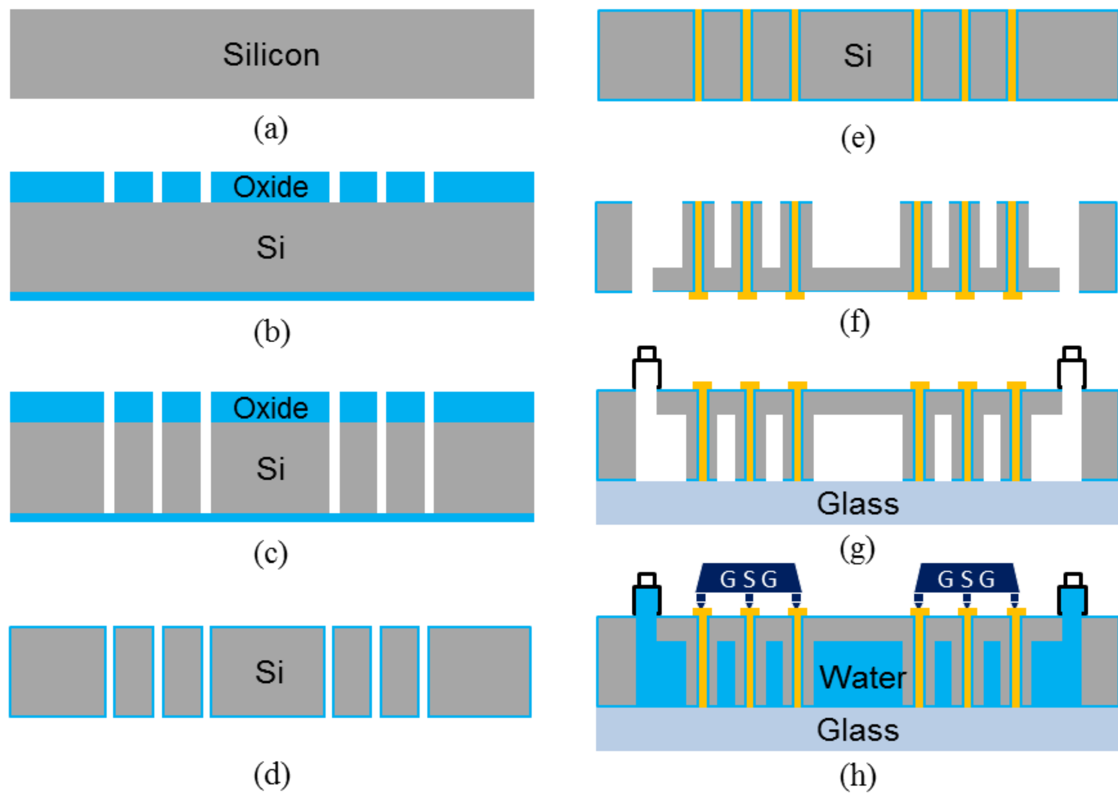
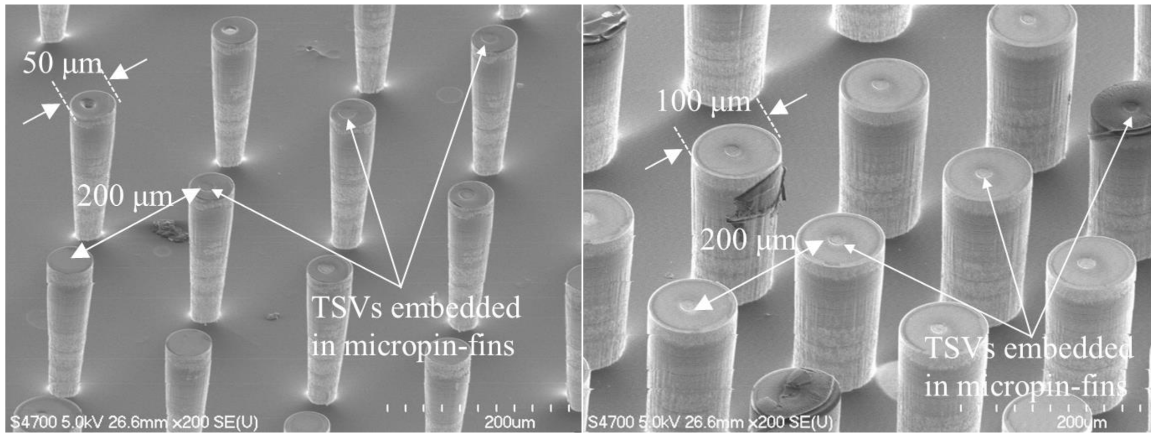
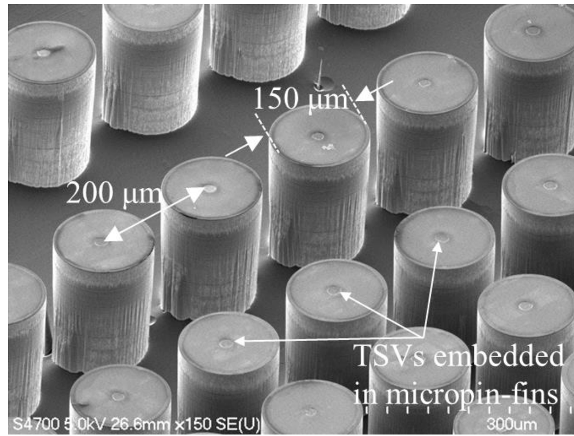


Figure 18. Schematic of the overall fabrication process of TSVs embedded in a micropin-fin heat sink and the assembly for high-frequency measurements with deionized water.



(a) (b)



(c)

Figure 19. SEM images of the fabricated micropin-fins with embedded TSVs: the micropin-fin diameter of (a) 50 µm, (b) 100 µm, and (c) 150 µm. The TSV pitch is fixed at 200 µm (each micropin-fin contains one TSV).

3.4 High-Frequency Characterization of TSVs within Deionized water

To characterize the high-frequency behavior of TSVs with deionized water, the fabricated testbed described in the previous section was filled with deionized water, as shown in Figure 18 (h). Figure 20 illustrates the used high-frequency characterization setup including the testbed, a microprobe station with Cascade |Z| probes, and an Agilent N5245A PNA-X network analyzer. To extract TSV capacitance and conductance from the measurements, single-port characterization of ground-signal-ground (GSG) TSVs is performed. Figure 21 illustrates the magnitude and the phase of S_{11} from the measurements and 3D full-wave simulation of TSVs in a silicon substrate and TSVs within deionized water, respectively. After the S-parameter (S_{11}) to Y-parameter (Y_{11}) conversion using (1), TSV capacitance and conductance are extracted from Y_{11} using (2)

$$Y_{11} = \frac{1}{Z_0} \cdot \frac{1 - S_{11}}{1 + S_{11}} \tag{1}$$

$$C_{TSV} = \frac{Im(Y_{11})}{\omega} \qquad G_{TSV} = Re(Y_{11}) \tag{2}$$

where Z_0 is the characteristic impedance [64]. The extracted capacitance and conductance from measurements and simulation for conventional TSVs in a silicon substrate and TSVs within a micropin-fin heat sink with deionized water are compared in Figure 22 and summarized in Table 4. As noted in Figure 16, the permittivity of deionized water is always higher than silicon permittivity; however, the effective conductivity of deionized water is initially lower than silicon conductivity but becomes higher as frequency increases. In Figure 22, it should be noted that the capacitance of TSVs within deionized water is lower at low frequencies than the capacitance of TSVs in silicon. This is because the extracted capacitance is not only a function of capacitance but also a function of

conductance of a material [64]. As frequency increases, the capacitance of TSVs within deionized water remains higher than TSVs in a silicon substrate. Similarly, the conductance of TSVs within deionized water is lower than TSVs in silicon at frequencies lower than approximately 5 GHz, but it becomes more conductive at higher frequencies.

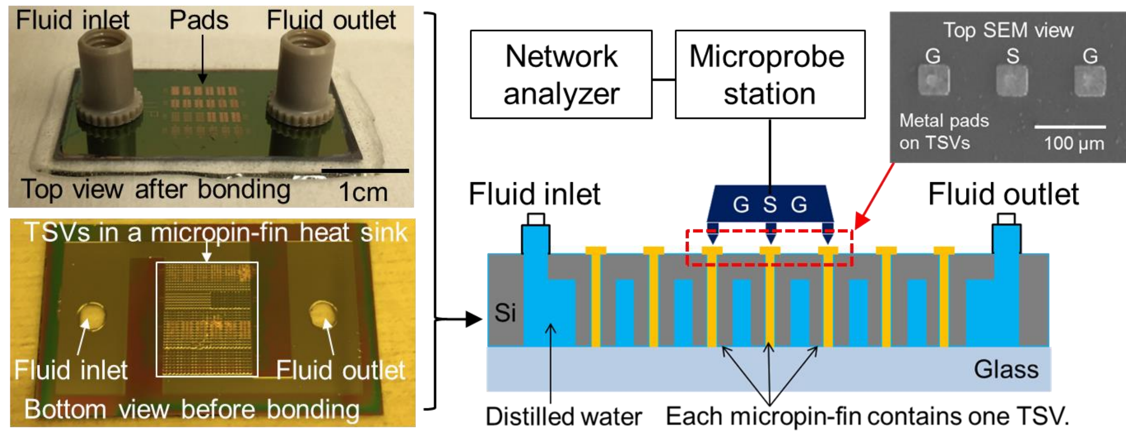


Figure 20. Schematic of the high-frequency characterization setup for TSVs within deionized water.

Table 4. Extracted capacitance and conductance for TSVs in a silicon substrate (silicon) and in a micropin-fin heat sink within deionized water (water).

Substrate (@ 20 GHz)	Capacitance (fF)		Conductance (mS)	
	Silicon	Water	Silicon	Water
Simulation	49.9	77.1	4.9	9.2
Measurements	44.7	91.5	4.7	10.4

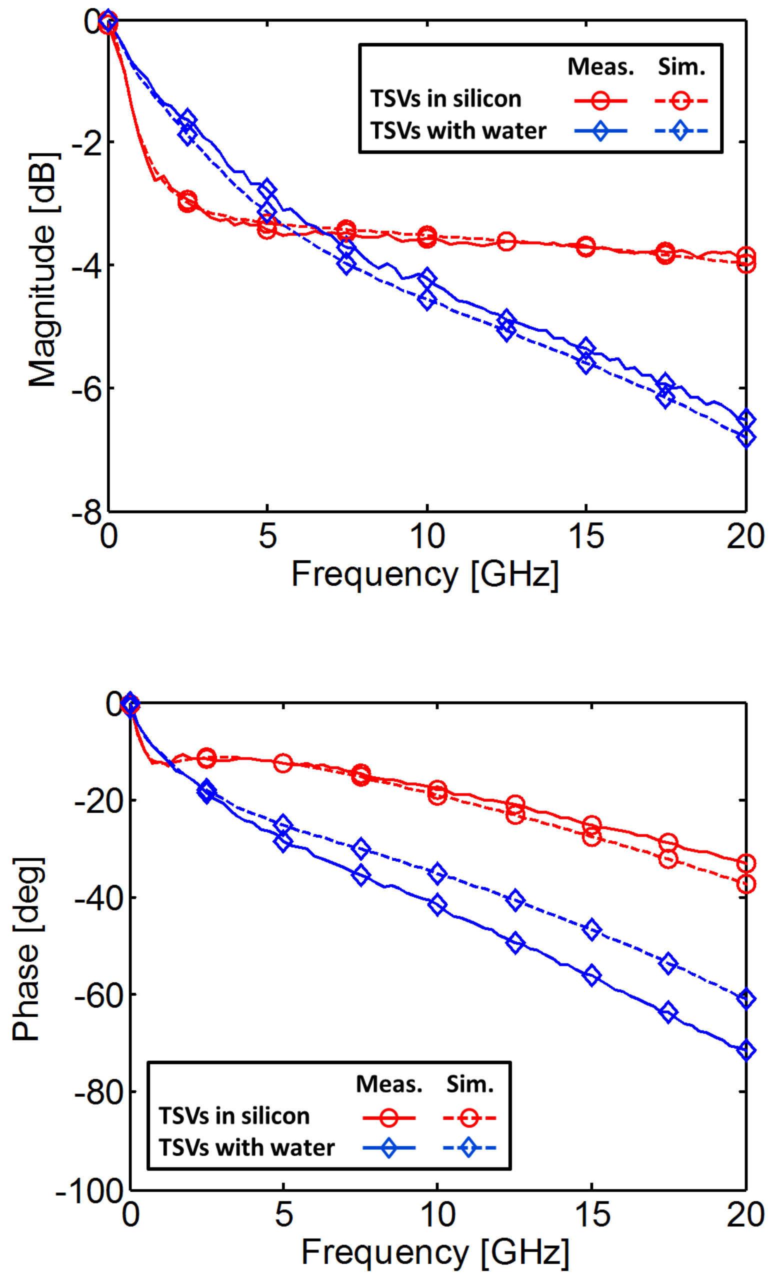


Figure 21. Magnitude and phase of S_{11} of TSVs in silicon and within deionized water from measurements and the HFSS simulation.

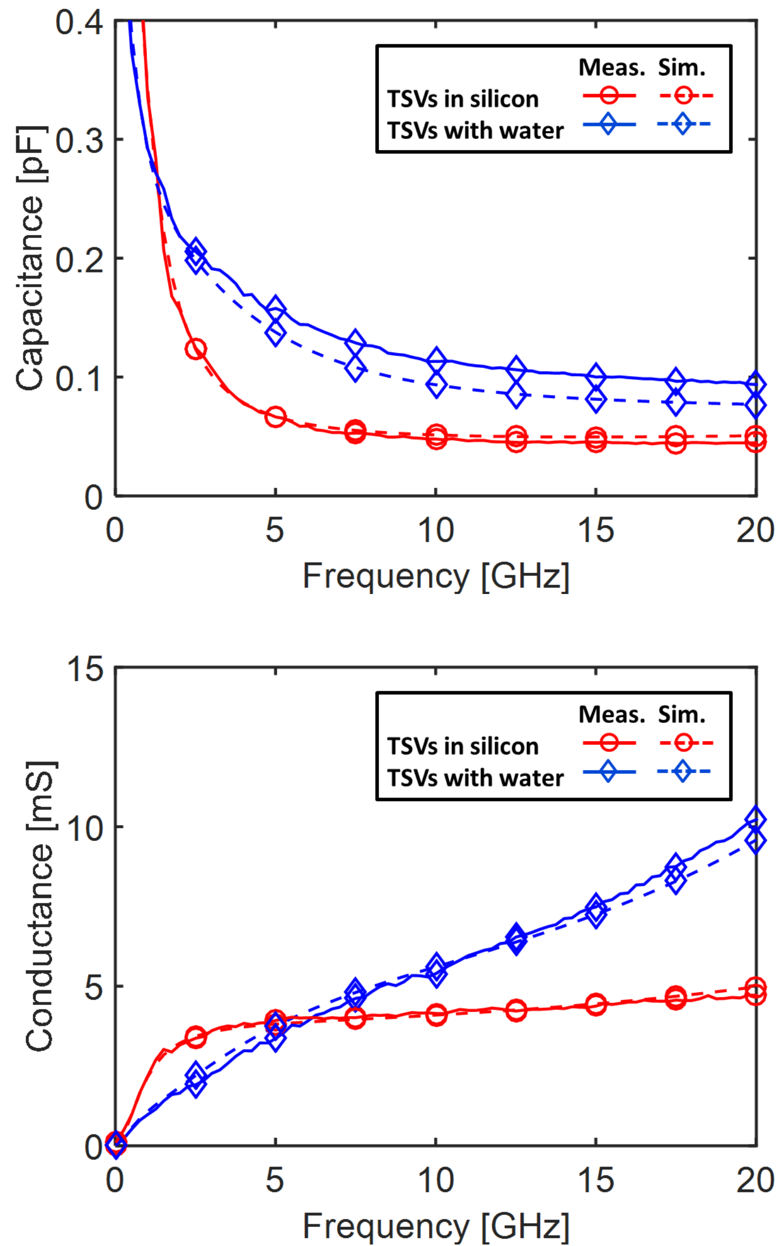


Figure 22. Capacitance and the conductance of TSVs in the silicon substrate and TSVs within deionized water from measurements and simulation.

To quantitatively analyze this behavior, the three measurements of TSVs in micropin-fins with different diameters (50, 100, and 150 μm) are compared at a fixed TSV pitch of 200 μm, as shown in Figure 23. Each plot compares the extracted

capacitance and conductance, respectively, from measurements for all cases (TSVs in silicon and TSVs in the three different diameters of micropin-fins). The results show that as the diameter of micropin-fins decreases, or equivalently as the volume of water between TSVs increases, TSV capacitance increases because of the high permittivity of deionized water. However, the conductance of TSVs within deionized water initially decreases as the volume of water increases at low frequency. On the contrary, at higher frequencies, the conductance increases as the amount of water increases, as shown in Figure 23 and Table 5. This is due to the conductive property of deionized water, which is less conductive than silicon at low frequency but more conductive than silicon at high frequency [53]. Moreover, this property of deionized water will significantly change the characteristic impedance of TSVs, which is a function of capacitance and conductance. The results imply that a micropin-fin heat sink geometry, or a microfluidic heat sink design, is one of the critical factors that determines the electrical performance of TSVs. Thus, for the liquid-cooled microsystems that require invariant signal transmission, signal TSVs should be isolated from such variations, which is analyzed in the next section.

Table 5. Extracted capacitance and conductance for each case; TSVs in a silicon substrate and TSVs within deionized water for different micropin-fin diameters.

Substrate (@ 20GHz)	Silicon	D* = 150 µm	D = 100µm	D = 50µm
Extracted capacitance (fF)	44.8	62.0	76.9	91.5
Extracted conductance (mS)	4.7	6.9	8.3	10.4

*D = the diameter of a silicon micropin-fin heat sink.

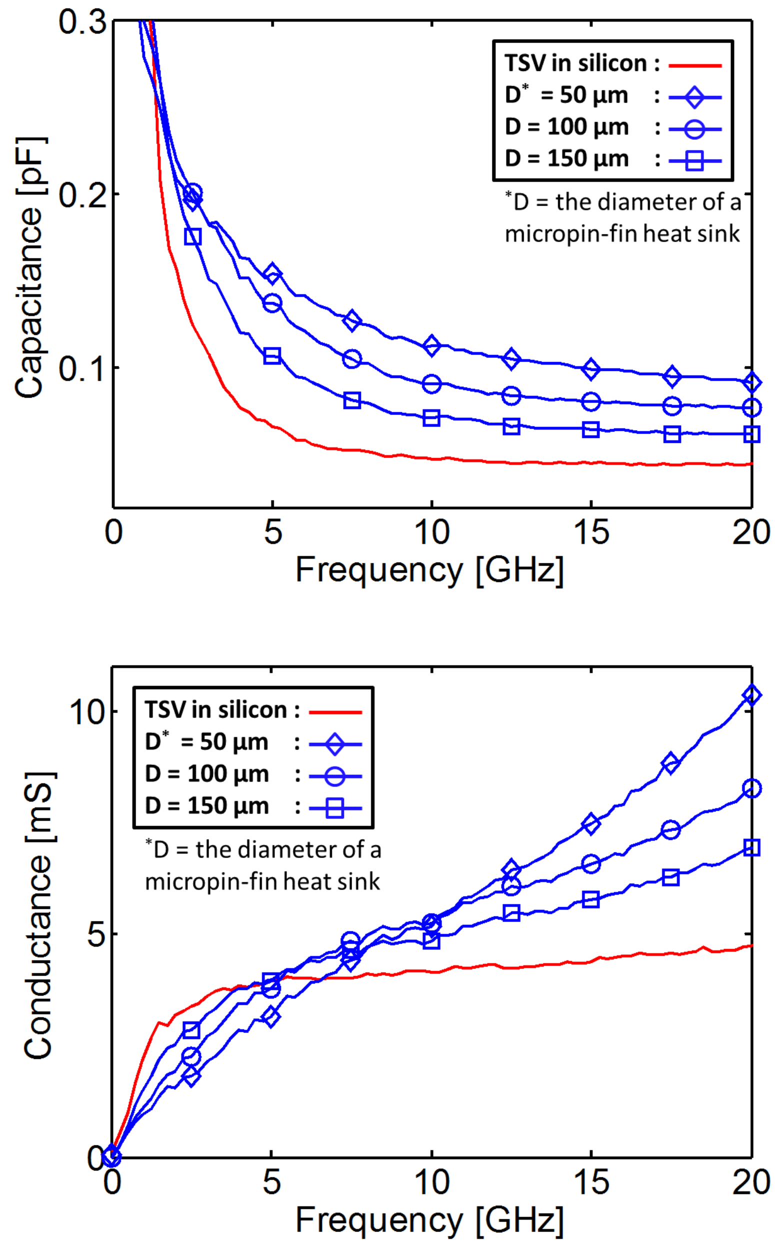


Figure 23. Extracted capacitance and conductance of TSVs within deionized water as a function of the micropin-fin diameter from measurements. TSVs in micropin-fins with three diameters (50, 100, and 150 µm) at the fixed TSV pitch of 200 µm are compared.

3.5 Coaxial-like TSV Configuration for Shielding TSVs from Surroundings

In this section, we propose a TSV configuration whose electrical attributes are invariant to the coolant or surroundings. A coaxial TSV configuration is a well-known solution to suppress undesirable substrate loss, noise, and coupling as well as provide excellent impedance matching [65]-[67], as summarized in Table 6. However, they face a number of fabrication challenges. First, the fabrication of a coaxial structure requires additional materials or processes, such as SU-8 [68],[69], Ajinomoto build-up film (ABF) [70],[71], or oxide using sub-atomic chemical vapor deposition (SACVD) [72]. Moreover, the outer ground conductor of the coaxial TSVs is typically larger in area than the center signal TSV. This is because the ground conductor is annular, while the signal via is circular; this geometry and size mismatch increases fabrication complexity in the Bosch process as well as in electroplating.

To address such issues, we propose a coaxial-like TSV configuration that consists of multiple ground TSVs (instead of a cylindrical layer) surrounding a signal TSV of the same copper dimension, as shown in Figure 24. In this configuration, a silicon micropin-fin consists of a single center signal TSV surrounded by multiple ground TSVs, and an annular shaped metal pad connects all ground TSVs.

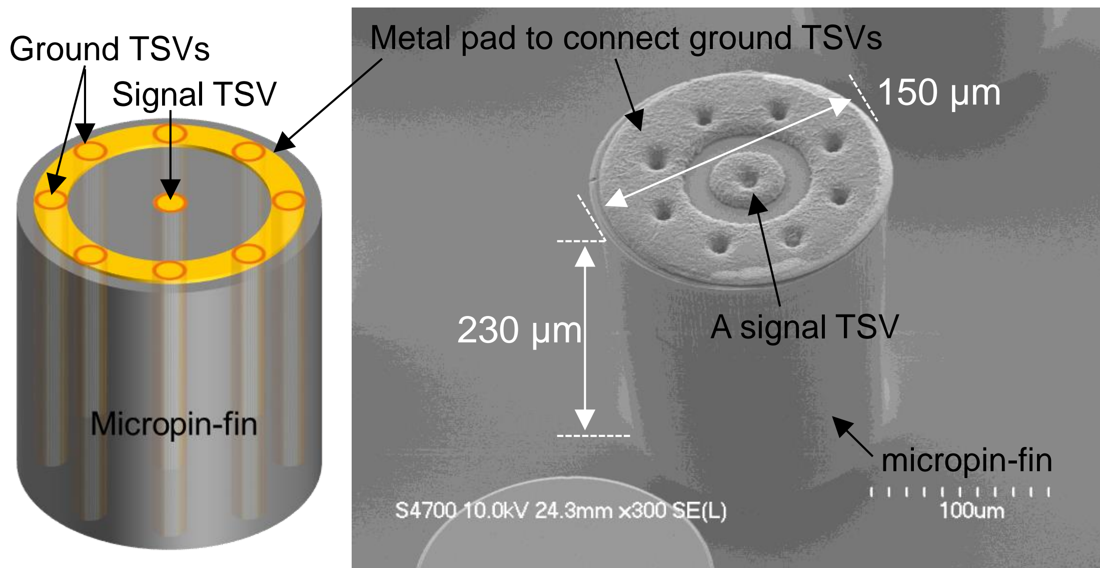


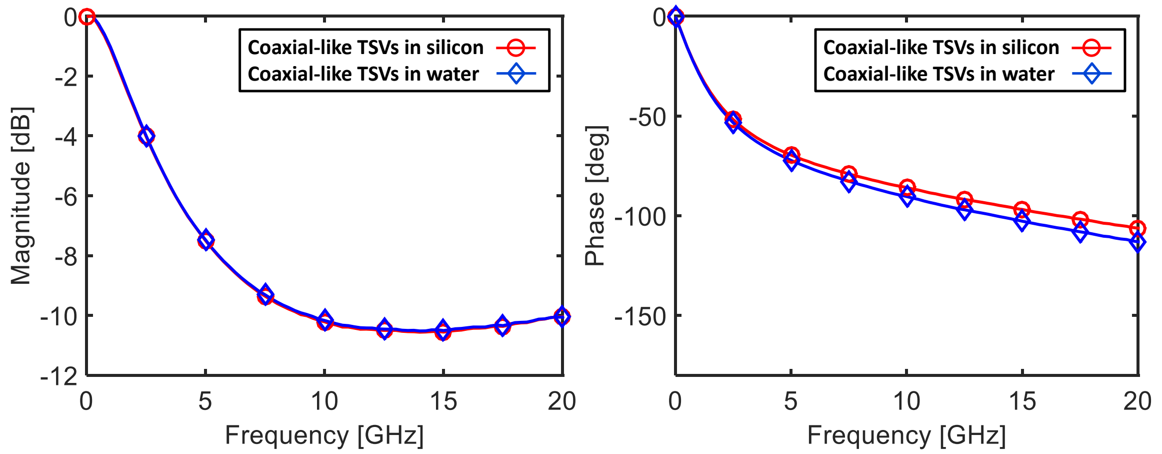
Figure 24. Schematic and SEM image of coaxial-like TSVs in a micropin-fin heat sink; multiple ground TSVs surround a center signal TSV.

Table 6. Comparison of coaxial TSVs in the literature

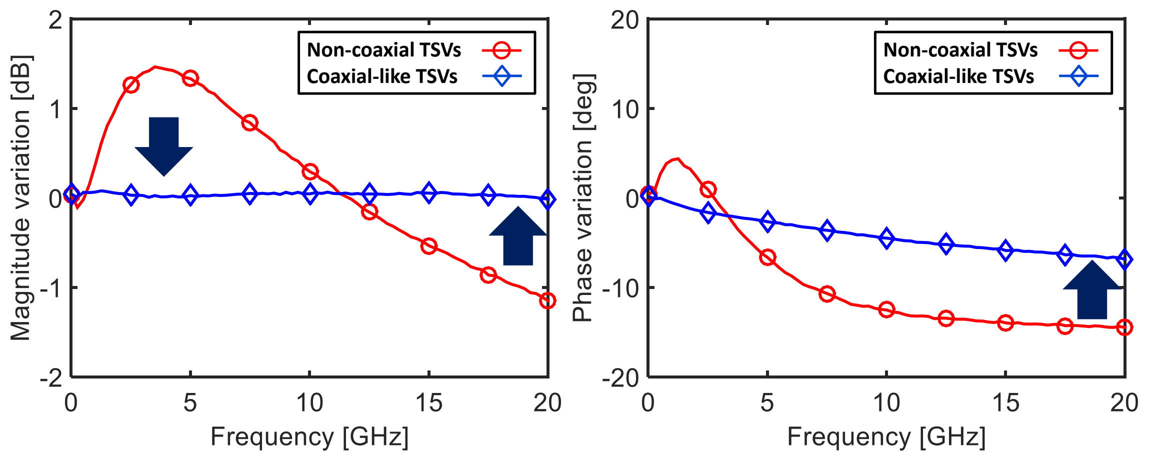
Parameters	S. W. Ho et al. [68]	P. Thadesar et al. [69]	D. H. Jung et al. [70]	J.-M Yook et al. [71]	S. Adamshick et al. [72]	H. Oh et al. [73]
TSV diameter	100 μm	65 μm	30/42 μm (inner/outer)	70 μm	5 μm	13 μm
TSV height	300 μm	285 μm	205 μm	150 μm	50 μm	320 μm
Insulator material	SU-8	SU-8	ABF*	ABF	Silicon dioxide	Silicon dioxide
Insulator thickness	500 μm	125/150 μm (TSV pitch)	25 μm	20 ~ 120 μm (20 μm step)	0.5 μm	50/100 μm (TSV pitch)
Coaxial TSV formation	Photolithography	Photolithography	Laser ablation	Laser ablation	SACVD oxide	Silicon etch (Bosch process)
Note	RO4350B substrate used for the bottom chip	Multiple ground TSVs (instead of annular ground)	Two metal layers at top and bottom (sig. and gnd.)	High-R silicon substrate used for the bottom chip	Two metal layers at top and bottom (sig. and gnd.)	Isolation of TSVs from surrounding deionized water

*ABF stands for Ajinomoto build-up film (ε_r = 3.7 and $tan\delta$ = 0.01).

The single-port measurements of coaxial-like TSVs are performed under two conditions: coaxial-like TSVs in silicon and coaxial-like TSVs in a micropin-fin within deionized water. To validate the shielding effect of coaxial-like TSVs, the S_{11} values of both cases are measured and plotted in Figure 25 (a). It is expected to exhibit approximately no variations between two measurements in S-parameters if coaxial-like TSVs have good shielding. In addition, non-coaxial TSVs, which consist of a single TSV in each micropin-fin (without ground TSVs), are also measured and compared under the same conditions. The measured S-parameters of each case are subtracted, and magnitude and phase variations are plotted in Figure 25 (b). In the plot, the magnitude difference of coaxial-like TSVs was less than ± 0.1 dB due to the ground shielding effect, while ± 1.3 dB magnitude difference was observed when there are no shielding TSVs. The results show that the ground TSVs (in the coaxial-like TSV case) successfully shield the signal transmission through the center signal TSV. Moreover, phase difference of 65.8% was alleviated due to the ground shielding effect. The coaxial-like TSVs exhibit a phase difference of approximately 6 degrees at 20 GHz, and this is believed to be caused by the non-perfect coaxial structure of the TSVs. Following the same Y-parameter conversion procedure as in the previous section, the extracted p.u.l. capacitance and conductance are plotted in Figure 26. It should be noted that the extracted capacitance and conductance of the coaxially shielded TSVs in silicon and in deionized water are highly consistent. Thus, when a stable signal transmission is required in a liquid-cooled 3D microsystem, the coaxial-like TSVs should be utilized to shield the signal TSVs.



(a)



(b)

Figure 25. (a) S_{11} magnitude and phase of coaxial-like TSVs and (b) variations of S_{11} magnitude and phase: coaxial-like TSVs exhibit shielding effects, showing less variation than non-coaxial TSVs.

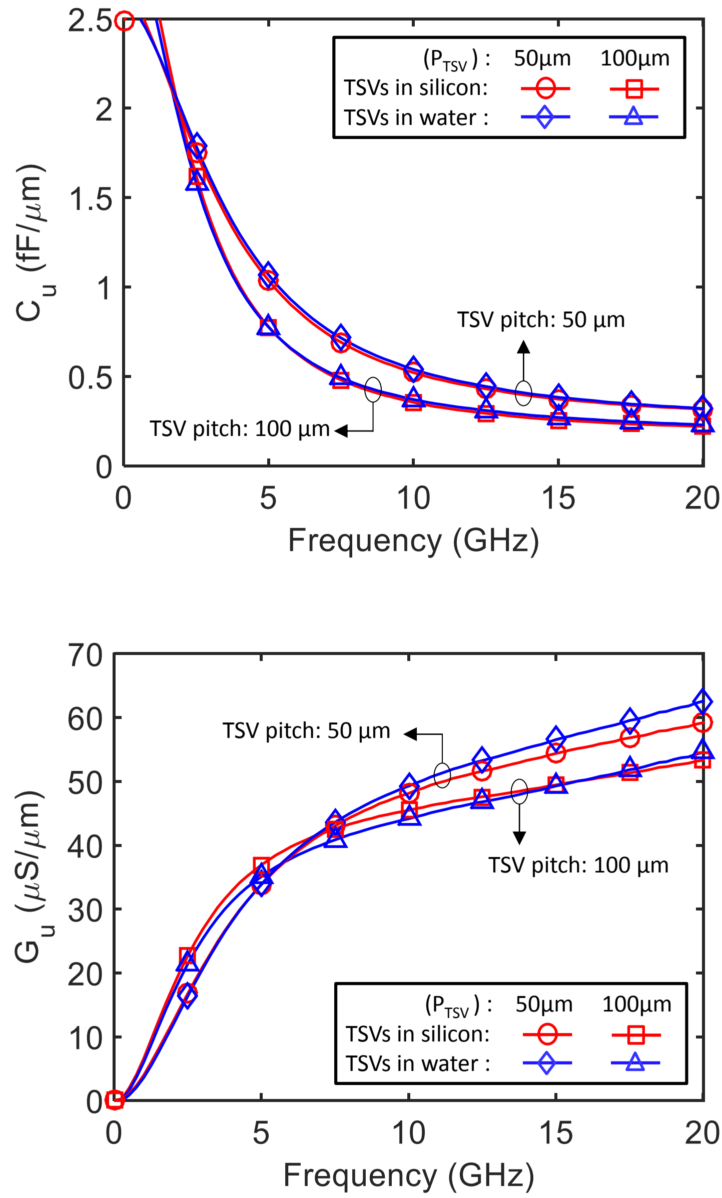


Figure 26. Extracted p.u.l. capacitance (top) and conductance (bottom) from measurements of TSVs in silicon and TSVs in deionized water. Two TSV pitches (100 μm and 50 μm) are shown in the plots.

3.6 Chapter Conclusion

This chapter, for the first time, experimentally analyzes the electrical performance of TSVs within distilled water for liquid-cooled microsystems. In this work, the fabrication of three diameters (50, 100, and 150 μm) of a silicon micropin-fin heat sink with embedded TSVs is presented. The fabricated testbed was assembled with a glass slide and filled with distilled water. The single-port measurements of ground-signal-ground (GSG) TSVs were performed for two cases: 1) conventional TSVs in a silicon substrate; and 2) TSVs within a micropin-fin heat sink surrounded by deionized water. The results demonstrate that TSVs within water have larger capacitance and conductance than TSVs in a silicon substrate due to the lossy characteristics of deionized water. As the volume of water increases between TSVs at a fixed TSV pitch, TSV capacitance and conductance increase at high-frequency. Moreover, a coaxial-like TSV configuration, which consists of multiple ground TSVs surrounding a center signal TSV, is proposed and demonstrated to shield signal TSVs from electrical variations caused by the working fluid.

CHAPTER 4.

AIR-ISOLATED THROUGH-SILICON VIAS FOR LOW-LOSS SILICON INTERPOSERS

This chapter introduces air-isolated TSVs for an envisioned thick silicon interposer supporting heterogeneous technologies. The electrical losses of the proposed air-isolated TSVs are compared to conventional TSVs of the same copper via dimensions, and the impact of air-isolation region widths between TSVs on the capacitance and the conductance of TSVs is quantified.

4.1 Introduction: Electrical-Mechanical Trade-offs of TSVs in Silicon Interposers

Figure 27 illustrates an envisioned silicon interposer supporting heterogeneous ICs with low-loss TSVs. In this example, two logic dice are assembled on the interposer and interconnected with high-density interconnects; the TSVs in the interposer are partially isolated by air. From an electrical perspective, TSV capacitance is proportional to the thickness of the interposer [63]. Moreover, TSV insertion loss is approximately proportional to the thickness of the interposer, as shown in Figure 28. The simulation results show that the TSV loss proportionally increases as the thickness of the interposer increases. Thus, a thinner silicon interposer is preferred to enhance the electrical performance of TSVs. On the other hand, from a mechanical perspective, the warpage of a wafer has an inverse relationship to its thickness; as the thickness of the wafer

decreases, the warpage increases [74]. Two warpage data points, which are marked in Figure 28 from [74], show that a thicker silicon interposer is preferred for thermomechanical reliability. This trend is opposite to that of TSV capacitance and loss. Thus, we propose the use of a relatively thick silicon interposer platform with low-loss TSVs to satisfy both mechanical and electrical constraints.

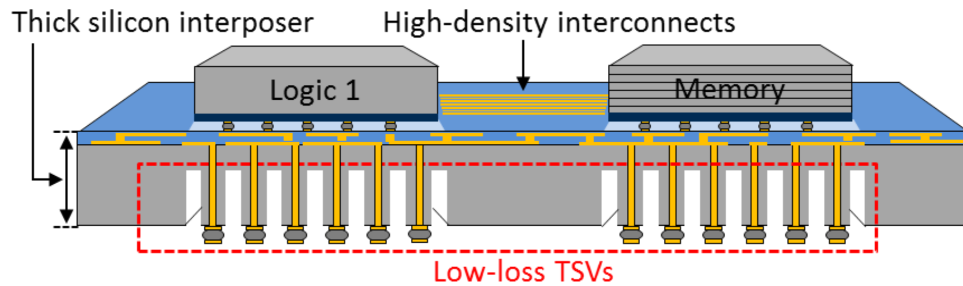


Figure 27. Schematic of a silicon interposer platform for heterogeneous integration with low-loss TSVs.

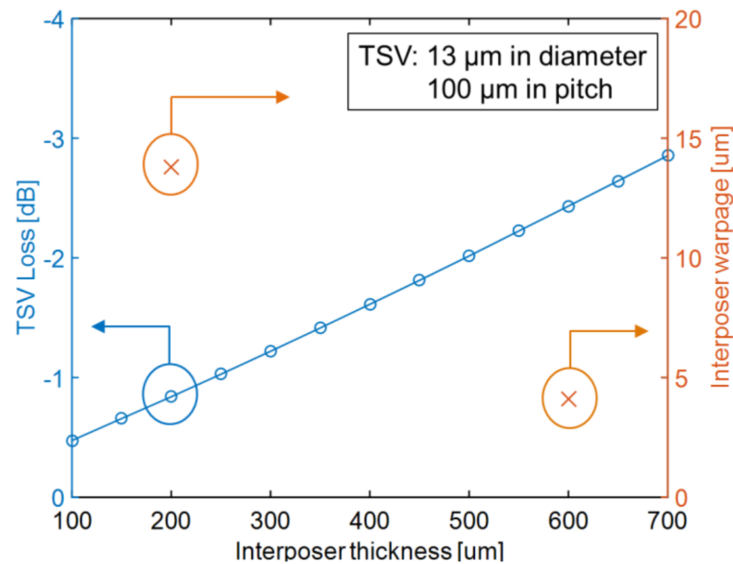


Figure 28. The results of TSV loss as a function of the interposer thickness. The two warpage data points are taken from [74].

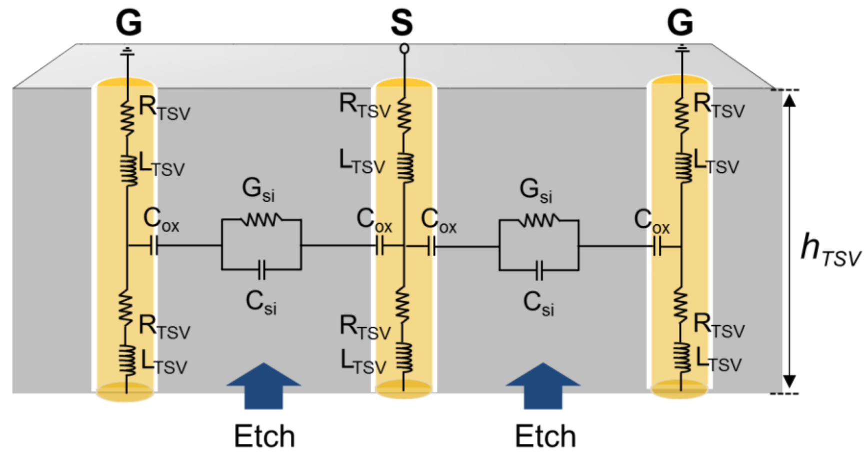
Figure 29 illustrates schematics of conventional and air-isolated TSVs along with their lumped circuit models [65]. In the model, the admittance portion of the air-isolated TSVs differs from conventional TSVs since there is an air region in parallel to a silicon base region, which partially isolates signal and nearby ground TSVs. This etched silicon region reduces TSV loss due to the reduced capacitance and conductance between TSVs. Table 7 summarizes the dimensions of the TSVs, the silicon pillars, and metal traces. Moreover, the L-2L de-embedding technique is applied to extract the loss of a TSV from the structure of TSVs and metal traces, as illustrated in Figure 30 [75].

Table 7. Dimensions of TSVs, silicon pillars, and metal traces[*].

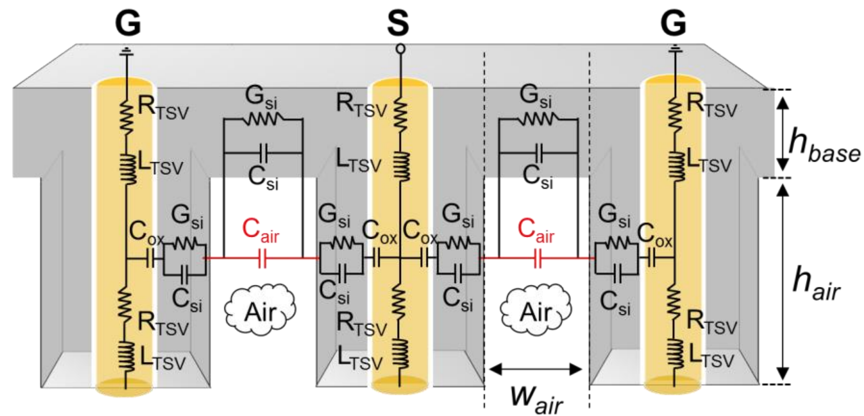
TSVs			Metal traces		Silicon pillars		
Radius	Height	Pitch	Top	Bottom	Width × Length	Height	w_{air}[**]
6.5	330	100/ 200	50 x 20	100 × 20 200 × 20	50 × 140 (L') 50 × 240 (2L')	230	50/100 /150

[*]All units are in microns.

[**]w_{air} refers to an air-isolation region width between silicon pillars. The widths of 100 μm and 150 μm are used only for a TSV pitch of 200 μm.



(a)



(b)

Figure 29. Lumped circuit models of (a) conventional TSVs and (b) air-isolated TSVs.

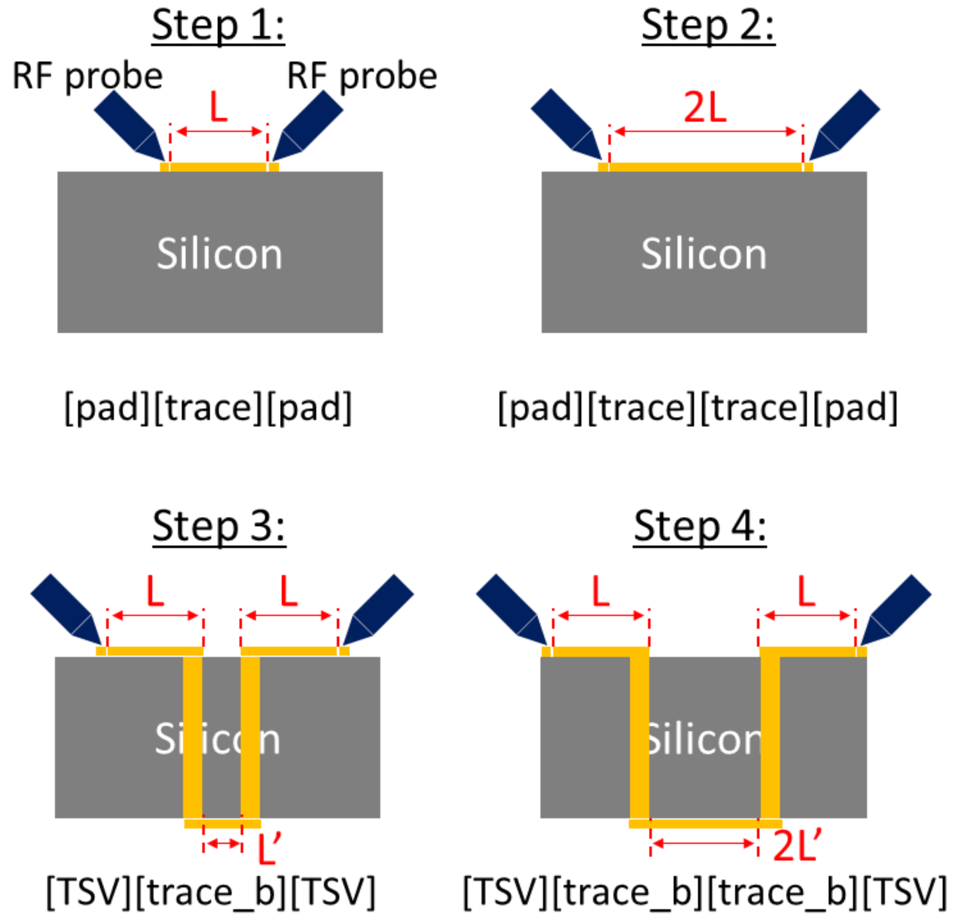


Figure 30. L-2L de-embedding technique containing four measurement steps for extracting the loss of a single TSV, or [TSV], from a trace-TSV-trace structure.

4.2 Literature Survey

To attain a significant reduction in TSV electrical loss, various approaches have been studied (as summarized in Table 8). Low-k materials and increased liner thickness were proposed to reduce capacitance and loss [63]. To reduce substrate losses at a higher frequency range, high-resistivity silicon and glass substrates were proposed [63],[76].

Moreover, instead of changing an entire substrate, several researchers have proposed the substitution of a localized silicon region with low-loss materials. One study proposed the formation of local polymer-wells with embedded TSVs in a silicon substrate [77]. In a similar manner, localized glass formation was demonstrated using glass reflow after partially etching a silicon substrate [78]. In addition, the formation of an air-gap between copper and silicon was proposed using propylenecarbonate (PPC) [79] or air trench formation [74]. The permittivity of air is approximately 1, and thus it is most attractive to use air for loss reduction. However, the fabrication of an air-liner or air-gap between copper and silicon is considered challenging since it requires additional materials and fabrication steps.

To address such challenges, this section discusses low-loss TSVs achieved by simply etching silicon that surrounds TSVs for silicon interposer applications [80]. This approach results in reduced loss, as well as capacitance of TSVs, while avoiding complex fabrication steps.

Table 8. Comparison of TSVs for electrical loss reduction in the literature

Parameters	P. Thadesar et al. [77]	J.-Y. Lee et al. [78]	V. Sukumaran et al. [76]	M. Sunohara et al. [74]	H. Oh et al. [80]	C. Huang et al. [79]
TSV diameter	65/100 μm	40 μm	15 μm (upper**) 7~8 μm (lower)	60 μm	13 μm	10/30 μm
TSV height	285 μm	100 μm	30 μm	350 μm	300 μm	50 μm
TSV pitch	250 μm	80/90/100 μm (TSV spacing)	27 μm	200 μm	100 μm	N/A
Low-loss technique	Localized SU-8 into silicon	Localized glass into silicon	Glass substrate	Air trench between silicon and copper	Air isolation in silicon	Air gap between silicon and copper
Low-loss formation	SU-8 fill after silicon etch	Glass reflow after silicon etch	Glass substrate	Silicon etch (width: 20~30 μm)	Silicon etch (width: 50 μm)	PPC*
Insertion loss	~1 dB @ 50 GHz	~0.4 dB @ 50 GHz	~0.1 dB @ 20 GHz	~6.2 dB @ 40 GHz	~0.5 dB @ 20 GHz	N/A
Characterization	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	Total loss of GSG TSVs and CPW	De-embedded single TSV loss	DC capacitance measurements

*PPC stands for propylenecarbonate.
**Tapered TSVs are shown with the dimension of 15 μm at an upper side and 7~8 μm at a lower side.

4.3 Fabrication of Air-isolated TSVs

Figure 31 summarizes the fabrication process for the air-isolated TSVs. Fabrication begins with the deposition of silicon dioxide followed by an anisotropic oxide etch. Using the etched oxide as a hard mask, the Bosch process is used to etch through the silicon wafer [Figure 31 (a)]. Following the Bosch process, thermal oxidation is performed to form a dielectric liner for the TSVs. To form a metal seed layer, titanium and copper are deposited using an e-beam evaporator on the back side of the wafer. The etched holes are filled with copper using bottom-up electroplating from the seed layer [Figure 31 (b)]. After electroplating, chemical mechanical polishing (CMP) is performed to remove over-electroplated copper. To facilitate probing, metal pads and traces are selectively deposited on TSVs at the both sides of the wafer. Lastly, the Bosch process is performed from the back side of wafer to attain the air-isolated TSV structure [Figure 31 (c)]. In this step, two lengths (L' and 2L') of rectangular silicon pillars are fabricated for L-2L de-embedding [68], as shown in Figure 32.

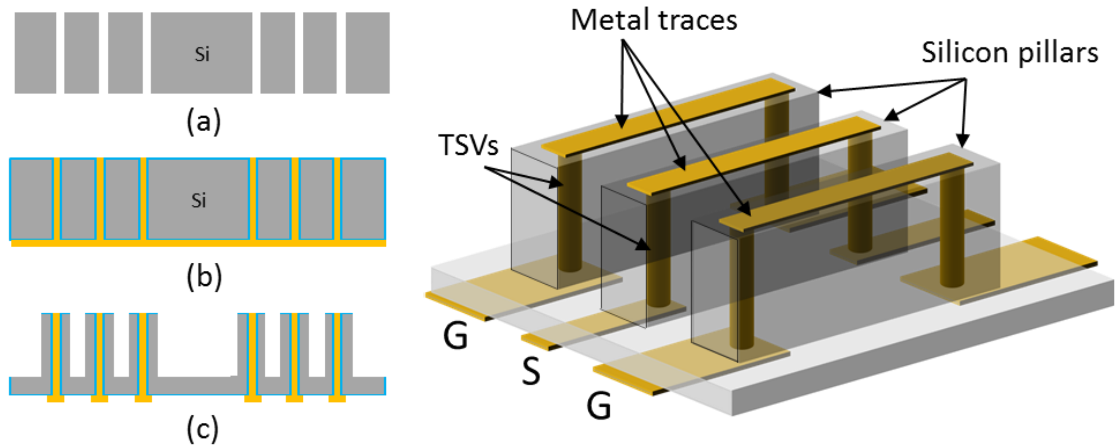


Figure 31. Overall fabrication process flow of air-isolated TSVs (left) and a 3D schematic of the proposed air-isolated TSVs for L-2L de-embedding (right).

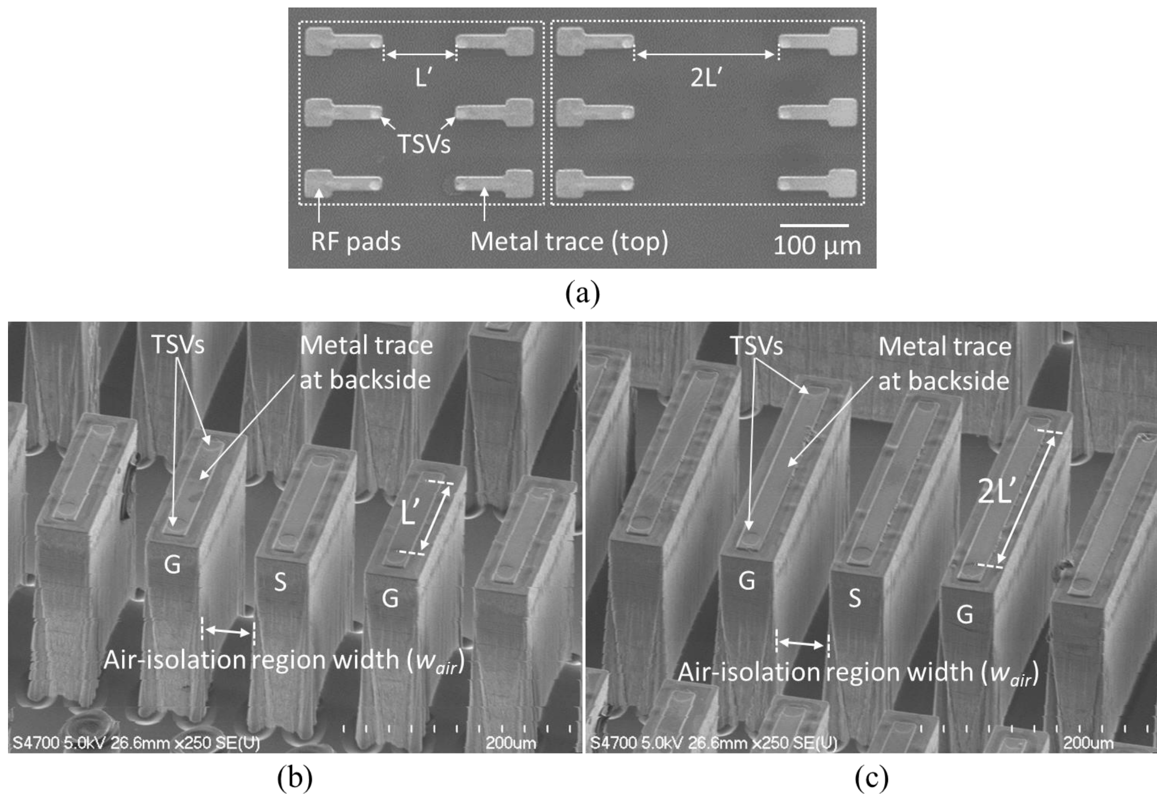


Figure 32. SEM images of air-isolated TSVs; (a) illustrates RF pads and metal traces with TSVs from the top side; (b) and (c) show etched silicon pillars with TSVs and back metal traces of lengths of L' and 2L', respectively.

4.4 High-Frequency Characterization of Air-Isolated TSVs

The fabricated testbed containing conventional and air-isolated TSVs is characterized using a microprobe station and an Agilent network analyzer. Using the de-embedding technique, the insertion loss of ground-signal-ground (GSG) TSVs is extracted from the measurements and the 3D full-wave simulations, shown in Figure 33. The results show a 46.7% reduction in the insertion loss using the proposed air-isolated TSV technique at 20 GHz compared to conventional TSVs. Following S-parameter to Y-parameter conversion, the capacitance and the conductance of TSVs are extracted as

$$C_{TSV} = Im\,(Y_{11} + Y_{12} + Y_{21} + Y_{22})\,/\,\omega \qquad (3)$$

$$G_{TSV} = Re\,(Y_{11} + Y_{12} + Y_{21} + Y_{22}) \qquad (4)$$

where ω is an angular frequency [64],[81]. To analyze the reduction in capacitance and conductance as a function of the width of the air-isolation region, three sets of air-isolated TSVs with air region widths of 50, 100, and 150 µm at a fixed TSV pitch of 200 µm are characterized. It is observed that as the width of air increases between TSVs (for fixed TSV pitch), or equivalently the amount of silicon volume decreases, the capacitance and the conductance of TSVs reduces, as shown in Figure 34. The results show that the capacitance of air-isolated TSVs decreases by 33.2 %, 48.0 %, and 63.2 % compared to the capacitance of conventional TSVs at 20 GHz with the air-isolation region widths of 50, 100, and 150 µm, respectively. In a same manner, the conductance of air-isolated TSVs decreases by 44.9 %, 55.7 %, and 63.6 %, respectively. The results are summarized in Table 9. The reduction in loss and capacitance will enhance digital signal transmission.

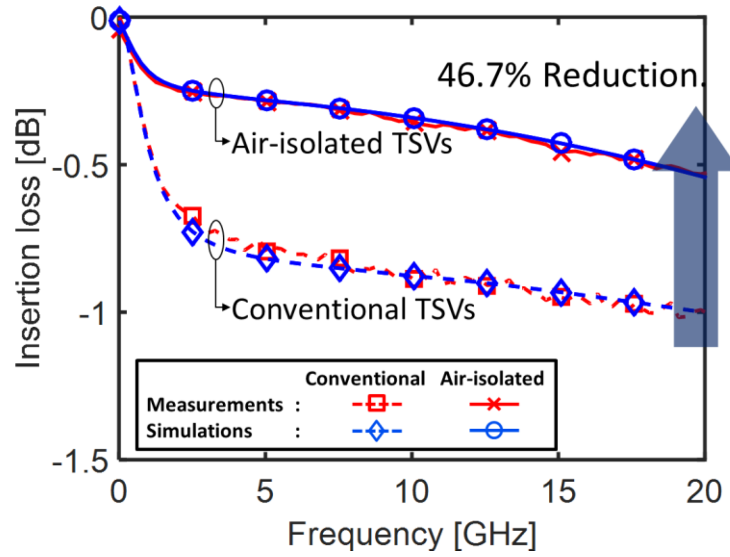


Figure 33. Insertion loss (S_{21}) comparison of conventional and air-isolated TSVs from measurements and simulations.

Table 9. Extracted capacitance and conductance from measurements: conventional and air-isolated TSVs with three air-isolation region widths at 20 GHz.

TSV Type	Conventional TSVs	Air-isolated TSVs		
		w_{air} = 50 μm	w_{air} = 100 μm	w_{air} = 150 μm
Capacitance	44.76 fF	29.90 fF	23.29 fF	16.46 fF
Reduction	N/A	33.2 %	48.0 %	63.2 %
Conductance	4.72 mS	2.60 mS	2.09 mS	1.72 mS
Reduction	N/A	44.9 %	55.7 %	63.6 %

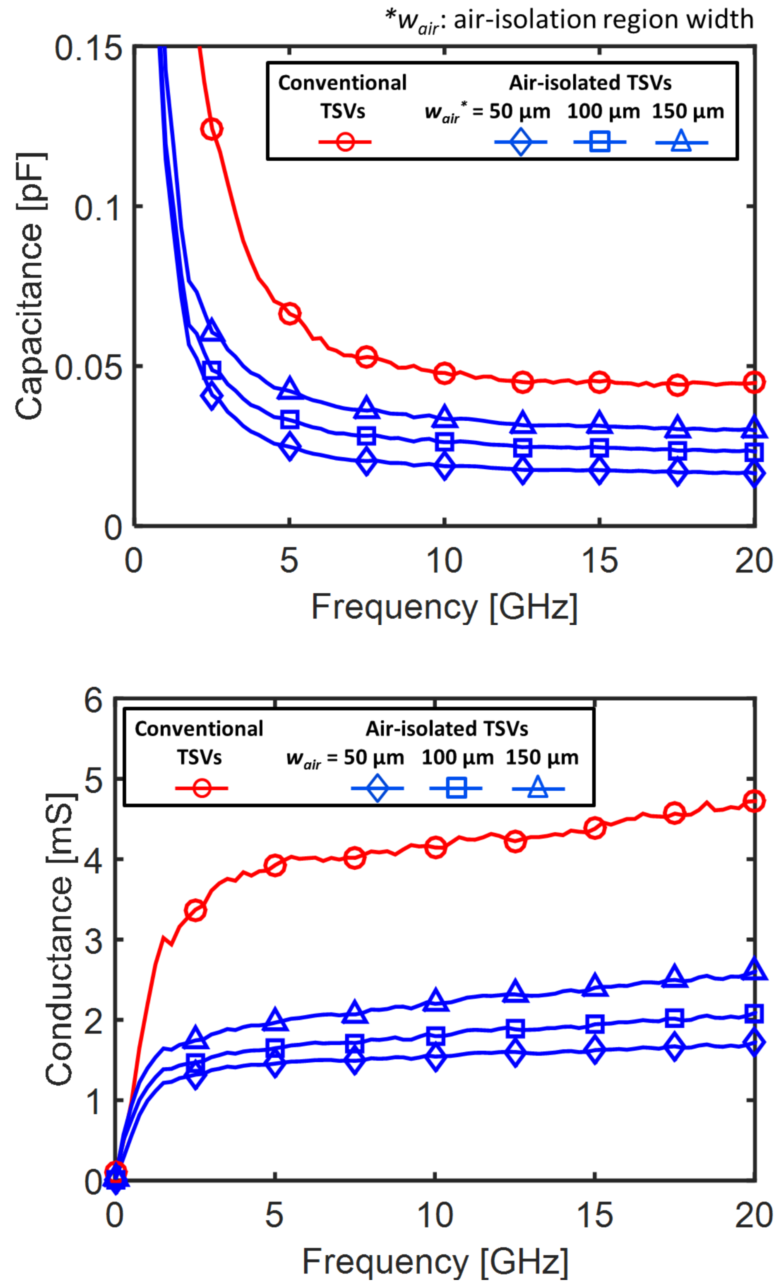


Figure 34. Extracted capacitance and conductance from measurements: conventional and air-isolated TSVs with three air-isolation widths.

4.5 Chapter Conclusion

This chapter proposes an air-isolated TSV technique for silicon interposers to reduce RF loss and capacitance. A testbed of conventional and air-isolated TSVs with L-2L de-embedding structures was fabricated and characterized from 10 MHz to 20 GHz. The measured results show that air-isolated TSVs reduce insertion loss by 46.7 % compared to conventional TSVs of the same copper via dimensions at 20 GHz. Moreover, the capacitance and the conductance of TSVs decrease as the air-isolation region width increases, showing a maximum capacitance and conduction reduction of 63.2% and 63.6%, respectively, for an air-isolation region width of 150 µm at 20 GHz.

CHAPTER 5

CIRCUIT MODELING OF TSVS EMBEDDED IN A SILICON MICROFLUIDIC PIN-FIN HEAT SINK FILLED WITH DEIONIZED WATER

5.1 Introduction and Literature Survey of TSV Circuit Models

Electrical characteristics of TSVs have been widely studied using various configurations that include ground-signal (GS), ground-signal-ground (GSG), and coaxial interconnect configurations [65],[82]-[86]. While electromagnetic-based models can be used to derive models that capture TSV parasitics [85],[86], these methods, in general, require relatively large computation time. To simplify the computation, Telegrapher's equations based on transmission line theory have been widely utilized to capture the electrical parasitics of TSVs, such as their resistance, inductance, capacitance, and conductance (RLCG), as functions of frequency. Several studies have analyzed the electrical characteristics of TSVs using lumped RLCG models [65],[81],[87],[88], where the use of pi- and T-models have led to simplified representations. In addition, the high-frequency characteristics of TSVs have been analyzed considering slow-wave, dielectric quasi-TEM and skin-effect modes based on substrate resistivity [65]. In [82], a detailed electrical model for TSVs that includes the interaction of microbumps and redistribution layers (RDL) has been discussed. The interactions between on-chip interconnects and TSVs have also been analyzed in terms of the performance of a 3-D link through

modeling and experiments in [83]. A distributed model using multi-segment RLC networks has been proposed in [84] to analyze the frequency-dependent behavior of TSVs. However, none of the published work in the available literature discusses the derivation of electrical models for TSVs in the presence of fluidic cooling. Moreover, using the above circuit models, it is not possible to model TSVs of the configuration shown in Figure 35, in which the TSVs are embedded in a silicon microfluidic pin-fin heat sink-immersed in deionized water. Specifically, our aim is to develop circuit models for the TSVs within a silicon substrate consisting of silicon cylinders (and surrounding deionized water) above a base silicon region and thus, the TSVs are essentially in a nonuniform medium.

In this section, circuit models are developed for TSVs embedded in a nonuniform medium. Specifically, this work focuses on the modeling of capacitance and conductance and the correlation of the derived models with simulations. Chapter 5.2 describes challenges and modeling approaches for such TSVs, and in Chapter 5.3, the circuit model for the TSVs is developed based on the theory of coaxial lines. Chapter 5.4 concludes the work.

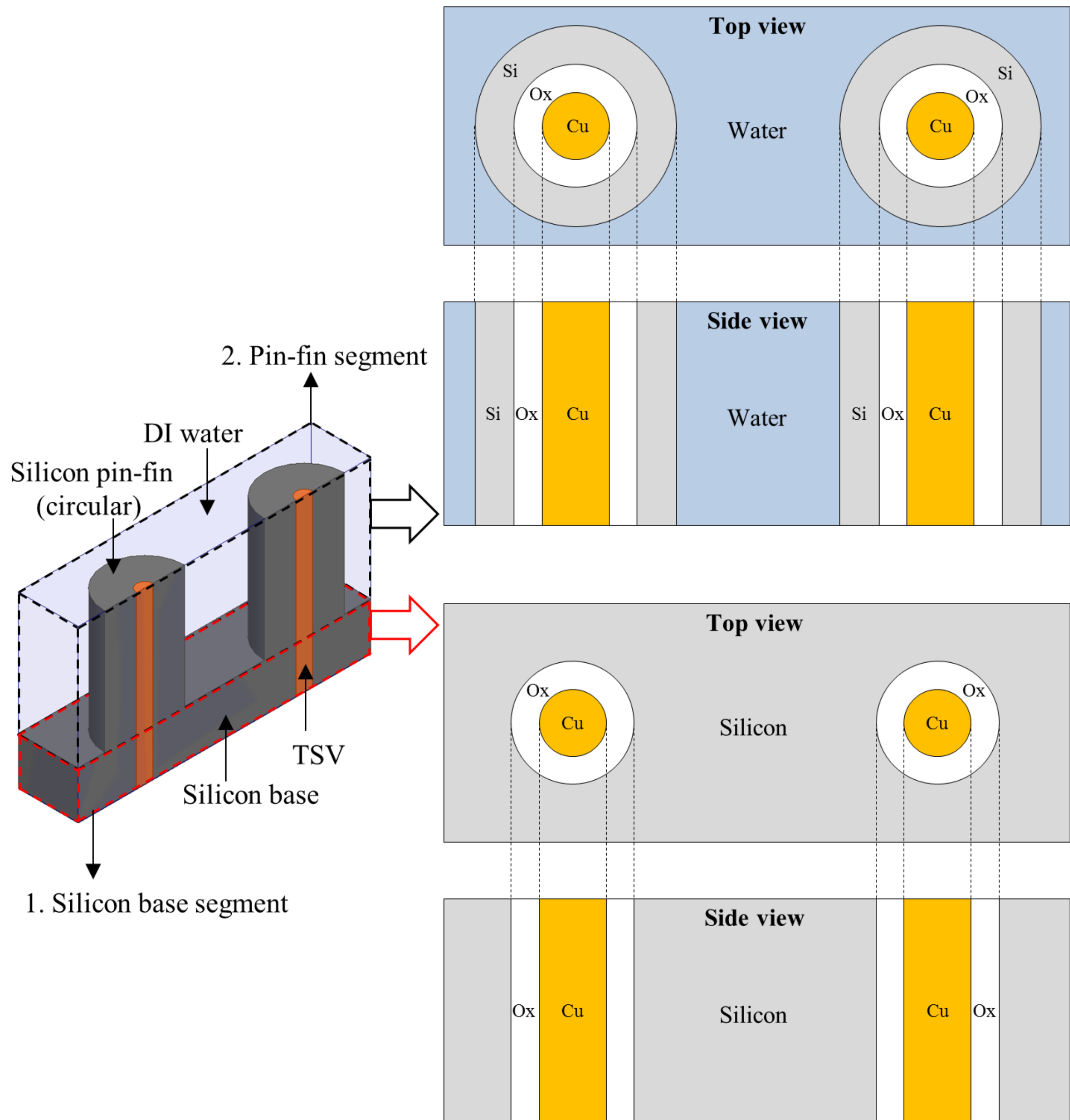


Figure 35. Modeling overview for TSVs in a silicon/water-mixed substrate with two segments. The first segment is for TSVs in a silicon substrate, and the second segment is for TSVs in circular silicon microfluidic pin-fins within a deionized water substrate.

5.2 Modeling Challenges and Approaches for TSVs Embedded in a Silicon Microfluidic Pin-Fin Heat Sink-Filled with Deionized Water

This section describes challenges and approaches for the modeling of TSVs embedded in silicon microfluidic pin-fins-filled with deionized water. As illustrated in Figure 35, TSVs are embedded in a nonuniform medium: the bottom portion of the TSVs is embedded in a silicon base, and the top portion of the TSVs is embedded in cylindrical silicon pin-fins with deionized water, which we refer to as "a pin-fin segment". First, such inhomogeneous (having more than one medium) structure cannot be modeled using conventional TSV circuit models [81]-[88]. Moreover, for our TSV configuration, resonance appears at several tens of gigahertz, and thus it is necessary to develop circuit models that capture their intrinsic resonance behaviors.

Unlike the permittivity of silicon that is almost constant (11.9), the permittivity of deionized water varies significantly with frequency [52],[53]. This frequency-dependent permittivity of deionized water is approximately 80 at DC and decreases as frequency increases. The permittivity becomes approximately 10 at 100 GHz, as shown in Figure 36. More importantly, the loss tangent of deionized water also varies with frequency. At DC, the loss tangent of deionized water is almost zero, acting as an insulator; however, as frequency increases, the loss tangent continues to increase and exceeds 1 beyond 20 GHz. The loss tangent can be derived from Ampere's law [89] as

$$\nabla \times \overline{H} = j\omega\varepsilon' \overline{E} + \left(\omega\varepsilon'' + \sigma\right)\overline{E} \tag{5}$$

$$\tan\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} \tag{6}$$

where ε', ε'', and σ, are real permittivity, imaginary permittivity, and conductivity, respectively. Here, the numerator of loss tangent, $\omega\varepsilon'' + \sigma$, is defined as effective conductivity, σ_{eff}, [89]. While the conductivity of deionized water is negligible (water conductivity of 0.5 μS/m used in [90]), the total effective conductivity of deionized water is relatively large, showing approximately 60 S/m at 50 GHz, as plotted in Figure 36. Considering silicon conductivity of 10 S/m is used in [90], the total effective conductivity of deionized water is relatively large. This is because the loss of deionized water is dominated by dielectric damping ($\omega\varepsilon''$), while the loss of silicon is dominated by conductivity loss (σ) [89].

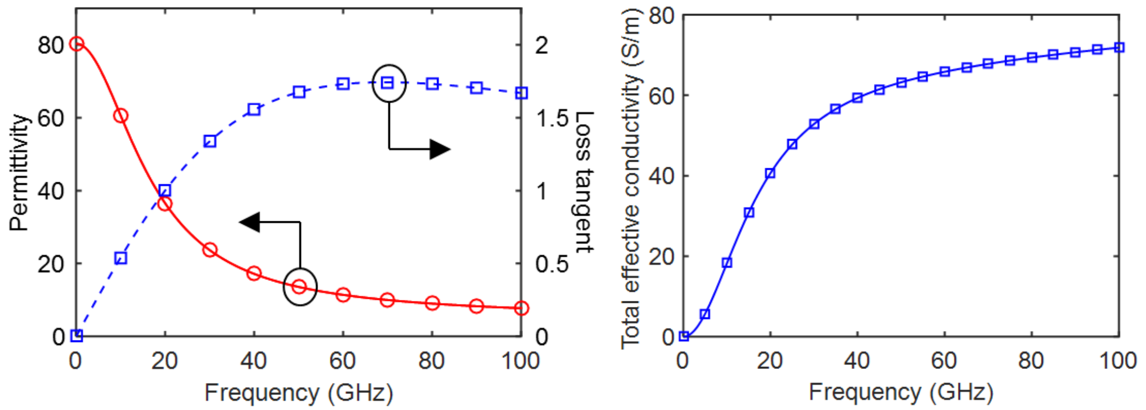


Figure 36. Electrical permittivity, loss tangent, and total effective conductivity of deionized water as a function of frequency [53].

Resonance appears when the imaginary part of impedance or admittance is canceled in any LC circuit, and thus TSVs, which are equivalently modeled with RLCG parameters, will exhibit resonance. Most TSV modeling studies [65],[82]-[88] do not account for the resonance behavior of TSVs because resonance typically does not appear in their frequency of interest (even up to 100 GHz) based on 'common' TSV dimensions.

However, in our case, resonance appears at several tens of gigahertz, and thus resonance should be accurately modeled. This is because our TSVs are embedded in an inhomogeneous structure of lossy silicon and high-permittivity deionized water, which results in effectively a large substrate capacitance. This large capacitance lowers the resonance frequency to the band of interest (since resonance frequency is inversely proportional to the square root of inductance and capacitance), which will be analyzed in the next sections.

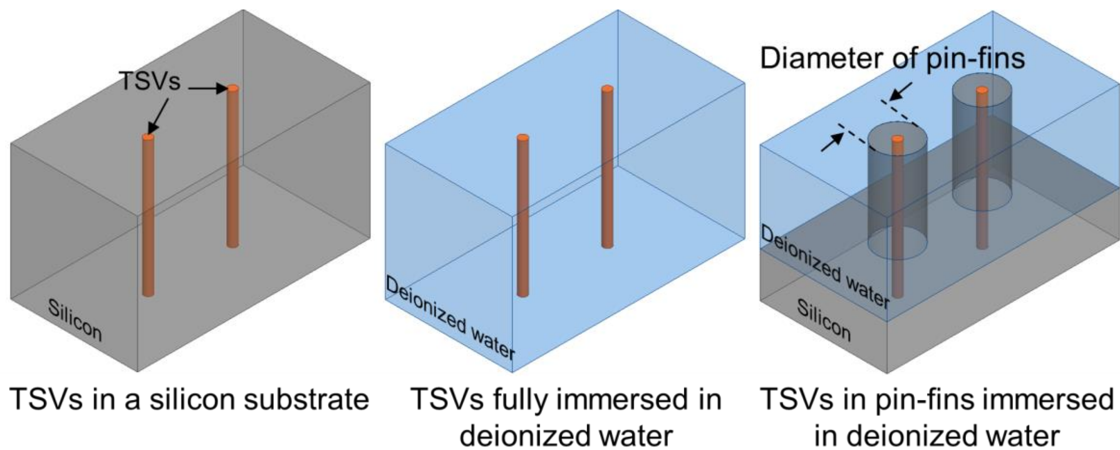


Figure 37. Three TSV configurations: TSVs in silicon (left), TSVs fully immersed in deionized water (middle), and TSVs in silicon microfluidic pin-fins immersed in deionized water (right).

Table 10. Resonance frequency of various TSV configurations extracted from HFSS simulations

TSV Type	TSVs in silicon	TSVs immersed in water	TSVs in pin-fins (D*=50um)	TSVs in pin-fins (D=100um)	TSVs in pin-fins (D=150um)
Resonance frequency	92.1 GHz	54.2 GHz	74.1 GHz	82.4 GHz	85.3 GHz

*D refers to the diameter of microfluidic pin-fins. The diameter, pitch, and height of the TSVs is 13 μm, 200 μm, and 330 μm, respectively, and the thickness of the oxide liner is 0.5 μm.

Figure 37 illustrates three TSV configurations used to compare the resonance frequency of TSVs in each substrate (TSVs in bare silicon, Copper-vias immersed in deionized water, and TSVs embedded in a silicon pin-fin heat sink filled with deionized water). The diameter, pitch, and height of the TSVs is 13 μm, 200 μm, and 330 μm, respectively, and the thickness of the oxide liner is 0.5 μm. Table 10 summarizes the resonance frequency of five TSV configurations using ANSYS high-frequency structure simulator (HFSS). First, the resonance frequency of TSVs in silicon and TSVs-fully-immersed in deionized water (without any silicon) are extracted. The resonance frequency of TSVs in silicon and TSVs-fully-immersed in deionized water appear around 90 GHz and 50 GHz, respectively. Next, three cases of TSVs in silicon microfluidic pin-fins-immersed in deionized water are compared with three silicon pin-fin diameters (50, 100, and 150 μm benchmarked from [90]). As expected, the resonance frequency of TSVs in silicon pin-fins-immersed-in deionized water appear between 50 and 90 GHz, depending on the geometry of silicon as well as the volume of deionized water.

To accurately model the resonance behaviors of TSVs, this work explores a distributed circuit model with segment number N, as illustrated in Figure 38. In this configuration, the length of TSVs is evenly divided by an integer factor, N, and the RLCG values of TSVs are also divided by a factor of N.

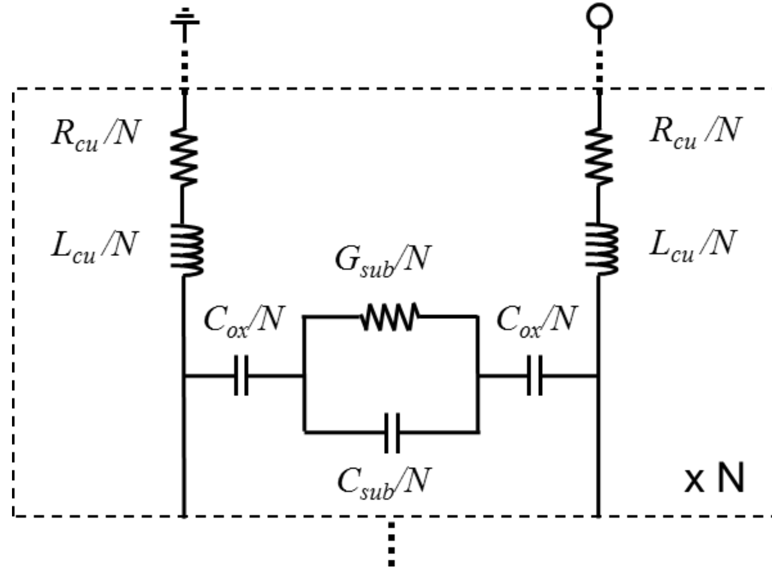


Figure 38. A distributed circuit model of TSVs with segment number N.

As an example, the capacitance and conductance of TSVs in silicon are extracted from analytical calculation (defined in Appendix A), lumped (pi- and T-) models [64],[88] using Keysight Advanced Design System (ADS), and HFSS simulations, as plotted in Figure 39. The pi- and T-models are relatively accurate up to 20 GHz. However, as we extend the analysis frequency up to 100 GHz, the results show a large discrepancy between the models and simulations; neither the capacitance/conductance values nor the resonance frequency/amplitude match. On the other hand, the proposed distributed circuit model successfully captures resonance, as plotted in Figure 40.

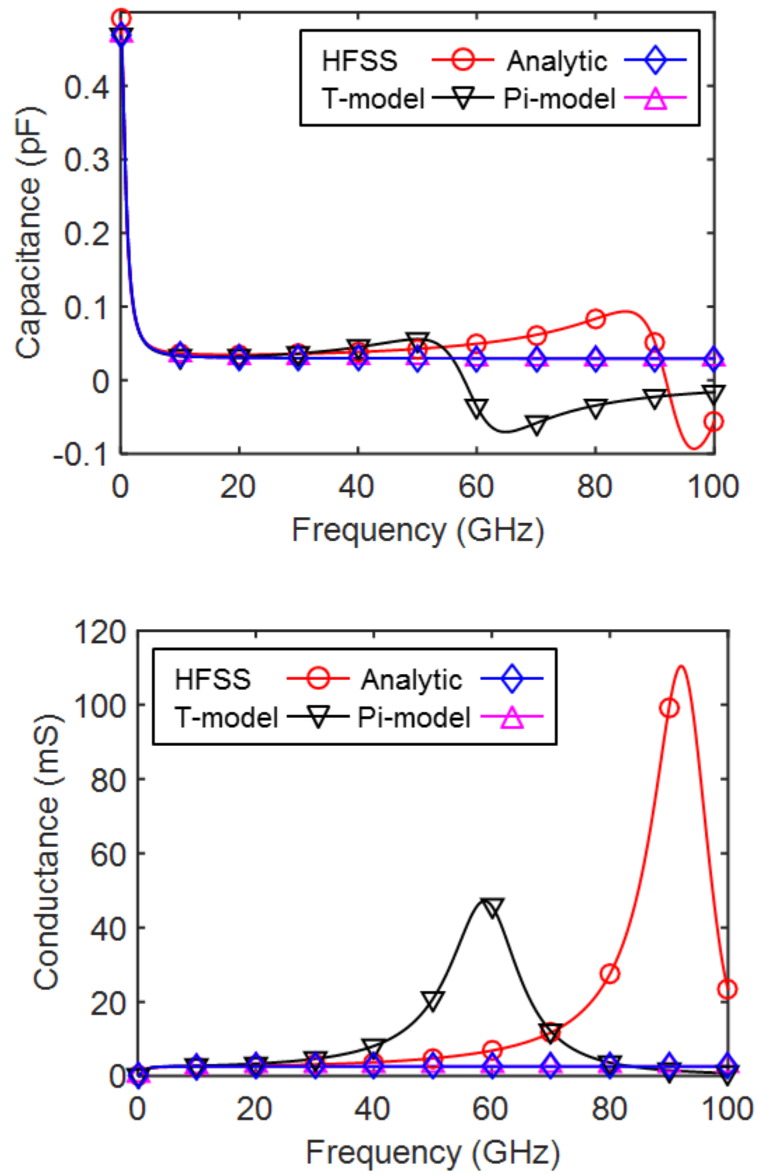


Figure 39. Extracted capacitance and conductance of TSVs in silicon using analytic calculation, lumped pi-model, T-model, and HFSS simulation up to 100 GHz.

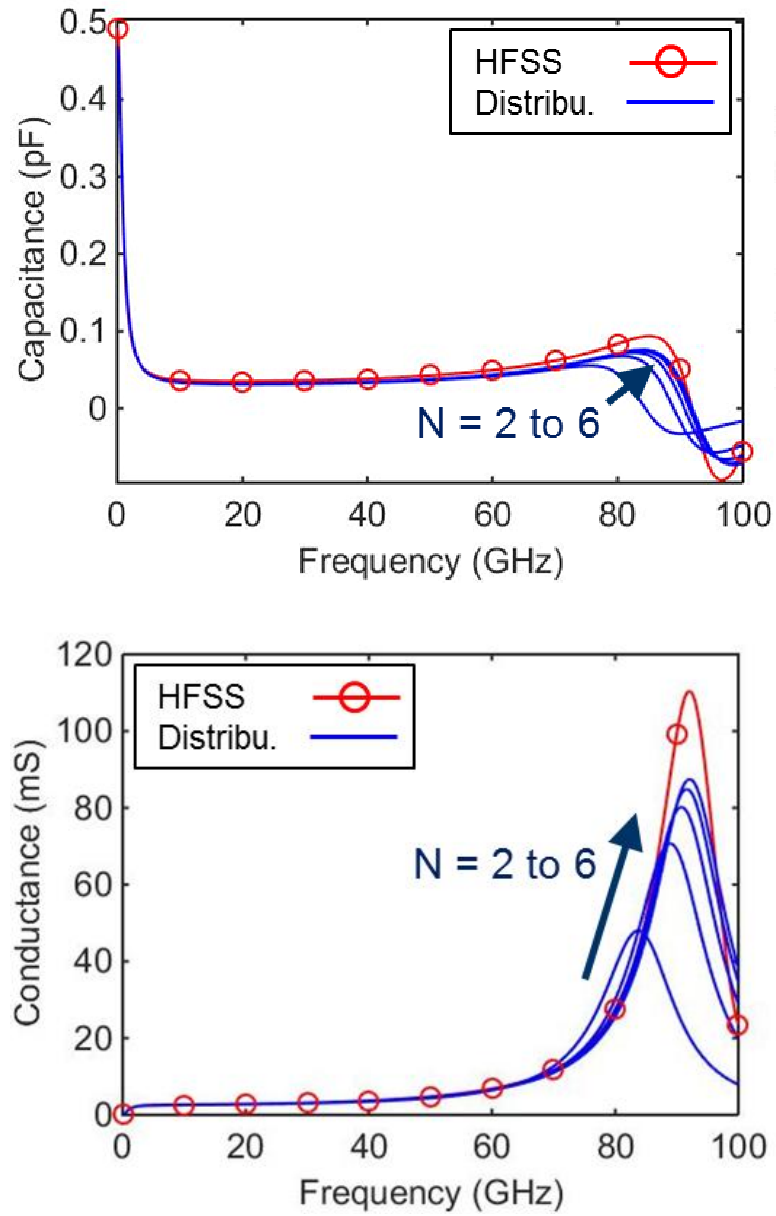


Figure 40. Extracted capacitance and conductance of TSVs in silicon using a distributed circuit model with respect to the number of distributions, or *N*, up to 100 GHz.

As we increase the segment number (N) from 2 to 6, not only does the resonance frequency increases, but also the magnitude. However, it should be noted that there is an optimal segment number beyond which the modeling results do not significantly change. For example, there is a large difference in resonance frequency/magnitude from $N = 2$ to $N = 3$, but the difference significantly reduces from $N = 5$ to $N = 6$. Moreover, a segment number greater than 6 does not improve the modeling results, exhibiting a negligible change. Thus, six, which gives a segment length of ~55 μm (330 μm divided by 6 segments), is an appropriate number for our distributed model. Table 11 summarizes resonance frequencies and peak conductance values with respect to the segment number, N.

Table 11. Resonance frequency, f_r, and its peak conductance value with respect to distribution number, N.

N	2	3	4	5	6	HFSS
f_r (GHz)	83.8	88.9	90.8	91.6	92.1	92.1
G_{peak} (mS)	48.0	70.7	80.2	84.9	87.5	110.4

The empirical formulas of TSVs in silicon are well-known [82]-[86] and summarized in Appendix A. Since this work discusses the modeling of TSVs in an inhomogeneous substrate, the feasibility of these circuit formulas for our TSV configurations should be investigated. First, the resistance and inductance of TSVs do not significantly change as a substrate changes; this includes our assumption that the proximity effect is not considered for sparsely distributed TSVs [91]. Thus, the resistance

and inductance formulas of (A.1) and (A.2) in the Appendix can be used in our circuit models without modification. However, the capacitance and conductance formulas of (A.3) and (A.4) are defined for homogeneous substrates. Thus, our inhomogeneous (silicon pin-fins and deionized water) substrate may not be modeled using the formulas. To this end, this work investigates the capacitance and conductance modeling of TSVs embedded in silicon pin-fins-immersed in deionized water. For validation, modeling results are compared with 3-D full-wave simulation results using HFSS throughout the work.

5.3 Modeling of TSVs in a Silicon Microfluidic Heat Sink-Immersed in Deionized Water

This section describes the modeling of TSVs in a silicon microfluidic pin-fin heat sink with the presence of deionized water using the distributed circuit model described in the previous section. First, the frequency-dependent characteristics of TSVs immersed in deionized water using a two-TSV model, and the modeling of TSVs in a pin-fin segment (the top schematic of Figure 35) are presented.

5.3.1 Circuit Model Validation for Deionized Water

As discussed in Section II, the permittivity and loss tangent of deionized water significantly change with operating frequency. While the circuit model described in the previous section works well with materials of constant conductivity, such as, silicon, or constant permittivity, such as polymer [77] or glass [76], there have been no studies on the electrical models of TSVs within frequency-dependent materials, such as deionized water. Thus, this section begins with the modeling of two TSVs fully immersed in deionized water, as illustrated in Figure 41, and compares the modeling results with simulations. In this model, the resistance, inductance, and capacitance terms can be used without any modification with respect to TSVs in silicon defined in the Appendix A. However, the conductance term should be redefined because the loss term of deionized water is defined by dielectric damping ($\omega\varepsilon''$) while the loss of silicon is defined by conductivity loss (σ) [89]. Thus, we propose to use effective conductivity, σ_{eff}, in the conductance terms for the rest of the chapter. The conductance of deionized water can be redefined as

$$G_{water} = \frac{\pi \sigma_{eff,water}}{\ln\left(\left(p_{TSV} / d_{TSV} \right) + \sqrt{\left(p_{TSV} / d_{TSV} \right)^2 - 1} \right)}. \tag{7}$$

where d_{TSV} and p_{TSV} are defined as the diameter and pitch of TSVs, respectively. Using the redefined conductance formula, the capacitance and conductance of TSVs fully immersed in deionized water are extracted from the distributed model and plotted in Figure 42. The model matches well with the simulations. It should be noted that the conductance of TSVs fully immersed in deionized water is much higher than that of TSVs in silicon before resonance. This is because the effective conductivity, σ_{eff}, of deionized water is relatively higher than that of silicon. Thus, it is expected that the TSV capacitance decreases as the diameter of pin-fins increases (or as the volume of water decreases), and vice versa.

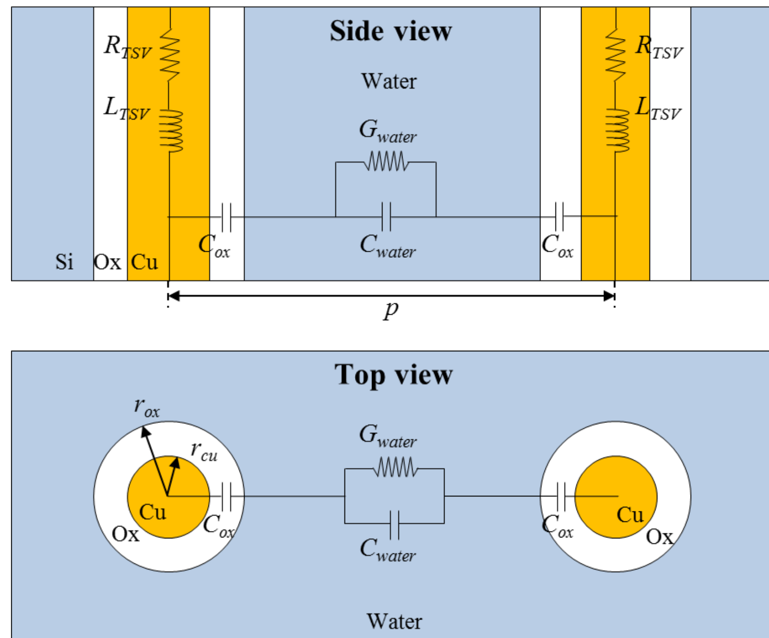
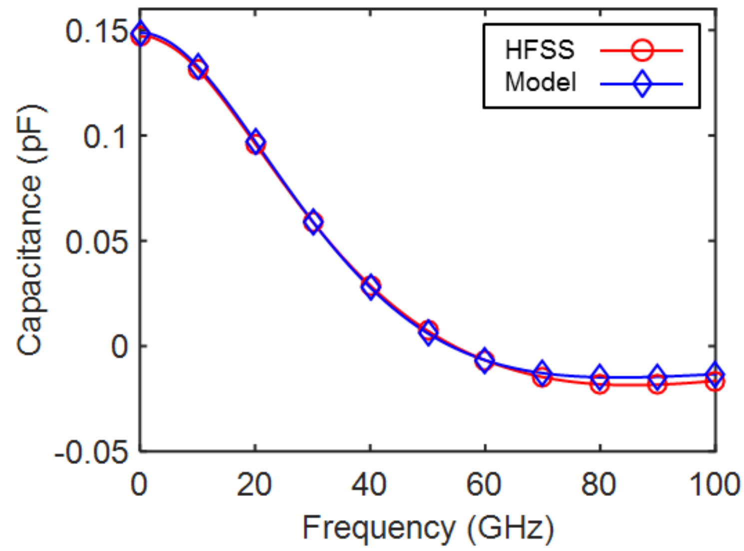
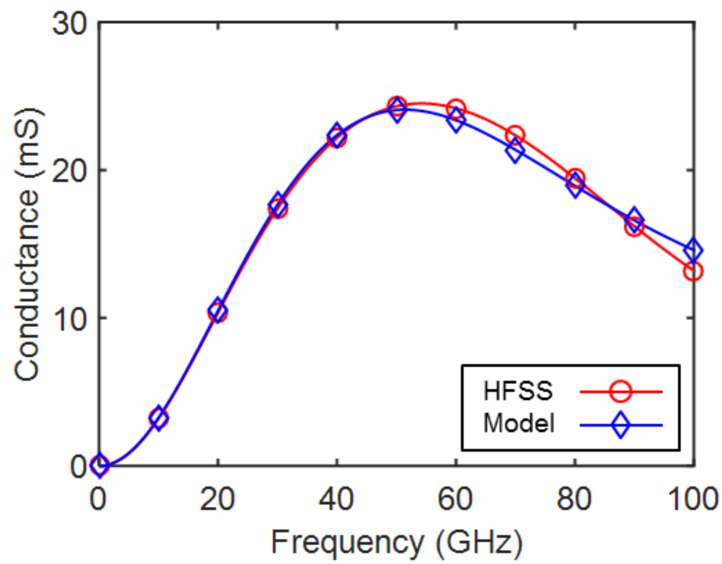


Figure 41. Circuit model of TSVs in a deionized water substrate from side and top views.



(a)



(b)

Figure 42. Extracted (a) capacitance and (b) conductance of TSVs fully immersed in deionized water using a distributed circuit model, compared with HFSS simulation.

5.3.2 Modeling of TSVs in a Pin-Fin Segment

Figure 43 illustrates the circuit configuration of a pin-fin segment. This configuration requires a new circuit model due to the increased complexity of the circular silicon pin-fins surrounding the TSV (with an oxide liner). Thus, this section discusses the modeling of multilayered (oxide and silicon) TSVs immersed in deionized water and compares the modeling results with simulations.

As illustrated in Figure 44 (a), conventional TSVs in silicon consist of a copper core with a single dielectric (oxide), which can be modeled using a single-dielectric coaxial-line equation defined in the Appendix (A.5). On the other hand, TSVs in a pin-fin segment consist of multilayers of oxide and silicon, as shown in Figure 44 (b). To equivalently model the multilayered TSVs using circuit elements, two-dielectric coaxial-line capacitance equations can be used as [92]

$$C_1 = \frac{2\pi\,\varepsilon_0\varepsilon_1}{\ln\left(\frac{b}{a}\right)}. \tag{8}$$

$$C_2 = \frac{2\pi\,\varepsilon_0\varepsilon_2}{\ln\left(\frac{c}{b}\right)}. \tag{9}$$

where ε_1 is the permittivity of the first dielectric, ε_2 is the permittivity of the second dielectric, a is the radius of a center core, b is the radius of the boundary between two dielectrics, and c is the radius of an outer shell, respectively. The derivation of two-dielectric coaxial-line capacitance equations is summarized in the Appendix B.

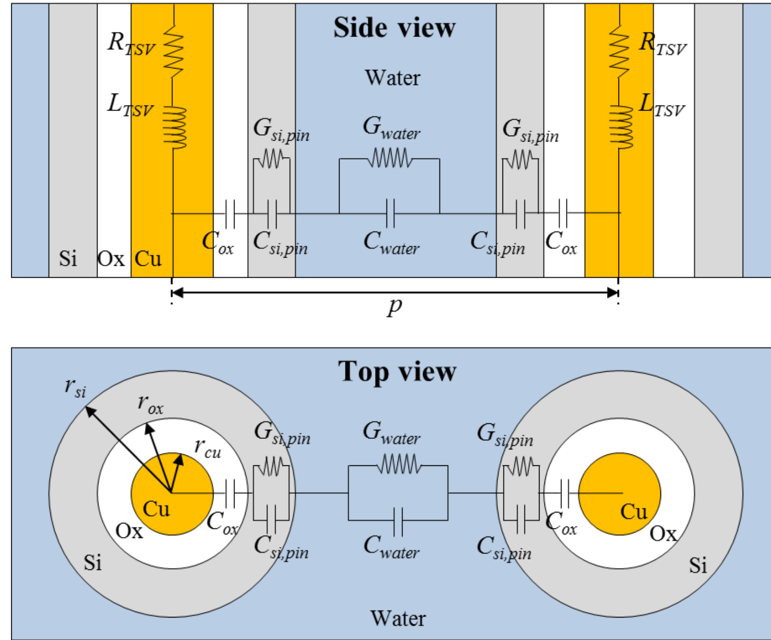


Figure 43. Circuit model of TSVs in a pin-fin segment from side and top views.

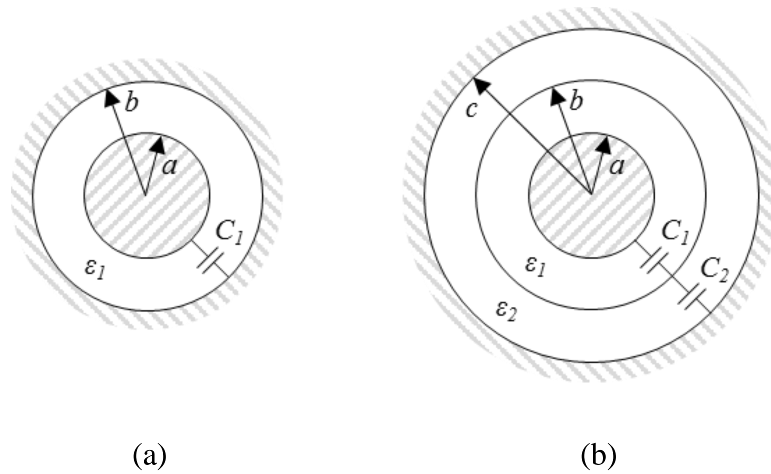


Figure 44. Cross-sectional schematics of (a) coaxial-lines with single dielectric with a permittivity of ε_1 and (b) two dielectrics with permittivities of ε_1 and ε_2.

For our TSVs under consideration, the first and second dielectric layers correspond to the oxide liner and the silicon pin-fin layer, respectively, as illustrated in Figure 43. First, the capacitance of the oxide liner, C_1, can be modeled using the coaxial-line capacitance equation defined in the Appendix (A.5). Second, the unit capacitance of silicon pin-fins can be defined using (9) as

$$C_2 = C_{si,pin} = \frac{2\pi\,\varepsilon_0\varepsilon_{si}}{\ln\left(\frac{r_{si}}{r_{ox}}\right)}. \tag{10}$$

Moreover, unlike an oxide liner, which is defined by only a capacitance term, the silicon pin-fins are defined by both capacitance and conductance terms since silicon exhibits a significant amount of conductor loss. This conductance term can be derived from its capacitance term; in which they have a relationship of [89]

$$G = \frac{\sigma_{eff}}{\varepsilon'} C. \tag{11}$$

Thus, the unit conductance of silicon pin-fins can be expressed using (10) and (11) as

$$G_{si,pin} = \frac{2\pi\,\sigma_{eff,si}}{\ln\left(\frac{r_{si}}{r_{ox}}\right)} \tag{12}$$

Lastly, the unit capacitance and conductance of deionized water should be redefined using two parallel conductor formulas from the boundary of one silicon pin-fin to the other pin-fin as

$$C_{water} = \frac{\pi\,\varepsilon_0\varepsilon_{water}}{\ln\left(\left(p/(2\,r_{si})\right)+\sqrt{\left(p/(2\,r_{si})\right)^2-1}\right)} \tag{13}$$

$$G_{water} = \frac{\pi \, \sigma_{eff,water}}{\ln\left(\left(p/(2\,r_{si}) \right) + \sqrt{\left(p/(2\,r_{si}) \right)^2 - 1} \right)}. \quad (14)$$

where r_{si} is the radius of silicon pin-fins. Using the defined capacitance and conductance in (A.5), (10), (12)-(14), the total admittance of the pin-fin segment, which is illustrated in Figure 43, can be computed. Moreover, it should be noted that this pin-fin segment consists of one water admittance, two oxide capacitances, and two silicon admittances in series. Therefore, the oxide and silicon terms are divided by a factor of 2. The total unit admittance of the segment can be expressed as

$$Y_{total} = \frac{j\omega C_{ox}}{2} \,||\, \left(\frac{G_{si,pin} + j\omega C_{si,pin}}{2} \right) ||\, \left(G_{water} + j\omega C_{water} \right) \quad (15)$$

The total unit capacitance of a pin-fin segment is extracted by taking the imaginary part of the total unit admittance divided by angular frequency. Similarly, total unit conductance is extracted by taking the real part of the total unit admittance. To compare the modeling results with HFSS simulations, the unit capacitance and conductance are multiplied by the height of the TSVs. Figure 45 illustrates TSV capacitance and conductance using analytical calculation and HFSS simulation up to 100 GHz when the diameter of pin-fins is 100 μm. Other dimensions of TSVs and pin-fins are summarized in Table 12. The analytical calculation gives quite accurate results up to 10 GHz, showing a maximum error of 6.2% and 1.3% in TSV capacitance and conductance, respectively. However, as frequency increases, the calculation results continue to deviate from the simulation results due to the presence of resonance. To capture resonances, the calculated admittance values are plugged into the distributed circuit model, and the results are plotted in Figure 45. It should be noted that the number of segments is chosen

where the modeling results saturate; in this case, the number of segments is chosen to be nine, in which the model clearly represents resonance.

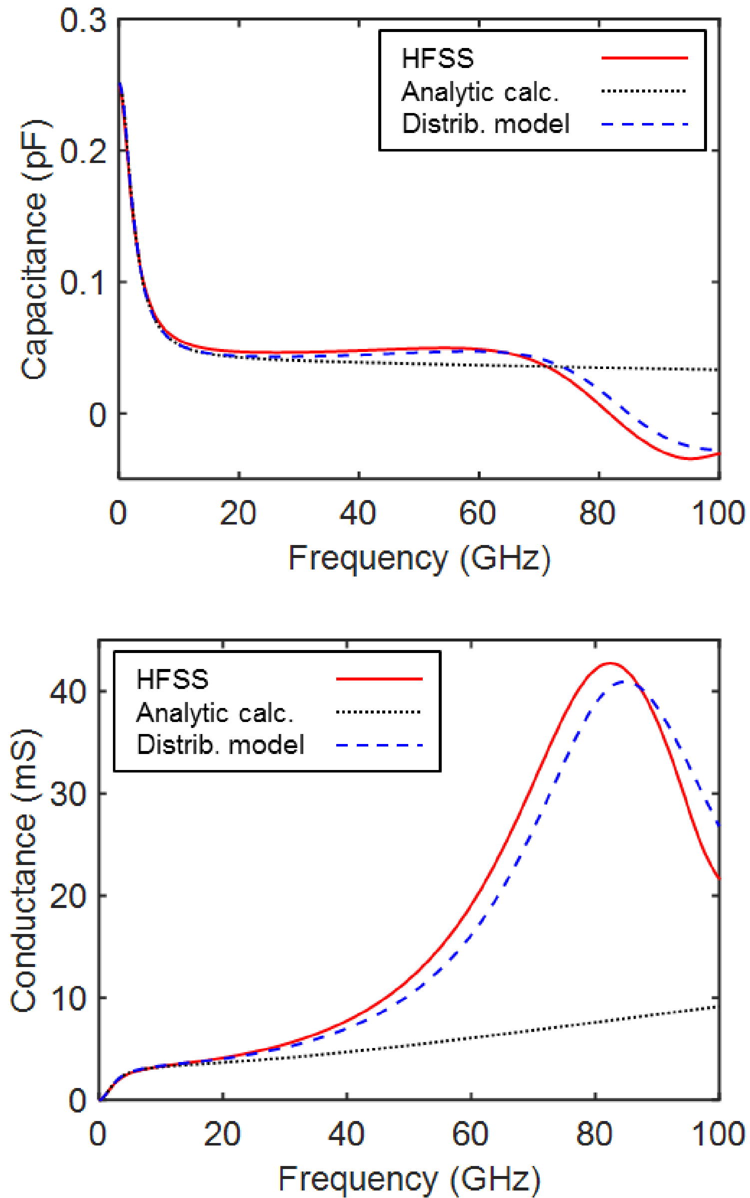


Figure 45. Capacitance and conductance of TSVs in a pin-fin segment using the analytic calculation, distributed circuit model, and HFSS simulations up to 100 GHz.

Table 12. Dimensions of TSVs and silicon microfluidic pin-fins.

Dimension	Diameter	Height	Pitch
TSV	13 μm*	330 μm	200 μm
Microfluidic pin-fin	50/100/150 μm	230 μm	200 μm

* Covered by a conformal oxide layer of 0.5 μm.

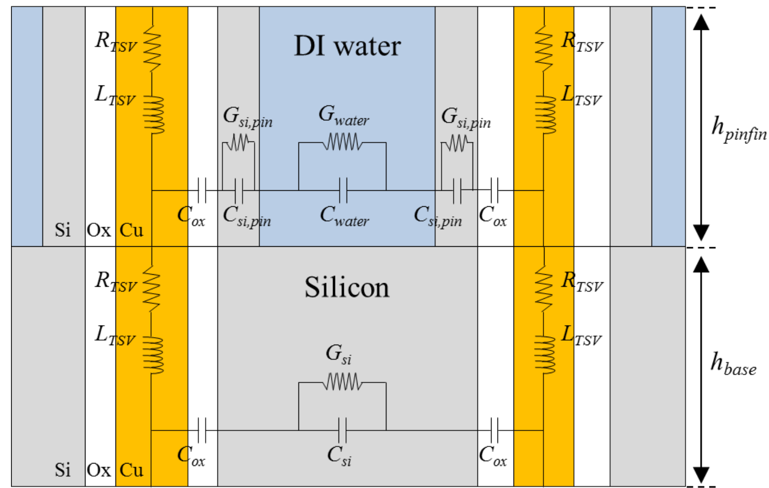
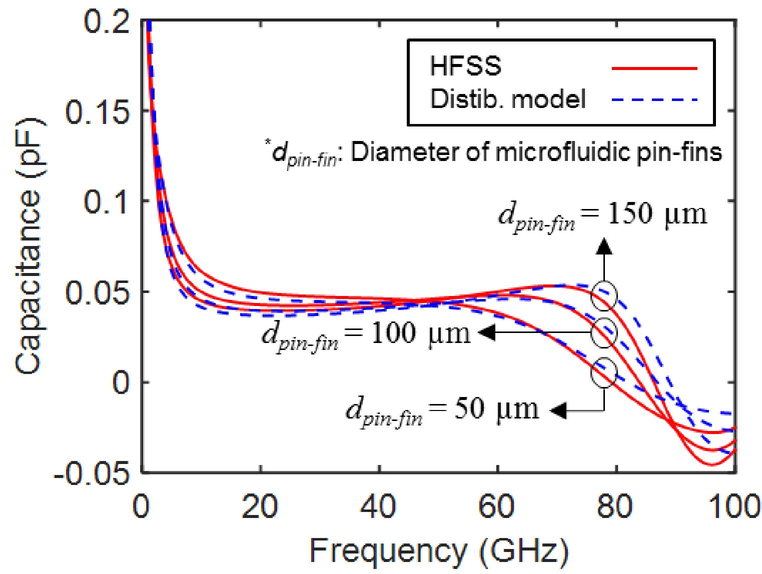


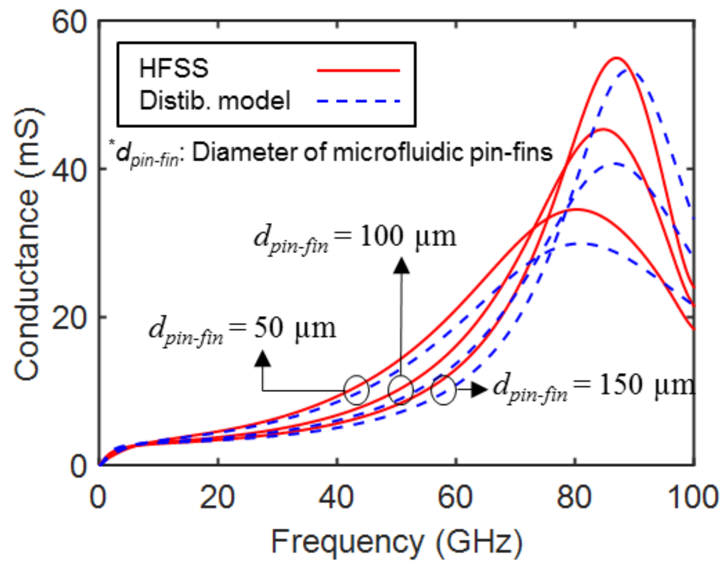
Figure 46. Modeling of TSVs in a silicon microfluidic heat sink with deionized water by integrating a silicon base segment and a pin-fin segment.

5.3.3 Modeling of TSVs in a Silicon Microfluidic Pin-fin Heat Sink-Filled-with Deionized Water by Integrating Two Segments

This section presents the last step of modeling for TSVs in a silicon microfluidic pin-fin heat sink-immersed in deionized water by integrating two segments: a silicon base segment and a pin-fin segment, as illustrated in Figure 46. The height of silicon base, h_{base}, and silicon pin-fin, $h_{pin\text{-}fin}$, are 100 μm and 230 μm, respectively. By multiplying the heights with the unit capacitance and conductance of each segment, the total TSV capacitance and conductance can be extracted by taking real and imaginary terms, respectively, as plotted in Figure 47. In the plots, three diameters (50, 100, and 150 μm) of silicon microfluidic pin-fins are chosen as benchmarked from [90]. As the diameter of pin-fins increases, or as the volume of water decreases between TSVs, the capacitance and conductance of TSVs decrease. Moreover, resonance frequency decreases as the diameter of pin-fins decreases; this can be seen from the peak point of conductance. This is because water capacitance is relatively larger than silicon capacitance as analyzed in the previous section.



(a)



(b)

Figure 47. (a) Extracted TSV capacitance and conductance using both approximation models and simulations (b) Extracted TSV capacitance and conductance for the water width of 50 and 100 μm using a volume-based model and simulations.

5.4 Chapter Conclusion

This work presents electrical circuit modeling of TSVs embedded in a microfluidic pin-fin heat sink immersed in deionized water. This chapter focuses on the extraction of capacitance and conductance and the correlation of the derived models with simulation and measurements. The circuit model consists of two segments: (1) a silicon base segment for the bottom part of TSVs and (2) a pin-fin segment for the top part of TSVs. Each segment is modeled based on the theory of coaxial lines; the silicon base segment is modeled using single-dielectric coaxial line equations, and the pin-fin segment is modeled using two-dielectric coaxial line equations. This work, for the first time, gives the electrical circuit models for TSVs in an inhomogeneous substrate of silicon and deionized water, and this modeling approach can be extended to various 3-D microsystem applications.

CHAPTER 6

SUMMARY AND FUTURE WORK

The chapter describes the summary of key research contributions followed by potential future activities.

6.1 Summary and Contribution of Presented Work

6.1.1 High-aspect ratio TSVs embedded in a silicon microfluidic pin-fin heat sink

The contribution of this chapter includes the fabrication and characterization of high-aspect ratio TSVs embedded in a microfluidic heat sink. The developed technologies in this research are described as follows. With respect to the first approach, TSVs with an aspect ratio of 23:1 are demonstrated using two types of silicon etch masks within a microfluidic pin-fin heat sink, followed by void-free TSV validation using X-ray inspection and four-point resistance measurements.

6.1.2 High-Frequency Analysis of TSVs Embedded in a microfluidic Pin-Fin Heat Sink with the Presence of Deionized Water

Moreover, to analyze the impact of microfluidic cooling on the electrical performance of TSVs, high-frequency measurements of TSVs within deionized water (deionized water presents between signal and ground TSVs) are performed from 10 MHz to 20 GHz using an Agilent network analyzer and Cascade microprobes. Extracted TSV capacitance and conductance from measurements are compared with conventional TSVs

in silicon; TSVs within deionized water have larger capacitances and conductance than TSVs in silicon due to the lossy characteristics of deionized water at high frequencies.

6.1.3 Air-Isolated TSVs for Low-Loss Silicon Interposer Platforms

Air-isolated TSVs are demonstrated for an envisioned thick silicon interposer supporting heterogeneous technologies. The low-loss TSVs are demonstrated by partially etching silicon between TSVs. Since TSVs are partially isolated by air, TSV loss and TSV capacitance reduce significantly. The proposed air-isolated TSVs exhibit significantly low electrical losses compared with conventional TSVs of the same copper via dimensions. Moreover, the impact of air-isolation region widths between TSVs on the capacitance and the conductance of TSVs is quantified.

6.1.3 Electrical Circuit Model of TSVs in a Silicon Microfluidic Pin-Fin Heat Sink with the Presence of Deionized Water

Electrical circuit modeling of TSVs is presented for the TSVs embedded in a microfluidic pin-fin heat sink with the presence of coolant. The model is based on the theory of coaxial lines with multilayer dielectric conditions. This chapter explores the electrical circuit modeling for TSVs in an inhomogeneous substrate of silicon and deionized water, and this modeling approach can be extended to various 3-D microsystem applications.

6.2 Future Work

The future research activities include firstly the analysis and measurements of TSV-to-TSV coupling within deionized water to assess the signal integrity of TSVs in liquid-cooled microsystems. Secondly, single TSV loss extraction would be performed within deionized water using an L-2L de-embedding technique. Thirdly, the impact of various liquids on the electrical characteristics of TSVs will be quantitatively analyzed. Lastly, the air-isolation technology will be applied to RF components, such as suspended antennas and inductors, for low-loss silicon microsystem platforms.

1. Single TSV loss extraction with microfluidic cooling using the L-2L de-embedding technique: as an extension of TSV capacitance and conductance extraction, single TSV loss within deionized water would be extracted using two-port measurements. For the insertion loss extraction of single TSV in pin-fins with deionized water, a TSV testbed containing micropin-fins with two-port measurement capability would be fabricated, and high-frequency measurements would be performed with the L-2L de-embedding technique [81]. The extracted loss of TSVs within deionized water will be compared to the loss of TSVs in a silicon substrate.

2. TSV coupling measurement with microfluidic cooling: TSV coupling measurements have been explored in the literature [66], [93] to analyze the impact on signal integrity. With the presence of deionized water, TSV coupling is expected to initially decrease at low frequency but significantly increase as the frequency increases due to the higher capacitive property of deionized water, as explored in Section 3. The measured TSV coupling within deionized water would be compared to the TSV coupling

in a conventional silicon substrate. These TSV coupling measurements are to be performed with different TSV distances.

3. TSV electrical characteristics with various fluids: as an extension of TSV performance with respect to deionized water, the electrical performance of TSVs will be quantitatively analyzed using various liquid fluids, such as nanofluids (water with nanometer-sized solid particles and fibers) [94] and liquid metals, such as, $Ga^{68}In^{20}Sn^{12}$, $Na^{27}K^{78}$, and *SnPbInBi* [95]. Moreover, the impact of two-phase cooling on TSV performance would be investigated.

4. RF silicon interposers with low-loss antennas/inductors: in addition to the air-isolated TSVs shown in Section 4, air isolation can help improve the performance of RF components such as antennas or inductors. This is because the presence of silicon underneath such components degrades radiation efficiency or Q factors, and this could be leveraged with the presence of air isolation between such components and a silicon substrate. RF silicon interposers would be demonstrated with air-isolated TSVs and RF components.

6.3 Research Conclusion

In this research, two key technology are demonstrated: (1) high-aspect ratio copper through-silicon vias embedded in a microfluidic heat sink and (2) low-loss through-silicon vias using air isolation. Their electrical model, microfabrication, and RF characterization are demonstrated. In the future, the demonstrated technologies would be implemented in system-level RF/millimeter-wave applications

APPENDIX A

ELECTRICAL CIRCUIT MODEL OF TSVS IN SILICON

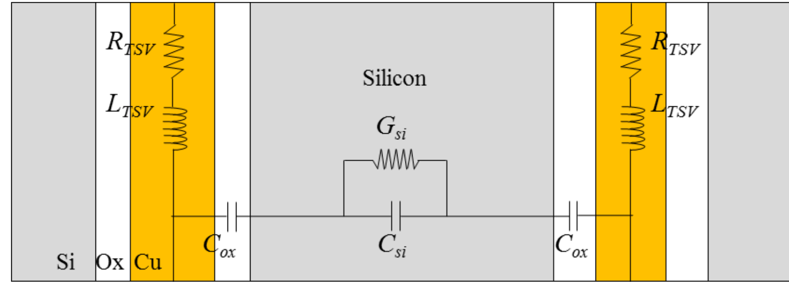


Figure A.1. Electrical circuit model of TSVs in silicon, consisting of copper as metal cores, silicon dioxide as insulator, and silicon as a substrate.

Figure A.1 illustrates the circuit model of TSVs in silicon, consisting of two parallel conductors (copper TSVs) in a substrate (silicon) with an insulator (silicon dioxide). The unit RLCG of this model exhibits empirical formulas given by (A.1)–(A.4), where σ_{cu} is the conductivity of copper, μ_0 is the permeability of free space, ε_0 is the permittivity of free space, and ε_{sub} is the permittivity of substrate material, respectively; r_{TSV}, d_{TSV}, h_{TSV}, and p_{TSV} are defined as the radius, diameter, height, and pitch of TSVs, respectively [65],[82]. In equation (A.1), the resistance of TSVs includes the effect of a skin depth (δ), which is defined by $\delta = \sqrt{\pi \mu_0 \sigma f}^{-1}$, where f is the operating frequency. In this model, the proximity effect is not considered for our TSV dimensions, in which TSV pitch is almost 20 times larger than TSV diameter [91].

$$R_{TSV} = \frac{1}{\sigma_{cu}\, \delta\, \pi\, r_{TSV}} \cdot \frac{p_{TSV}/d_{TSV}}{\sqrt{\left(p_{TSV}/d_{TSV}\right)^2 - 1}} \qquad \text{(A.1)}$$

$$L_{TSV} = \frac{\mu_0}{\pi} \ln\left(\frac{p_{TSV}}{d_{TSV}} + \sqrt{\left(\frac{p_{TSV}}{d_{TSV}}\right)^2 - 1} \right) \qquad \text{(A.2)}$$

$$C_{si} = \frac{\pi\, \varepsilon_0\, \varepsilon_{si}}{\ln\left(\left(p_{TSV}/d_{TSV}\right) + \sqrt{\left(p_{TSV}/d_{TSV}\right)^2 - 1} \right)} \qquad \text{(A.3)}$$

$$G_{si} = \frac{\pi\, \sigma_{si}}{\ln\left(\left(p_{TSV}/d_{TSV}\right) + \sqrt{\left(p_{TSV}/d_{TSV}\right)^2 - 1} \right)} \qquad \text{(A.4)}$$

In addition, a coaxial-line capacitance model is used for an oxide liner, which is a conformal layer between the copper TSV core and the silicon substrate, as in (A.5) [89].

$$C_{ox} = \frac{2\pi\varepsilon_0\varepsilon_{si}}{\ln\left(\frac{r_{TSV} + t_{ox}}{r_{TSV}} \right)} \qquad \text{(A.5)}$$

The total capacitance and conductance of TSVs can be analytically computed by calculating two oxide capacitances and a substrate capacitance in series [88] as

$$C_{Analytic} = \mathrm{Im}\left(\left(\frac{2}{j\omega C_{ox}} + \frac{1}{G_{sub} + j\omega C_{sub}} \right)^{-1} \right) / \omega \qquad \text{(A.6)}$$

$$G_{Analytic} = \mathrm{Re}\left(\left(\frac{2}{j\omega C_{ox}} + \frac{1}{G_{sub} + j\omega C_{sub}} \right)^{-1} \right) \qquad \text{(A.7)}$$

where *Im* and *Re* stand for imaginary and real parts, respectively, and ω is angular frequency. Alternatively, the total capacitance and conductance of TSVs can be extracted

from pi and T-models using y-parameters, converted from scattering parameters [64],[86], as defined in (A.8)–(A.9).

$$C_{Extracted} = \frac{\mathrm{Im}\left(Y_{11} + Y_{12} + Y_{21} + Y_{22}\right)}{\omega} \tag{A.8}$$

$$G_{Extracted} = \mathrm{Re}\left(Y_{11} + Y_{12} + Y_{21} + Y_{22}\right) \tag{A.9}$$

APPENDIX B

CAPACITANCE FORMULA FOR COAXIAL-LINES WITH MULTILAYER DIELECTRICS

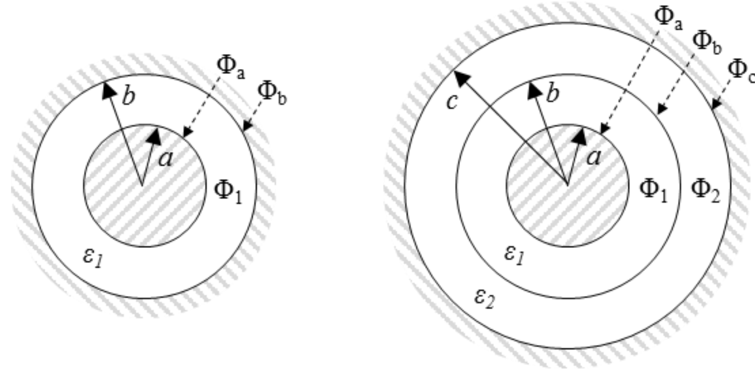


Figure B.1. Cross-sectional schematics of coaxial-lines with single dielectric with a permittivity of ε_1 (left) and two dielectrics with permittivities of ε_1 and ε_2 (right).

Figure B.1 illustrates the cross-sectional view of coaxial-lines with single and two dielectrics, respectively. Under transverse electromagnetic (TEM) mode, the capacitance of a coaxial-line with single dielectric is defined by total charge divided by potential difference between a core and an outer shell as

$$C_{water} = \frac{\pi \varepsilon_0 \varepsilon_{water}}{\ln\left(\left(p/(2 r_{si}) \right) + \sqrt{\left(p/(2 r_{si}) \right)^2 - 1} \right)} \tag{B.1}$$

where Q, Φ_a, Φ_b, and V_{ab} are total charge, potential at the core boundary of radius a, potential at the outer shell boundary of radius b, and potential difference between

boundaries a and b, respectively [92]. On the other hand, for a coaxial-line with two dielectrics, potential distributions in dielectrics 1 and 2 are defined as

$$\Phi_1 = V_0 \left[1 - \frac{\ln(r/a)}{\ln(b/a) + (\varepsilon_1/\varepsilon_2)\ln(c/b)} \right], \quad a < r < b \tag{B.2}$$

$$\Phi_2 = V_0 \frac{(\varepsilon_1/\varepsilon_2)\ln(c/r)}{\ln(b/a) + (\varepsilon_1/\varepsilon_2)\ln(c/b)}, \quad b < r < c \tag{B.3}$$

where r is a radius in the coaxial-lines, c is the outer shell boundary of dielectric 2, and V_0 is a potential at the center core with radius of a [92]. In this multilayered configuration, potential differences between dielectric boundaries a and b, V_{ab}, and boundaries b and c, V_{bc}, can be calculated from (20) and (21) as

$$V_{ab} = V_0 \frac{\varepsilon_2 \ln(b/a)}{\varepsilon_2 \ln(b/a) + \varepsilon_1 \ln(c/b)} \tag{B.4}$$

$$V_{bc} = V_0 \frac{\varepsilon_1 \ln(c/b)}{\varepsilon_2 \ln(b/a) + \varepsilon_1 \ln(c/b)}$$

Assuming there are same potential distributions in dielectric 1, or Φ_1, for the both cases in Figure B.1, the potential difference of dielectric 2 can be expressed using (22) and (23) as

$$V_{bc} = V_{ab} \frac{\varepsilon_1 \ln(c/b)}{\varepsilon_2 \ln(b/a)} \tag{B.5}$$

Thus, the capacitance of dielectric 2 can be defined as

$$C_2 = \frac{Q}{V_{bc}} = \frac{Q}{V_{ab}} \frac{\varepsilon_2 \ln(b/a)}{\varepsilon_1 \ln(c/b)} = C_1 \frac{\varepsilon_2 \ln(b/a)}{\varepsilon_1 \ln(c/b)} = \frac{2\pi\varepsilon_0 \varepsilon_2}{\ln(c/b)} \tag{B.6}$$

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