HETEROGENEOUS INTEGRATION OF CHIPLETS USING SOCKETED PLATFORMS, OFF-CHIP FLEXIBLE INTERCONNECTS, AND SELF-ALIGNMENT TECHNOLOGIES

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HETEROGENEOUS INTEGRATION OF CHIPLETS USING SOCKETED PLATFORMS, OFF-CHIP FLEXIBLE INTERCONNECTS, AND SELF-ALIGNMENT TECHNOLOGIES

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To

my parents and brothers

for their unconditional love and support

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LIST OF SYMBOLS AND ABBREVIATIONS

2D	Two-dimensional
3D	Three-dimensional
3D-MiM	3D MUST-in-MUST
ACF	Anisotropic conductive film
AI	Artificial Intelligence
ALD	Atomic layer deposition
AMD	Advanced Micro Devices
AMI	Acetone, methanol, and isopropanol
APS	Ammonium persulfate
Au	Gold
BARC	Bottom antireflective coating
BEOL	Back End of Line
BIM	Biosensing Interface Module
BOE	Buffered oxide etch
C4	Controlled Collapse Chip Connection
Cascade Lake AP	Cascade Lake Advanced Performance
CHIPS	Common Heterogeneous Integration and IP Reuse Strategies
CMI	Compressible MicroInterconnect
CMOS	Complementary metal-oxide-semiconductor
CMP	Chemical mechanical polishing
COTS	Commercial off-the-shelf
CPU	Central processing unit

CTE	Coefficient of thermal expansion
Cu	Copper
DARPA	Defense Advanced Research Projects Agency
DI water	Deionized water
DOE	Design of experiments
DP-QPSK	Dual-polarization quadrature phase shift keying
DRAM	Dynamic random-access memory
E-beam evaporation	Electron-beam evaporation
EMIB	Embedded Multi-die Interconnect Bridge
EPYC	Extreme Performance Yield Computing
FEA	Finite element analysis
FinFET	Fin Field-Effect Transistor
FPGA	Field-programmable gate array
GaAs	Gallium arsenide
GaN	Gallium nitride
GPU	Graphics processing unit
H_2O_2	Hydrogen peroxide
H_2SO_4	Sulfuric acid
HBM	High Bandwidth Memory
HIST	Heterogeneous Interconnect Stitching Technology
IC	Integrated Circuit
ICP	Inductively coupled plasma
IEN	Institute for Electronics and Nanotechnology
InFO	Integrated Fan-Out

InP	Indium phosphide
IoT	Internet of Things
IP	Intellectual property
KGD	Known Good Die
KOH	Potassium hydroxide
LGA	Land grid array
LNA	Low-noise amplifier
LPCVD	Low pressure chemical vapor deposition
MCS	Multi Channel Systems
MEA	Multi-electrode array
MEMS	Microelectromechanical systems
MFI	Mechanically Flexible Interconnect
MMIC	Monolithic microwave integrated circuit
MOGA	Multi-objective genetic algorithm
MUST	Multi-stack
NF	Noise figure
NiW	Nickel tungsten
NRE	Non-recurring engineering
NSGA-II	Non-dominated sorting genetic algorithm-II
NTI	Non-TSV Interposer
ODI	Omni-Directional Interconnect
PA	Power amplifier
PBS	Phosphate-buffered saline
PC (plating)	Pulsed current
PCB	Printed circuit board

pHEMT	Pseudomorphic high-electron-mobility transistor
PoP	Package-on-Package
PSAS	Positive self-alignment structures
QP	Quilt Packaging
RF	Radio frequency
RIE	Reactive ion etching
RTU	Ready-to-use
SAL	Sterility assurance level
SEM	Scanning electron microscope
Si	Silicon
Si_3N_4	Silicon nitride
SiGe	Silicon germanium
SiP	System-in-Package
SLIM	Silicon-Less Integrated Module
SLIT	Silicon-Less Interconnect Technology
SNR	Signal-to-noise ratio
SoC	System-on-Chip
SoL	Sea of Leads
SSE	Sum of squares error
T_g	Glass transition temperature
Ti	Titanium
TiN	Titanium nitride
TMAH	Tetramethylammonium hydroxide
TSMC	Taiwan Semiconductor Manufacturing Company
TSV	Through-silicon via

UV	Ultraviolet
VPD	Vertical plastic deformation
WAVE	Wide area vertical expansion

SUMMARY

Non-permanent, fine-pitch heterogeneous integrated systems and their enabling technologies are introduced and developed throughout this thesis. The key technologies to enabling this non-permanent, tightly integrated system are: 1) a non-permanent off-chip, fine-pitch interconnect technology and 2) a non-permanent alignment (self-alignment) technology. This thesis presents the use of three different fine-pitch interconnect technologies in such non-permanent integrated systems: Mechanically Flexible Interconnects (MFIs), Compressible MicroInterconnects (CMIs), and PariPoser. MFIs and CMIs (which are implemented throughout the majority of the thesis) are both compliant interconnects and given the significant role assumed by these interconnects for non-permanent integrated systems, a chapter in this thesis is dedicated to the optimization of a wide variety of complaint interconnect technologies. Experimental data of the fabricated optimized compliant interconnects demonstrated approximately 30% improvement in the interconnect's mechanical performance (e.g., lower maximum von Mises stress) relative to non-optimized designs.

This thesis also presents the implementation of three different self-alignment technologies: Ball-in-Pit, PSAS-in-Pits, and PSAS-to-PSAS. The PSAS-to-PSAS is an original work and is expanded upon in detail. This PSAS-to-PSAS technology is substrate material agnostic, rendering it a valuable self-alignment mechanism, especially in the context of heterogeneous systems. This technology has been demonstrated to achieve sub-micron alignment accuracy.

Finally, this thesis presents two novel, socketed, non-permanent heterogeneous integrated systems: the **B**io-sensing **I**nterface **M**odule (BIM) intended for bio-sensing applications and the re**P**laceable, **IN**tegrated **CH**iplet (PINCH) assembly intended for heterogeneous integrated applications. Design and engineering, fabrication and corresponding fabrication challenges, and experimental data (e.g., alignment, electrical) are all demonstrated for these two integrated systems. The aforementioned enabling technologies are also incorporated into these systems.

CHAPTER 1. INTRODUCTION

1.1 Growing Need for Heterogeneous Integration

Emerging applications including machine learning, 5G, cloud computing, Internet-of-Things (IoT), autonomous vehicles, and artificial intelligence (AI) require an ever-increasing demand in increased compute capabilities and functionalities. This demand increase is reflected, in part, in the growing volume of the datasphere, which is estimated to reach 175 zettabytes globally by 2025 as demonstrated in Figure 1 [1] (one zettabyte is equivalent to one trillion gigabytes).

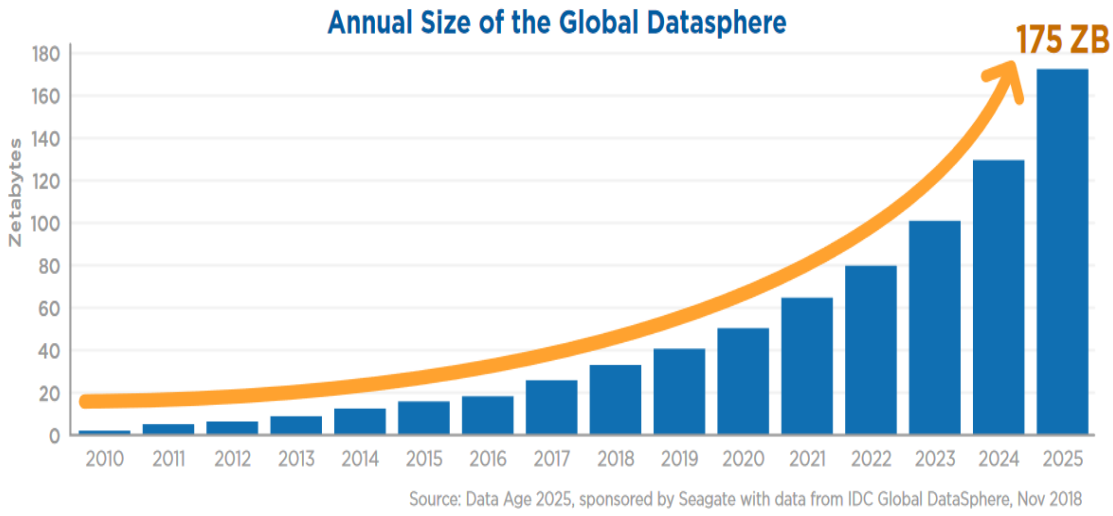


Figure 1. Annual size of the global datasphere [1].

A conventional means to meeting computational and functional demands has been to increase the number of integrated transistors and functional blocks within the same monolithic IC system (e.g., system-on-chip [SoC]) partially via transistor scaling (i.e.,

Moore's law). Efforts to sustain this improved performance via continued scaling has been facilitated via several innovations including high-k gate dielectrics [2], [3], Cu on-chip interconnects [4], [5], multi-core parallel processing [6], on-chip low-k dielectrics [7], strained silicon [8], and multi-gate transistors (e.g., FinFET) [9].

However, not all systems would benefit from scaling alone. Certain systems may require a larger degree of functionality via the incorporation of a wider variety of functional blocks (e.g., MEMS, photonics, RF, logic, analog) and there are potential limits to the degree of complex functionality that can be integrated into a single, monolithic die (e.g., SoC), especially with performance in mind. For example, certain material substrates are better suited to achieve optimal performance versus other material substrates for certain applications: GaN for power amplifiers to achieve higher power densities [10], SiGe for certain high-frequency applications including automotive radar [11], GaAs pHEMTs for LNAs that require low noise figures (NFs) and a wide broadband performance [12], fused silica to provide a low-loss dielectric substrate for mm-wave applications including 5G [13], and InP photodiodes for high-performance DP-QPSK receivers [14]. Additionally, SoCs that require a high degree of functionality may also suffer from high design costs and a prolonged time-to-market, which may prove especially challenging for fast-pace, emerging markets such as IoT or low-to-medium volume markets including the defense industry [15], [16].

In general, several challenges and limitations facing SoCs can be summarized as follows: (1) a slowdown in Moore's law (Figure 2) due to, in part, the surging cost of development for advanced technology nodes [17], [18], which may contribute to an increase in the size of the SoC to meet surging performance and functionality demands, (2) a decrease in wafer

yield in the case where said larger SoC die are required for certain applications (Figure 3) [19], [20], (3) reticle size limitations for a single die, (4) increased SoC design costs and design lead times as systems move towards more advanced technology nodes, especially as IP availability at these more advanced technology nodes become limited (Figure 4 and Figure 5) [21], and (5) less optimal die performance due to the inability to use the most optimal material substrate for a specified application [22].

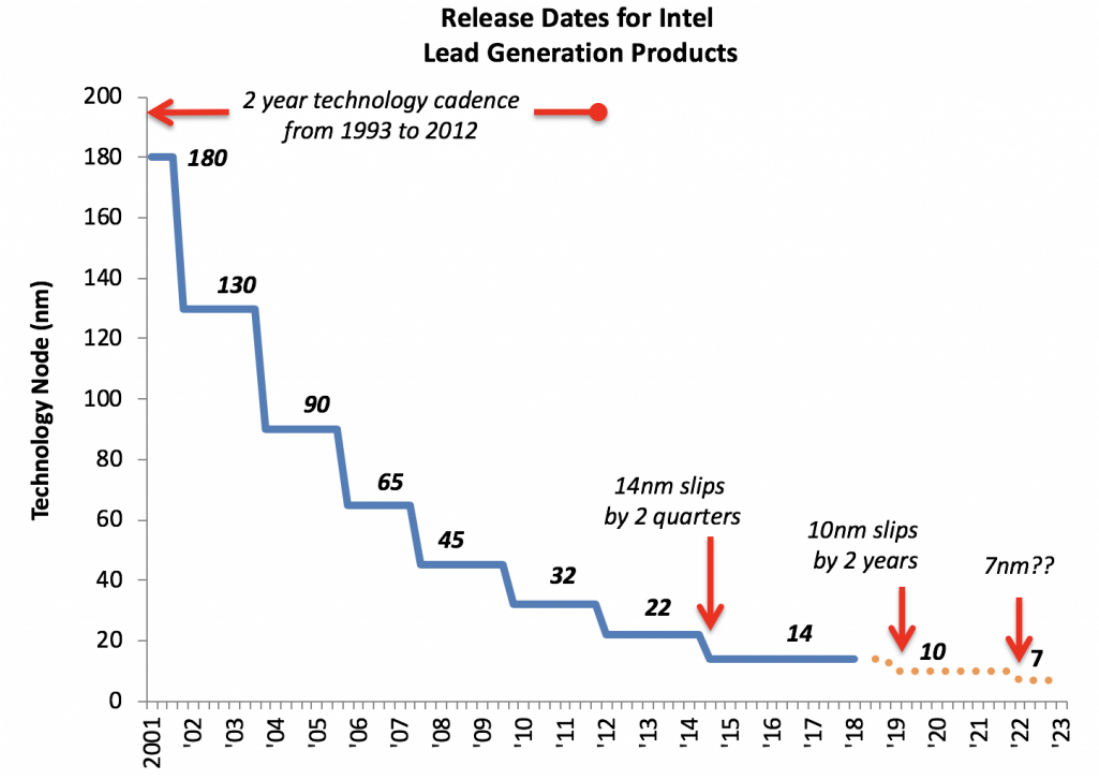


Figure 2. Advanced technology nodes are taking longer to develop as seen via the delay in development for the two most recent technology nodes from Intel [23].

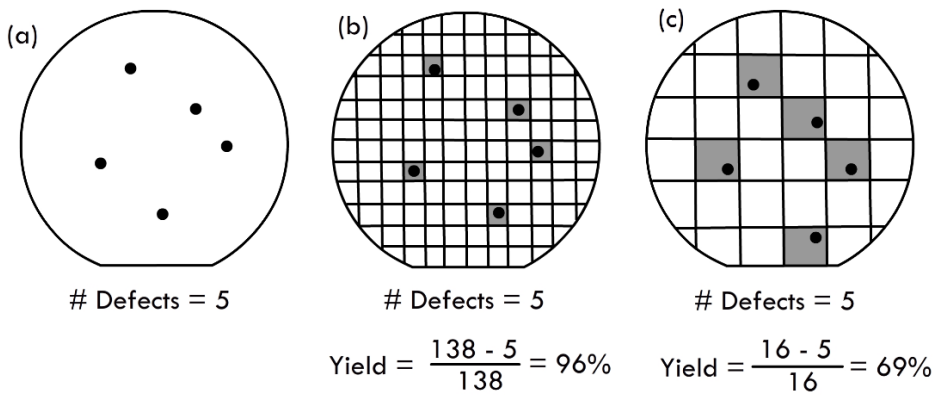


Figure 3. Five random defects on (a) wafer, (b) wafer with smaller die, and (c) wafer with larger die. Die with larger areas result in lower wafer yields [20].

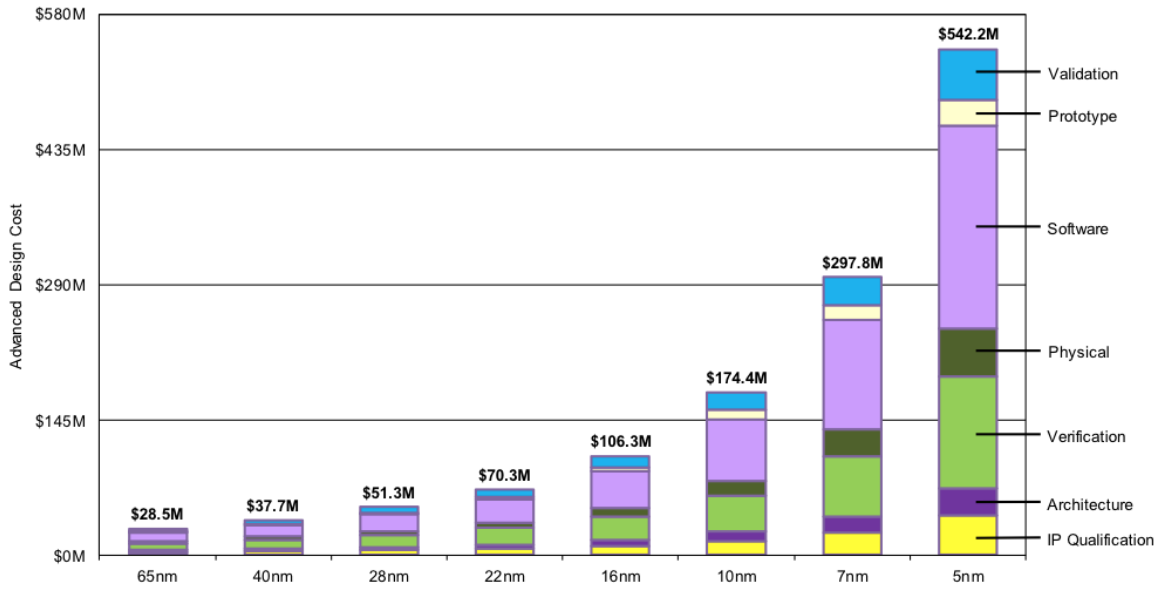


Figure 4. SoC design costs skyrocket as technology nodes advance [24].

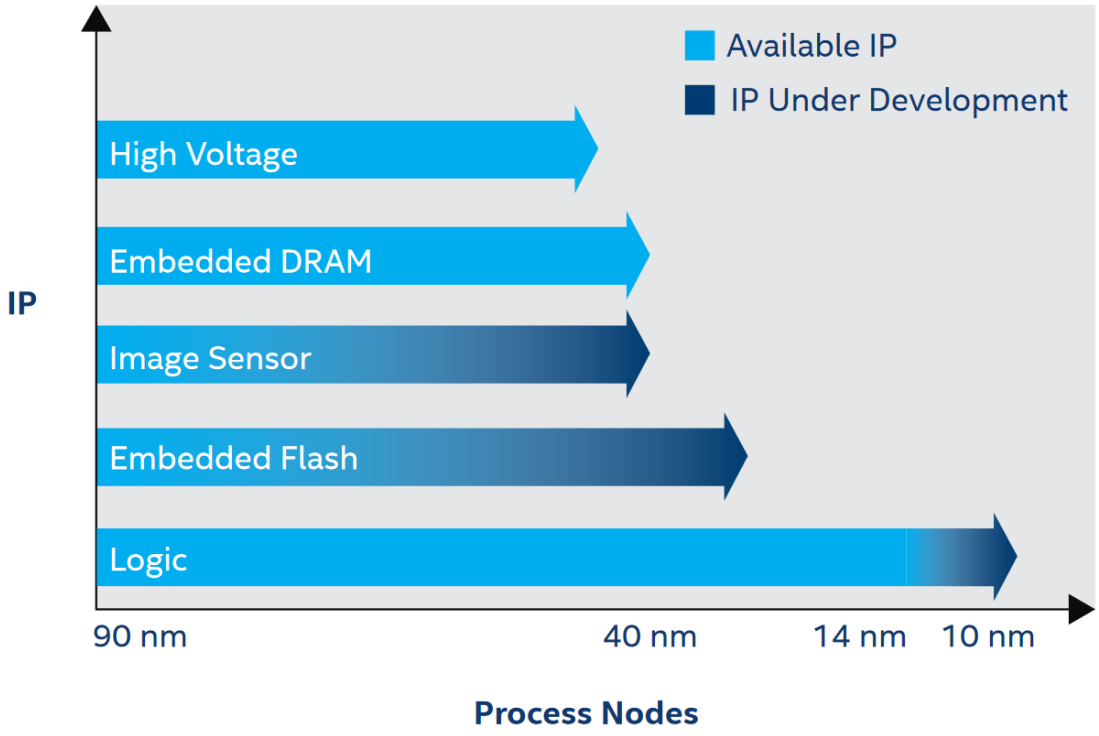


Figure 5. IP maturity for certain IP blocks at different process nodes [25].

Additionally, although packaging discrete die at the board level would circumvent many of the aforementioned SoC challenges, it would not attain the needed performance, bandwidth, and/or footprint for a wide variety of applications (e.g., AI, machine learning, 5G, RF, IoT). A more tightly integrated package with physically closer die and tighter I/O pitches will be needed instead. These requirements typically necessitate (1) the need for a very flat interconnecting substrate for lithographic purposes, such as those material substrates with crystallographic planes, and (2) the need for fine-pitch, off-substrate interconnects.

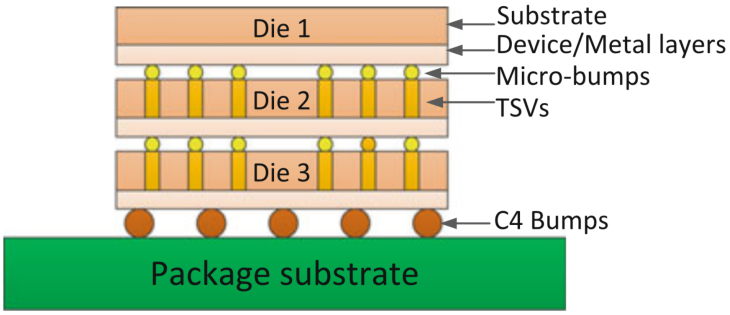
These challenges have therefore led some system designers to shift away from SoCs (and board-level packages) and towards tightly integrated multi-die heterogeneous systems (e.g., system-in-package [SiP]). This SoC-to-SiP migration directly addresses the

aforementioned challenges via lowering overall system design and fabrication costs, employing a mix and match of different material substrates and technology nodes (including IP reuse), decreasing time-to-market, and circumventing the reticle size limit (as smaller die are interconnected on a common substrate/package, which can enable a larger-than-reticle-size overall system).

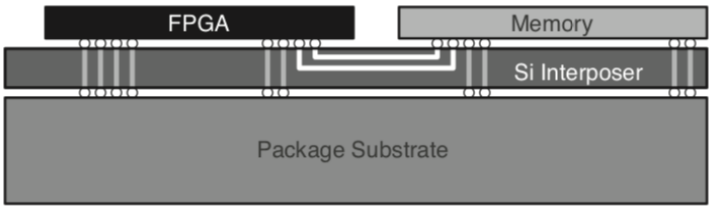
Several IC system designers/manufacturers have already begun to embark on this SoC-to-SiP transition. AMD's EPYC 32-core server CPU uses 4 discrete integrated 8-core "chiplets" whose total combined area exceeds the maximum printable die area of a single die (852 mm^2 and 777 mm^2, respectively) [26]. This chiplet integration approach not only provides more functionality relative to its SoC adaptation, but it also improves overall yield. In fact, AMD estimates that manufacturing costs are reduced by approximately 40% even when considering the 10% overhead that is needed for the inter-die (or inter-chiplet) interconnects [26]. Intel's Cascade Lake AP 56-core processor also uses a multi-die approach via integrating together 2 28-core Cascade Lake dice as a means to circumvent the yield challenges (and associated costs) of manufacturing a monolithic 56-core SoC [27], [28]. Other examples include AMD's Fiji GPU where they implement a 2.5D Si interposer integration scheme for the GPU and HBM memory stacks [29], Intel's 10nm Agilex FPGA using their embedded multi-die interconnect bridge (EMIB) technology [30], DARPA's CHIPS (Common Heterogeneous Integration and IP Reuse Strategies) program where chiplets in the form of IP blocks are envisioned to integrate together to build heterogeneous integrated systems while cutting down on design cost and time [31], and Apple's iPhone 11 Pro Max using TSMC's thin-profile Integrated Fan-Out (InFO)

package-on-package (PoP) technology which integrates the Apple A13 application processor with DRAM [32].

General multi-chip, fine-pitch advanced packaging solutions come in several forms (some of which are shown in Figure 6): 3D stacking [33]–[35], silicon interposers [36]–[40], TSV-less non-bridge interposers (SLIT, NTI, SLIM) [41]–[43], TSV-less bridged-based interposers (EMIB, HIST) [44]–[46], organic interposers [47], and other advanced packaging solutions which may use a combination of the above packaging configurations (Foveros, Co-EMIB, ODI, 3D-MiM) [48]–[51]. Figure 7 illustrates a general categorization of System-in-Package (SiP) systems.



(a)



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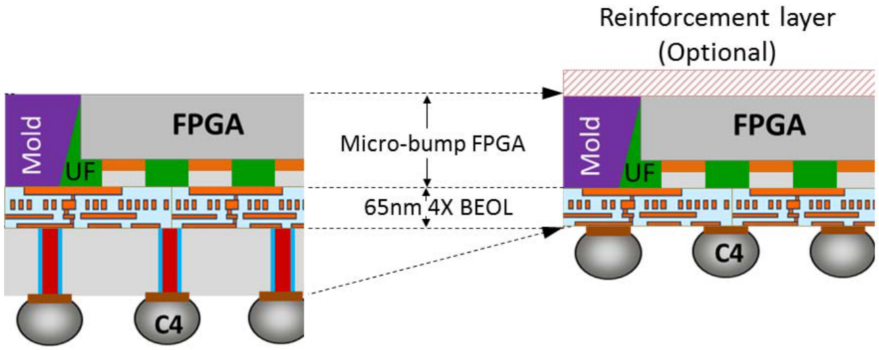

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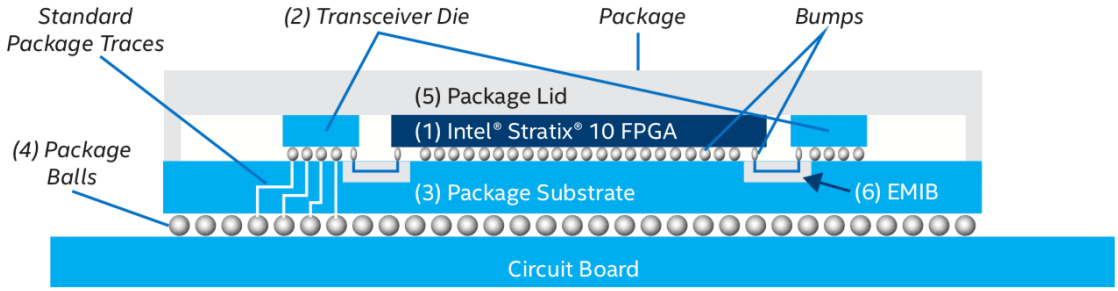


(d)

Figure 6. Different SiP package configurations: a) 3D stacking, b) 2.5D-based silicon interposer, (c) SLIT (TSV-less, non-bridge interposer package type) on right compared to 2.5D interposer system on left, (d) TSV-less, bridge-based package (EMIB in this case) [52]–[54].

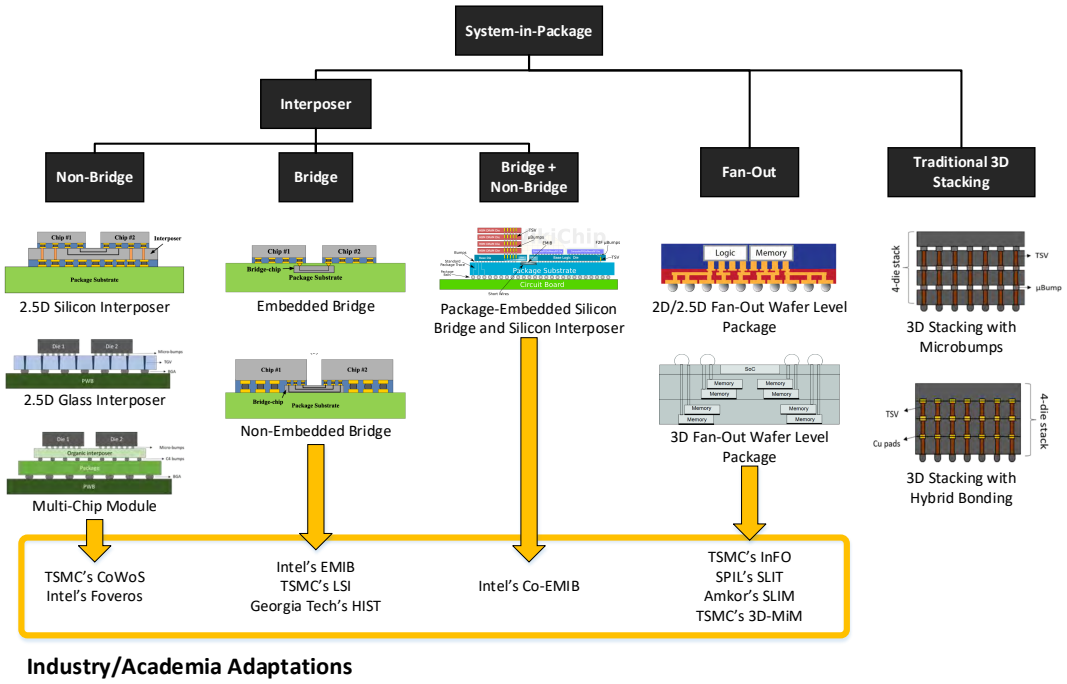
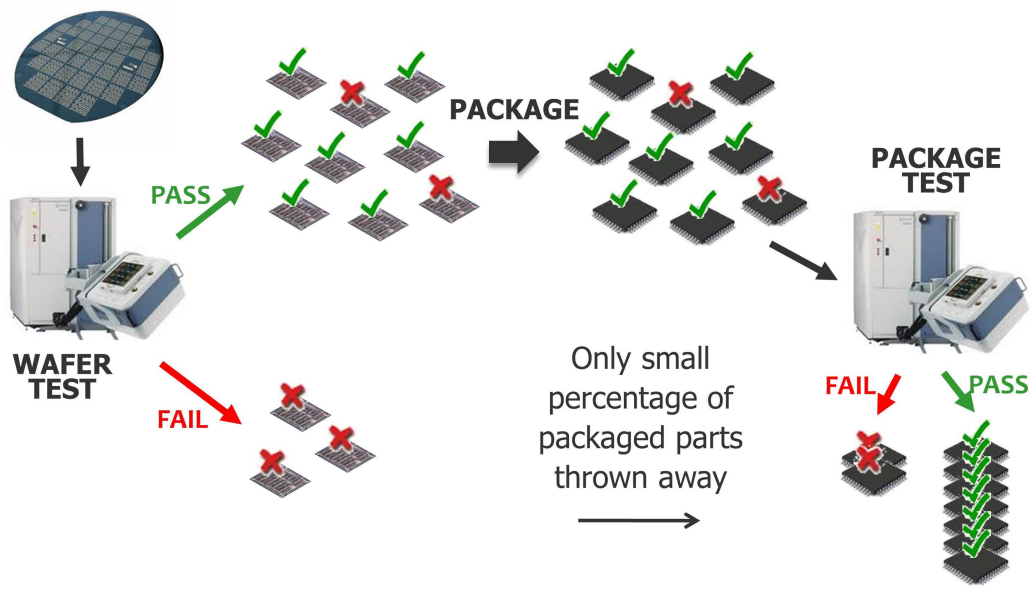


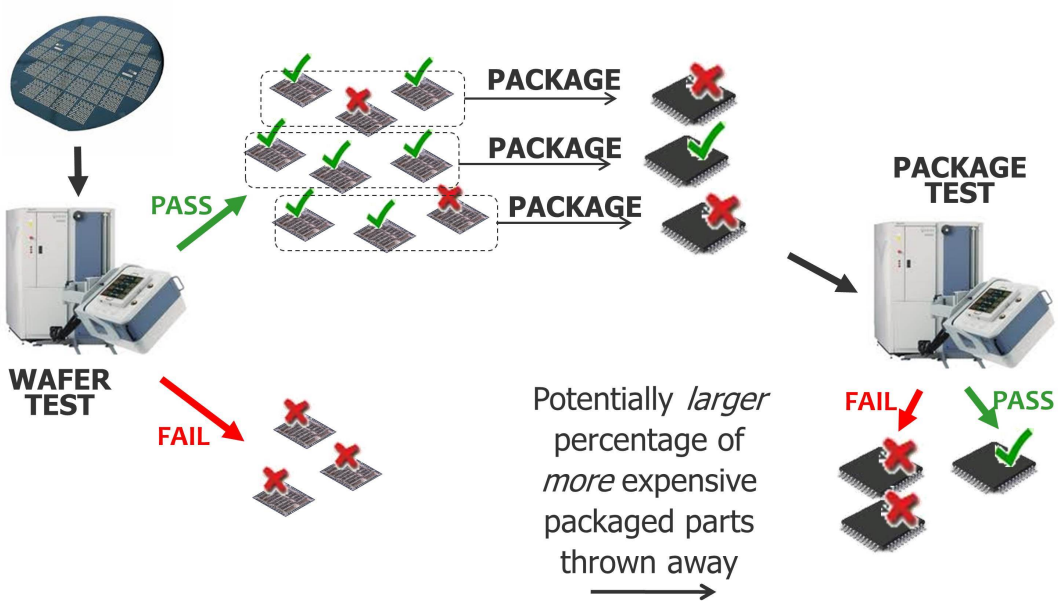
Figure 7. General categorization of different System-in-Package (SiP) systems. Some industry and academic adaptations of these SiP systems are also listed.

However, most of these multi-chip advanced packaging solutions are permanently integrated/interconnected in fixed configurations via either bumps or some other advanced off-chip interconnect technology (e.g., solder-capped Cu pillars, copper-to-copper direct bonding, hybrid bonding) due to the metallurgical and/or diffusive bonding process required for these interconnects to properly function. Some applications require the heterogeneity and fine-pitch provided by these multi-chip SiP systems while also requiring a non-permanent setup for: reworkability, prototyping, testing/characterization, upgradeability, etc. Additionally, as heterogeneous systems continue to expand and further dis-integrate (via adding more and more chiplets) as aforementioned to meet ever-growing demands, the overall system yield would suffer considerably as the SiP yield is proportional to the product of the individual die yield; said SiP yield therefore will decrease

as the number of dice within the SiP increases [55]. Figure 8 illustrates this concept via comparing the traditional packaged single die versus a packaged multi-die system. In the former case (i.e., single die), even if an individual bad die escapes detection during the wafer tests and becomes packaged, only the one subsequent "bad" package fails the package test and is defective. However, for the case of multi-die systems, if an individual bad die escapes detection during the wafer tests, it may become packaged with other known good die (KGD), hence rendering the entire system defective. For larger multi-die systems, the system yield begins to decrease considerably. A non-permanent setup for these large-chiplet based systems could prove very valuable in overcoming these yield challenges.



(a)



(b)

Figure 8. Wafer vs. package test for (a) the traditional case where dice are stand-alone systems (SoCs). In this case, even if an individual bad die escapes the wafer tests and becomes packaged, only the one subsequent "bad" package fails the package test. However, (b) for the case of multi-die systems such as 3D ICs, if an individual bad die escapes the wafer tests, it may become packaged with other known good die (KGD), hence rendering the entire system defective. For larger multi-die systems, the system yield begins to decrease considerably [56].

To achieve a non-permanently integrated, fine-pitch SiP system, two general primary requirements or enabling technologies are required as seen in

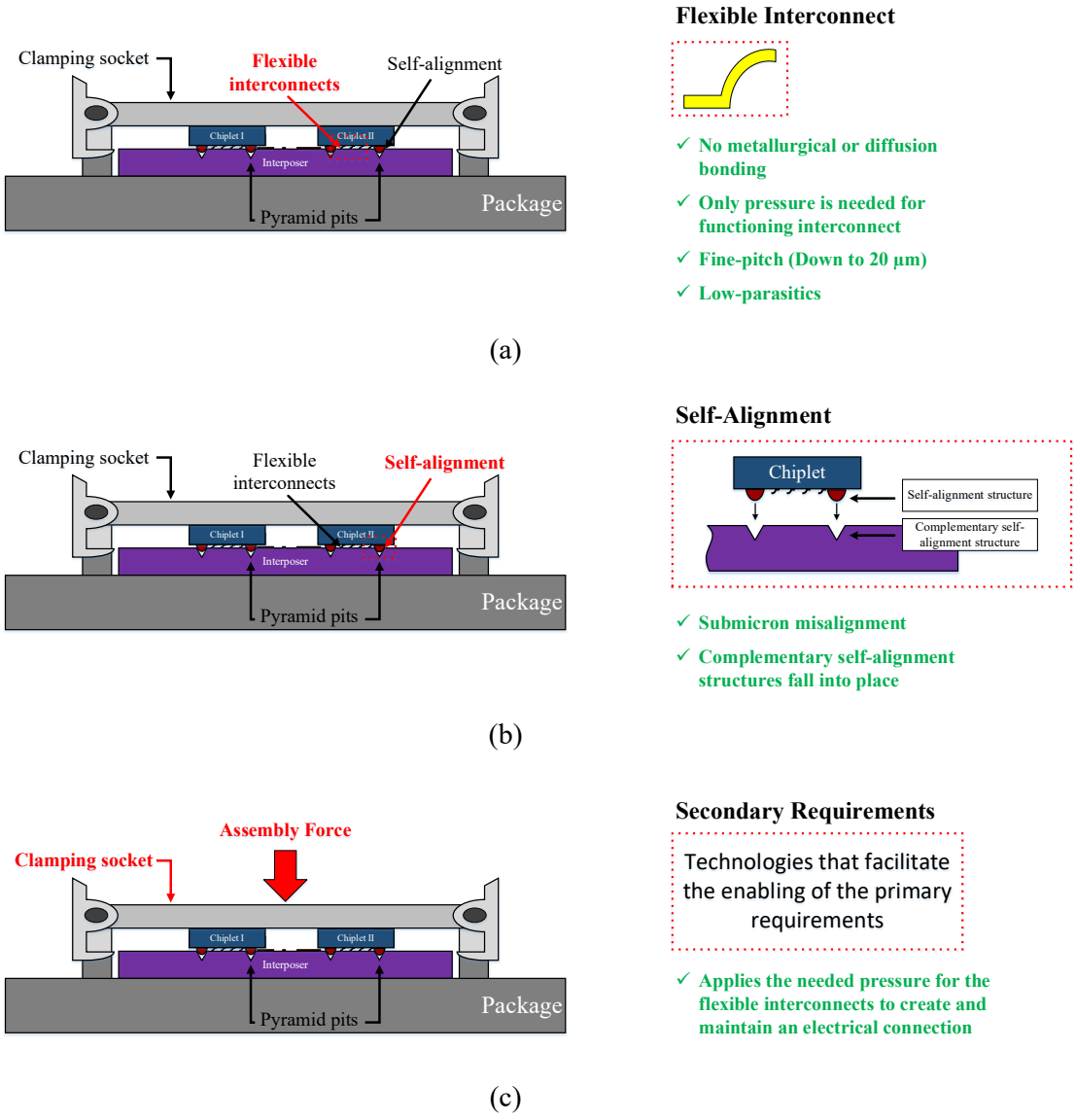
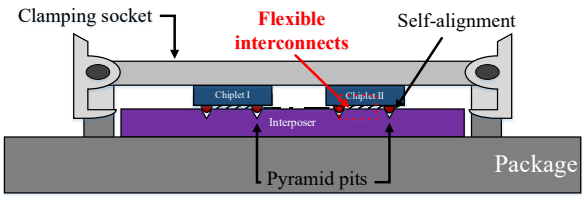
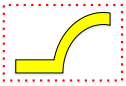


Figure 9: 1) a non-permanent off-chip, fine-pitch interconnect technology and 2) a means to align the die to substrate (or die to die) and maintain said alignment in a non-permanent manner (i.e., a non-permanent alignment technology).

The first primary requirement is satisfied via the use of flexible interconnects as employed throughout this thesis. Flexible interconnects provide a non-permanent electrical connection unlike in the case of traditional advanced off-chip interconnects (e.g., microbumps) as they do not require a metallurgical and/or diffusive bonding process. Instead, a pressure-based mechanism is required to create and maintain an electrical connection for these flexible interconnects. The second primary requirement is satisfied via the use of self-alignment mechanisms as employed throughout this thesis and as seen

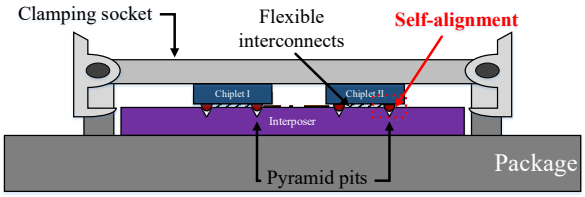


Flexible Interconnect

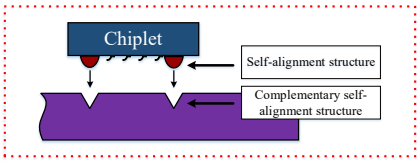


- ✓ **No metallurgical or diffusion bonding**
- ✓ **Only pressure is needed for functioning interconnect**
- ✓ **Fine-pitch (Down to 20 µm)**
- ✓ **Low-parasitics**

(a)

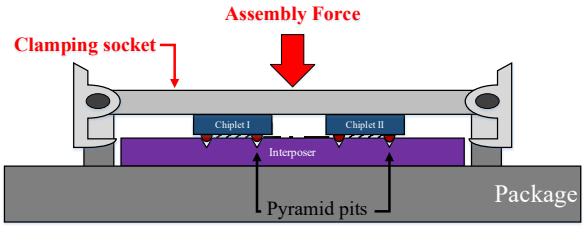


Self-Alignment



- ✓ **Submicron misalignment**
- ✓ **Complementary self-alignment structures fall into place**

(b)



Secondary Requirements

Technologies that facilitate the enabling of the primary requirements

- ✓ **Applies the needed pressure for the flexible interconnects to create and maintain an electrical connection**

(c)

in

Figure 9(b). As one self-alignment structure physically couples with another complementary self-alignment structure, a non-permanent alignment mechanism results. Finally, secondary requirements are also needed to enable a non-permanent SiP. Secondary requirements refer to any technologies that facilitate the enabling of the primary requirements. To apply the needed pressure for flexible interconnects to operate properly, socket structures are employed throughout this thesis for the purpose of applying this pressure to the flexible interconnects. Both primary enabling technologies that satisfy the primary requirements of a non-permanent SiP (e.g., flexible interconnects and self-alignment) are emphasized in this thesis and will be expanded upon in Section 1.3.

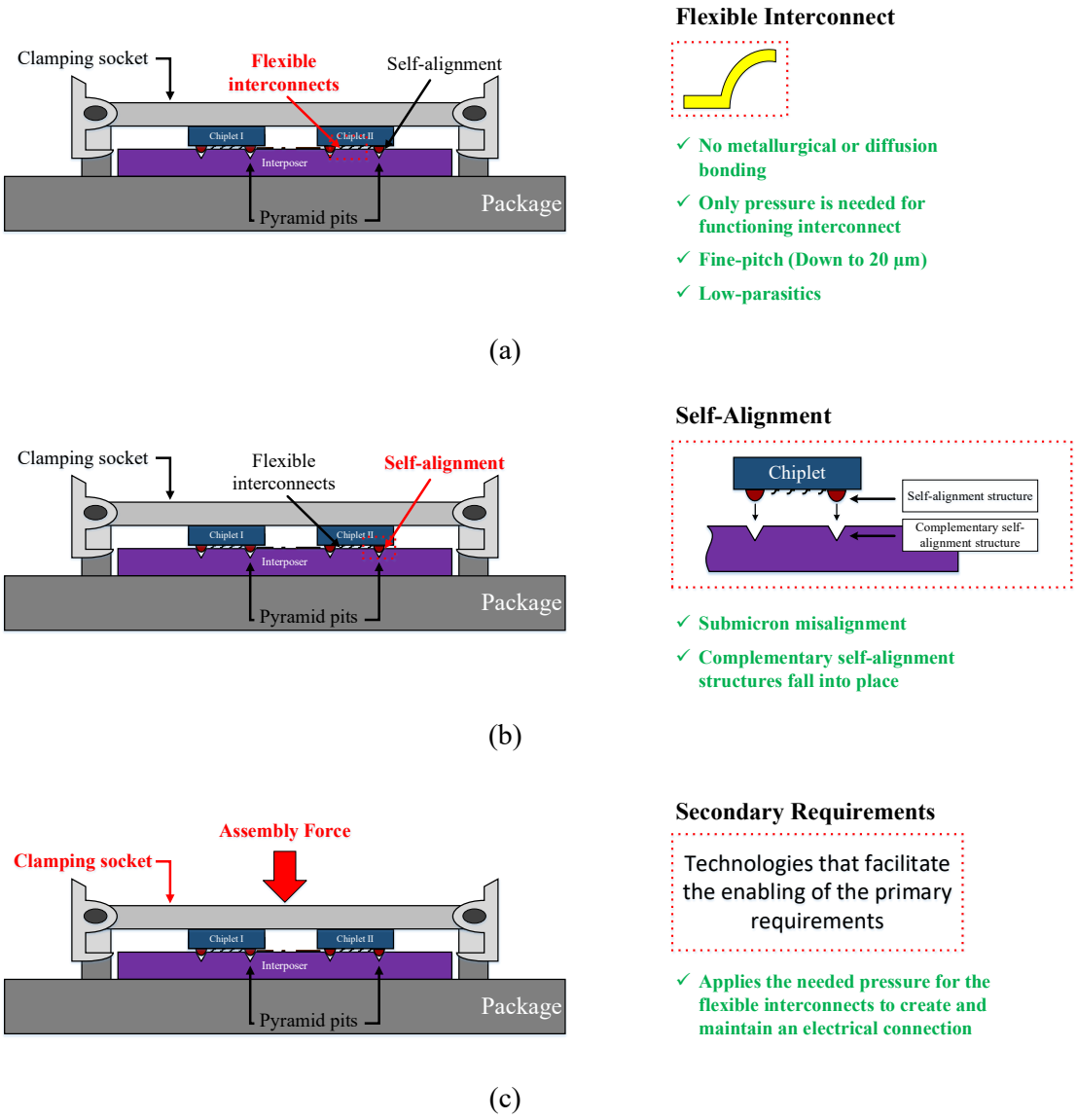


Figure 9. (a) First primary requirement for the non-permanent SiP. This first primary requirement is satisfied via flexible interconnects. (b) Second primary requirement for non-permanent SiP, which is satisifed via self-alignment. (c) Secondary requirements of the non-permanent SiP, which is satifisfied by a clamping socket to apply the needed pressure for flexible interconnects to create and maintain an electrical connection.

1.2 Applications That Benefit from Non-Permanent Heterogeneous Integrated Systems

1.2.1 Chiplet-Based Rapid Prototyping

Chiplets continue to push the "disintegration" paradigm away from SoC and toward polylithic integration. As seen in Figure 10, the primary motive behind chiplets is to disintegrate the SoC to such a high degree that the resulting small modular components (or "chiplets") can act as standardized hardware IP blocks (e.g., logic, flash, DRAM), which can significantly expedite the system design cycle time at a lower cost [57]–[59]. DARPA predicts decrease in turn-around times and cost to reach approximately 70% [60], [61]. This faster time-to-market and overall reduced costs are beneficial to a wide variety of designers/manufacturers ranging from those in the fast-pace consumer mobile electronics market and those in the low-volume electronics markets (e.g., defense, fast-pace IoT) where high non-recurring engineering (NRE) costs consume a substantially large portion of the overall system budget with relatively low expected returns [16].

In the IoT market specifically, rapid prototyping remains a central component of the overall system design process in speeding up the final design of the targeted system, especially as said market is very diverse, ever-changing, and low volume as aforementioned (due to its fast-pace); hence, a quick time-to-market is needed where upfront costs are minimized (due to the potential low volume and the corresponding inability to justifiably offset these costs) [15].

One company that is actively spearheading the IoT chiplet prototyping market is zGlue. zGlue offers a rapid means to prototyping a die via integrating off-the-shelf chiplets and

assembling them onto an active Si interposer (which they label Smart Fabric), as seen in Figure 11, where connections inside the Smart Fabric are programmed in much the same way as the connections between logic gates within an FPGA are programmed [61]. Although zGlue offers a great means to minimize IP design while offering some flexibility between chiplet and interposer interconnections, the chiplets themselves appear permanently integrated atop the Smart Fabric despite what appears to be a bed of compliant interconnects that comprises the off-substrate interconnect portion of the Smart Fabric (a non-permanent alignment mechanism is not mentioned nor observed, nor is there any mention or depiction of a non-permanent securing of the chiplets in place atop the Smart Fabric). This limitation restricts the flexibility system designers may require during the prototyping phase. As discussed previously, heterogeneous integrated systems come in a variety of different configurations (e.g., 3D stacking, Si interposers, bridge-based interposers) and some of these configurations may be preferred depending on the specific targeted application. A non-permanent version of the zGlue system would enable system designers far greater flexibility in their packaging design to the extent where they could better manage their system's signal integrity and power integrity (SI/PI), bandwidth, and communication latency. Furthermore, zGlue's Smart Fabric off-interposer interconnects appear to have a pitch of 100 μm (according to zGlue's Q&A [62]) and hence a system that could achieve an even tighter interconnect pitch would result in further increased performance. This thesis introduces such a scalable tight-pitch and non-permanent heterogeneous integrated system, which will be introduced in CHAPTER 6.

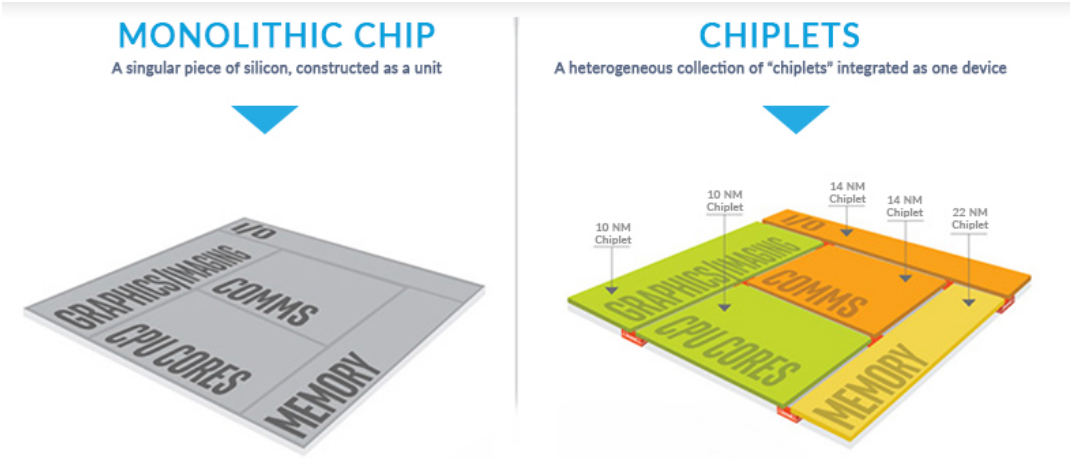


Figure 10. Chiplets break down a monolithic die into IP blocks and interconnect them via very fine-pitch interconnects [63].

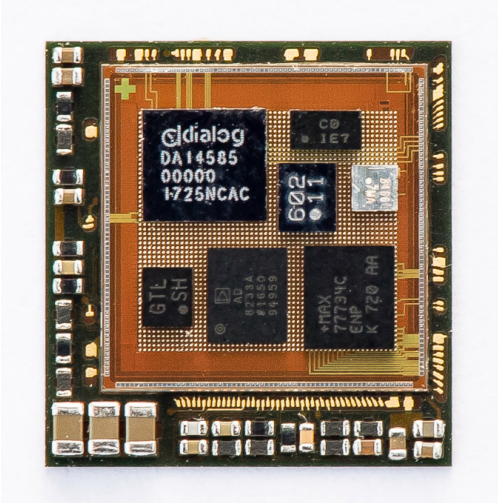


Figure 11. zGlue's chiplet-based SiP where chiplets sit atop an active and programmable Si interposer [64].

1.2.2 Biosensing Applications

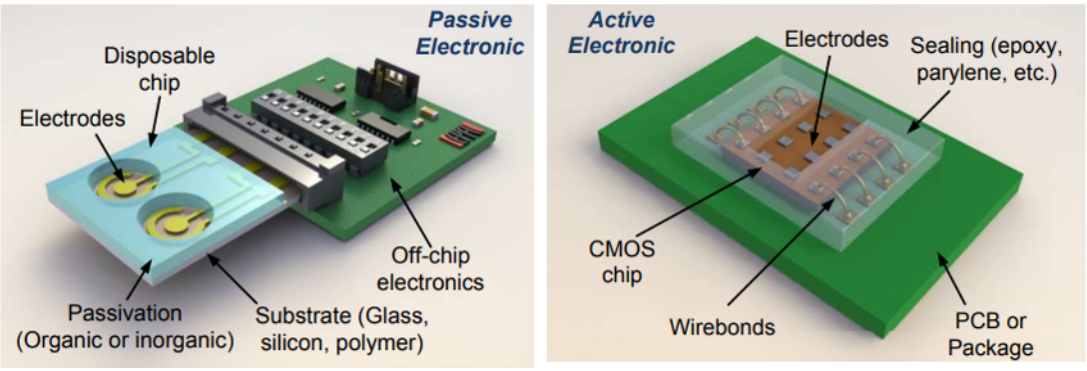
Biosensing platforms, including CMOS biosensors, continue to impact a wide variety of different biomedical applications ranging from point-of-care testing to synthetic

exoelectrogens engineering [65]–[70]. One effective approach to manufacturing these biosensing platforms with the goal of holistic characterization is to design said platforms such that a variety of sensing modalities and sensing sites (in addition to signal processing capabilities) are integrated into a single die (e.g., SoC) [70]–[74].

However, the sensing sites on CMOS biosensing platforms generally require post-processing both to create a bio-compatible surface and also to maximize the recording signal SNR, which is, in part, a function of the sensing sites or surface electrodes (both their material and their geometry) [75], [76]. When cells are grown and tested on these sensing sites, both contamination and electrode degradation occur [77]–[81] and must be addressed; in regards to contamination, a general approach here is to perform a limited clean on the electrodes after each use for sterilization purposes (more thorough cleans may degrade electrodes or negatively affect active devices as in the case of gamma irradiation sterilization) [82]–[84]. Eventually, the entire biosensor is discarded after several uses (due to excessive electrode degradation which degrades SNR). For a generally expensive SoC (especially when the volume of the SoC is low to medium), this biosensor-discarding approach can become non cost-effective.

Additionally, there are a very wide variety of different sensing modalities (e.g., extracellular potential recording, electrical stimulator, complex impedance measurement, PH sensing, magnetic sensing, fluorescent detection, optical detection), some of which may be challenging or sub-optimal to integrate monolithically into a single die [85]–[92]. Hence, an integrated discrete IC approach may prove useful in addressing the aforementioned challenges.

Some solutions have addressed separating the sensing sites from the active CMOS circuitry for the purposes of re-using the active biosensor, as seen in Figure 12, and instead discarding the passive site after a single use or multiple uses. This configuration can minimize contamination as no active circuity exists (hence gamma irradiation sterilization can be used) while also being more cost-effective as the SoC itself is less expensive due to no needed post-processing and the ability to extend the life of the SoC. However, such solutions generally integrate the sensing sites and the CMOS bio-platform at the board-level in a 2D configuration (as seen in Figure 12(a)) [93], [94]. This packaging scheme results in lower sensing resolution, potential loss of high-frequency components of transient signals emanating from the biochemical reactions under study, and injected noise, the latter two due to the long electrical interconnect paths between said sensing sites and the readout circuits, which in turn can potentially invalidate some of the resulting characterizations, especially in the case where multiple discrete IC sensing modalities are interconnected to the same sensing sites (and a holistic characterization of said biochemical reactions is sought, which is the purpose of a multi-modality approach).



(a) (b)

Figure 12. Comparison between (a) a 2D integrated biosensor and (b) a monolithic biosensor [94].

Therefore, a tightly integrated solution (e.g., SiP) that allows for a non-permanent setup can address all the aforementioned challenges in addition to the providing the general advantages of manufacturing an SiP in place of an SoC (e.g., ability to discard passive sites while retaining the active die, minimize contamination, maximize resolution, maximize signal integrity, lower design costs and expedite time-to-market, lower per die manufacturing costs). This thesis introduces such a solution that will be discussed in further detail in CHAPTER 3.

1.3 Enabling Technologies for Non-Permanent Heterogeneous Integrated Systems

As aforementioned, the two general technologies to enable a tightly integrated non-permanent heterogeneous integrated system are: 1) a non-permanent off-chip, fine-pitch interconnect technology and 2) a non-permanent alignment technology. Both of these technologies will now be discussed.

1.3.1 Non-permanent off-chip/off-substrate interconnects

The two types of non-permanent off-chip interconnects considered in this thesis are compliant interconnects and anisotropic conductive films (ACFs). As the majority of the thesis incorporates compliant interconnects (or focuses on compliant interconnects), the review here will largely examine compliant interconnect technologies and only touch on ACFs.

1.3.1.1 Compliant Interconnects

Due to their potential non-permanent connections (although they can be permanent), their compliance, and their elastic range of motion (either vertically, horizontally, or both), compliant interconnects have several applications ranging from systems that require or seek temporary connections or probing (e.g., probe cards and other testing systems, LGA sockets or other upgradeable/replaceable systems, characterization, prototyping) to systems that seek to alleviate stress on low-k or ultra low-k dielectrics, or decrease warpage in the substrate due to coefficient of thermal expansion (CTE) mismatch [72], [95]–[99].

There are a wide variety of different compliant interconnects in the literature as seen in Figure 13, which generally be categorized into several groups:

1. Stress-engineering compliant interconnects: Stress-engineered compliant interconnects, including microsprings and stressed-metal springs [100]–[102], Microcantilevers [103], and J-Springs [104], employ a pressure variation process during the thin film metallization of the interconnect such that a stress gradient is formed throughout the length of the interconnect. This stress gradient can be engineered to form a specific radius of curvature of the finalized released metal film. Coiled microsprings [105], which also rely on stress-engineering, use a

different stress-inducing approach; the coiled microsprings consist of two layers of different materials with very different thermal expansion coefficients for the purpose of inducing stress.

2. Complaint interconnects that achieve their compliance via primarily sitting on or within a polymer substrate: Sea of Leads (SoL) interconnects [106]–[108] employ embedded air gaps underneath the interconnect to attain compliance in the vertical direction. Floating Pads Technology employs a similar approach [109]. WAVE Package [110] embeds the interconnects within a low-modulus polymer substrate (during thermal cycling, deformation of the compliant interconnect occurs). The compliances of these compliant interconnects primarily derive from the material and structural properties of the polymer.
3. 3D, non-stressed-engineered, free-standing compliant interconnects: B-Helix [111], [112] and G-Helix [113], [114] are lithographically-

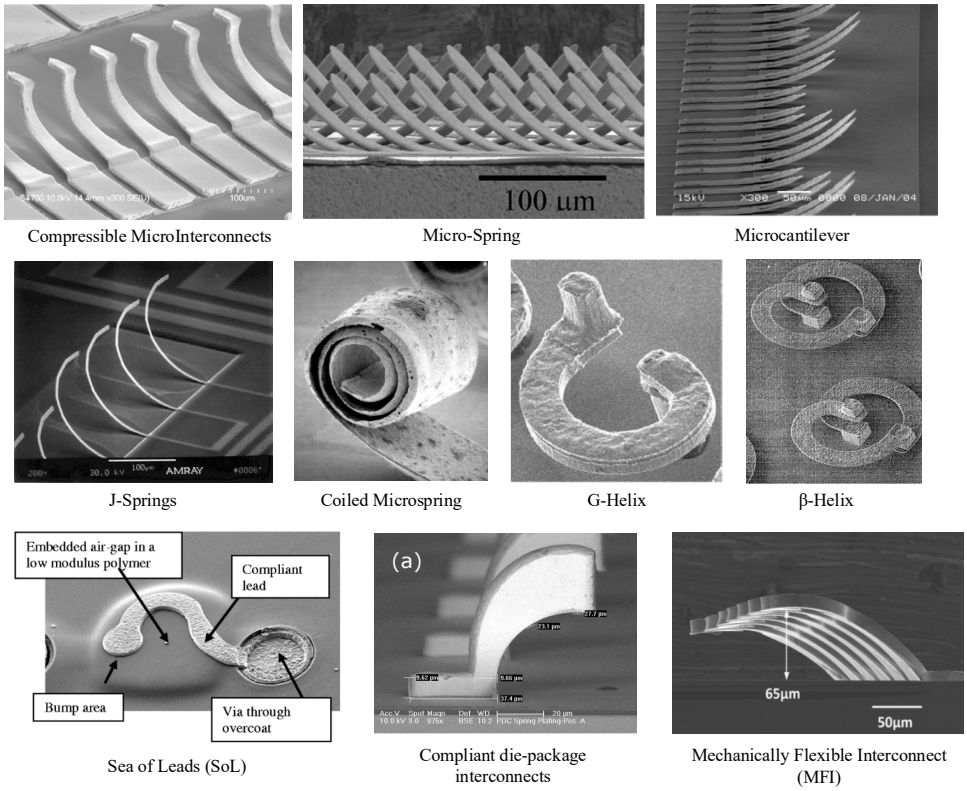


Figure 13. SEM images of various compliant interconnect technologies.

defined electroplated compliant interconnects that incorporate an arcuate beam and vertical end posts to achieve compliance in the three orthogonal directions. Mechanically Flexible Interconnects (MFIs) [115], [116] and Compliant Die-Package Interconnects [117] are fabricated via the use of a thermally reflowed (> T_g) sacrificial photoresist layer, which can provide large range deformation in the vertical direction, especially for thick sacrificial photoresist layers. Compressible MicroInterconnects (CMIs) [118] employ a lithographic technique to create a concave pattern in the resist layer for the shape of the compliant interconnect, which can also provide a large vertical range of motion. Both MFIs and CMIs

are employed/studied throughout this thesis (MFIs in CHAPTER 2 and CHAPTER 3; CMIs in CHAPTER 6).

1.3.1.2 Anisotropic Conductive Films (ACFs)

Anisotropic conductive films (ACFs) are interconnection systems where conductive particles/balls are aligned in separated (and hence electrically-isolated) vertical columns within a polymer matrix, as seen in Figure 14. Conventionally, ACFs have been used for a variety of flat-panel display module packages, including liquid crystal displays (LCDs), plasma display panels, and organic light emitting diodes (OLEDs) due to several advantages that it can provide: low-temperature processing, fine-pitch, environmentally friendly, flux-free or solvent-free processing [119]. ACFs have also been used as replacements for soldering technologies for fine-pitch surface mount components [120]–[122]. Additionally, ACFs have been employed on flexible substrates [123]–[125] and rigid PCB substrates [125], [126].

This thesis employs a specific ACF interconnection system, PariPoser, in CHAPTER 4, primarily as it provides a non-permanent, fine-pitch method to interconnect die and substrate, and is hence an alternative to the aforementioned compliant interconnect technologies. Further details regarding PariPoser and its composition will be discussed in CHAPTER 4.

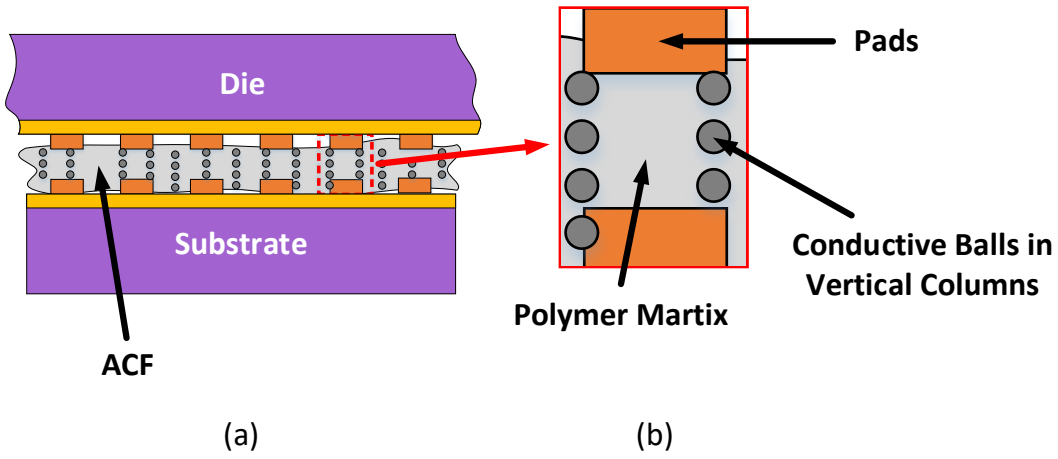
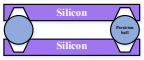
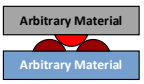
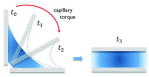
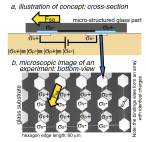
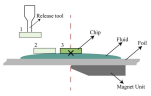


Figure 14. (a) Anisotropic conductive films enable a vertical electrical connection between corresponding pads. (b) The vertical columns are composed of conductive balls within a polymer matrix. These columns are electrically isolated from one another.

1.3.2 Self-Alignment Mechanisms

Self-alignment mechanisms can be primarily categorized into several different groups: surface tension based, electro-static, magnetic, and mechanical (or a combination of these categories). A comparison of several different self-alignment technologies is listed in Table 1.

Table 1. Comparison table of different self-alignment technologies [127]–[131].

Metric	Self-Alignment Technologies					
	Ball-in-Pit [127] 	**PSAS-in-Pits** [128] 	**PSAS-to-PSAS** [Thesis work] 	**Surface-Tension Driven** [129] 	**Electrostatic** [130] 	**Magnetic** [131] 
Alignment Accuracy	< 1 µm ✓✓	< 1 µm ✓✓	< 1 µm ✓✓	< 1 µm ✓✓	≈ few µm ✗	≈ 10-15 µm ✗✗
Substrate Invasive	Yes ✗	Semi ✓	No ✓✓	No ✓✓	No ✓✓	No ✓✓
Substrate Agnostic	No ✗	Semi ✓	Yes ✓✓	Yes ✓✓	Yes ✓✓	Semi ✓
Heterogeneous Integration Suitability	Low ✗✗	Medium ✗	High ✓✓	High ✓✓	High ✓✓	Medium ✗
Fabrication/Pre-treatment Complexity	High ✗	Medium ✓	Low-to-Med. ✓	Very High ✗✗	Medium ✓	Med.-to-High ✗

1. <u>Surface tension based self-alignment:</u> Surface tension based self-alignment techniques employ the surface tension of some liquid or glassy material to pull one substrate to another substrate (that contains the droplet) in the direction of the capillary force vector such that accurate alignment occurs. This concept is illustrated in Figure 15 [129]. Droplet materials/structures used for this self-alignment technique have been solder balls [132], indium solder bumps [133], water [134], and flux [135]. Many factors are critical for these self-alignment techniques to function properly including pre-treatment and cleaning of the die (e.g., hydrophobicity), the levelling of the die, and precise volume control.

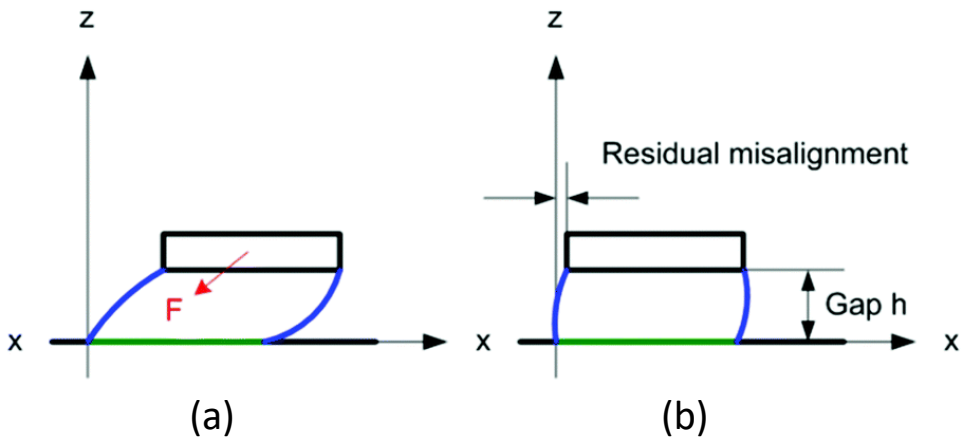


Figure 15. (a) Component being acted upon via the droplet's capillary force. (b) End of the alignment process with possible residual misalignment [129].

2. Electrostatic self-alignment: Electro-static self-alignment uses electrostatic attraction between two substrates (via corresponding pads) to self-align said substrates as seen in Figure 16 [130]. More specifically, a charge reallocation at the pad sites is performed (perhaps via connecting neighboring pads together via an external voltage source). This charge reallocation at the pad sites of one substrate will induce charge reallocation of the corresponding pad sites of the aligning substrate, which then in turn creates horizontally directed electrophoretic forces (in addition to perpendicular forces) to align the substrates. One obstacle to this approach is the friction and adhesion between substrates. Several solutions to overcoming this obstacle has been demonstrated including the use of ultrasonic or mechanical vibration [136], [137] and carrier fluid [138].

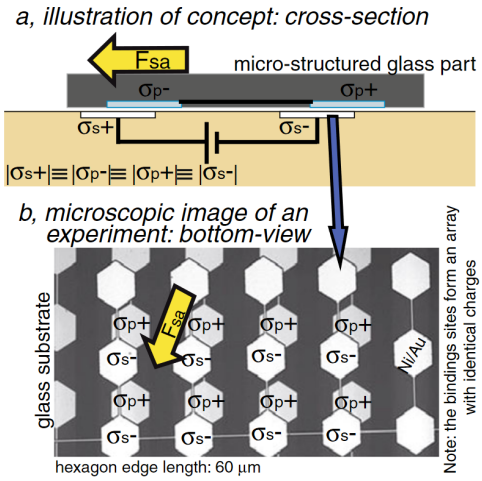


Figure 16. (a) Two neighboring pads can be electrically connected to an external voltage source which creates an electric field causing surface charge reallocation at these sites. In the case of horizontal misalignment, horizontally directed electrophoretic forces self-align the substrates. (b) A microscopic image (bottom-view) showing an array of pads for both top and bottom substrates and their corresponding charges [130].

3. Magnetic self-alignment: Magnetic self-alignment operates either via 1) an interaction between embedded hard magnetic materials on the aligning die and an externally applied magnetic field (created by hard magnets or an electromagnet) or 2) magnetization of soft magnetic materials on the die by an externally applied magnetic field created either by hard magnets or an electromagnet. Kuran et. al. [131] employs an inhomogeneous magnetic field created by a magnetic unit placed underneath the substrate to align the aligning die. Both substrates contain asymmetric nickel patterns that, in combination with the aforementioned magnetic unit, creates the aforementioned magnetic field. This die follows the magnetic field gradient upon being released by the release tool as it falls through the air. A confined layer of liquid is used on the substrate to increase the aligning die's

mobility. Morris et. al. [139] employs both capillary forces for short-range self-alignment and magnetic forces for longer-range attraction.

4. Mechanical self-alignment: Mechanical self-alignment techniques employ physical features to self-align one die to its substrate. Quilt Packaging (QP) [140], [141] employs nodules that extend directly out the sides of the chips for edge-to-edge self-alignment where several die reside on a common substrate (e.g., SiP). Note that almost all the self-alignment techniques discussed here employ self-alignment mechanisms for one die to align to a substrate underneath it (as opposed to the case of QP where the alignment is edge-to-edge on a 2D layout). Ball-in-Pit technology [127], [142] uses pits formed via the anisotropic wet etching of (100) silicon on both aligning substrates and a precision ball (sapphire, ruby, metal, etc.) that fits into both complementary pits. PSAS-to-Pits self-alignment technique [128] employs lithographically-defined complementary physical features on two substrates that require self-aligning. These features include a reflowed patterned photoresist layer on one substrate and a KOH/TMAH-etched pit (similar to the Ball-in-Pit technology) in the other substrate. As these features are lithographically-defined, submicron alignment resolution has been achieved [128]. This thesis employs a combination of the Ball-in-Pit and the PSAS-to-Pits technologies in CHAPTER 3 and CHAPTER 4. Another similar self-alignment technique to PSAS-to-pits is PSAS-to-PSAS where both aligning substrates employ only PSAS. This PSAS-to-PSAS self-alignment technique will be discussed in detail in CHAPTER 5 and employed in a system-level demonstration in CHAPTER 6.

1.4 Organization of this Thesis

This thesis is arranged as seen in Figure 17 and as described as follows:

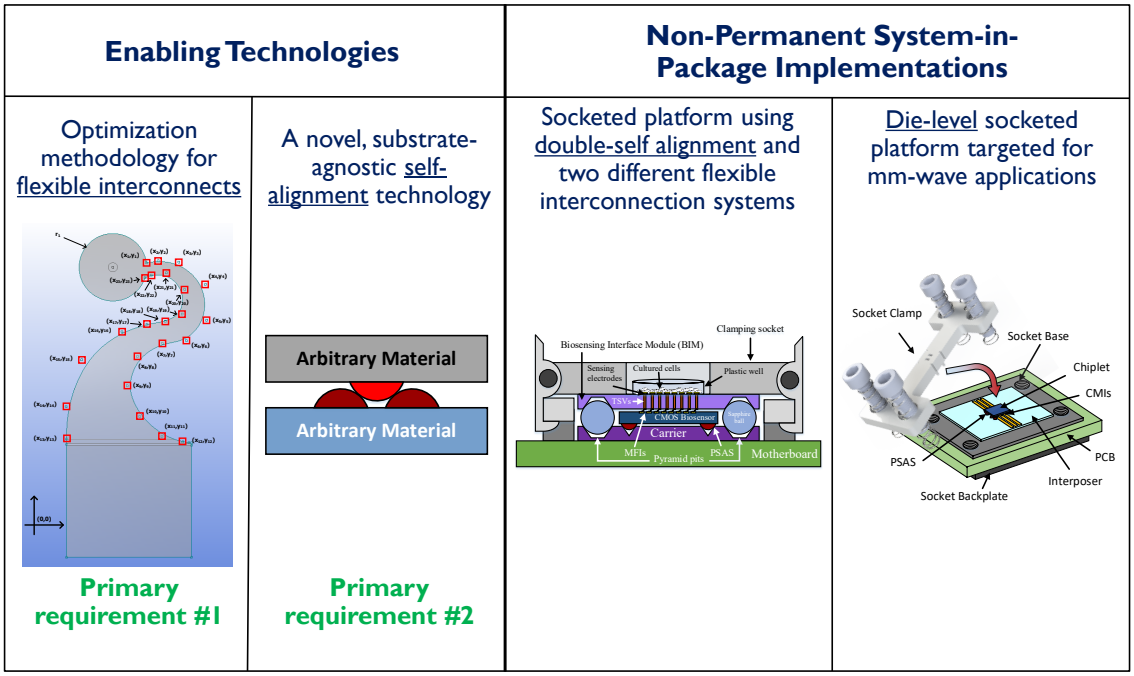


Figure 17. Structure of thesis divided into two enabling technologies (one focused on flexible interconnects and the other one focused on self-alignment) and two implementations of non-permanent SiPs.

1) Chapter 2: An optimization methodology is introduced for the design of MEMS-type compliant interconnects (or 3D compliant interconnects). The mechanical reliability of these interconnects is targeted; hence the optimization goals are to minimize maximum von Mises stress (in an attempt to minimize plastic deformation) and to maintain compliance within a specified range (for a balance between low contact resistance and low stress). This design methodology targets the photomask design of the compliant interconnect such that said methodology is directly applicable to a wide set of complaint interconnect technologies including MFIs and CMIs. Additionally, spline-based parametrization is employed to

minimize stress singularities and to increase the geometry design space. A multi-objective genetic algorithm (MOGA) is employed to perform the optimization of the compliant interconnect design (MFIs were used as the subject of the design). MFIs were then fabricated and the optimization process is experimentally verified.

2) Chapter 3: A novel socketed 3D packaging configuration is designed and fabricated for biosensing applications; said packaging configuration is referred to as a Biosensing Interface Module (BIM). The BIM enables the physical separation between the passive sensing sites and the active biosensor to minimize or eliminate post-processing on the active component, increase the sterilization options for the passive sensing sites, allow for the simple replacement of the sensing sites which can minimize electrode erosion and hence maintain a targeted SNR, and provide the general technical and logistical advantages held by SiP systems over SoC systems (e.g., a non-CMOS passive sensing site die that can increase SNR via increasing electrode surface area and employing more suitable, non-CMOS electrode materials). Additionally, as the BIM employs 3D integration, high resolution and short electrical connections are enabled. The BIM design (which includes several enabling technologies, including MFIs and a double self-alignment mechanism) is discussed in detailed. The BIM fabrication process flow is demonstrated and fabrication challenges discussed. Four-point resistance of the MFIs are measured when the BIM is fully assembled. Additionally, the alignment provided by the double self-alignment mechanism is also measured. As the BIM enables the replacement of the passive sensing sites from time to time, alignment repeatability measurements were also performed.

3) Chapter 4: The BIM of Chapter 3 was extended to include through silicon vias (TSVs) and a different non-permanent interconnection system, PariPoser, which is an anisotropic conductive film (ACF). As the BIM in its full implementation requires the inclusion of TSVs, this chapter details the TSV fabrication process flow within the passive component of the BIM system in addition the corresponding fabrication challenges and potential solutions. Employing the PariPoser as the interconnection system for the BIM also demonstrates the agnostic nature of the BIM system in regards to its use of enabling technologies. Finally, four-point resistance of the TSV + PariPoser connection is measured when the BIM is fully assembled.
4) Chapter 5: A novel self-alignment mechanism is developed where the aforementioned PSAS-to-Pits technology is modified to a PSAS-to-PSAS self-alignment technology where only PSAS structures are fabricated on the aligning substrates. Such a self-alignment approach does not require invasive wet etch procedures as is the case for the KOH/TMAH-etched pits required in the PSAS-to-Pits technology. Additionally, as (100) Si is no longer needed for said anisotropic wet etching, a much wider variety of substate materials can be used, including glass-on-glass substrates. The PSAS-to-PSAS engineering mathematics is detailed in this chapter (e.g., relationship between substrates' gap and PSAS height, PSAS width, horizontal PSAS-to-PSAS spacing). The PSAS-to-PSAS fabrication process flow is discussed. Finally, PSAS-to-PSAS alignment is measured and alignment repeatability of this self-alignment technology is also measured.

5) Chapter 6: A socketed 2.5D/3D packaging configuration is designed and fabricated for heterogeneous integrated applications. Glass substrates are used to minimize loss through the substrates (as opposed to Si substrates). As glass substrates are used and a non-permanent configuration is sought, the PSAS-to-PSAS self-alignment technology from Chapter 5 is employed here to enable the self-alignment between passive chiplet and interposer. The design of the socketed system is discussed (e.g., socket design, PSAS-to-PSAS gap, CMI compliance). The fabrication process flow is also demonstrated. Finally, four-point resistance of the CMIs are measured when the system is fully assembled.
6) Chapter 7: Future works is discussed. Addressing certain challenges are discussed here in addition to next steps for some of the work completed in this thesis.

CHAPTER 2. COMPLIANT INTERCONNECT OPTIMIZATION FOR IMPROVED MECHANICAL PERFORMANCE

2.1 Introduction

An optimization-based design is employed to improve the mechanical properties of compliant interconnects. This chapter focuses not only on the optimization process itself, but it also offers a simplified means to implement this process for a large range of MEMS-type flexible interconnect technologies, regardless of the specific fabrication process flow via: 1) optimizing only the photomask design of the interconnect and 2) implementing a spline-based parametrization in addition to more conventional parametrizations (e.g., widths, radii, etc.) of the interconnect geometry so that this optimization process is flexible enough to accommodate a large variety of geometric designs (that are to be optimized). In this chapter, we present: 1) an attempt at a generalized multi-objective optimization approach that is applicable to a wide variety of flexible interconnects, 2) the optimization of MEMS-type mechanically flexible interconnects (MFIs) as a proof-of-concept, 3) the extraction of certain structural properties of microfabricated MFIs from the measured data, and 4) a comparison between the optimized and initial MFI structures for both simulation and experimental scenarios.

2.2 Design Approach

To demonstrate the workings of our multi-objective optimization process, we use as a proof-of-concept our prior work on MEMS-type MFIs [115], [143], [144]. The design targeted is the photomask design; this approach avoids modifying the fabrication process flow and hence simplifies efforts to improve the MFI's mechanical properties. Additionally, the targeting of the photomask design allows for extensive design freedom as virtually any shape can be achieved.

Figure 18 illustrates a flowchart of the overall optimization methodology process presented here. We follow this design flow below.

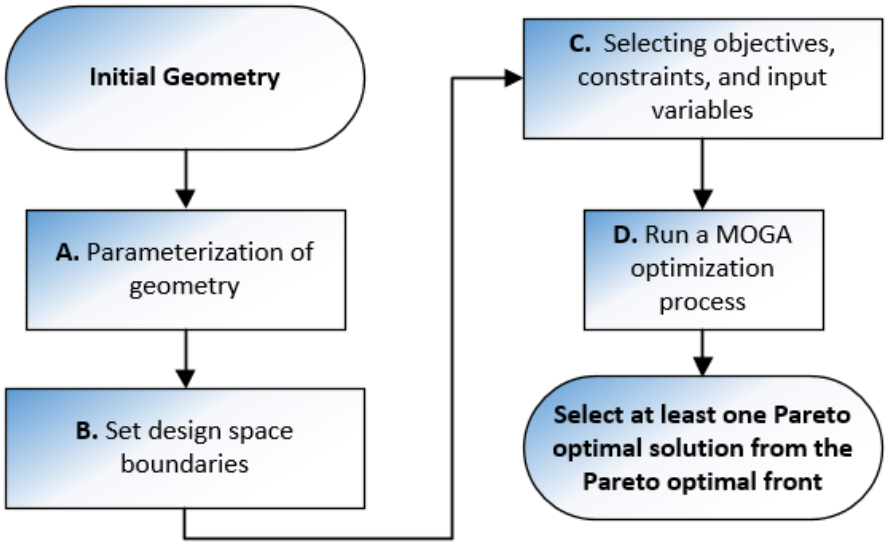


Figure 18. Flowchart of the optimization methodology process.

2.2.1 Parametrization of Geometry

We first parametrize our initial design as mostly a collection of spline control points, as seen in Figure 19. These control points determine the shape of the overall spline, allowing for a very fluid exploration of different designs. Additionally, a spline-based geometry allows for a continuity in the curvature profile of the interconnect, hence it is more likely to avoid high stress corners relative to geometries comprised of an abrupt connection of curves, lines, etc. This continuity in the curvature profile also helps the mesh processing as stress singularities are avoided along the spline. Therefore, via modifying the (x, y) coordinates of the spline control points, the shape of the MFI mask geometry is effectively modified. Additionally, in this case, the radius of the head or tip of the MFI is also a parameter that partially controls the photomask geometry.

2.2.2 Set Design Space Boundaries

After parametrizing the interconnect geometry, our optimization process calls to impose the design space boundaries. Specifically, each (x,y) coordinate of the MFI spline control points and the radius of the MFI tip must fall within some specified ranges. These ranges must be chosen so to avoid any intersecting and hence non-physical geometries and also to constrain the interconnect geometry from becoming too large.

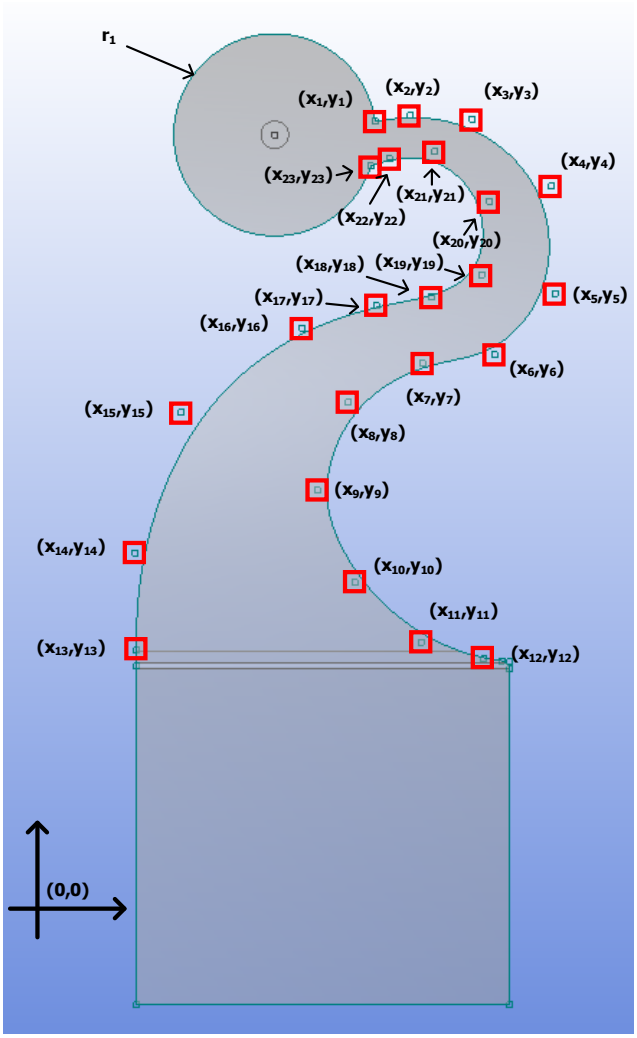


Figure 19. Parametrization of the MFI as a collection of spline control point (x,y) coordinates. Additionally, the radius of the MFI "head/tip" is also a parameter.

2.2.3 Selecting objectives, constraints, and input variables

After setting the design space boundaries, the objectives, constraints, and input variables of the multi-objective genetic algorithm are selected. Table 2 shows the input and objective variables used in this chapter. Note that in this case, vertical displacement acts as both an input and objective variable (discussed in Section 2.3).

For demonstration purposes, the improved mechanical robustness of the interconnect is the targeted outcome. More specifically, we are targeting the improvement of the mechanical robustness of the interconnect in scenarios where the interconnect is utilized as a temporary probing mechanism (e.g., probe cards, etc.).

Table 2. Input and Objective Variables

Input Variables	Objective Variables
(x,y) coordinates of the 23 spline points	Maximum von Mises stress
MFI tip radius	Mechanical compliance
Vertical displacement	Vertical displacement

To obtain the aforementioned outcome, the objective variables that we seek to optimize include: 1) the maximum von Mises stress within the interconnect, 2) the vertical (z-axis) displacement imposed upon the tip of the MFI, and 3) the mechanical compliance of the MFI. In short, our optimization process seeks to minimize the aforementioned maximum von Mises stress while simultaneously maximizing the vertical displacement of the MFI. Additionally, we impose a constraint upon the compliance of the MFI to stay within a specified range of 2 mm/N to 10 mm/N. In this specific demonstration, the reason for an upper limit on compliance is due to contact resistance considerations.

No surrogate model was used but instead a direct approach was pursued to achieve a more accurate optimization process. However, to expedite the process, a surrogate model such as Kriging (useful for computer experiments such as FEA-based simulations) may prove useful [145].

2.2.4 MOGA optimization process

After performing an optimal space-filling design of experiment (DOE), a multi-objective non-dominated sorting genetic algorithm-II (NSGA-II) is implemented. The optimization process eventually converges once the change in the mean and the standard deviation of max von Mises stress values and vertical displacement values are 2% or less relative to these same values in the previous generation.

2.3 FEA-Based Optimized Results and Discussion

2.3.1 FEA-based results and discussions

As seen in Figure 20, the initial MFI design has a stand-off height of 65 µm, a length of 150 µm from its anchor junction to the peak of the MFI tip, and a thickness of 9 µm. These dimensions are purposely left unchanged during the optimization process to minimize any modifications to the fabrication process. Modifying the photomask design, alternatively, is straightforward.

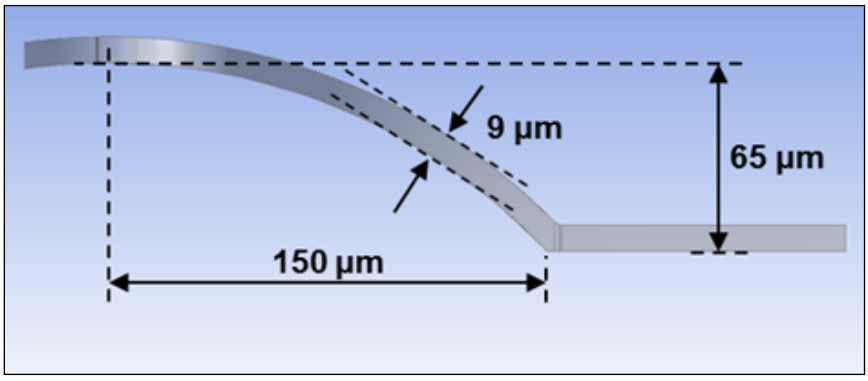


Figure 20. MFI side-geometry and corresponding dimensions.

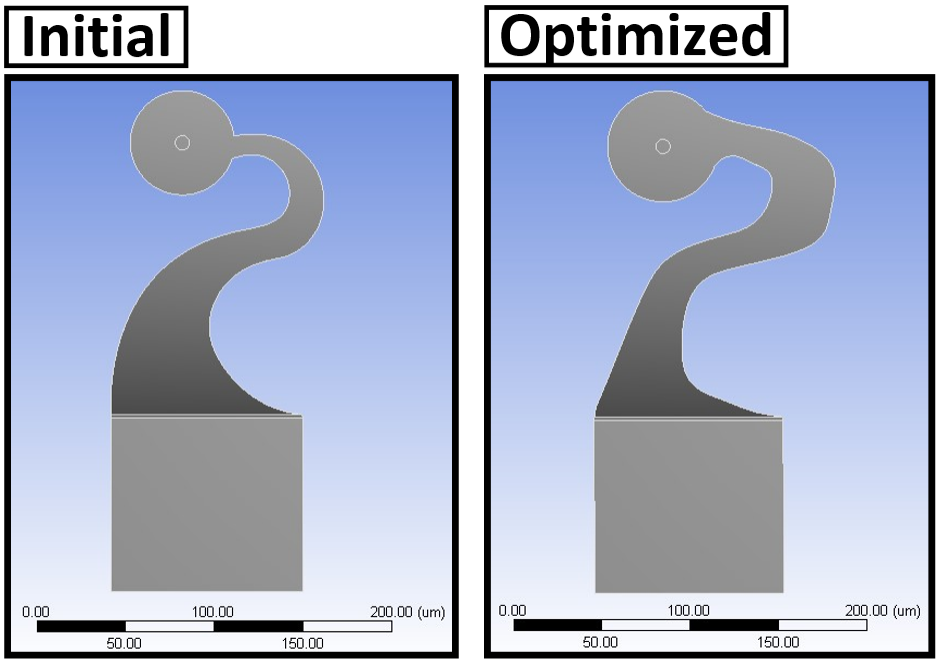


Figure 21. Geometry comparison of the initial, non-optimized MFI (left) and optimized MFI (right).

Figure 21 shows this optimized MFI (on the right) alongside the initial, non-optimized MFI (on the left). As is seen, the optimized MFI clearly has a different geometry relative to the initial MFI design.

Table 3. Optimization Results

	Max von Mises Stress (MPa)	**Compliance (mm/N)**
Initial MFI	1882.5	4.93
Optimized MFI	1324.2	5.52

ANSYS Workbench is used to evaluate the max von Mises stress in the MFIs. Furthermore, a nickel tungsten (NiW) alloy is chosen as the material of the MFI due to the relatively high yield strength that it can achieve (1.93 GPa [146]) compared to copper (Cu). This 1.93 GPa yield strength for NiW is used in the simulations. The NiW Young's modulus used was 180 GPa [146]. Using ANSYS Workbench, both MFIs (initial and optimized) are indented vertically (z-axis) at their tips to a depth of 24 μm, which results in only elastic deformation in both MFIs (maximum von Mises stress is below the NiW yield strength). The results are shown in Figure 22 and in Table 3. As is seen, for a 24 μm vertical displacement, the maximum von Mises stresses in the initial MFI and in the optimized MFI are 1882.5 MPa and 1324.2 MPa, respectively. Furthermore, the compliances of the initial MFI and the optimized MFI are 4.93 mm/N and 5.52 mm/N, respectively. Therefore, the optimization process resulted in a design that lowered max stress by 29.7% relative to the initial design while achieving a compliance of 5.52 mm/N within the targeted range of 2 mm/N to 10 mm/N.

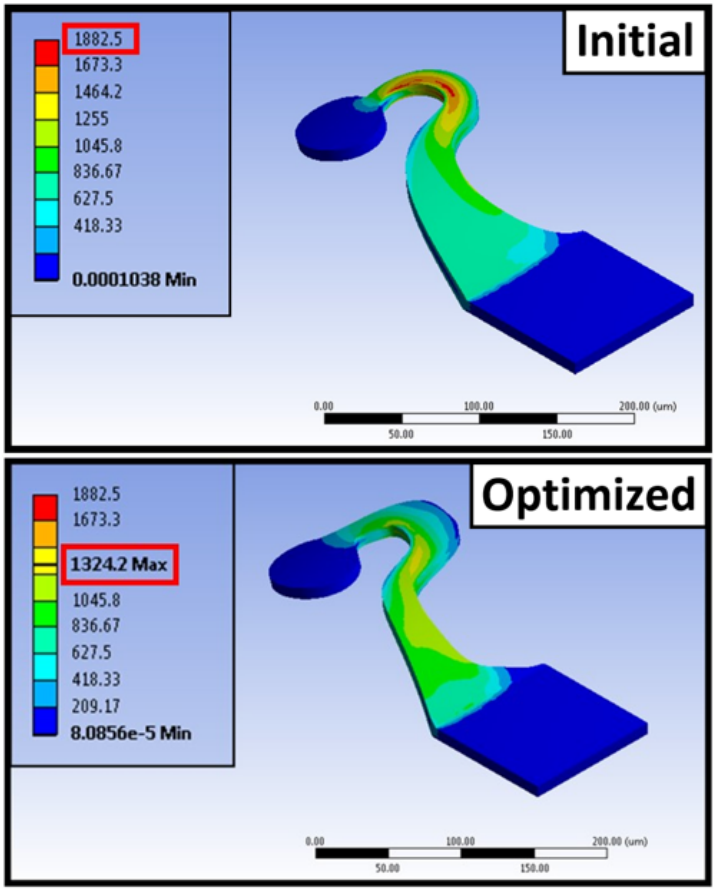


Figure 22. Von Mises stress results (in MPa) of the initial and optimized MFIs. A 29.7% decrease in max stress (1.88 GPa →1.32 GPa at 24 μm) is observed in the optimized MFI relative to the initial MFI.

Since simulations involving plastic deformation are more complex and hence slower, plastic deformations were ignored in the optimization process for simplicity and instead, all behavior was considered elastic. The omission of plastic deformation was also beneficial for the optimization process itself.

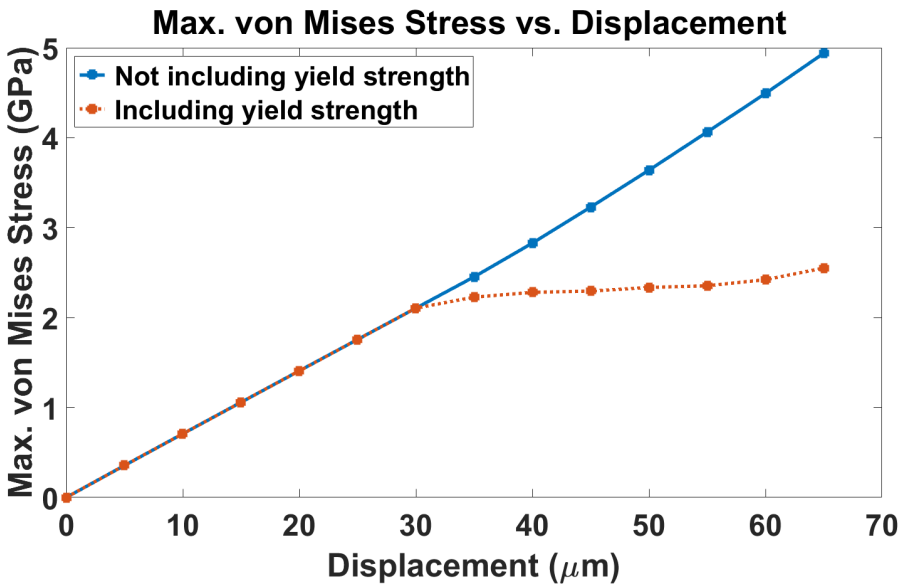


Figure 23. Maximum von Mises stress vs. displacement, with and without the incorporation of a plastic deformation model. If yield strength is considered, maximum stresses that exceed the yield strength of 1.93 GPa used in the simulations do not increase as quickly as stresses lower than yield strength. In an optimization framework, these "above yield strength" stresses are penalized on a different scale than stresses below yield strength, which is not the intent of the optimization process.

Specifically, when the yield strength of a material is exceeded, the stress/strain ratio decreases and hence any additional strain is associated with a lesser increase in stress relative to increases in strain that occur within the elastic region. From the perspective of the optimization process, this change in stress/strain ratio between the elastic region and the plastic region creates a scenario where increases in strain in the elastic region are penalized more heavily (i.e., higher relative stress) than increases in strain in the plastic region, which is not the intent of the optimization process. This concept is illustrated in Figure 23.

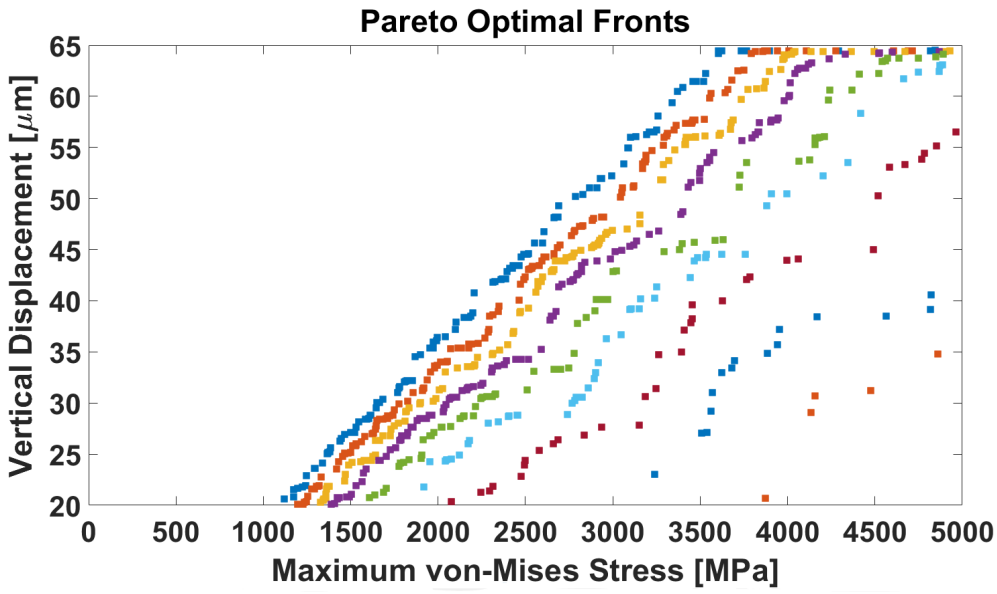


Figure 24. Pareto front successions (each Pareto front is identified as a different color) resulting from 31 iterations of multi-objective NSGA-II. Final Pareto front is in dark blue (most left).

Figure 24 demonstrates several Pareto fronts of the Pareto-optimal solutions (each identified as a different color on Figure 24) from the multi-objective NSGA-II optimization process. As observed in this figure, the solutions begin to converge near the left side of the graph until they finally converge at the final Pareto front (most left). Since all the solutions at the final front are Pareto optimal, it is left up to the designer's discretion to choose among these solutions. However, in this specific case, since one of the output variables is vertical displacement, it is possible that these "different" solutions result in the same MFI design. Therefore, to choose the final optimized solution, all the Pareto-optimal solutions were vertically indented at the same depth (this depth may be application specific). From these solutions, the selected MFI design exhibits the least amount of maximum von Mises stress. This optimized design is what is shown in Figure 21 and Figure 22.

The main reason the optimization process did not aim to minimize max von Mises stress at a fixed vertical displacement is since we wanted to obtain a variety of different MFI designs where some MFI designs are better suited for smaller vertical displacements and others are better suited for larger vertical displacements.

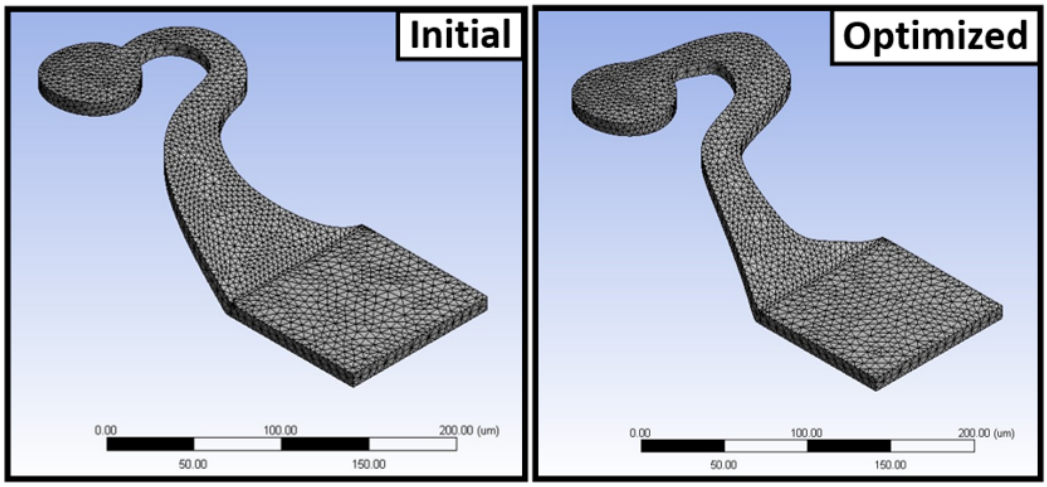


Figure 25. Mesh for the initial (left) and optimized MFIs (right) as implemented during the optimization process (not adaptive mesh refinement).

Table 4. Adaptive mesh refinement for the initial and optimized MFI meshing

MFI	Refinement Loop	Equivalent Stress (MPa)	Change (%)	Nodes	Elements
Initial	-	1882.5	-	25065	14105
	1	1861.8	-1.11	47551	28804
	2	1873.8	0.64	172127	115276
Optimized	-	1324.2	-	23870	13371
	1	1318.8	-0.41	76769	48432
	2	1319.7	6.8e-2	322868	221308

2.3.2 Meshing considerations

To obtain sufficiently accurate FEA-based max von Mises stress results, it is important that a high-quality mesh be implemented as these results are mesh size dependent. Moreover, it is critical to reduce the risk of simulation artifacts (e.g., stress singularities) as these also lead to inaccuracies. To address these challenges, this chapter has: 1) taken several steps to avoid stress singularities and 2) evaluated our meshing strategy in order to ensure sufficient mesh granularity to avoid inaccuracies.

To address the matter of stress singularities, extensive efforts were performed to smooth corners and interfaces. Specifically, as aforementioned, spline-based parametrization was implemented, in part, to ensure smoothly-varying structural profiles. In addition, fillets were used extensively to soften sharp edges of the modeled MFI structure as seen in Figure 26.

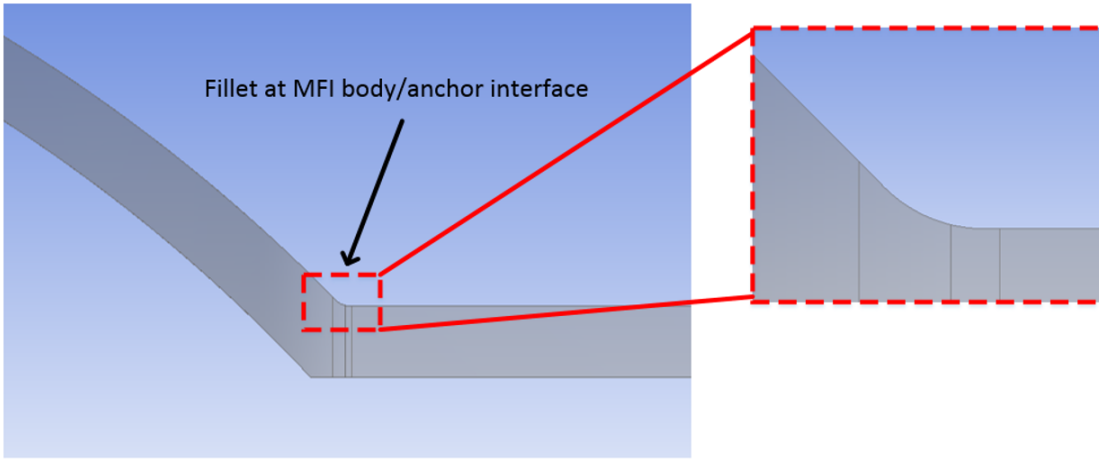


Figure 26. Fillets were used to “soften” sharp edges of the MFI geometry.

We also evaluated our meshing profile using the adaptive mesh refinement feature in ANSYS Workbench for both initial and optimized MFIs to test the accuracy of the simulation results. Additionally, we display the original mesh of the initial and optimized MFIs as shown in Figure 25. The adaptive mesh refinement results, shown in Table 4. Adaptive mesh refinement for the initial and optimized MFI meshing, demonstrate that the max von-Mises changes little (≈1% or less) even after a large increase in the number of elements (about an order of magnitude larger) is adaptively added to the mesh.

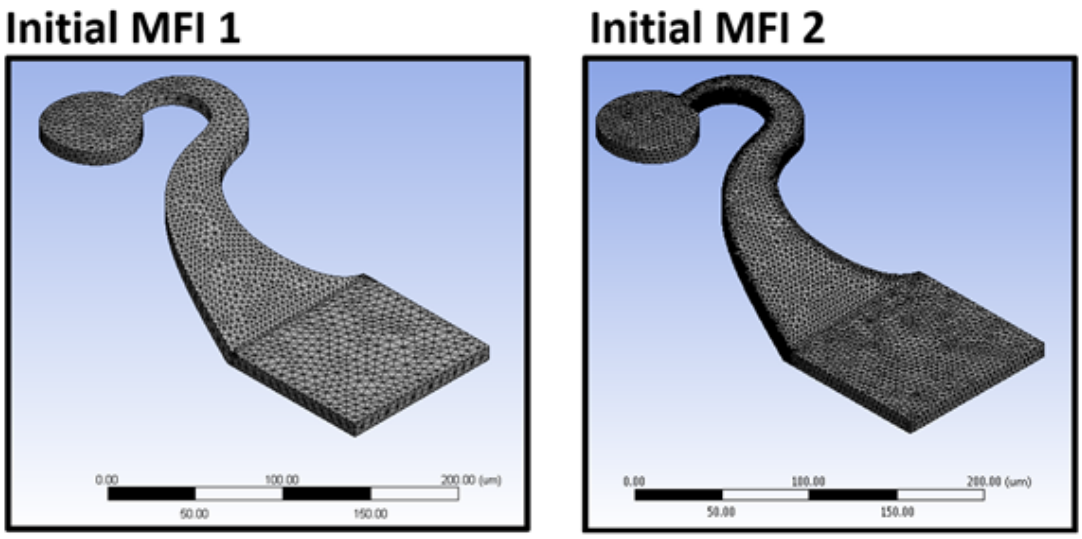


Figure 27. Mesh quality comparison between "Initial MFI 1" mesh and "Initial MFI 2" mesh.

Furthermore, for further validation, the optimization process was performed again using a finer overall mesh on the MFI model as seen in Figure 27 and reported in Table 5. To distinguish between the original MFI mesh model and the "finer-mesh" MFI mesh model, we designate the former as "Initial/Optimized MFI 1" and the latter as "Initial/Optimized MFI 2."

The converged optimized outcome of the "Optimized MFI 2," as seen in Figure 28, resulted in a design that lowered max Von Mises stress (relative to the pre-optimized MFI) by an additional 1.7% compared to the "Optimized MFI 1" max Von Mises stress result (1292.2 MPa vs. 1324.2 MPa) as seen in Table 5. However, due to the finer mesh quality, the overall optimization process time for "Optimized MFI 2" was approximately twice as long as the original optimization process for "Optimized MFI 1." Overall, the similarities between "Optimized MFI 1" and "Optimized MFI 2" provide further validation that the original mesh quality is sufficient.

Table 5. "Optimized MFI 1" vs. "Optimized MFI 2"

	Mesh quality for Initial MFI (1 and 2)					
MFI	**Number of elements**	**Number of nodes**	**Max von Mises Stress at 24 µm (MPa)**	**Compliance (mm/N)**	**Number of optimization iterations**	**Optimization duration relative to Optimized 1**
Optimized 1	14105	25065	1324.2	5.52	31	1
Optimized 2	72667	115340	1292.2	5.15	29	≈2

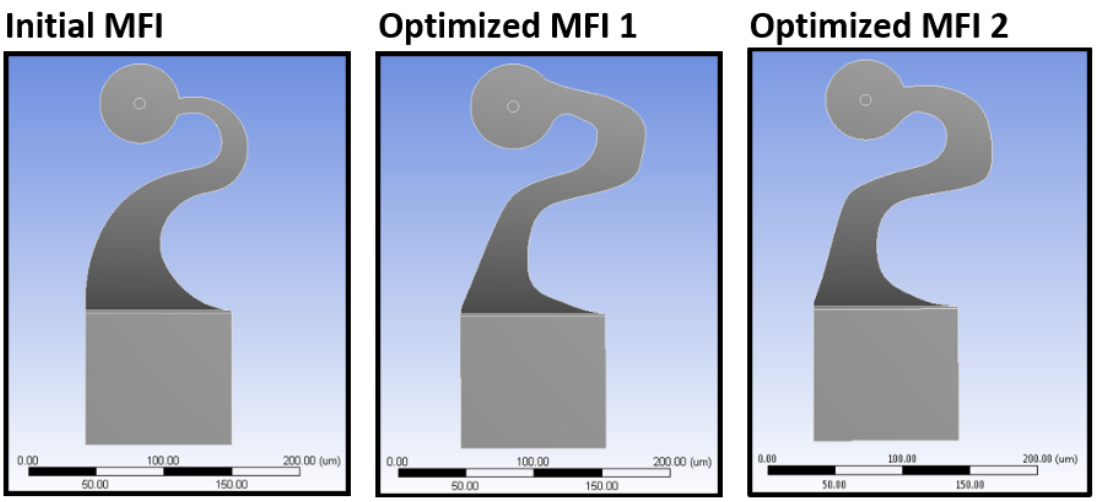


Figure 28. Geometrical comparison between "Optimized MFI 1" and "Optimized MFI 2" (and the initial, pre-optimized MFI).

Since there exists an inherent tradeoff between high fidelity simulations and simulation run time (and therefore overall optimization process time), it is at the discretion of the designer as to how he/she prioritizes these factors. This chapter attempted to achieve a sufficiently high-quality mesh for our MFIs while maintaining the average simulation run time to a reasonable limit.

As a note, the remainder of this chapter alludes only to the simulation results associated with "Initial/Optimized MFI 1."

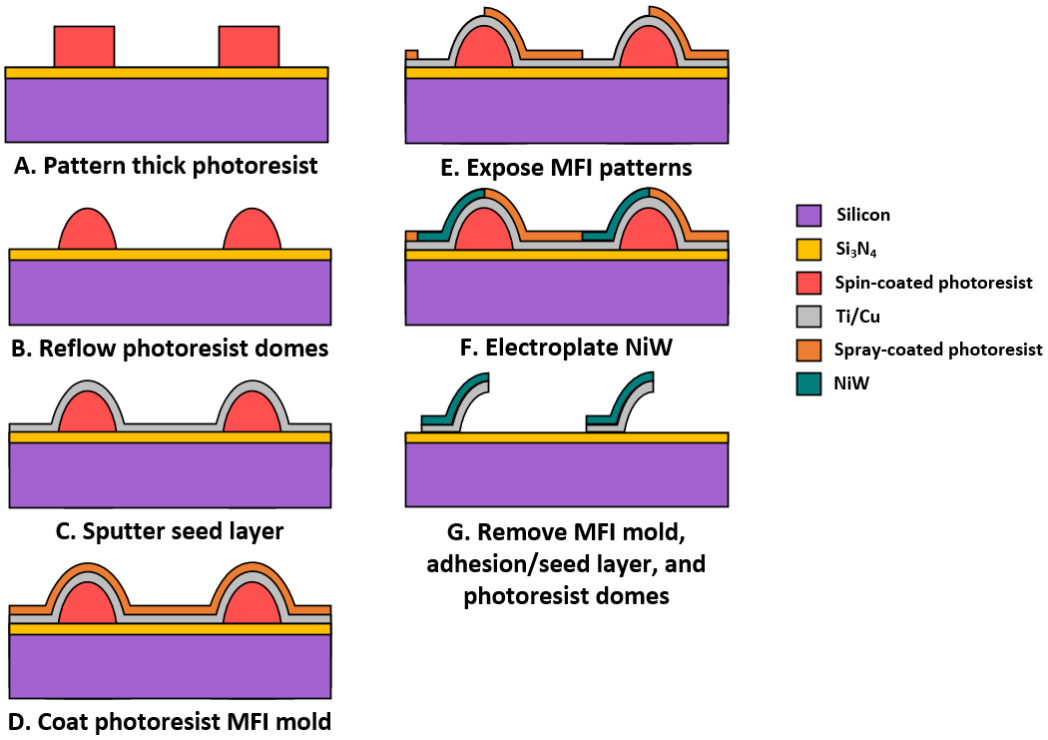


Figure 29. Fabrication process flow for MFIs.

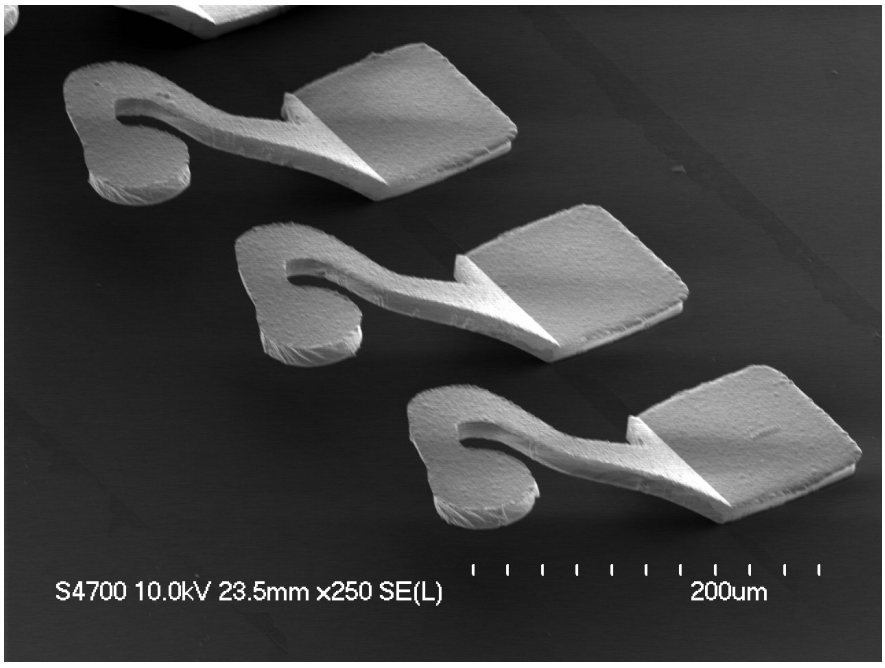


Figure 30. SEM image of optimized MFIs.

2.4 Experimental Results

2.4.1 Microfabrication

To provide a more complete analysis of the simulated optimization process, MFIs were microfabricated via a reflowed polymer-dome process [115], [143], [144], [147], as seen in Figure 29, with the initial and optimized photomask designs. The MFI process flow begins with the patterning of a thick sacrificial spin-coated photoresist layer so that a relatively large stand-off height for the MFIs is attainable. Next, the patterned photoresist is thermally reflowed via exceeding the glass transition temperature (T_g) of the photoresist. A 30 nm thick titanium (Ti) adhesion layer followed by a 300 nm thick Cu seed layer is then sputtered onto the sample. To form the electroplating molds for the MFIs, a photoresist layer is first spray-coated onto the reflowed domes and then patterned. The sample is then placed into an electroplating bath where a NiW alloy is electroplated into the molds. The specifics of the electroplating recipe will be discussed in the next paragraph. Finally, the spray coated photoresist, the Ti adhesion layer and Cu seed layer, and the sacrificial reflowed photoresist dome are removed in sequence, leaving free-standing NiW MFIs. Figure 30 shows an SEM image of several microfabricated optimized MFIs and Figure 31 shows an SEM image of the optimized MFI alongside the initial MFI.

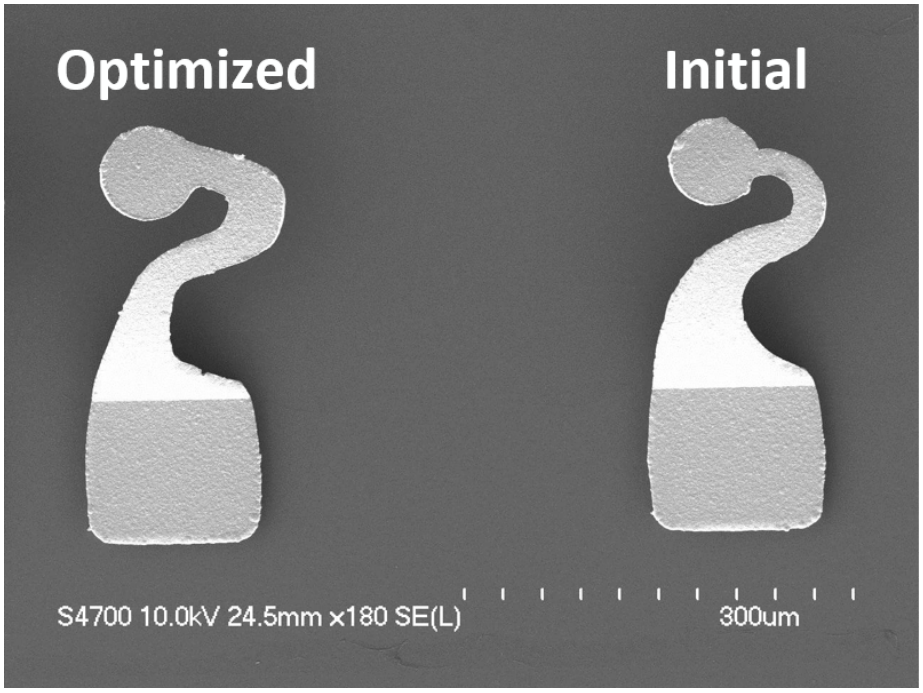


Figure 31. SEM image of the optimized MFI (left) and initial, non-optimized MFI (right).

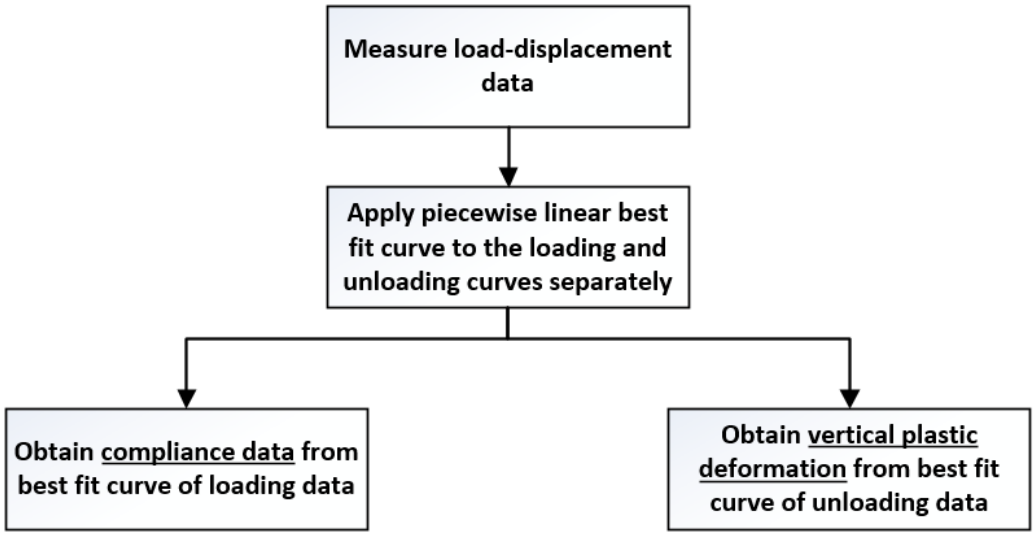


Figure 32. Flowchart illustration of the experimental data extraction process.

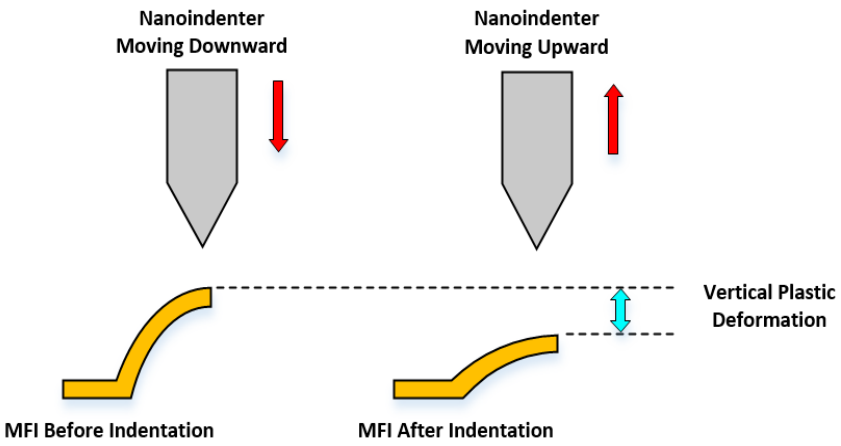


Figure 33. MFI side-view illustration shown before indentation occurs and after indentation occurs. This single indentation induces a certain vertical plastic deformation (if yield strength is exceeded).

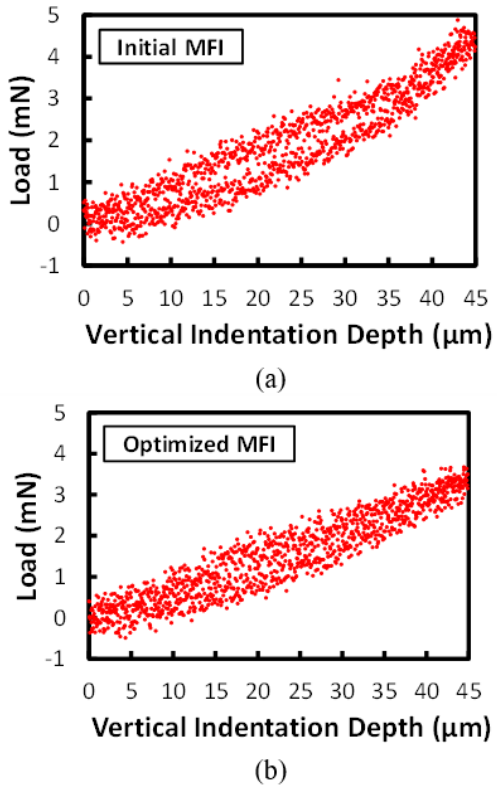


Figure 34. Raw "load vs. displacement" data for an MFI pair, (a) initial and (b) optimized, indented to a vertical depth of 45 μm.

The MFIs were electroplated using the general procedures found in [146] to carry out this process, as we have done in the past [115], [143], [147]. Specifically, the MFIs were electroplated using a nickel sulfamate bath (Elevate Ni 5910 RTU from Technic) with the addition of sodium tungstate dihydrate and citric acid to provide a certain tungsten concentration to the bath that ultimately forms a NiW alloy electroplating solution. We added approximately 3.5 g of sodium tungstate dihydrate to 1 L of the nickel sulfamate solution (i.e., 3.5 g/l). The bath was then heated to approximately 50°C before electroplating. The NiW deposition was then performed using pulsed current (PC) plating. The electroplated NiW thickness for the MFIs was measured to be approximately 6.9 μm.

Since we desired to plastically deform both initial and optimized MFI samples so that a quantitative comparison between the two designs was possible, the MFIs were fabricated in such a way that plastic deformation of the MFIs was observable for a given indentation depth. To this end, the NiW yield strength was deliberately decreased via using a lower tungsten concentration in the plating solution. A higher tungsten concentration (i.e., 20 g/l sodium tungstate dihydrate [146]) added to the Ni sulfamate plating solution contributes to a higher yield strength such that only elastic deformation may occur over a full indentation (i.e., indented up to the point where the MFI tip touches the substrate).

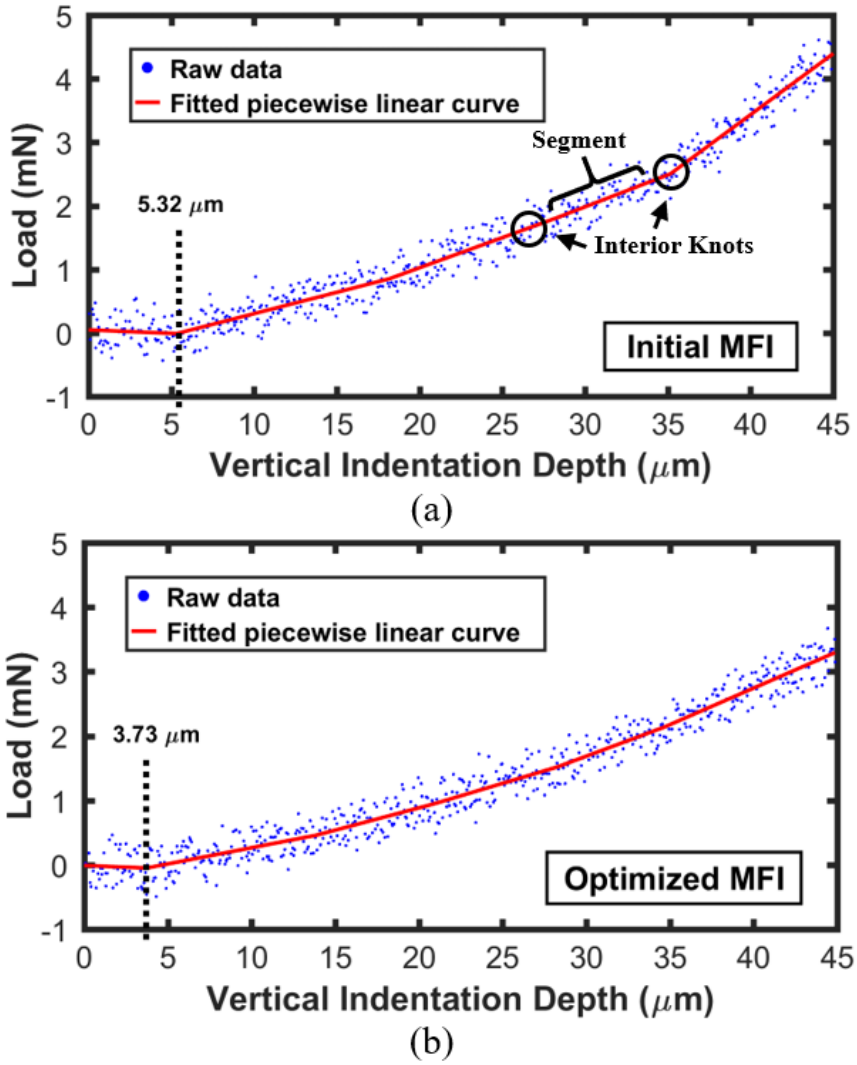


Figure 35. Unloading portion of the experimental load-displacement data with a best fit piecewise linear curve. Data for (a) initial MFI and (b) optimized MFI both indented to a depth of 45 μm is shown. Interior knots of the best fit curve (and segment) are also shown.

2.4.2 Measurements and Data Analysis

Figure 32 illustrates a flowchart of the measurement extraction process followed in this chapter. After electroplating and fabricating our structures, we indented our MFIs using a Hysitron Triboindenter with a Cono-Spherical probe to obtain load (and unload)

vs. displacement data. From these measurements, we sought to determine two data points for each indented MFI: 1) the amount of vertical plastic deformation, as seen in Figure 33, and 2) the mechanical compliance. Figure 34 shows the raw load vs. displacement data of closely located initial and optimized MFIs, both indented to a depth of 45 μm.

To analyze this data more accurately, a best fit piecewise linear curve (or first-order spline) was implemented using MATLAB built-in functions on the loading and unloading portions of the raw data as seen in Figure 34. The interior knots of the piecewise linear curve (a seven-segmented piecewise linear curve, each segment joined together via the interior knots) were positioned such that the overall curve was a best fit to the raw data; specifically, the sum of squares due to error (SSE) of the best fit curve with respect to the data was minimized for a given number of interior knots. The best fit curves seen in Figure 35 were applied to the unloading portions of the raw data seen in Figure 34. As seen in Figure 35, the vertical plastic deformation is extracted from the best fit curve.

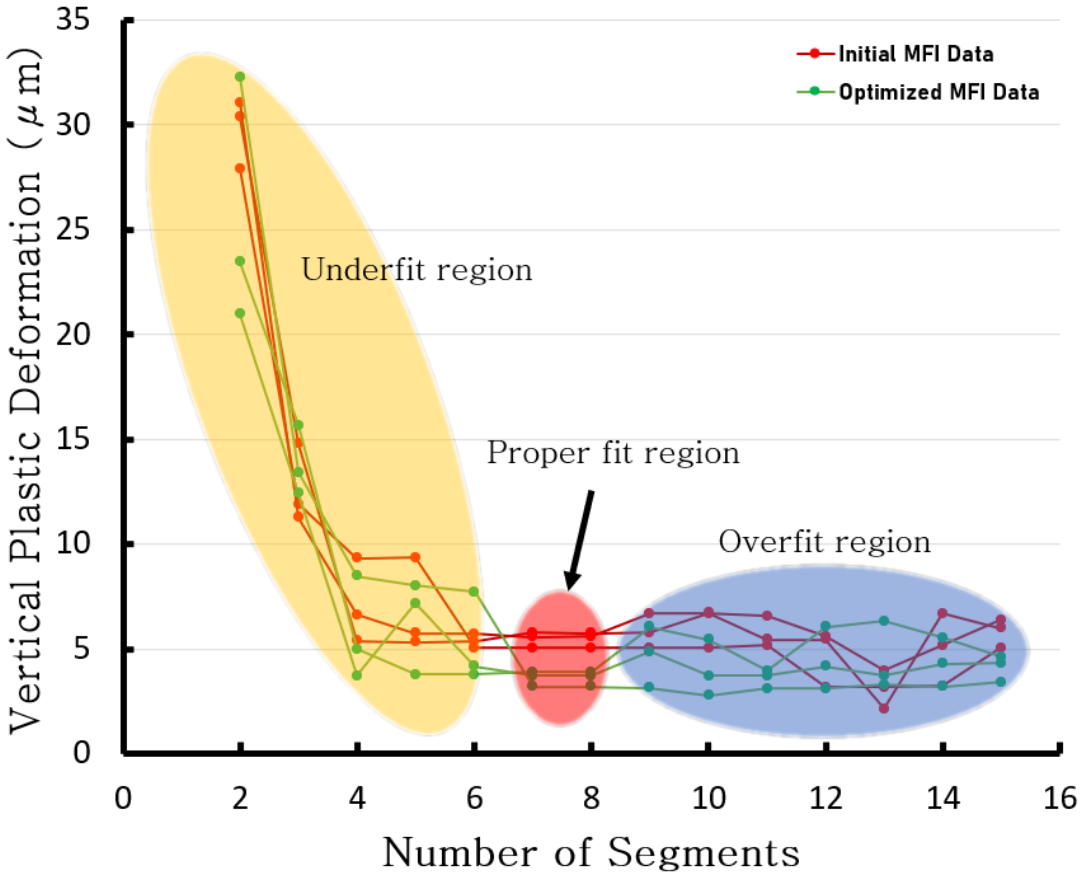


Figure 36. Number of segments (N_s) of the best fit curve for extracting plastic deformation versus the extracted plastic deformation of the indented MFI. The number of segments chosen for the best fit curve comes from the "Proper fit region" as opposed to the underfit and overfit regions.

The number of interior knots chosen for the aforementioned seven-segmented best fit piecewise linear curve was determined via plotting the number of segments of the N_s-segmented best fit piecewise linear curve (where N_s refers to the number of segments of said best fit curve) against the extracted vertical plastic deformation of the MFI from each N_s-segmented best fit curve where N_s varies from 2 to 15. This plot is shown in Figure 36. The relationship between the number of segments of the best fit curve, N_s, and the number of interior knots of the best fit curve, N_k, is shown below in Equation (1).

$$N_k = N_s - 1 \tag{1}$$

As seen in Figure 36, changing the number of segments (or interior knots) of the best fit curve changes the resulting extracted vertical plastic deformation. When there is an insufficient number of segments, the best fit curve is underfitted; the underfit region consequently demonstrates the large variation in extracted vertical plastic deformation for both the optimized and initial MFIs. Alternatively, when there is an excess number of segments, the best fit curve is overfitted; the overfit region also demonstrates a large variation in the extracted plastic deformation values. In between these underfit and overfit regions exist a "proper fit" region where the number of segments (or interior knots) of the best fit curve yields consistent results for the initial MFI samples and the optimized MFI samples. It is within this region where we wish to have our best-fit curve; therefore, the number of segments chosen for the best fit piecewise linear curve was seven (or six interior knots). An eight-segmented best fit piecewise linear curve results in almost the same exact extracted plastic deformations results as seen in Figure 36.

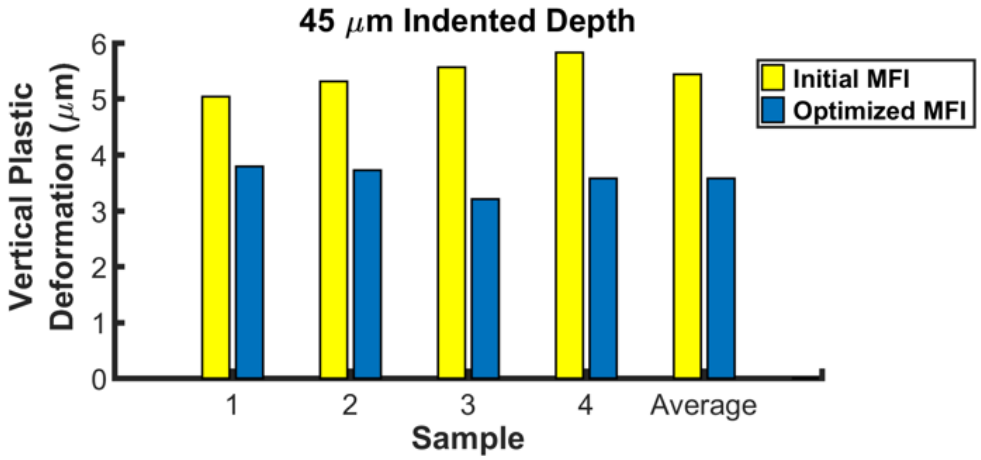


Figure 37. Vertical plastic deformation of optimized and initial MFI samples for MFIs indented to a depth of 45 μm.

Table 6. Compliance for initial and optimized MFI pairs

Sample	Initial MFI Compliance (mm/N)	Optimized MFI Compliance (mm/N)
1	11.17	12.10
2	10.57	12.42
3	11.31	11.69
4	11.13	14.09
5	11.19	11.49
6	10.93	12.75
7	10.20	11.23
Average	**10.93**	**12.25**

Table 6 shows the experimentally-obtained compliance measurements. Recall that the fabricated MFI thickness was measured to be approximately 6.9 μm as opposed to the simulated MFI thickness of 9 μm. Therefore, as expected, the measured compliance is higher than the simulated compliance.

To more specifically compare against the aforementioned experimental compliance data, 6.9 μm thick MFIs were simulated to obtain compliance. As seen in Table 7, we obtain a simulated compliance of 9.69 mm/N and 11.10 mm/N for the initial MFI design and the optimized MFI design, respectively. The main source of discrepancy between the experimental data and the simulation data may potentially derive from a difference in the Young's modulus used in the simulation (i.e., 180 GPa [146], [148]) and the actual Young's modulus of the microfabricated MFIs. Differences in geometry between simulated and fabricated MFIs may also play a role.

Table 7. Experimental and simulated compliance for initial and optimized 6.9 μm thick MFI pairs

Data Type	Initial MFI Compliance (mm/N)	Optimized MFI Compliance (mm/N)
Experimental (Avg.)	10.93	12.25
Simulation	9.69	11.10

In an effort to obtain vertical plastic deformation measurements, this same implementation of a best fit piecewise linear curve was performed on the remaining additional raw unloading data and is recorded in Figure 37. Comparisons in Figure 37 between optimized MFIs and initial MFIs are done for different MFI samples or pairs. In this chapter, MFI pairs are defined as an initial MFI and an optimized MFI that are physically near each other on the Si wafer (on the same polymer dome for example) so that geometric parameters such as height and thickness are as similar as possible for the two

structures. As seen in Figure 37, the average vertical plastic deformation for the initial MFI and the optimized MFI indented to a depth of 45 μm is 5.44 μm and 3.58 μm, respectively, a 34.2% average decrease in vertical plastic deformation for the optimized MFI.

To reiterate, the observed plastic deformation of the MFIs was intentionally desired so that a quantitative comparison between initial and optimized designs was possible. Typically, we wish to avoid plastic deformation. As aforementioned, increasing the yield strength of the electroplated NiW is one means by which such plastic deformation is avoided. This elastic-only behavior (up to 65 μm) has been reported with our MFIs in the past [115].

2.4.3 Material Data Extraction First-Order Approximation

To extract a first-order approximation of the mechanical material properties of the fabricated NiW MFIs, an optimization process was performed where the corresponding optimization goals were the experimentally-obtained data (vertical plastic deformation and compliance). Specifically, the extracted material properties of the NiW-alloy MFI were 1) Young's modulus, 2) the tangent modulus at yield strength, 3) yield strength, and 4) Poisson's ratio.

These specific material properties correspond to the full set of material properties of the used elastic-plastic model in ANSYS Workbench; more specifically, the elastic-plastic model used is an "isotropic elasticity" + "bilinear isotropic hardening" model. Hence, this elastic-plastic model was used during the material extraction optimization process. In other words, these material properties were varied using the elastic-plastic model until an optimal

set of these properties were attained, which resulted in simulated results that matched the corresponding experimental results (for both vertical plastic deformation and compliance).

Specifically, these MFI material properties were optimized in ANSYS Workbench (via the elastic-plastic model) such that the corresponding simulation results matched the aforementioned experimental data: 1) an optimized MFI compliance of 12.25 mm/N, 2) an initial MFI compliance of 10.93 mm/N, 3) an optimized MFI average vertical plastic deformation (at a 45 μm displacement) of 3.58 μm, and 4) an initial MFI average vertical plastic deformation (at a 45 μm displacement) of 5.44 μm. Note that only the 45 μm indentation data was used for this material extraction process.

To provide validation to these extracted first-order approximation material properties, which are shown in Table 8, the experimental vertical plastic deformation for both optimized and initial MFIs were compared against the corresponding simulation results when said MFIs were vertically indented downward by 40 μm (as opposed to 45 μm). The corresponding comparisons between experimental data and simulation results for both optimized and initial MFIs (with indented depths at both 40 μm and 45 μm) when using the extracted material properties for the simulation model is shown in Table 9.

For emphasis, the optimization process to extract the material properties from the experimental data (and matching it to the simulations where we varied the material properties of the simulated MFIs) used only the experimental 45 μm indented depth average vertical plastic deformation data and not the 40 μm indented depth average vertical plastic deformation data. The latter data (40 μm indented depth data) was only used to compare against the corresponding simulation results to provide validation that the material

properties that were extracted is a good fit in matching the simulation and experimental results (at least near the 45 μm indentation depth mark, hence first-order approximation).

The extracted first-order approximation Young's modulus is approximately 166.4 GPa. As is seen in the previous literature [146], [149], this value falls within a reasonable range, especially given the temperature of the bath (50° C) and the current density of the electroplating process (≈7.5 mA/cm^2). As expected, the extracted first-order approximation tangent modulus at yield strength of 64.4 GPa is lower than the Young's modulus. Additionally, this extracted value is similar to the NiW tangent modulus at yield strength obtained in [146] of approximately 75.7 GPa.

The first-order approximation extracted yield strength of the MFI's NiW is approximately 966.8 MPa. As aforementioned, we attempted to follow the general procedures in [146] for electroplating NiW and the resulting yield strength of the NiW alloy in [146] with the lowest tungsten concentration (tungsten concentration of 4.2 g/l) and a current density of 10 mA/cm^2 is approximately 1070 MPa. In our case, as aforementioned, a lower tungsten concentration of 3.5 g/l was used, which would result in a lower yield strength as observed.

Table 8. Extracted electroplated NiW first-order approximation mechanical properties

Extracted Mechanical Parameters			
Young's Modulus	Tangent Modulus at Yield Strength	Yield Strength	Poisson's Ratio
166.4 GPa	64.4 GPa	966.8 MPa	0.26

Table 9. Experimental and simulation results for vertical plastic deformation

Indented Depth	Vertical Plastic Deformation for Optimized MFIs			Vertical Plastic Deformation for Initial MFIs		
	Avg. Experimental	Simulation	Sim. Pct. Difference relative to Experimental	Avg. Experimental	Simulation	Sim. Pct. Difference relative to Experimental
45 µm	3.58 µm	3.63 µm	**+1.40%**	5.44 µm	5.37 µm	**-1.29%**
40 µm	1.79 µm	1.82 µm	**+1.68%**	3.67 µm	3.62 µm	**-1.36%**

Any differences between the experimental data and simulation results may be attributed to differences in the "good fit" model of the extracted material values used in the simulations and the actual material parameters of the electroplated NiW. Other differences between experiment and simulation may derive from: 1) differences in the overall geometries between experimental MFIs and simulation MFIs and/or 2) different positions on the tip of the MFI where the nano-indenter probe is exerted (for example, simulations have the indentations being exerted at the exact center of the MFI tip; this situation may not be the exact case for the experimentally indented MFIs).

For emphasis, the extracted material data is a first-order approximation as it is a good fit in matching the corresponding simulation and experimental results (near the 45 µm indented depth mark).

2.5 Discussion of Idealized Loading

For the idealized loading condition (i.e., force aligned with z-axis) employed in the simulation as seen in Figure 38, the only goal of the optimization process is to minimize the maximum observed von Mises stress within the MFI structure while this MFI structure operates within a specified compliance range (2-10 mm/N). The optimization process did not include a means to eliminate stress concentrations, which is why a stress concentration is still observed in the optimized design. Additionally, the optimized design is not a globally optimized design within the specified design space. It is an optimized design in the sense that the optimization process converged on a solution which satisfied the compliance restriction while minimizing the absolute maximum stress as described in Section 2.2.4. This optimized design is likely near a local optimum (rather than a global optimum). A gradient-based algorithm may be implemented in future work after arriving at this converged optimized design to perhaps reach the "peak" of the local optimum region. Additionally, to this end, a more stringent convergence criteria may be employed.

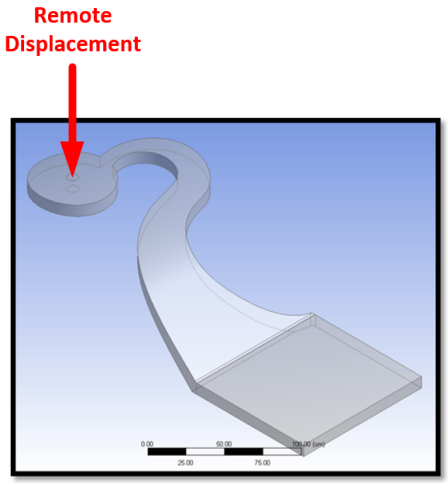


Figure 38. A remote displacement (completely vertical) is exerted atop the center of the circular region of the MFI (the MFI "head") for the simulations. This remote displacement represents an ideal loading condition.

For this particular optimized MFI design and ideal loading condition, it appears as if additional material is added to the neck region to reduce the average stress value in this region relative to the initial design as seen in Figure 39. A stress concentration still appears in the neck region of the optimized design but to a lesser extent and with less maximum stress for the given ideal loading condition with the maximum stress value for the optimized design reduced to greater than 30% of the original value (i.e., <1324 MPa for the optimized design vs. 1882 MPa for the initial design for an indentation depth of 24 μm, which is a greater than 30% reduction in the maximum stress in the neck region). The main stress concentration of the optimized design appears in the upper body region of the MFI as seen in Figure 39. However, the overall maximum stress in this region (and throughout the entire optimized MFI structure) is less than the maximum stress in the initial design's neck region, which is consistent with the goal of the optimization process of minimizing maximum stress. To reiterate, the optimization process only accounts for an ideal loading

condition and only targets the minimization of maximum stress (and not the elimination of stress concentrations).

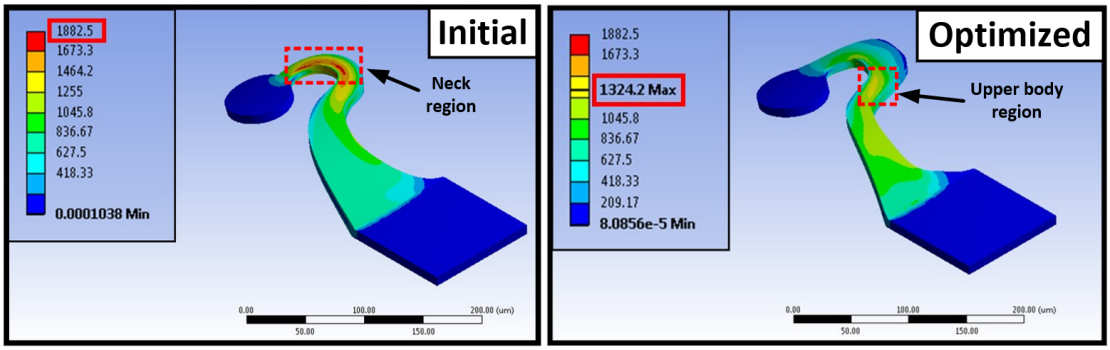


Figure 39. Neck region and upper body region of the MFI are identified.

That being said, it is important for future work to incorporate several factors into consideration. Although it is observed that the maximum stress was minimized for the optimized design relative to the initial design for the specific ideal loading condition applied in this optimization work, it is certainly possible that in a more practical scenario where non-ideal loading conditions would be exerted that we may observe a higher maximum stress in the stress concentrations of the optimized design relative to the stress concentrations of the initial design, which would be the opposite of what is targeted. Future work should not only focus on minimizing maximum stress alone, but it should also potentially implement some geometric constraints to minimize stress concentrations as well since the removal of stress concentrations will aid to prevent unexpected failures. For example, such geometric constraints may force certain radii of portions of the MFI structure to exceed some specified radius minimum. In other words, the reduction of geometric stress concentrations is a useful metric to include in future studies so long as the compliance and strain constraints are met. Additionally, future work should incorporate

not just a single ideal loading condition, but it should also explore the effect of non-ideal loads in an attempt to increase the mechanical performance of the MFI structure in a more realistic environment where different non-ideal loads may exist in practice (i.e., loads at angles to the z-axis not centered on the MFI head/pad). This section regarding future work will be repeated again in the Future Work section of CHAPTER 7 for emphasis.

2.6 Conclusion

This chapter introduced a generalized optimization methodology for MEMS-type flexible interconnects using a multi-objective, non-dominated sorting genetic algorithm-II (NSGA-II) to minimize maximum von Mises stress and maximize vertical displacement while maintaining a compliance within a targeted range. Relative to the initial NiW MFI design, the simulated results for the optimized MFI demonstrate an increase of 29.7% in vertical displacement before the MFI's max von Mises stress exceeded its yield strength. After microfabrication of the NiW MFIs, indentations were performed on these MFIs and load vs. displacement data were collected. To more accurately analyze and interpret this data, a best-fit piecewise linear curve was implemented from which compliance and vertical plastic deformation was extracted. The optimized microfabricated MFI demonstrated a 34.2% decrease in vertical plastic deformation relative to the initial MFI for a 45 μm indentation depth. In both simulation and experimental scenarios, the optimized MFI demonstrated less stress/plastic deformation relative to the initial MFIs for the same given indented depth, as intended.

CHAPTER 3. A DISPOSABLE AND SELF-ALIGNED 3D INTEGRATED BIO-SENSING INTERFACE MODULE (BIM) FOR CMOS CELL-BASED BIOSENSOR APPLICATIONS

3.1 Introduction

Cell-based biosensing platforms, including CMOS biosensors, continue to impact pre-clinical pharmaceutical development, point-of-care testing, environmental monitoring, and pathogen detection [65]–[69], [74], [150]–[156]. CMOS cell-based biosensors in particular are attractive due to their high degree of integration, unparalleled signal processing, fast response, and low power, all at a potential low cost. Important for many CMOS cell-based biosensors in the aforementioned applications are the following: 1) high throughput, 2) minimal contamination (sterility assurance level (SAL) of 10^{-6}), 3) low cost, 4) large field-of-view, and 5) high resolution.

Currently, CMOS cell-based biosensors require post-fabrication processing typically due to the electrochemical instability of their foundry-fabricated surface electrodes (e.g., aluminum) in a saline-based medium, due to certain necessary surface treatments to improve cell adhesion and growth, and due to efforts to minimize signal-to-noise ratio (SNR), all which serve to increase processing costs [65], [71], [77], [152], [157]. Throughput is also limited if the CMOS biosensor is reused as sterilization is necessary to minimize cross-contamination (and sterilization methods are limited as CMOS devices are present) [158], [159]. Disposing and replacing the biosensor is another (and more effective)

option to circumvent cross contamination; however, this route is difficult/impractical as the biosensor is likely to be permanently attached and wire bonded to the package or board.

In an attempt to address these challenges, this chapter presents a non-permanent 3D SiP-based biosensor system, termed a biosensing-interface module (BIM), as seen in Figure 40 and Figure 41, that serves to act as a 3D integrated interface between the underlying CMOS biosensor and the cells grown atop the surface. This electrical interface circumvents the need to post-process the CMOS biosensor while allowing for a quick and manual place-and-replace mechanism for high throughput testing. Additionally, as the BIM is scalable, high resolution and large field-of-view data is achievable. As few 3D packages for biosensing applications exist, such as the BIM presented here, the focus of this chapter is on the die-level socketed module and hence, for demonstration purposes, the BIM is interfaced with a test die and not a CMOS biosensor.

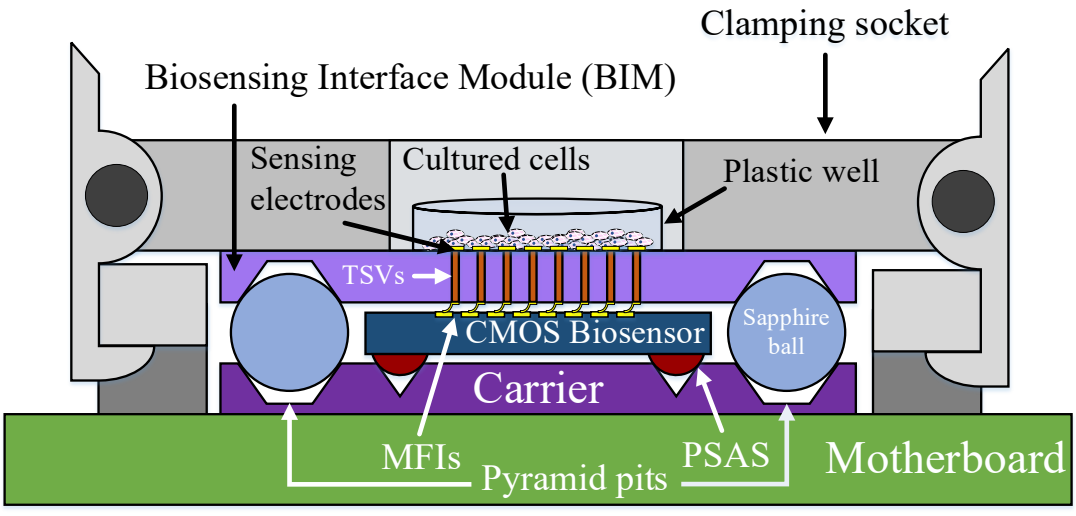


Figure 40. Biosensing-interface module (BIM) in a modular testing system.

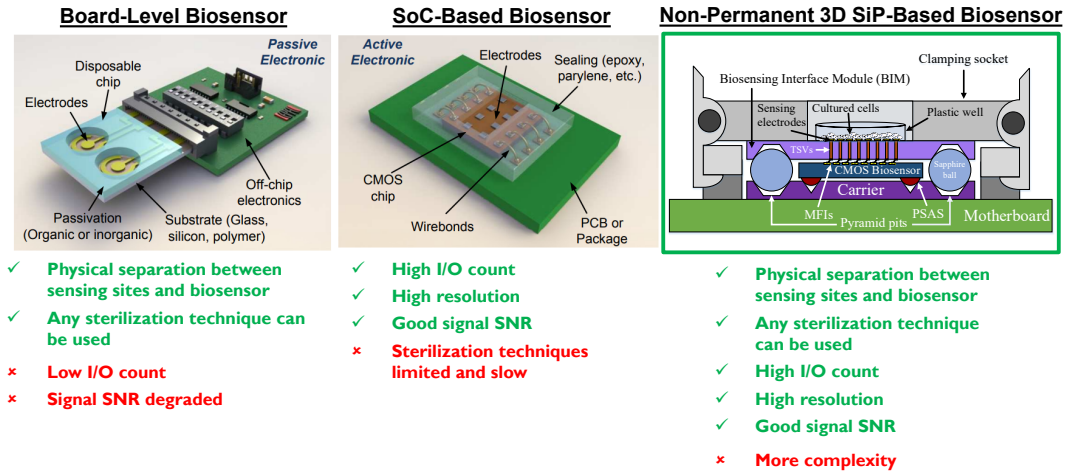


Figure 41. Comparison between board-level biosensors, SoC-based biosensors, and the presented non-permanent 3D SiP-based biosensor introduced in this chapter.

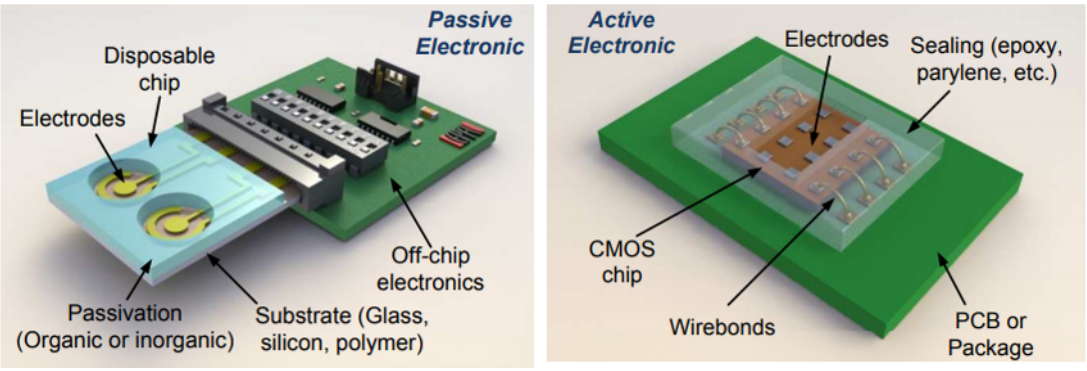
The advantages associated with the presented BIM include the following: 1) self-alignment facilitates temporary interconnections, increases testing throughput as alignment placement tools are avoided, and enables field-deployable applications as a simple manual placement suffices for assembly, 2) temporary interconnections allow for the disposal of the BIM, which circumvents cross contamination, and hence leads to increased throughput as sterilization processes are avoided, and 3) since the BIM does not contain any CMOS devices, etc., it does not require a CMOS-only fabrication process, hence culture medium biocompatible materials and necessary surface treatments are easily incorporated into the overall fabrication process, which can potentially be performed at the wafer level, hence leading to decreased costs in accordance with economies of scale.

Our previous work introduced an "electronic-microplate" (e-microplate) that demonstrated preliminary data on the functionality of such an interface platform [72]. However, the e-microplate was not disposable/replaceable nor did it possess self-alignment

capabilities, which are needed to facilitate the replaceability of the interface system. In contrast to the module introduced in this chapter, permanent bonding using epoxy resin and flip-chip alignment/assembly were necessary to secure and position the e-microplate. Thus, we demonstrate: 1) self-alignment of the BIM to the underlying test die, which removes the need for an alignment/assembly placement tool, and corresponding alignment data, 2) an attachable/detachable clamp-socket based structure that compresses the BIM so that electrical connections are formed and maintained, and 3) temporary electrical connections between the BIM and the test die via mechanically flexible interconnects (MFIs) and corresponding four-point resistance data.

3.2 Literature Review of Other Similar Interface Bio-Systems

Some commercial vendors selling Multi Channel Systems MCS GmbH recommends several commonly used sterilization techniques (employed after cleaning steps to remove organic matter and/or coatings) for their MEAs, including sterilization with ethanol and ultraviolet (UV) light, autoclavation, dry-heat sterilization, and sterilization with hot water [83]. In general, to reuse MEAs that currently have cultures, the organic matter present must be removed after which the MEA must be sterilized. Hales [84] recommends incubating 300-400 µl of 0.25% trypsin in phosphate-buffered saline (PBS) on the MEA at 35 - 37°C for 20 min. The MEA is then rinsed with DI water and then inspected with a light microscope. If cellular matter remains, then the trypsin step is repeated until clean. If the MEAs are clean, then they are rinsed with DI water and then allowed to soak in 70% ethanol for 15 minutes. These MEAs are then placed in a laminar flow hood with the UV light on overnight.



(a) (b)

Figure 42. Comparison between (a) passive-electronic biosensor and (b) active-electronic biosensor. (Reproduced here from Table 11 for convenience purposes) [94].

Other solutions include manufacturing a disposable substrate that is discarded after a single use (or possibly multiple uses). These solutions separate the sensing component of the biosensor from the active electronics of the biosensor (this hybrid system is sometimes referred to as a passive-electronic biosensor as shown in Figure 42) [93], [94]. Active-electronic biosensors, on the other hand, comprise a sensing site that is monolithically integrated with the rest of the CMOS chip. A comparison of both passive- and active-electronic biosensors is shown in Table 10 [160].

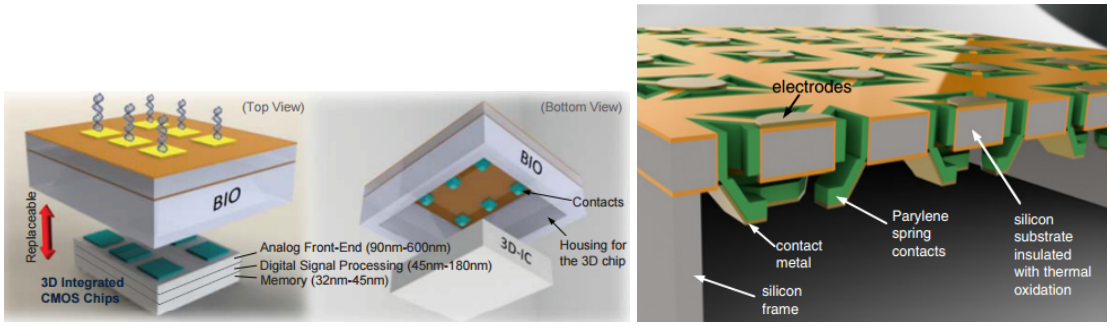
Table 10. Comparison table of passive-electronic biosensors and active-electronic biosensors (adapted from [160])

	Passive-Electronic Biosensor	**Active-Eletronic Biosensor**
Pixel array density	Low	**Medium - High**
Cost per chip	**Low**	High
Electrical performance (signal integrity)	Medium	**High**
Disposablity	**Practical**	Less practical

Guiduicci [161] and Temiz [94], [162] sought to combine the best of both passive- and active-electronic biosensors via developing a 3D integrated sensing-site that sits atop the CMOS biosensor, hence creating a bio-system capable of high resolution, where the passive sensing module is practically disposable/replaceable, which allows for the retaining of the CMOS chip, as shown in Figure 43. Although an intriguing concept, the off-chip interconnections used in Guiducci's biosensor system came with many microfabrication challenges [160]. Additionally, said interconnects are rigid, which can create functional and reliability issues (e.g., some connections open, erosion on biosensor pads, etc.). Temiz attempted to fabricate more compliant-based interconnections; however, these interconnects were not properly electrically (or mechanically) characterized. A contact resistance ranging from 500 Ω to 1 kΩ is measured, but this resistance measurement is dependent upon the degree of contact between the interconnect and the probe tip [160]. Not enough details are provided to determine whether or not this degree of contact is representative of the typical contact between interconnect and corresponding biosensor mating pad in an application setting. Additionally, as the probe tip is pushed against the interconnect, said interconnect is said to break, which brings into question the mechanical reliability of these interconnects [160]. As no mechanical compliance data (or other

mechanical data) is provided, it is difficult to know whether or not these interconnects can operate reliably. Furthermore, the fabrication steps for these interconnects used by Temiz also appear very involved. Additionally, it does not appear that this biosensor system as a whole was ever tested, not even in a mock setup type manner.

In the aforementioned cases involving the 3D integrated sensing-site component of the biosensor, the off-chip (or 3D) interconnection technology appears to be the main challenge. Compliant interconnects, in general, however still appear to present a viable solution to overcoming the aforementioned challenges, specifically due to their mechanical properties and their capability to temporarily mate with their respective contact pads. Given the proper compliant interconnect technology and perhaps a proper compliant interconnect design, the aforementioned challenges may possibly be addressed.



(a) (b)

Figure 43. 3D integrated biosensor with (a) rigid interconnects and (b) compliant interconnects [94].

3.3 System Overview

As seen in Figure 40, the modular system is composed of: a carrier, a test die (or biosensor), the BIM, the clamped socket, and a PCB. The carrier contains self-alignment KOH-etched pits to self-align both the test die (via positive self-alignment structures or

PSAS) and the BIM (via sapphire precision balls) [128], [163]. The BIM hence self-aligns to the test die via the carrier. The test die is also wire bonded to the carrier, which itself is wire bonded to the PCB for four-point resistance measurements (reported in Section 3.8.3). After the BIM is self-aligned to the carrier and hence the test die, the clamp is inserted into its socket so that the BIM can electrically interconnect to the underlying test die electrodes via 58 μm pitch MFIs (a BIM contains two arrays of 1,024 MFIs for a total of 2,048 MFIs) [115], [143], [147].

3.4 System Design and Considerations

3.4.1 MFI Compliance Considerations

As aforementioned, the BIM contains two arrays of 1,024 MFIs at a pitch of 58 μm. Due to this relatively large number of MFIs and tight pitch (a tighter pitch implies, in general, a more stiff MFI as seen in Figure 44), a relatively large force is needed to exert the necessary pressure on the MFIs to create and maintain sufficient electrical contacts and to attain the alignment created by the self-alignment mechanisms. This large force can potentially create several challenges: 1) A stiff MFI, in general, can potentially delaminate during the assembly process, 2) Stiff MFIs, in general, may limit the targeted depth of deformation, which itself creates challenges in regard to deformation depth tolerance, and 3) A large set of MFIs (especially if these MFIs are stiff) can potentially induce significant stress into the underlying substrate (and possibly lead to fracture) during the assembly process.

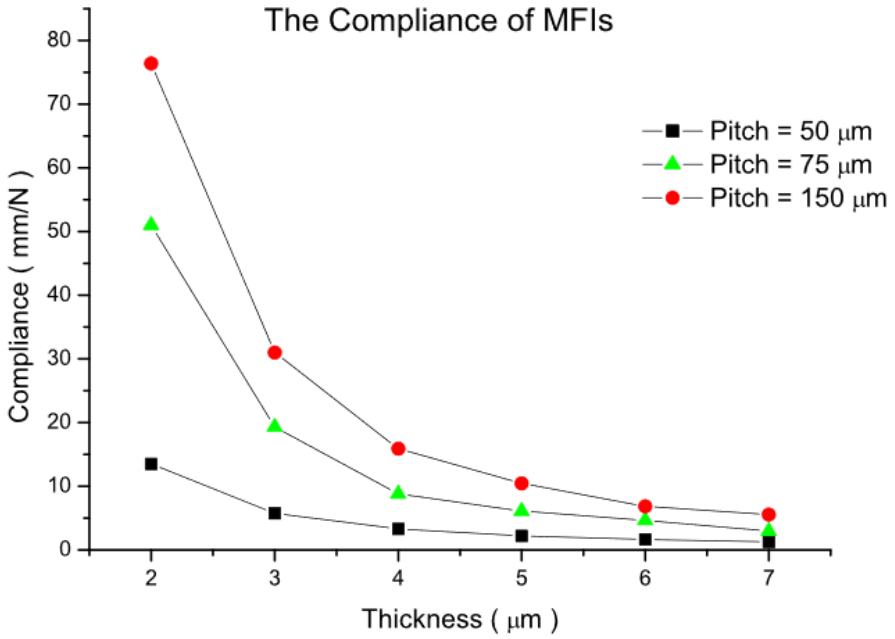


Figure 44. Compliance of the MFIs as a function of thickness and pitch. Smaller pitches shift the compliance curves downwards [164].

Therefore, in an attempt to decrease the assembly force needed for the BIM system, the MFI arrays were designed to increase the overall compliance of the MFIs. Specifically, the MFIs themselves were not only subject to an optimal design for compliance purposes (optimization process employed follows design methodology detailed in CHAPTER 2), but the MFI array was configured in such a manner to further increase MFI compliance. Conventionally, an MFI array is designed as seen in Figure 45, where each MFI has its own reflowed dome (these reflowed domes are thermally-reflowed positive resist, which will be discussed in detail in Section 3.5). These MFIs also have "outward" anchors, which attach to the substrate. To meet the pitch constraints, the dome width plus MFI anchor length cannot be larger than the pitch. In this case, the maximum dome width plus anchor length combination is less than the MFI pitch of 58 μm. Additionally, the height of the dome is related to the width of the dome (i.e., this height can only be so large for a given

width). Approximately, the dome height cannot exceed half the width of the dome. A taller (or longer) MFI however is, on average, more compliant due to a larger torque (assuming other geometrical variables remain the same including MFI thickness, etc.).

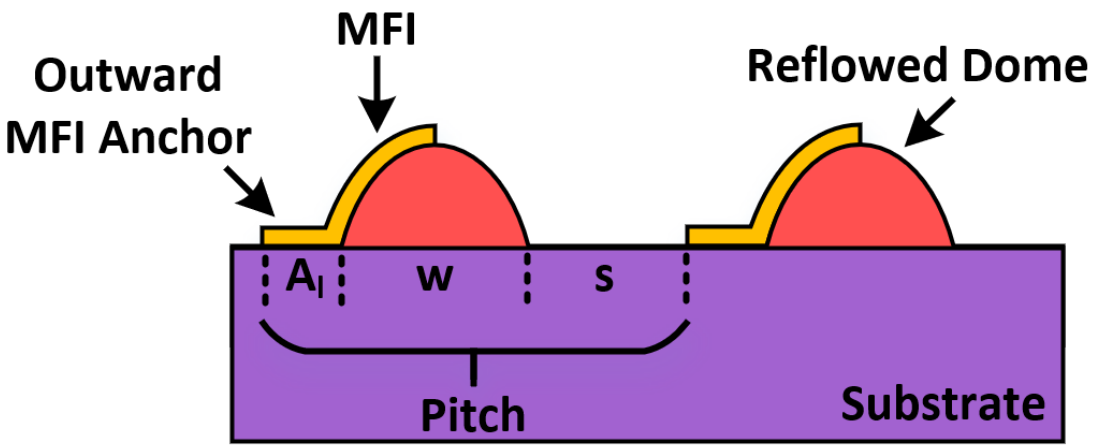


Figure 45. Conventional MFI array configuration where each MFI 1) has its own reflowed dome and 2) has an outward anchor. The pitch is equal to the length of the outward anchor (A_l), the width of the reflowed dome (w), and the space between the reflowed dome and the edge of the MFI anchor (s). Note that the dome with is smaller than the pitch. Also, note that the domes are removed upon finalization of the fabrication process.

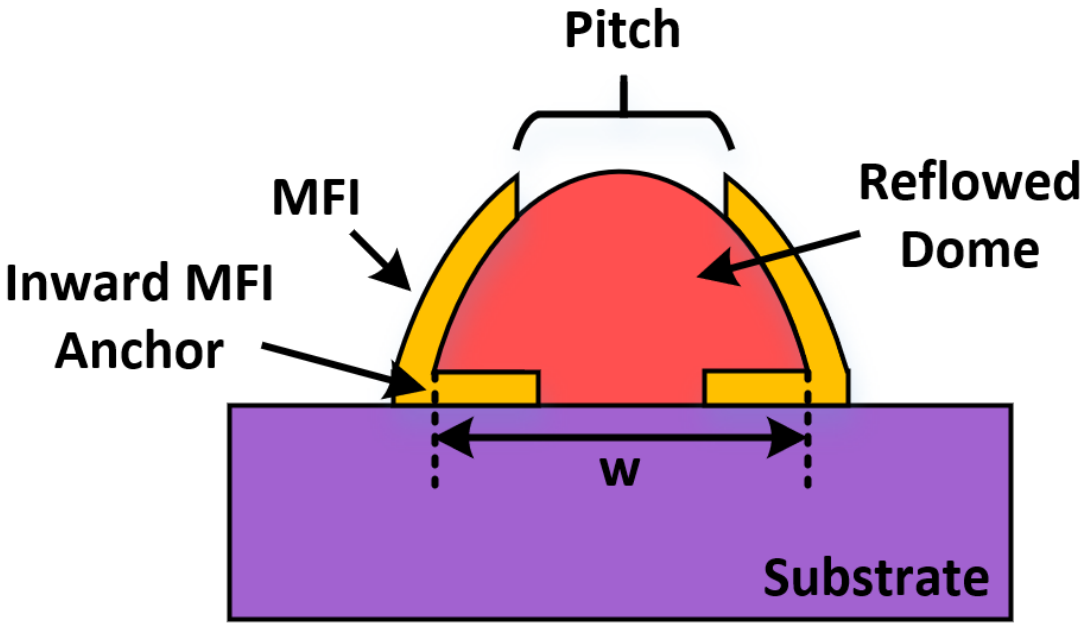
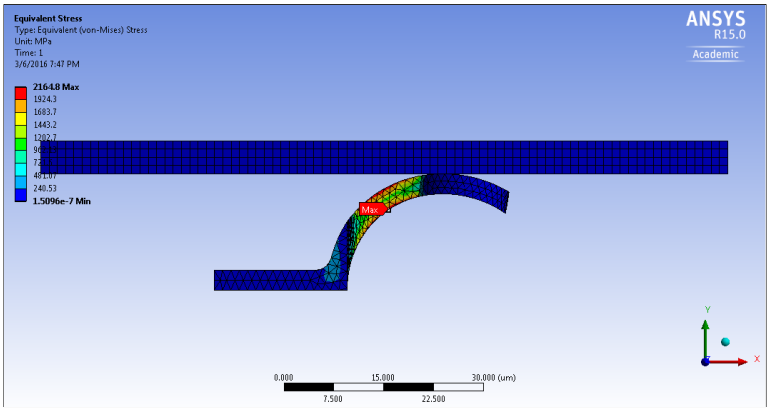


Figure 46. New MFI array configuration design where two MFIs share a larger reflowed dome and each MFI has an inward anchor. The combination of the larger dome and the inward anchor serve to increase the width and hence the height of the dome, which in turn increases the height of the MFI (and the corresponding compliance of the MFI). Note that, in this case, the width of the dome (w) is larger than the MFI pitch. Also, note that the dome is removed upon finalization of the fabrication process.

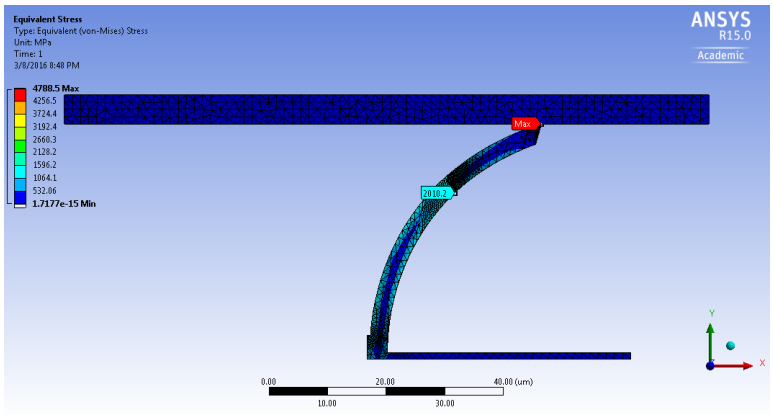
Conventional MFI



<u>Compliance:</u> 0.5707 mm/N
<u>Total Assembly Force:</u> 17.94 N

(a)

More Compliant MFI



<u>Compliance:</u> 1.914 mm/N
<u>Total Assembly Force:</u> 5.35 N

(b)

Figure 47. ANSYS Workbench simulations demonstrating the MFI compliance and the corresponding total assembly force needed for the BIM system for (a) the conventional MFI array and the (b) new and more compliant MFI array. The total assembly force is needed to deflect 2,048 MFIs (two arrays of 1,024 MFIs) by a depth of 5 μm each.

Therefore, to increase the MFI compliance, the MFI height was increased via 1) replacing two smaller domes (having one MFI each) by one larger dome (having two MFIs, one on each side of the dome) and 2) replacing the conventional "outward" MFI anchor by an "inward" MFI anchor (and hence allowing a wider and taller dome). Hence, the maximum width of the larger dome is approximately twice the maximum width of the smaller dome and hence the maximum height of the MFI is about twice as high as the previous MFI from the conventional array configuration. Figure 46 illustrates this new array design concept.

Figure 47 demonstrates the simulated differences in MFI compliance and the total needed system assembly force (for the 2,048 MFI system) between the traditional MFI array configuration and the more-compliant MFI array configuration. As is demonstrated by these simulations, the total assembly force needed to deflect 2,048 MFIs (two arrays of 1,024 MFIs) by a depth of 5 μm is reduced by approximately 3.4x with the new MFI array configuration relative to the conventional MFI array configuration.

3.4.2 Self-Alignment Design and Self-Alignment Fabrication Considerations

3.4.2.1 Precision Ball Size Limits for a Given Pit Width

As aforementioned in Section 3.3, part of the self-alignment mechanism involves using KOH-etched pits (etched into (100) Si). Precision balls (precision sapphire balls in this case) are coupled with the KOH-etched pits to align the BIM to the carrier. These precision balls fit into the KOH-etched pits, hence providing the targeted self-alignment. However, to achieve a proper fit, the precision balls cannot be too large as seen in Figure 48 (precision balls can more easily be moved out of the pits as they don't securely fit inside the pits but instead are almost "on top" of the pits)

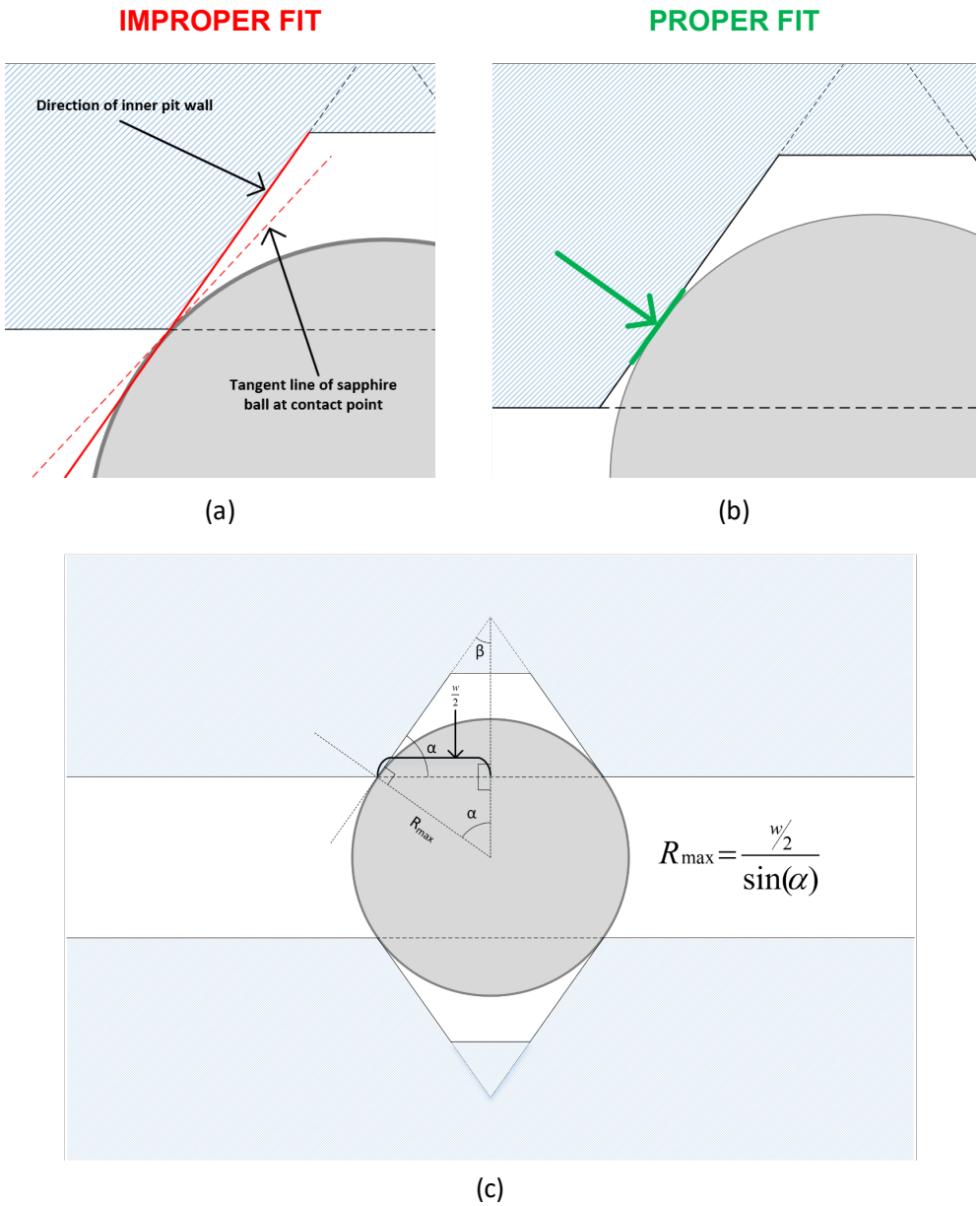


Figure 48. Precision balls that are too large relative to their mating pits can more easily move out of these pits (during assembly, during movement of the system, etc.). Such "too large" precision balls "improperly" fit into the pits. This "improper fit" is (a) defined as a non-coincident intersection between the tangent line of the sapphire precision ball at the contact point of the pits and the tangent line of the inner pit wall. A "proper fit" is (b) defined as the coincident overlap between these two aforementioned tangent lines. The precision balls fit more securely when they "properly" fit into the pit. Therefore, (c) in order for a proper fit to be attained, a maximum radius limit for the precision ball is defined.

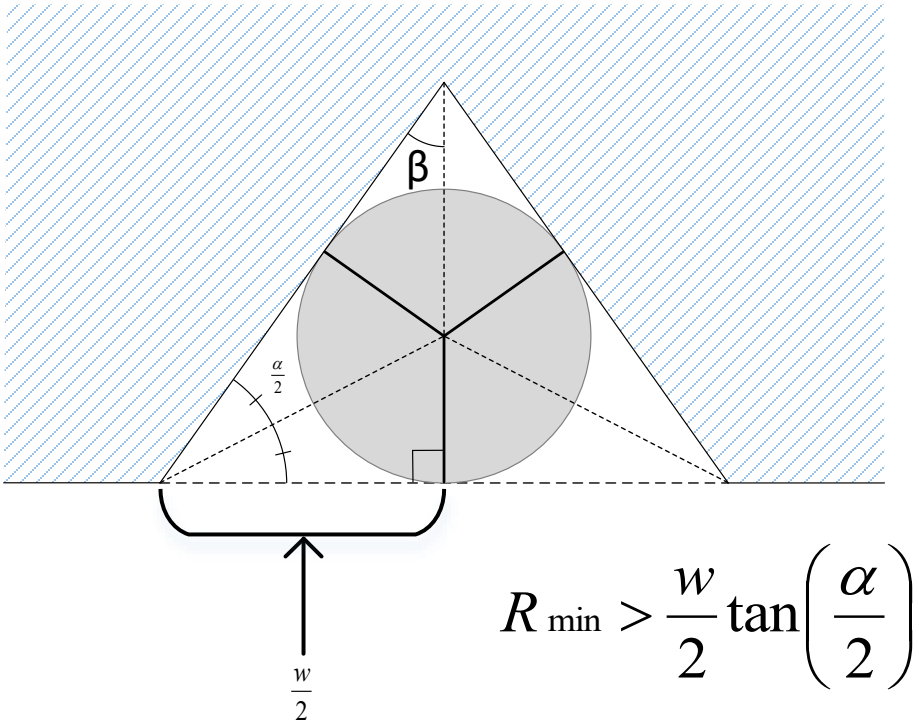


Figure 49. Too small a precision ball cannot serve its self-alignment function. Hence, a minimum radius limit for the precision ball is defined.

or too small as seen in Figure 49 (precision balls fit completely inside the pits and therefore do not act to self-align the interfacing substrates). Therefore, boundary conditions are set to ensure that the precision balls fit properly into the corresponding pits while enabling self-alignment between the interfacing substrates. The maximum radius (R_{max}) of the precision ball for a pit of width, w, is:

$$R_{max} = \frac{w/2}{\sin(\alpha)} \tag{2}$$

Where

w = the pit opening width,

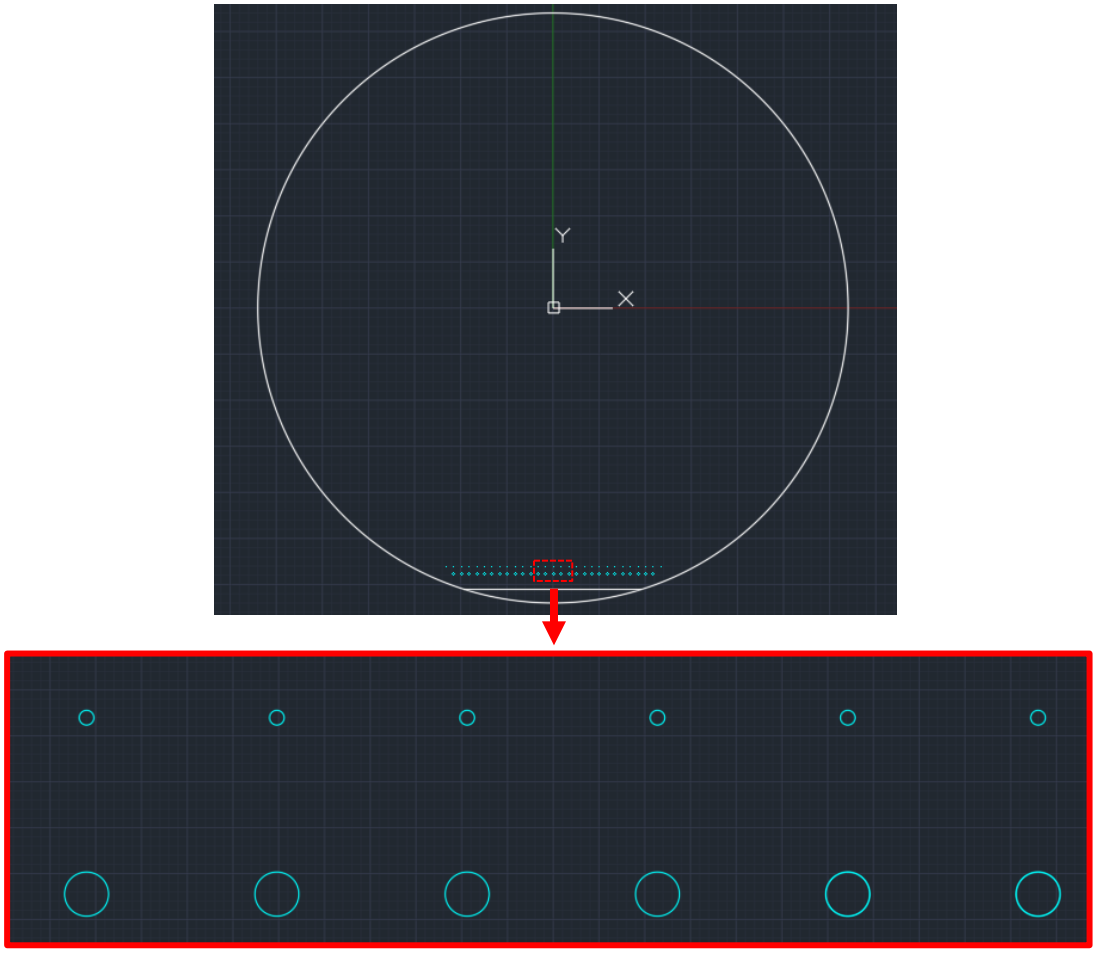


Figure 50. “Pre-etch” pattern used to expose the (110) crystal plane during a KOH etch. The subsequent KOH etched pattern is aligned against this exposed (110) to minimize undercut.

α = angle at which the (100) Si plane is etched relative to the (111) plane by KOH (≈ 54.74°)

The minimum radius of the precision balls for a pit of width, w, is:

$$R_{min} > \frac{w}{2}\tan\left(\frac{\alpha}{2}\right) \tag{3}$$

The geometric representation of these variables are demonstrated in Figure 48(c) and Figure 49. Note that this analysis assume that the pit is deep enough (the pitch has been KOH etched long enough).

3.4.2.2 Engineering of the Gap Between Interfacing Substrates

Depending on the size of the pit and the precision balls (or PSAS), a certain gap is formed between the interfacing substrates. Moreover, the pits must also be etched long enough (to be deep enough) so that the corresponding precision ball (or PSAS) can fit (i.e., precision ball or PSAS should not touch the bottom of the pit). An engineered gap analysis for PSAS to pits is provided in [128]. A similar analysis is performed for the case of precision balls to pits.

The outcome of these analyses for gap engineering was written into a variety of MATLAB programs as seen in Appendix A.1. Appendix A.1 shows a list of these programs, which are briefly discussed here:

1. *full_sphere_w* – For a given precision ball radius and for a targeted gap, this program returns the needed opening pit width, whether or not the size of the precision ball will provide a "proper" fit as defined in Section 3.4.2.1, and the minimum etch depth needed for the pit. It also provides how deep the pits can etch (assuming we let the pits etch until the (111) planes converge into a vertex) and the opening width on the back side of the Si substrate in the event where the pits etch all the way through the substrate.
2. *full_sphere_rad* – For a given pit width and for a targeted gap, this program returns the need precision ball radius, a "proper" fit evaluation, and the minimum etch

depth for the pit. Pit depth (when pit vertex is formed) and backside opening width (if pit etches through substrates) is also provided.

3. *full_sphere_gap* – For a given pit width and a given precision ball radius, this program returns the gap between the interfacing substrates.
4. *trunc_half_sphere_w* – For a given PSAS radius (and the degree to which this PSAS is truncated relative to a perfect half-sphere) and for a targeted gap, the program returns the same parameters as in *full_sphere_w* minus the backside opening width (as the PSAS pits were smaller than the precision ball pits and never etched all the way through the substrate).
5. *trunc_half_sphere_rad* – For a given pit width, a given amount of PSAS truncation relative to a perfect half-sphere, and a targeted gap, this program returns the same parameters as in *full_sphere_rad* minus the backside opening width.
6. *trunc_half_sphere_trunc2* – For a given pit width, a given PSAS width (not radius), and a targeted gap, this program returns the radius of the PSAS, the maximum achievable gap (equal to the gap achieved by a non-truncated PSAS), and the required height of the PSAS.

Note that for the PSAS gap design, the program *trunc_half_sphere_trunc2* is likely more useful than the other PSAS gap design programs as it relates to actual fabrication parameters (e.g., PSAS width, PSAS height) as opposed to the PSAS radius which is an indirect parameter in the case of a truncated PSAS. A truncated PSAS is essentially a truncated half-sphere so the radius of this half-sphere is not as useful a parameter as is the chord of this truncated half-sphere (PSAS width) or the height of the arced portion (PSAS height).

3.4.2.3 Minimizing Pit Undercut During KOH Etching in Si Sample

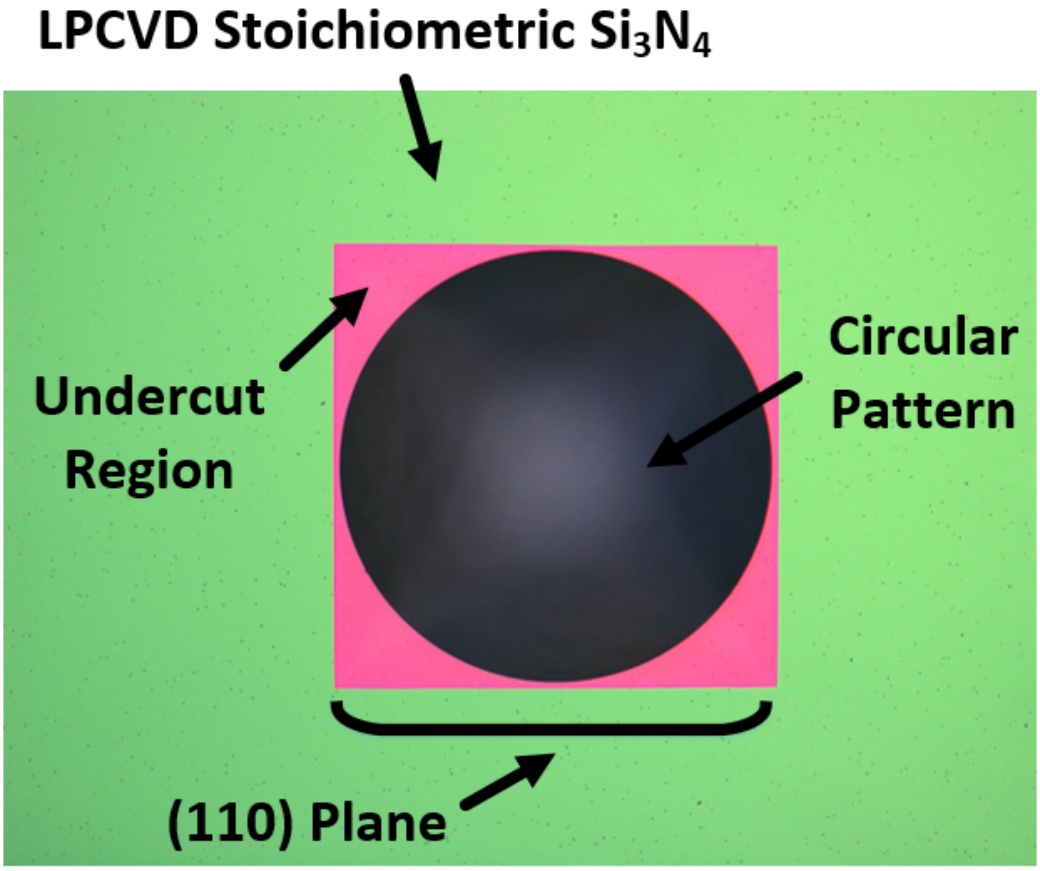


Figure 51. Microscope image of (110) plane exposed after KOH etching of "pre-etch" circular patterns. Note that, in reality, the labeled (110) plane is not the same plane but instead a set of parallel (110) planes. For subsequent alignment purposes to the (110) plane, the corners of this labeled (110) plane is used for alignment.

To minimize pit undercut during KOH etching, misorientation of the pits relative to the (110) crystal plane is minimized via first performing a "pre-etch" step that exposes the (110) crystal plane. This (110) crystal plane exposure is performed via patterning a set of circles near the primary flat of the (100) Si wafer as seen in Figure 50. Upon KOH etching of this pattern, the (110) crystal plane is revealed via each of these patterned circles as seen in Figure 51. In reality, what is revealed is a set of parallel (110) crystal planes as the

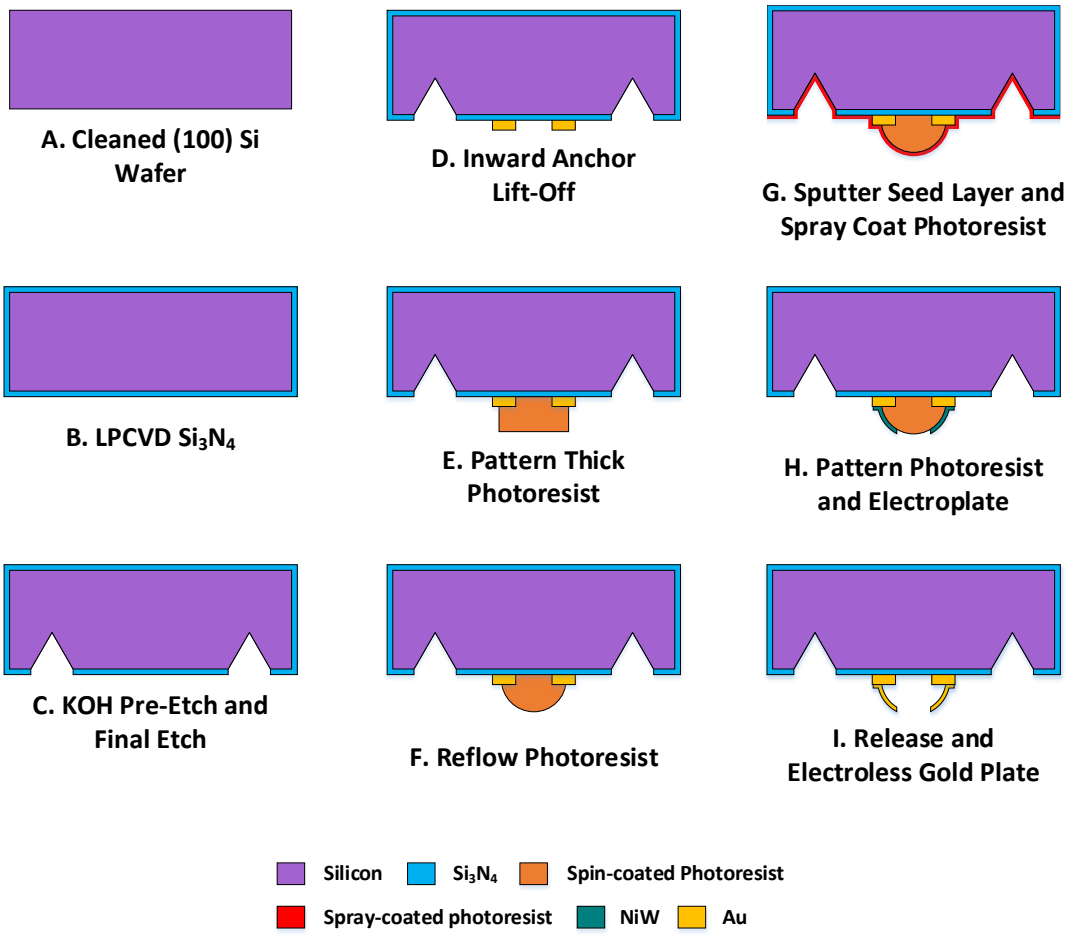


Figure 52. Fabrication process flow for the bio-sensing interface module (BIM).

corners of the "square" undercut are slightly behind (in regards to etching time) relative to the center of the edges of this "square" undercut. Therefore, for subsequent alignment purposes to the (110) plane (for patterns that will be KOH-etched), the corners of the bottom side (or top side) of the "square" undercut are used for alignment.

3.5 Fabrication Process Flows

Three different die were fabricated for the overall BIM system: 1) the BIM itself, 2) the carrier, and 3) the test die (which represents the biosensor). The process flows for each die will be described below.

3.5.1 BIM Fabrication Process Flow

Figure 52 illustrates the fabrication process flow for the BIM. The BIM 500 μm thick Si (100) wafers begin with a piranha bath (3 parts H_2SO_4 to 1 part H_2O_2) for 20 minutes at 120°C. The wafers are then transferred to a dump rinser for 3 cycles. A spin rinse dryer is then used to dry the wafers. The wafers are then placed inside an LPCVD furnace for stoichiometric Si_3N_4 deposition. Approximately 125 nm of Si_3N_4 is deposited (film thickness is measured via a spectroscopic reflectometer). This LPCVD Si_3N_4 film is used as a mask during the KOH etching process.

The Si_3N_4-coated wafers are then prepared for spin coating via first performing an acetone, methanol, and isopropanol (AMI) clean process. A dehydration bake follows. NR5-8000 is spin coated and then patterned using the "pre-etch" mask. The exposed Si_3N_4 (not covered by the resist mask) is etched away using a reactive ion etching (RIE) process. The resist is then subsequently removed and is now ready for KOH etching.

The wafers are placed into a 45% KOH bath at 70°C for approximately 5 hours. Recall that the purpose of the "pre-etch" step is to reveal the (110) plane. Therefore, we examine whether or not there is sufficient undercut as seen in Figure 51 before proceeding to the next step. If not, more time is added to the KOH etching process.

Once this step is completed, the wafers are prepared for the next lithography step. Care is taken so not to damage the Si_3N_4 overhang in the undercut region (as it is easier to see the (110) plane with the overhang intact). The wafer undergoes another AMI clean and dehydration bake. NR5-8000 is spin coated and patterned (using the "real" etch pattern). RIE removes the exposed Si_3N_4. The resist is then removed. The wafers are then placed into a 45% KOH bath at 90°C for approximately 2.5 hours, which results in a depth of approximately 300 μm (which are to carry the precision balls).

After the KOH etching is completed, the wafers undergo another AMI clean. NR9-1500PY is spin coated and patterned. A slight over-development is performed (≈25% longer than standard) to achieve undercut for lift-off purposes. Prior to metallization, a 30 second descum is performed using an RIE process. E-beam evaporation is then used to deposit a 20 nm Ti adhesion layer, a 300 nm Cu layer, and a 100 nm Au layer. The sample is then placed into an acetone bath overnight for lift-off.

After cleaning, a thick photoresist (AZ40XT) is spin coated and patterned. This photoresist is then reflowed on a hot plate at a temperature above its glass transition temperature (T_g) similar to what has been performed in [128]. Several experiments were run for reflowing this photoresist at temperatures ranging from 120°C to 138°C for reflow times ranging from 30 seconds to 20 minutes. Too low/short a temperature/time recipe results in a non-sufficiently reflowed photoresist as seen in Figure 53 whereas too high/long a temperature/time recipe results in a photoresist that expanded too much (hence covering most of the inward anchors) as seen in Figure 54 or results in partial delamination at the edges of the photoresist. Without addressing these challenges (non-sufficient reflow, excessive reflow, or resist edge partial delamination), shorting will occur between the

MFIs. These challenges will be described in more details in Section 3.6.1. The optimal temperature and reflow time were determined to be 133°C for 45 seconds as seen in Figure 55.

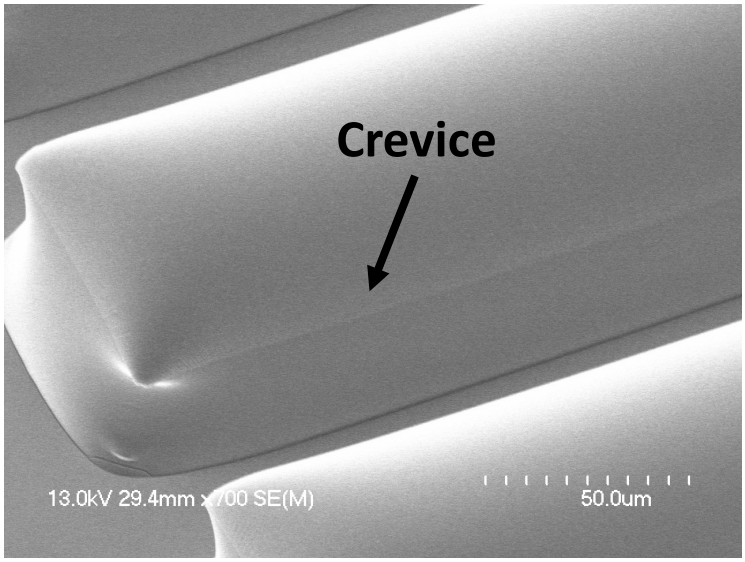


Figure 53. SEM image of an insufficiently reflowed photoresist dome demonstrating the presence of a crevice, which later creates challenges during the electroplating process. Reflow recipe used here is 120°C for 30 seconds.

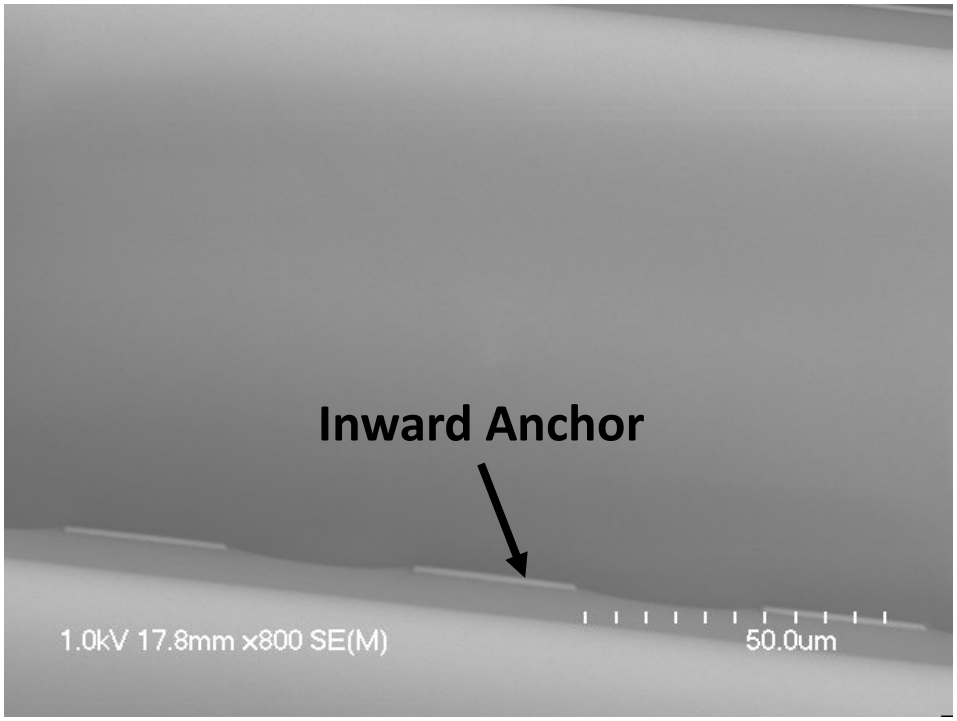
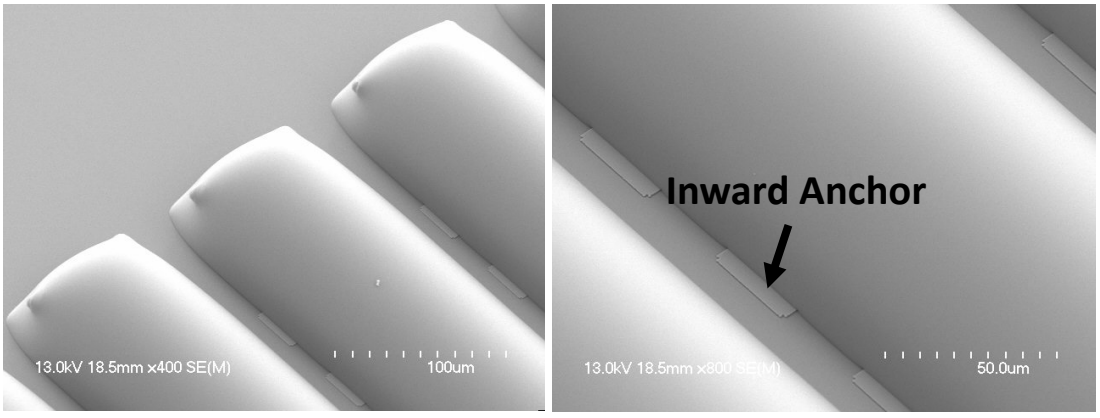


Figure 54. SEM image of an excessively reflowed photoresist dome, where it has expanded to the point of almost completely covering the inward anchors. Reflow recipe used here is 138°C for 1 min.



(a) (b)

Figure 55. SEM image (a) 400x and (b) 800x of the reflowed photoresist dome after using the optimally-developed reflow recipe of 133°C for 45 seconds. No crevice is seen.

After the photoresist domes have been reflowed, the electroplating seed layer must be deposited. A 15 second descum process is initially performed. 20 nm Ti/300 nm Cu/20 nm Ti is then sputtered onto the domes. The top Ti layer is deposited to act as a lift-off layer to remove resist residue after development of the patterned MFI resist mold prior to electroplating (this step will be discussed in more detail shortly).

Approximately 10 μm of AZ4620 is then spray coated onto the seed film-covered domes. The MFI mask is then patterned onto these domes. After the development process, some resist residue often remains in the patterned regions. Hence, the top Ti thin film in the patterned regions is removed with BOE in order to remove this resist residue. At this point, the sample is ready for electroplating.

The MFIs were electroplated using a nickel sulfamate bath (Elevate Ni 5910 RTU from Technic). Sodium tungstate dihydrate and citric acid were added to this bath to provide a specific tungsten concentration that ultimately forms a NiW alloy electroplating solution. Approximately 8.9 g of sodium tungstate dihydrate was added to 1 L of the nickel sulfamate solution (i.e., 8.9 g/l). The bath was then heated to approximately 50°C prior to electroplating. The NiW deposition was then performed using pulsed current (PC) plating. The electroplated NiW thickness for the MFIs was measured to be approximately 2.1 μm.

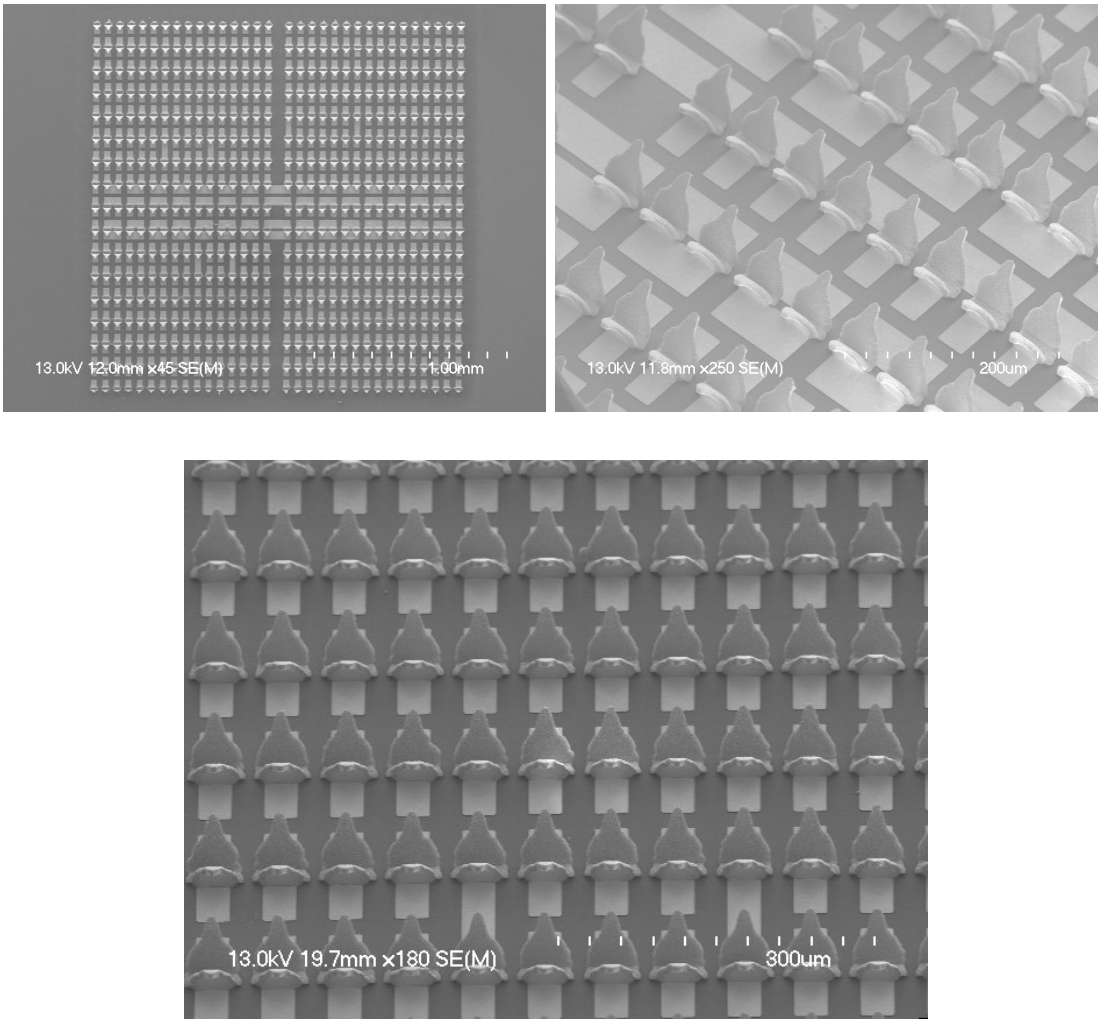


Figure 56. SEM images of microfabricated MFIs on the BIM.

After electroplating, the sample is washed thoroughly with DI water and then dried with a N_2 gun. The spray-coated photoresist (e.g., AZ4620 – a positive resist) is then flood exposed with UV light and then subsequently developed. BOE is then used to remove the top Ti layer. APS is used to remove the Cu layer. Then BOE is used again to remove the bottom Ti layer. At this point in the process flow, an isotropic descum is performed to remove the very top layer of the reflowed photoresist domes. The sample is then subsequently dipped briefly back into BOE to remove any possible Ti that may have

diffused into the top layer of the reflowed photoresist dome. This specific step (e.g., isotropic descum followed by another BOE dip) and the reasons behind it will be discussed in more detail in Section 3.6.2.

The sample is then dipped into acetone to remove the reflowed photoresist dome. A 1-minute descum follows to remove any remaining photoresist residue. Finally, the MFIs are passivated via immersing the sample into an electroless gold plating solution such that all exposed MFI surfaces are coated with gold [115]. The fabricated MFIs are shown in Figure 56.

3.5.2 Carrier Fabrication Process Flow

Figure 57 illustrates the fabrication process flow for the carrier. The process flow for the carrier is identical to the process flow for the BIM up to the lift-off portion of the inward anchors. Therefore, the detailed process flow will not be repeated here. The only additional note here is that there are two sets of pits during the KOH etching process: 1) the larger pits for the precision balls (approximately 300 μm depth in Si) and 2) the smaller pits for PSAS (these pits converge into a vertex at a depth of approximately 220 μm).

For clarity, both the larger and smaller pits are etched simultaneously. The difference in pit sizes is related to the targeted gaps. The larger pit and precision ball dimensions were determined (via methods described in 3.4.2.2) so to target a gap of approximately 345 μm. This gap is targeted since within this gap must exist a 300 μm thick die and 38 μm tall MFIs. The smaller pit and PSAS dimensions were determined so to target a gap of

approximately 20 µm (we had flexibility here regarding what this gap may be). These gaps resulted in the MFIs deflecting to a depth of approximately 13 µm.

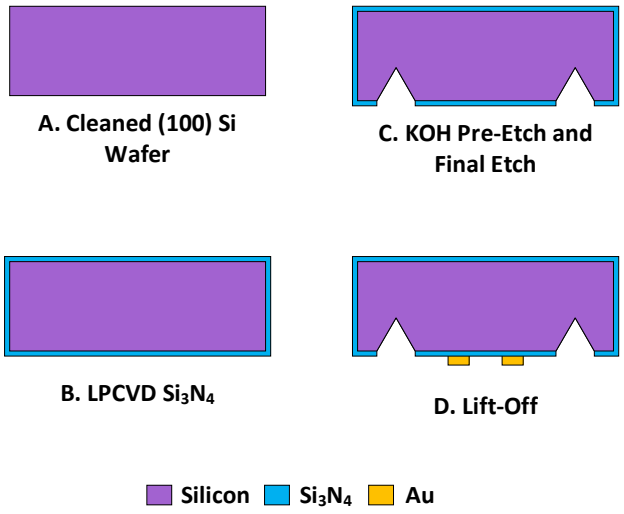


Figure 57. Fabrication process flow for the carrier.

3.5.3 Test Die Fabrication Process Flow

Figure 58 illustrates the fabrication process flow for the test die. LPCVD silicon nitride was used as a passivation layer as the nitride deposition process was done in batch for several wafers (including the wafers for the BIM and the carrier). However, SiO_2 could have been used as well. Back-side alignment was used to align the lift-off patterns on the front side of the wafer to the PSAS patterns on the backside of the wafer. The front-side lift-off patterns contained, in part, Vernier scales to measure the alignment between BIM (which also contained corresponding Vernier scales) and the test die. The backside PSAS is designed to align with the smaller pits of the carrier.

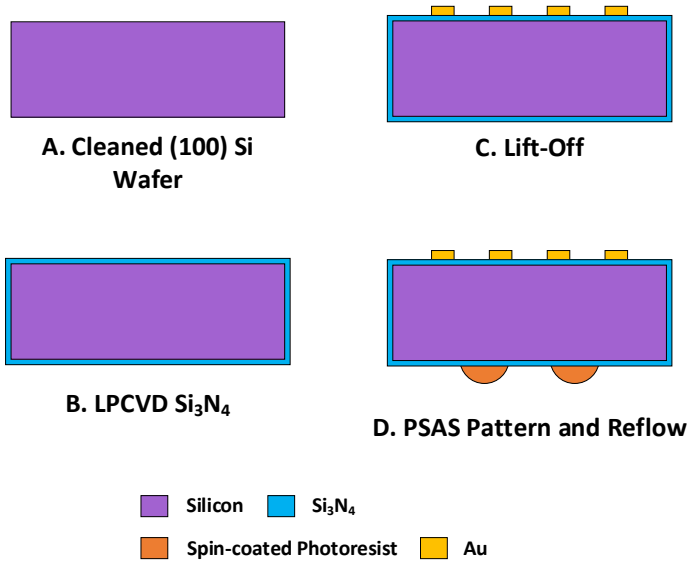


Figure 58. Fabrication process flow for the test die.

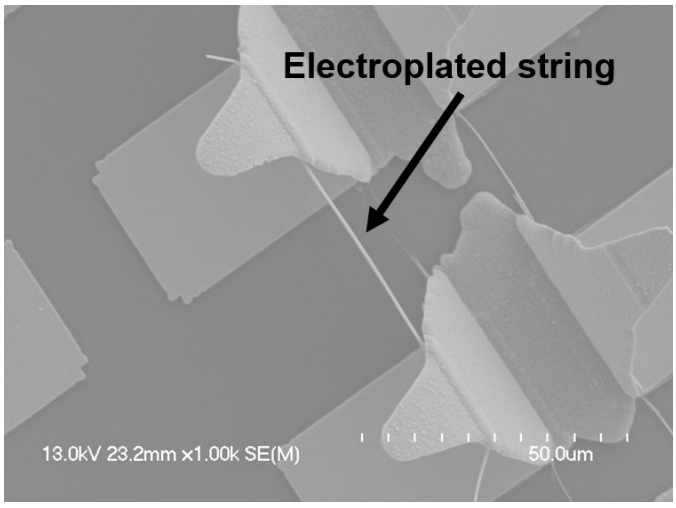
3.6 Fabrication Challenges

Several challenges were confronted during the fabrication process flow for the BIM. These challenges led to MFI shorting and will be discussed in more detail below.

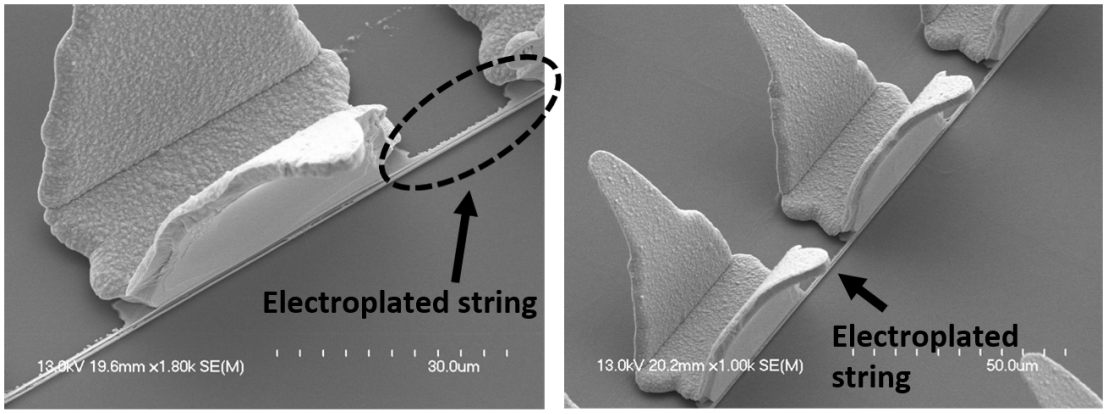
3.6.1 NiW Electroplated Strings

NiW electroplated strings are NiW strings that connect MFIs to one another (hence shorting them) as seen in Figure 59. There are two types of electroplated strings: 1) top electroplated strings and 2) bottom electroplated strings. These strings appear to result from improperly reflowed domes. Top electroplated strings appear when there is a sufficient crevice remaining in the dome after reflow as seen in Figure 53. Bottom strings appear when there exists a gap between the edges of the dome and the substrate as seen in Figure 60. To minimize these "faults" in the dome, reflowing the resist at a single temperature results in less faults relative to a ramped temperature reflow recipe. Additionally, optimizing the

temperature and time of reflow also minimizes these faults as discussed in Section 3.5.1. After said optimizing, these strings are eliminated as demonstrated by the lack of strings (and no shorted connections during four-point measurements, which will be described in Section 3.8.3) in the finalized sample as seen in Figure 56.



(a)



(b)

Figure 59. Electroplated NiW strings that short together adjacent MFIs. Two types of strings exist: a) top electroplated strings and b) bottom electroplated strings.

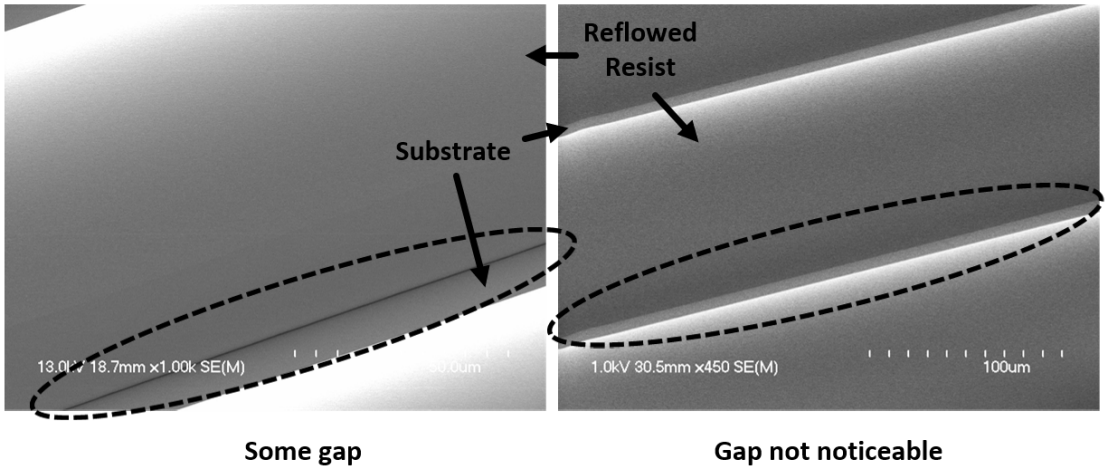


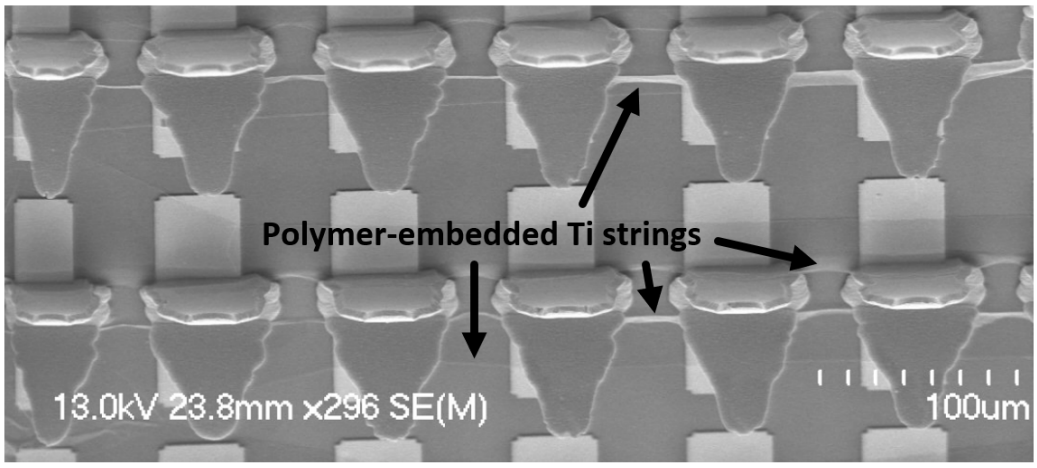
Figure 60. Gap between reflowed resist and substrate contribute to bottom electroplated strings between MFIs.

3.6.2 Polymer-Embedded Ti Strings

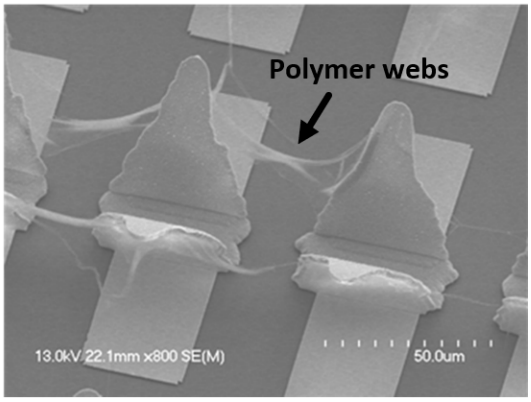
Polymer-embedded Ti strings, as seen in Figure 61, are hypothesized to be strings formed when the bottom layer of Ti partially diffuses into the outermost portion of the reflowed photoresist dome, possibly during the spray coating process as the wafer holder is heated (65°C for approximately 15 minutes) and possibly during the electroplating process due to the heated bath (50°C for approximately 10 minutes). During the releasing process where the bottom layer of Ti is removed via BOE, some of the diffused Ti is masked from the BOE via the outermost portion of the reflowed photoresist dome, hence this portion of the Ti film remains. During the subsequent acetone bath process for removal of the reflowed photoresist domes, the masked Ti remains, surrounded by strands of resist that it attaches to. Unfortunately, these strings short the MFIs (as demonstrated via four-point resistance measurements) and hence must be removed.

This hypothesis was initially formulated after viewing the domes in the SEM after the bottom layer of Ti was removed. Although the domes are a dielectric material (non-conducting), no charge build-up was observed regardless of the amount of time the sample remained in a BOE bath (as a note, too long in the BOE bath would cause delamination of the MFIs). This lack of charge build-up was in contrast to the charge build-up seen in these same domes prior to sputtering. It was at this moment where it was hypothesized that perhaps some of the Ti had diffused partially into the reflowed photoresist domes.

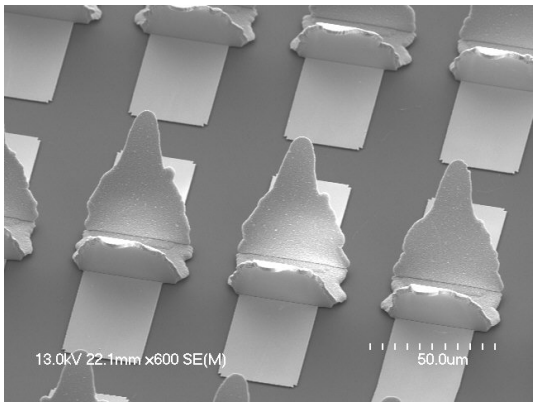
To address this challenge (and as aforementioned during the BIM MFI process flow in Section 3.5.1), after the initial bottom Ti layer removal via BOE, an isotropic descum is performed to remove the outermost portion of the reflowed photoresist dome that masks the diffused Ti. As these domes are non-planar, an isotropic descum process was used as opposed to the more typical anisotropic descum process, which would only remove the top portion of the outermost layer of the reflowed photoresist dome. The YES-R1 Plasma Cleaner in the IEN Marcus Inorganic Cleanroom was used to achieve this higher degree of isotropy. After this isotropic descum process is performed, the sample is dipped back into BOE to remove the remaining Ti. The sample is then placed into an acetone bath to remove the reflowed photoresist domes. At this point, polymer webs remain as seen in Figure 61(b); however, these webs do not short the MFIs. These webs can be removed via a standard anisotropic descum process. This overall solution removes the polymer-embedded Ti strings (and polymer webs) as seen in Figure 56 and as demonstrated via the non-shorted four-point resistance measurements.



(a)



(b)

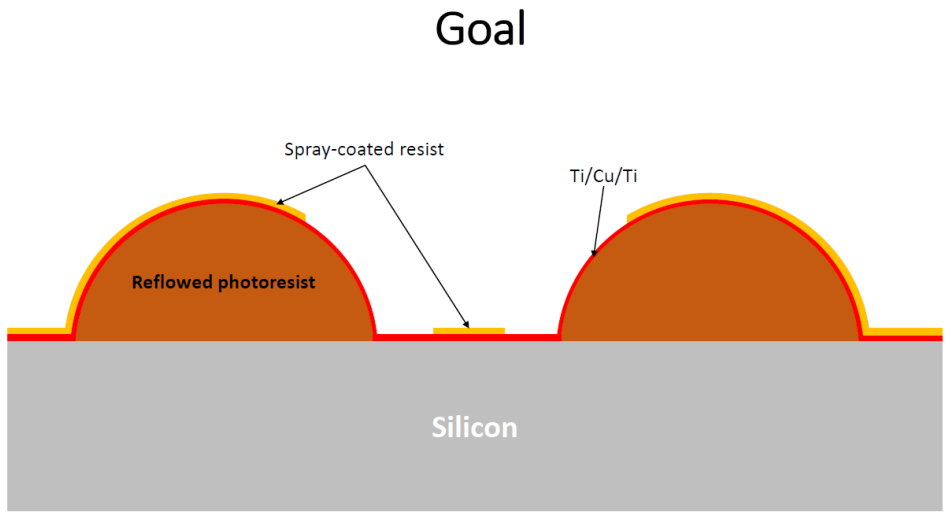


(c)

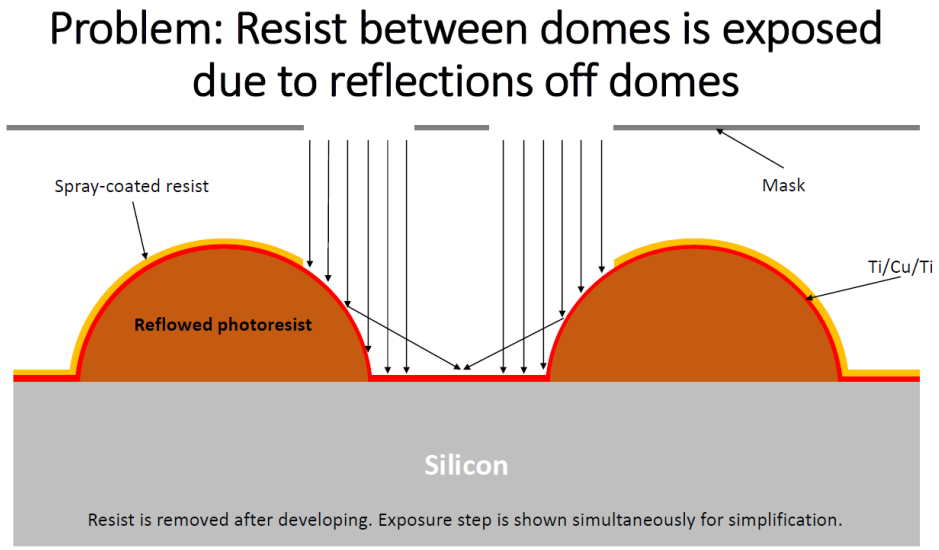
Figure 61. SEM images of (a) MFIs shorted together via polymer-embedded Ti strings. (b) After an isotropic and subsequent BOE process is performed (followed by an acetone bath to remove the domes), these polymer-embedded Ti strings are removed, leaving behind only polymer webs, (c) which are then removed via a standard anisotropic descum (sometimes an isotropic descum here also helps).

3.6.3 Reflection Off Domes During Exposure

Due to the size and the proximity of adjacent domes, reflection off the domes occurs during exposure, which causes UV light to intersect with unintended resist regions as seen in Figure 62. Specifically, the spray-coated resist between back-to-back MFIs is exposed and hence removed during the development process. This resist removal causes these back-to-back MFIs to be shorted via their anchors as seen in Figure 63.



(a)



(b)

Figure 62. (a) The spray-coated resist between the domes should remain after exposure and development. However, (b) due to reflections off the domes, this portion of spray-coated resist is exposed and hence removed during the development process.

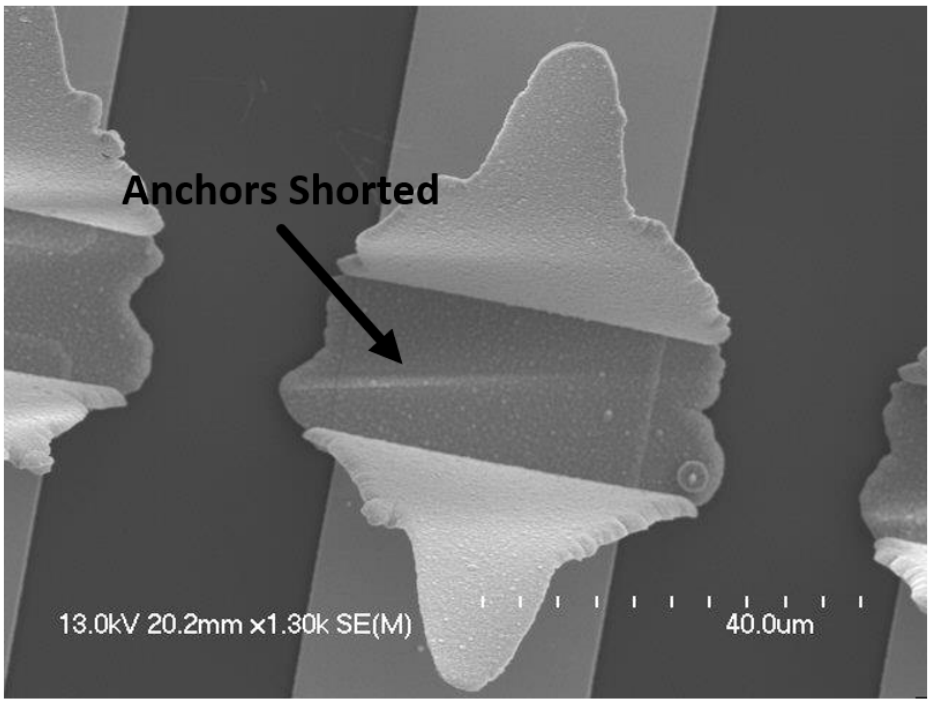


Figure 63. The anchors of back-to-back MFIs are shorted due to the removal of the separating spray coated photoresist as a result of reflection off the domes.

Unfortunately, this issue was not ultimately addressed. The initial solution was to apply a coating of a bottom antireflective coating (BARC) film (AZ Barli II) to the reflowed domes after sputtering and prior to spray coating. The initial spin coating of AZ Barli II did not seem to properly coat the domes and only coated the area between the domes as seen in Figure 64. Therefore, spray-coating of AZ Barli II was attempted; however, the correct diluted recipe (for viscosity purposes) for the AZ Barli II was never achieved. As the back-to-back MFI shorting did not affect the four-point resistance measurements, the addressing of this issue was side-lined by the addressing of the other aforementioned challenges (e.g., strings). Additionally, the MFIs were open to be replaced by other interconnection systems, including anisotropic conductive films such as PariPoser. The use of PariPoser as the interconnection system will be discussed in more detail in CHAPTER 4. Ultimately, future

work will need to address this challenge, which may involve further pursuit of the BARC film or perhaps another MFI array configuration.

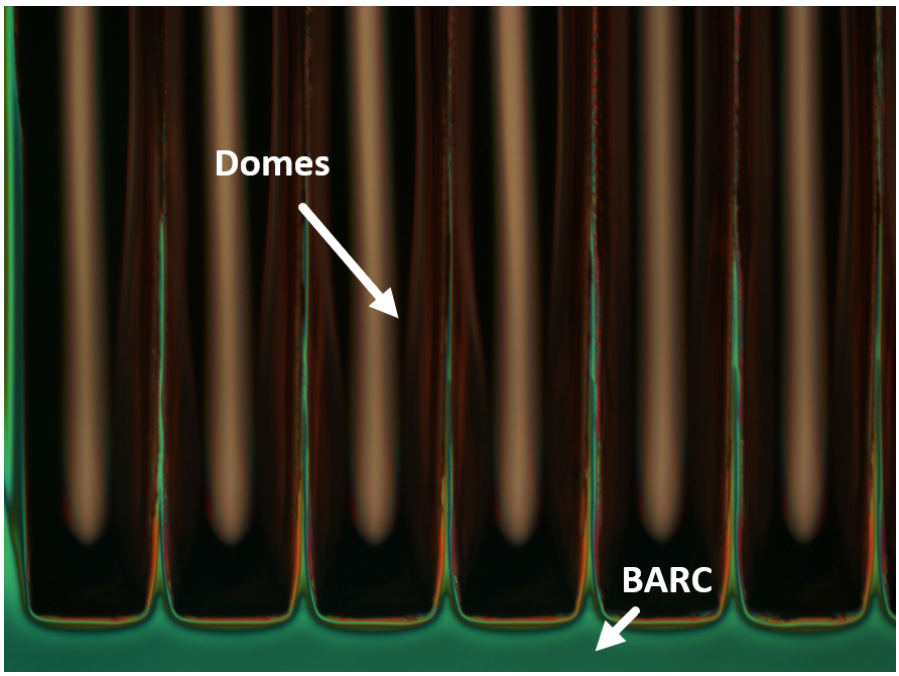


Figure 64. Spin-coating of the bottom anti-reflective coating (BARC) layer only covered the region between the domes and not the domes themselves.

3.7 Other System Components

3.7.1 Clamp-based Socket

The clamp was designed to fit the BIM dimensions and the MFI array dimensions. This clamp was also designed to exert approximately 17N of force via 6 low force springs within the peripheral of the clamp. The clamp final design and manufacturing was performed by Ironwood Electronics, as seen in Figure 65. The blocks in Figure 65 represent the plastic wells that would contain the culture medium and corresponding cells during a bio-sensing experiment.

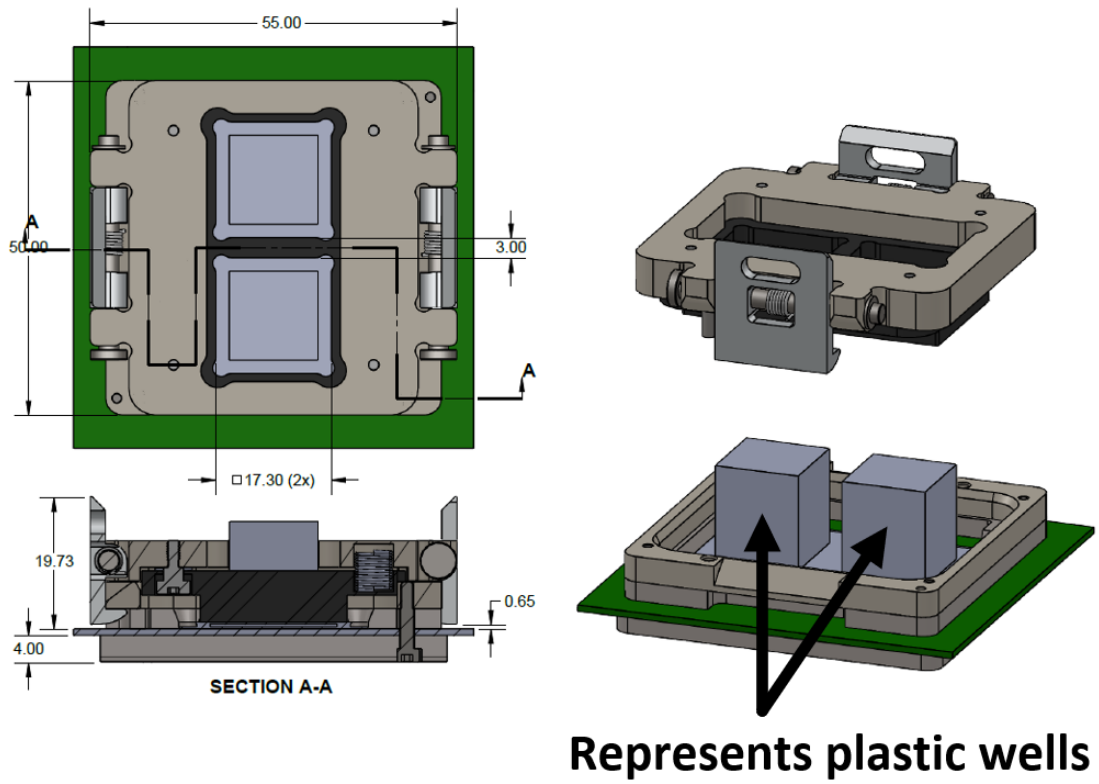


Figure 65. Schematic design of the socket used for the BIM system. Approximately 17N force can be exerted with this clamp via 6 springs (or 11.38N via 4 springs).

3.7.2 PCB Substrate

To obtain accessible test points for four-point resistance measurements of the MFIs, a PCB was designed to simply route the traces on the test die from test die to carrier to PCB. This PCB design is seen in Figure 66. Wire bonds were used to interconnect the test die and carrier in addition to the carrier and PCB.

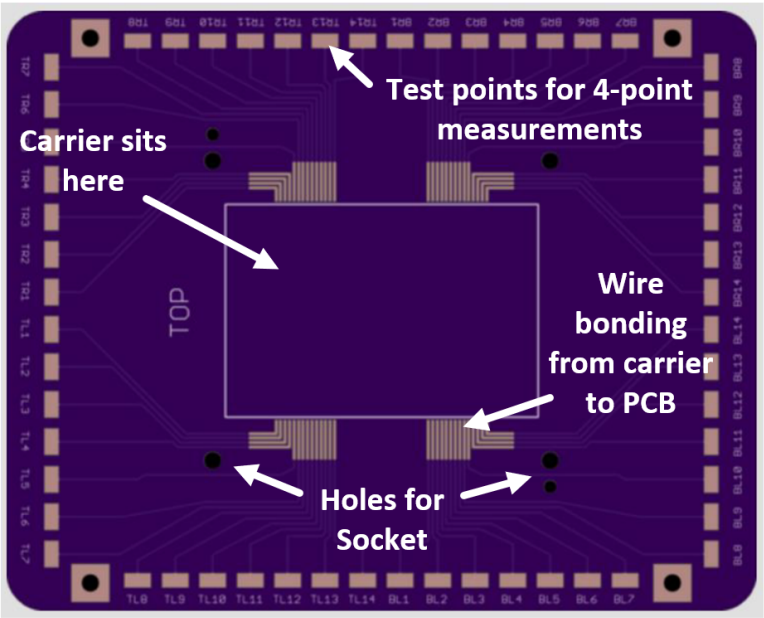


Figure 66. PCB used to access test points for the four-point resistances of the BIM MFIs.

3.8 Setup, Results, and Discussion

3.8.1 Assembly and alignment

To obtain self-alignment between the BIM and the test die, a double self-alignment mechanism was implemented: 1) self-alignment between the BIM and the carrier and 2) self-alignment between the test die and the carrier (both shown in Figure 40). The purpose of the carrier, as aforementioned, is to enable both levels of self-alignment and hence self-alignment between the BIM and the test die. To apply the necessary force onto the BIM so that the MFIs form an electrical connection, the clamp is inserted into the socket.

Different mechanisms, as aforementioned, enable each level of self-alignment as shown in Figure 67: 1) a PSAS-pit mechanism self-aligns the test die to the carrier and 2) a sapphire precision ball-pit mechanism self-aligns the BIM to the carrier. Due to the size of

the pits, the misalignment tolerance during the initial assembly of the BIM is 0.43 mm. The accuracy and repeatability of the self-alignment between BIM and test die is reported in Section 3.8.2.

All assembly and alignment are performed via manual placement. Specifically, the carrier is manually picked up and placed into the socket base, the test die is picked up and placed onto the carrier, the BIM is picked up and placed onto the carrier, and the clamp, as shown in Figure 67(c), is picked up and inserted into the socket base. Self-alignment occurs at every level with high accuracy as shown next in Section 3.8.2.

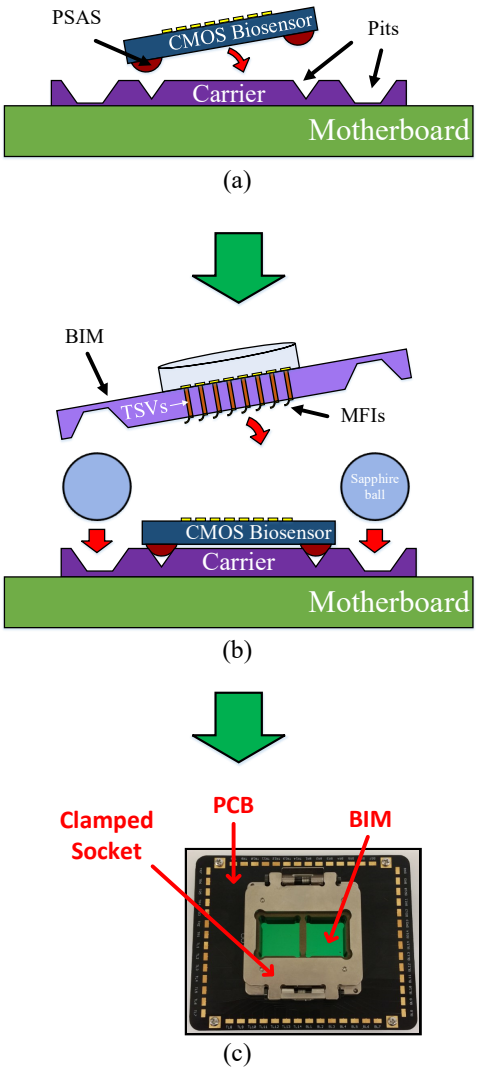


Figure 67. Double self-alignment process flow demonstrating two levels of self-alignment: (a) CMOS biosensor to carrier self-alignment via a PSAS/pit mechanism, (b) BIM to carrier self-alignment via a sapphire ball/pit mechanism. Final clamped state (c) follows.

3.8.2 Alignment measurements and alignment repeatability

To measure the alignment accuracy between the BIM and the test die, X-ray images were first captured using a Dage X-Ray Inspection System (XD7600NT model), as shown in Figure 68. The Dage X-Ray built-in measurement tools are then used to measure the

misalignment from the X-ray images. To calibrate the X-ray tool, several features of known size were initially measured and all other measurements were scaled accordingly.

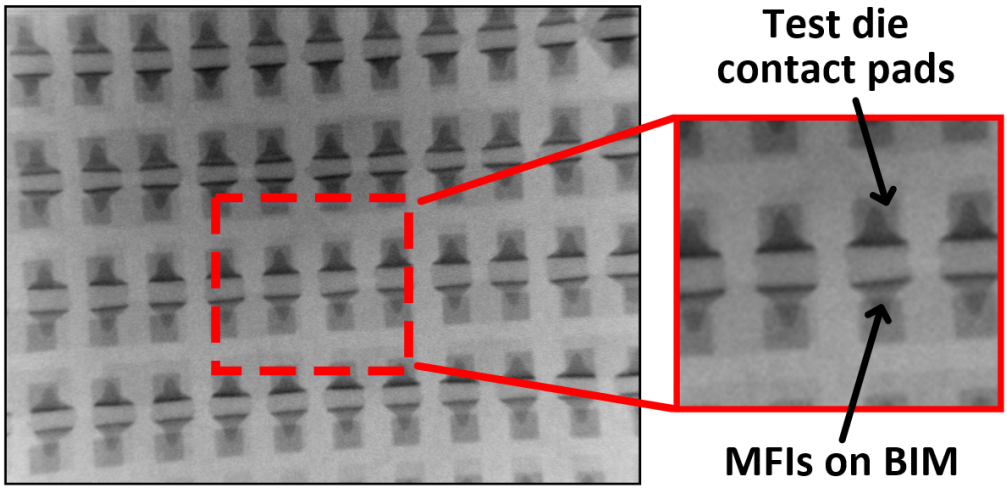


Figure 68. X-ray image showing alignment between MFIs and corresponding electrodes on the test die.

Alignment measurements are performed for each quarter of the MFI area array (e.g., top left, top right, bottom left, and bottom right). For each quarter, the x- and y- misalignment is recorded via measuring the distance (in the x- and y-directions) between the MFIs on the BIM and the electrodes on the test die. Several measurements were performed for each quarter (for both x- and y-) from which the average is computed and recorded, as shown in Table 11. Initial alignment measurements demonstrate less than 5 μm of misalignment for every quarter (and each direction). Recall that the misalignment tolerance for manually placing the BIM onto the carrier is ±0.43 mm (±430 μm).

Table 11. Self-alignment repeatability measurements

Number of manually placed assemblies	Top Left (μm)		Top Right (μm)		Bottom Left (μm)		Bottom Right (μm)	
	x	***y***	***x***	***y***	***x***	***y***	***x***	***y***
1	-3-4	+3	-3-4	+3-4	-4	+3-4	-4	+3-4
10	-3-4	+3	-3-4	+3-4	-4	+3-4	-3-4	+3
20	-3-4	+3	-3	+3-4	-3-4	+3-4	-4	+3-4
50	-3-4	+3-4	-3-4	+3-4	-3-4	+3-4	-3-4	+3-4
100	-3-4	+3-4	-3-4	+3	-3-4	+3-4	-3	+3-4

Since the biosensor is intended for reuse, we performed multiple manually placed assemblies on the test die to test self-alignment repeatability. The results of these tests are also shown in Table 11. As shown, 100 different manually placed assemblies are performed where the BIM is removed and then re-assembled onto the test die (and re-clamped). Little difference is observed between each self-alignment measurement, which demonstrates that self-alignment accuracy is consistent after repeated use. Self-alignment accuracy can be improved with better lithographic equipment and better lithographic alignment.

3.8.3 Electrical data

To test the temporary electrical interconnections after the BIM is self-aligned, assembled, and clamped onto the test die, four-point resistance measurements of 2.1 μm thick MFIs were performed and recorded, as shown in Figure 69 and Figure 70. Figure 70(b) records several individual four-point IV curve measurements from one BIM sample; one is shown in Figure 70(a). As shown, an average of approximately 207.2 mΩ is recorded. Furthermore, the uniformity of this data (standard deviation of ±10.1 mΩ) likely demonstrates that structural uniformity exists among the MFI structures and that a uniform

assembly force is provided by the clamp. Modifying the gap between the BIM and test die (and the assembly force if necessary) will likely alter the contact resistance of the MFIs and hence their overall resistance.

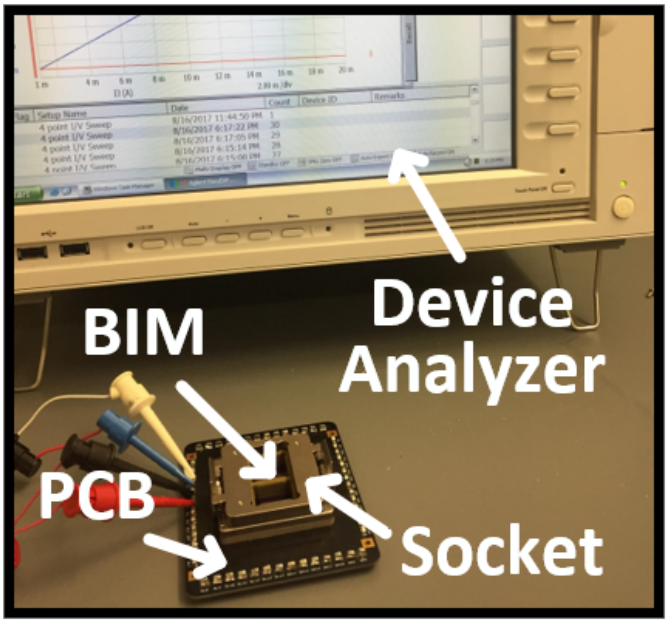


Figure 69. Four-point resistance setup.

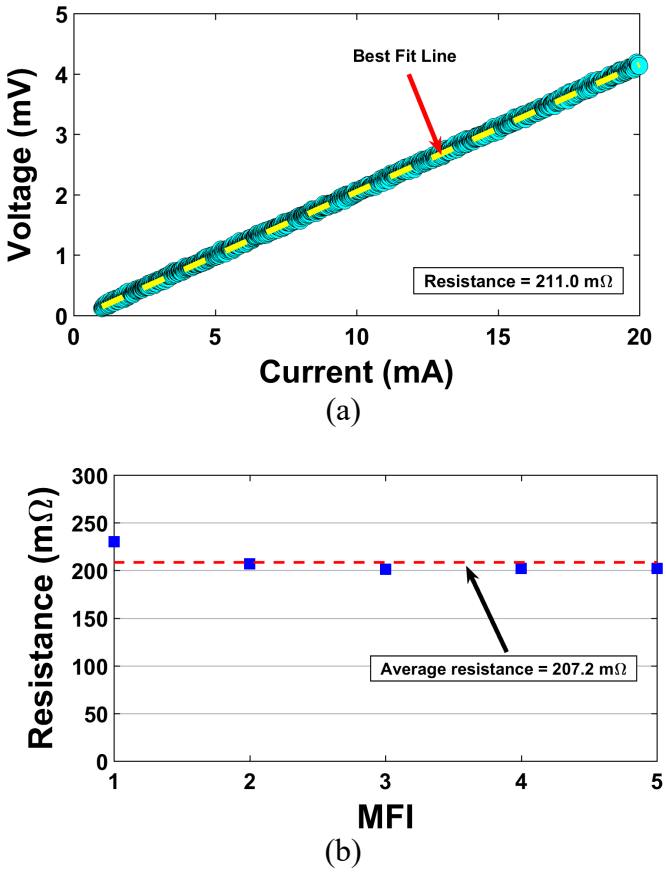


Figure 70. (a) Extracted resistance from an IV curve of one of the MFIs on the BIM and (b) four-point resistance measurements (including contact resistance) for five different MFIs (2.1 μm thick) on the same BIM sample.

These resistance measurements demonstrate that self-alignment is successfully achieved (as also seen previously via the alignment data) and that a sufficient assembly force is applied, hence an electrical connection can be formed and maintained (and removed at any time). The implications of these results convey that the potential exists for the development of a high-resolution, large field-of-view CMOS cell-based biosensor system that is field-deployable and that has the ability to deliver high-throughput testing.

3.9 Conclusion

A 3D integrated, self-aligned, and die-level socketed biosensing interface module (BIM) was microfabricated for CMOS cell-based biosensor applications. The enabling technologies of the BIM allowed for 1) the self-alignment of the BIM upon manual placement, achieving an accuracy of better than 5 μm, and 2) the ability to form and maintain temporary electrical interconnections. An average of 207.2 mΩ four-point resistance for 2.1 μm thick MFIs was recorded. Given these capabilities, the BIM has potential to assist in a wide variety of biosensing applications.

CHAPTER 4. BIOSENSING INTERFACE MODULE SYSTEM WITH THROUGH SILICON VIAS AND AN ANIOSTROPIC CONDUCTIVE FILM

4.1 Introduction

PariPoser was also used as the interconnection system between the BIM and the test die for the overall BIM system as seen in Figure 71. PariPoser is an anisotropic conductive film (ACF) where separated vertical columns of Ag-coated Ni balls within a matrix of silicone electrically connect the pads on the test die to the pads on the BIM. As these columns are separated from one another, they are electrically isolated when not in contact with the same pad. Hence, electrical connections can be formed between BIM and test die using PariPoser in much the same manner as when using MFIs as the interconnection system. Additionally, the BIM of CHAPTER 3 did not contain any through silicon vias (TSVs). However, the BIM in its full demonstration should contain TSVs to electrically connect the electrodes atop the BIM and the interconnection system underneath the BIM; hence this chapter also introduces the implementation of TSVs into the BIM.

Thus, we demonstrate: 1) the full fabrication process flow of incorporating TSVs into the PariPoser-based BIM, 2) the self-alignment and assembly process of the TSV-based, PariPoser-based BIM, 3) four-point resistance measurements of the standalone TSVs in addition to the "TSV + PariPoser" electrical links, and 4) TSV-based, PariPoser-based BIM fabrication challenges and potential solutions that address these challenges.

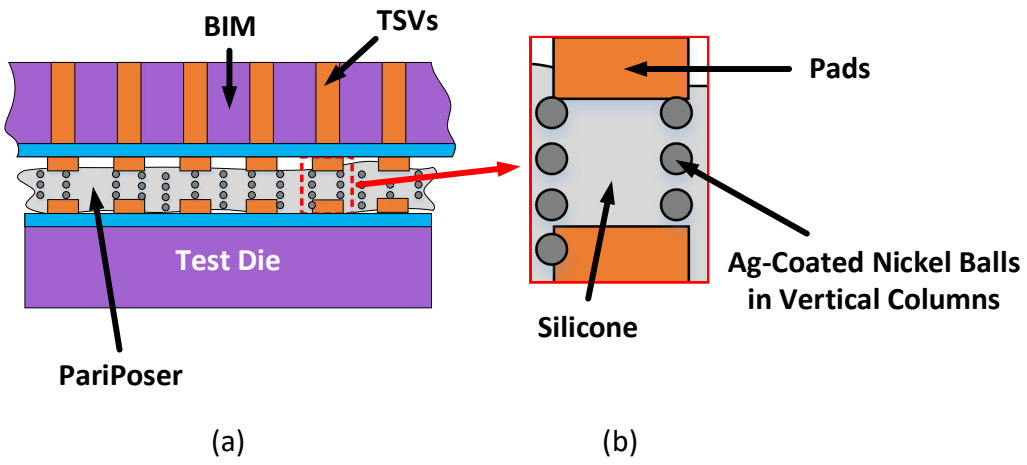


Figure 71. (a) Pariposer is used as the interconnection system between BIM and test die for the overall BIM system. Pariposer is (b) an anisotropic conductive film (ACF) where separated vertical columns of Ag-coated Ni balls within a matrix of silicone connect the pads on the test die to the pads on the BIM.

4.2 TSV-Based, PariPoser-Based BIM Fabrication Process Flow

Figure 72 illustrates the fabrication process flow for the TSV-based, PariPoser-based BIM. Silicon (100) wafers of 300 µm thickness were initially cleaned with a piranha bath (3 parts H_2SO_4 to 1 part H_2O_2) for 20 minutes at 120°C. As the diameter of the etched vias were 30 µm, 300 µm thick Si wafers were used in order to maintain the aspect ratio of the etched vias to no greater than approximately 10:1 (via depth to via diameter) as the via etching process requires a complete etch through the wafer (as opposed to the case of blind vias). The wafers were then transferred to a dump rinser for 3 cycles. A spin rinse dryer is then used to dry the wafers. The KOH pre-etch and final etch processing steps are identical to the corresponding KOH steps for the BIM of CHAPTER 3; however, the details of these steps will be repeated here for stand-alone purposes.

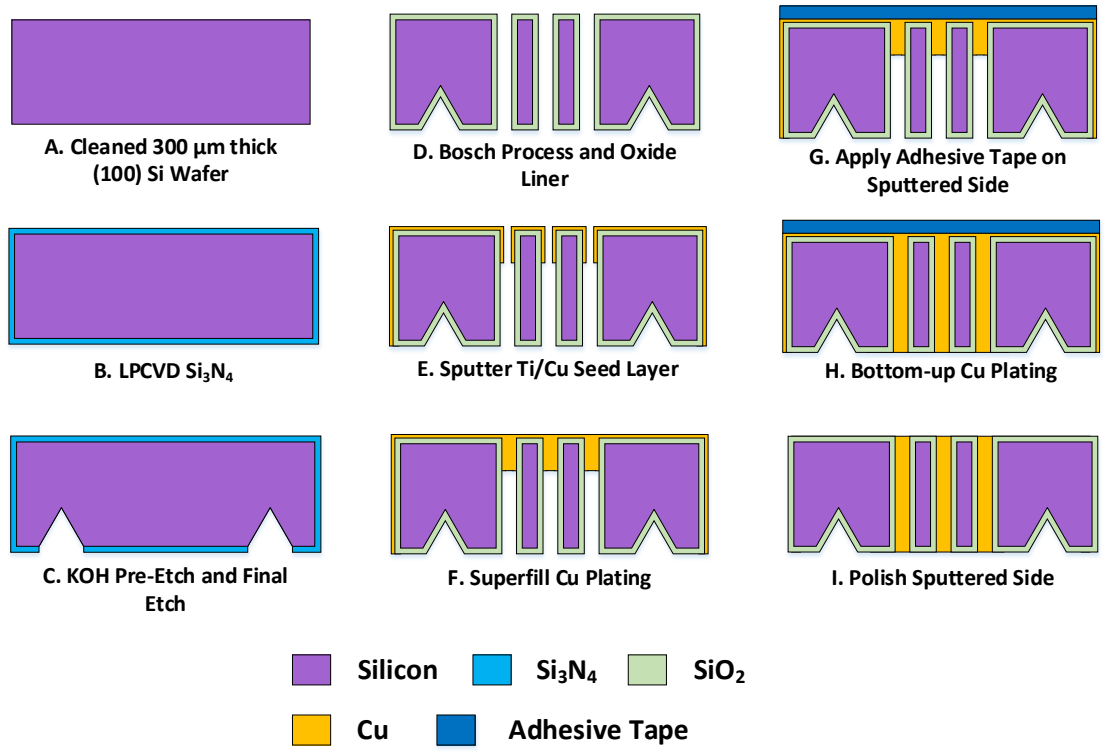


Figure 72. Fabrication process flow for the PariPoser-based BIM with through silicon vias (TSVs).

4.2.1 KOH Pre-Etch and Final Etch

After the wafers have been piranha-cleaned and dried, these wafers are then placed inside an LPCVD furnace for stoichiometric Si_3N_4 deposition. Approximately 125 nm of Si_3N_4 is deposited (film thickness is measured via a spectroscopic reflectometer). This LPCVD Si_3N_4 film is used as a mask during the KOH etching process.

The Si_3N_4-coated wafers are then prepared for spin coating via first performing an AMI clean process. A dehydration bake follows. NR5-8000 is spin coated and then patterned using the "pre-etch" mask. The exposed Si_3N_4 (not covered by the resist mask) is etched

away using an RIE process. The resist is then subsequently removed and is now ready for KOH etching.

The wafers are placed into a 45% KOH bath at 70°C for approximately 5 hours as part of the "pre-etch" step. Recall that the purpose of the "pre-etch" step is to reveal the (110) plane. Once this step is completed, the wafers are prepared for the next lithography step. Care is taken so not to damage the Si_3N_4 overhang in the undercut region (as it is easier to see the (110) plane with the overhang intact). The wafer undergoes another AMI clean and dehydration bake. NR5-8000 is spin coated and patterned using the "real" etch pattern, which is aligned to the just-revealed (110) plane. RIE removes the exposed Si_3N_4. The resist is then removed. The wafers are then placed into a 45% KOH bath at 90°C for approximately 2 hours, which results in a depth of approximately 280 μm (which are to carry the precision balls). Care is taken to not etch completely through the wafer. After the KOH etching is completed, the wafers undergo another AMI clean. A piranha clean may be performed as well.

4.2.2 Via Through Etching

NR5-8000 resist is spin coated at 1100 RPM on the "backside" of the wafer where pits are not present. Backside alignment is needed in this case to align the features on the pit-side to the features on the opposite side of the wafer. After patterning the "via opening mask," the exposed Si_3N_4 (not covered by the resist mask) is etched away using an RIE process. The wafer is then flipped over to the side where the pits are present and another Si_3N_4 dry etch process is performed to remove the entire Si_3N_4 thin film on the pit-side of the wafer.

This process step is performed to minimize footing during the inductively-coupled plasma (ICP) etching process. The wafer is now ready to undergo a Bosch etching process.

A separate clean, blank 500 μm thick Si wafer is prepared; this wafer will act as a carrier wafer to the BIM wafer during the Bosch process. This carrier wafer must have no passivation film to minimize footing. Cool grease (a thermally-conductive paste) is applied only to the peripheral of the carrier wafer (mostly where no patterns exist on the corresponding BIM wafer). An alternative to applying cool grease onto the carrier wafer is applying crystal bonder. Although ideally cool grease should be applied uniformly throughout the entire carrier wafer for the purposes of minimizing the air gap between carrier and BIM and hence improving thermal conductivity between the wafers (for the purposes of achieving a more uniform etching process throughout the wafer), cool grease exposure to the ICP plasma should be avoided. If not avoided, a residue is left behind in the areas of the exposed patterns (on the bottom side of the etched vias; same side as pit side); a solution to the removal of this residue has not been found. Additionally, contaminants are introduced into the ICP chamber. Performing a blind via etch can circumvent these challenges, which will be discussed in Section 4.4.2.

After applying cool grease to the peripheral of the carrier wafer, the BIM wafer is attached to the carrier wafer. Some pressure is applied to the BIM wafer atop the carrier wafer to ensure a good “connection” of the cool grease between BIM and carrier wafers (so to minimize or eliminate any air gaps between said wafers, at least at the peripherals of the wafers), and to promote adhesion so that the BIM wafer does not slide away from the carrier wafer during the ICP etching process. The wafer is then placed into an ICP tool and a Bosch process is performed. The Bosch process is performed until the etched pattern can

be seen on the pit-side of the wafer, which implies that the vias have etched all the way through the BIM wafer.

After the Bosch process is completed, the NR5-8000 dry etch mask is removed via acetone or a resist remover such as RR41 or 1165. An AMI clean is performed after this dry etch mask removal. To remove the remaining cool grease on the BIM wafer, a tex wipe sprayed with IPA is used to gently remove said cool grease. Note that at this point that the 300-µm thick BIM wafer contains large pits in addition to a large number of etched-through vias; therefore, gentle handling of the wafer is very critical as the wafer is fragile due to the aforementioned cavities and thin wafer. This point will be discussed in more details in Section 4.4.

4.2.3 Oxide Liner

A piranha clean is performed on the BIM wafers for 20-30 minutes at 120°C. Afterwards, a 2-minute descum is performed on the non-pit side. The remaining Si_3N_4 is then removed via dry etching (this film was protected by the NR5-8000 dry etch mask during the Bosch process). An alternative to the dry etching of Si_3N_4 is to perform a wet etch using a phosphoric acid bath at approximately 185°C. The details of this wet etching process setup will be omitted.

After the Si_3N_4 film has been removed, the BIM wafer is cleaned again via another piranha bath for 20-30 minutes at 120°C. The wafers are then rinsed and dried prior to being placed inside an oxide furnace where a wet oxidation process at 1100°C is performed. An oxide thickness of 1µm to 1.5µm is targeted. This specific oxide thickness is targeted due to both polishing considerations (not too thin) and time/stress considerations (not too thick).

4.2.4 Seed Layer Deposition

After the via oxide liner has been grown, the BIM wafer is ready for seed layer deposition. A 30 second descum process is performed on the non-pit side. The non-pit side is chosen as polishing is later required on this side and polishing is deemed to proceed more smoothly on the non-pit side. 20 nm Ti/400 nm Cu is sputtered. This seed layer only goes partially into the via due to aspect ratio limitations as illustrated in Step E of Figure 72 (approximately 1/3 of the way into the via).

4.2.5 Electroplating

4.2.5.1 Superfill Pinch-Off Plating

The TSV superfill electroplating process was performed using a copper sulfate solution (Elevate Cu Electrolyte 20). 0.6% V/V of a brightener additive and 1% V/V of a carrier additive were added to this bath to support the superfill electroplating process. The bath was not heated and operated at room temperature. The Cu deposition was then performed using pulsed current (PC) plating (5 milliseconds on and 3 milliseconds off) as seen in Figure 73. The electroplated Cu pinches-off and partially fills the via as illustrated in Step F of Figure 72. After electroplating is completed, the sample is washed thoroughly with DI water and then dried with a N_2 gun.

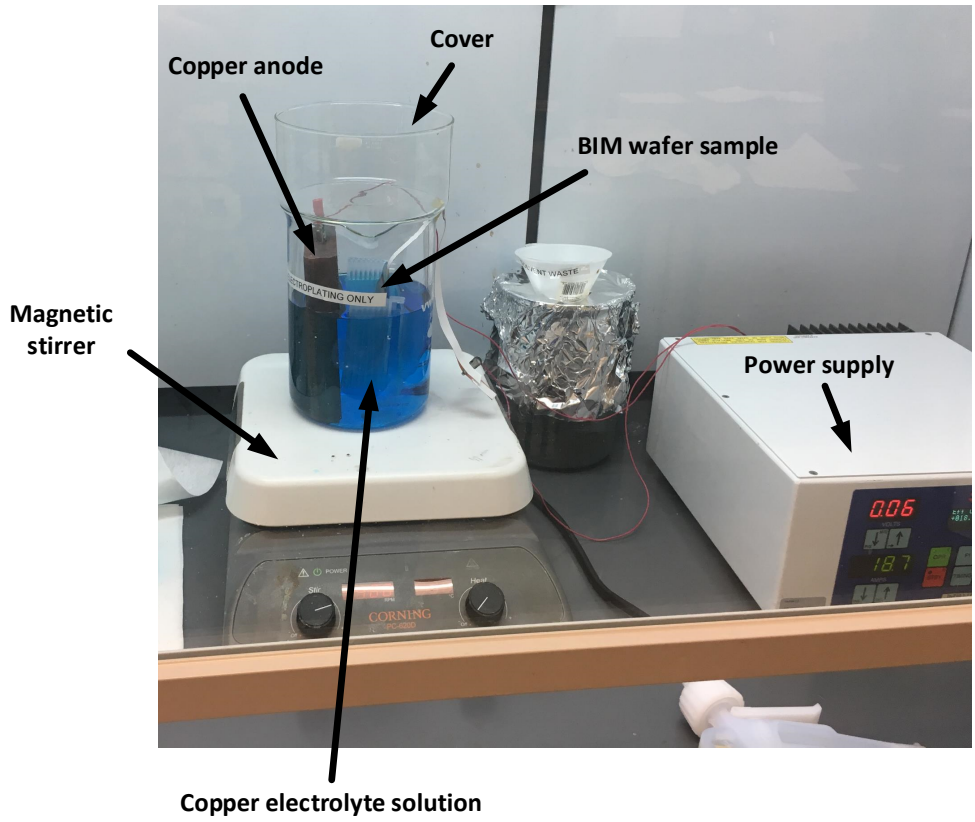


Figure 73. Cu TSV electroplating bath setup.

4.2.5.2 Bottom-Up Plating

The electroplated side of the BIM wafer is covered with an adhesive tape to prevent further electroplating on the pinch-off, non-pit side as illustrated in Step G of Figure 72. The same bath (at room temperature again) is used in addition to the same pulse plating recipe. This plating continues until the via is filled as seen in Step H of Figure 72. After electroplating is completed, the sample is washed thoroughly with DI water and then dried with a N_2 gun. A small excess of electroplated Cu is seen protruding out the vias on the pit-side of the wafer. These are purposely left as is to act as stubs for the PariPoser assembly

process as the PariPoser silicone acts as an incompressible fluid and requires compression of the silver-coated nickel particles (hence space is needed for the silicone to flow into as the stubs compress). Alternatively, this pit-side can be polished and properly plated stubs can be added at these TSV sites.

4.2.6 Polishing

The sputtered side or the non-pit side can be polished to remove the excess electroplated Cu and seed layer as seen in Figure 74. As four-point resistance of the TSVs and PariPoser were to be measured, this side was initially left untouched for measurement purposes. When Cu polishing was needed however, a grind and chemical mechanical polishing (CMP) process was outsourced to Aptek Industries, Inc. in San Jose, CA.

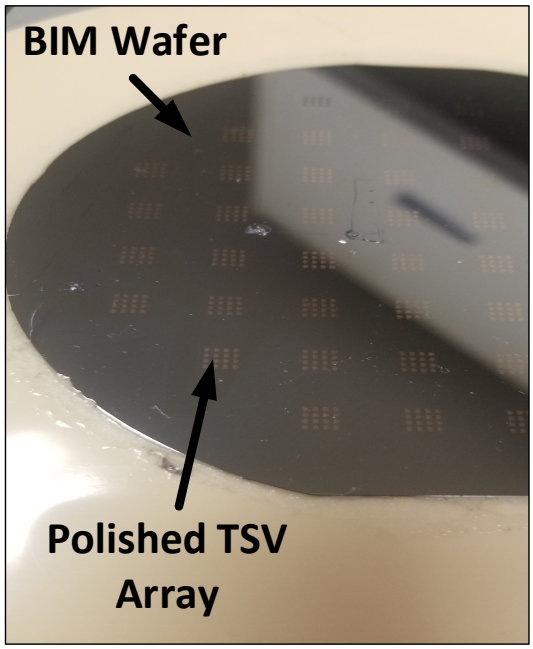


Figure 74. TSV-based, PariPoser-based BIM wafer after polishing (on non-pit side). As a note, a different TSV layout is used here relative to the primary layout used throughout CHAPTER 3 and the rest of CHAPTER 4.

4.2.7 Fabricated TSV Array Dimensions

X-ray images of the fabricated TSVs are shown in Figure 75. TSV diameter is 30 µm, TSV depth is 300 µm (equivalent to the thickness of the 300 µm thick BIM wafer), TSV pitch is approximately 58 µm, and a total of 1,024 TSVs exist in the TSV array (just as was the case for the MFIs of the BIM of CHAPTER 3 as the same layout dimensions are used).

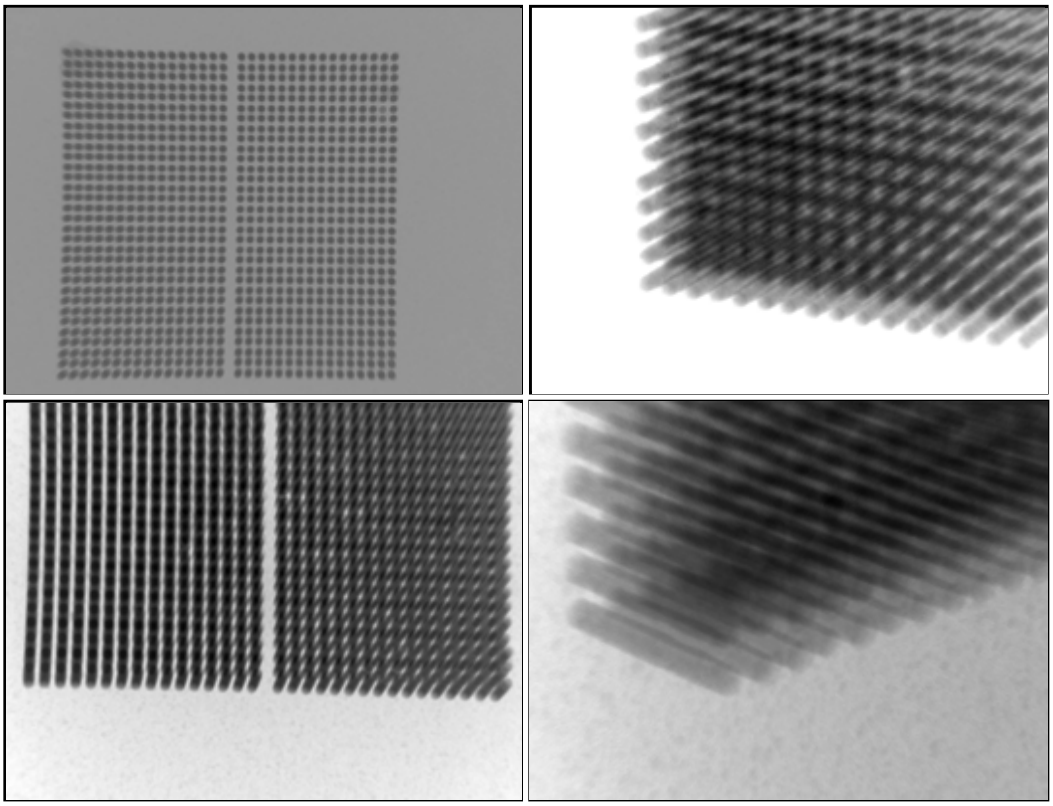


Figure 75. X-ray images of the fabricated BIM TSVs.

4.3 Setup, Results, and Discussion

4.3.1 Assembly and alignment

The double self-alignment mechanism implemented for the TSV-based, PariPoser-based BIM is identical to that of the BIM of CHAPTER 3. The same socket of CHAPTER 3 was also used to apply the needed pressure onto the BIM so that the PariPoser electrically connects electrodes between the BIM and the test die. The assembly process with PariPoser is illustrated in Figure 76.

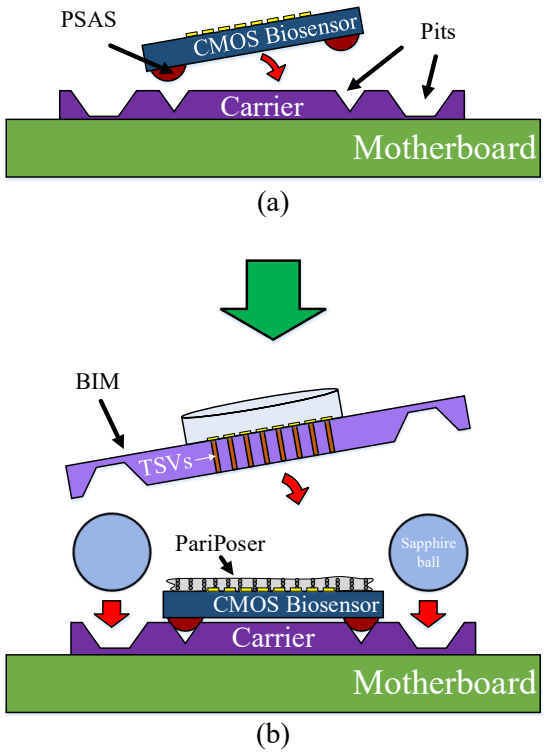


Figure 76. Double self-alignment process flow demonstrating two levels of self-alignment: (a) CMOS biosensor to carrier self-alignment via a PSAS/pit mechanism, (b) BIM to carrier self-alignment via a sapphire ball/pit mechanism. The PariPoser interconnection system is used here in place of MFIs to electrically connect the "CMOS Biosensor" to the BIM. TSVs in the BIM electrically connect the bottom of the BIM to the top of the BIM, where cells are to be grown.

All assembly and alignment are performed via manual placement as in the case of the BIM of CHAPTER 3. Specifically, the carrier is manually picked up and placed into the

socket base, the test die is picked up and placed onto the carrier, the PariPoser interconnection system is picked up and placed roughly onto the center of the test die (alignment does not matter here), the BIM is picked up and placed onto the carrier, and the clamp is picked up and inserted into the socket base. As alignment and alignment repeatability were demonstrated for the BIM system of CHAPTER 3, no alignment data was collected for the TSV-based, PariPoser-based BIM.

4.3.2 Electrical data

Both the standalone TSV four-point resistance measurements and the "PariPoser + TSV" four-point resistance measurements were performed and recorded. The setups and measurements results for each case will be described next.

4.3.2.1 Standalone TSV four-point resistance

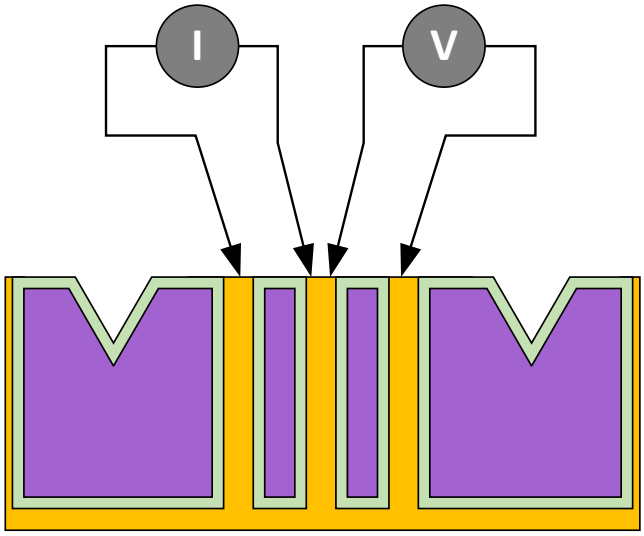


Figure 77. Standalone TSV four-point resistance measurement setup with electrically isolated electrodes on one side and an electroplated coating shorting all electrodes on the other side. A probe station is used to measure the TSV's four-point resistance.

The individual BIM wafer with TSVs was left with electrically isolated electrodes on one side and an electroplated coating shorting all electrodes on the other side as seen in Figure 77. A probe station was used to measure the four-point resistance of the TSVs. These results are shown in Figure 78, where the TSV four-point resistance varies from 3.74 mΩ to 4.10 mΩ with an average resistance of 3.94 mΩ.

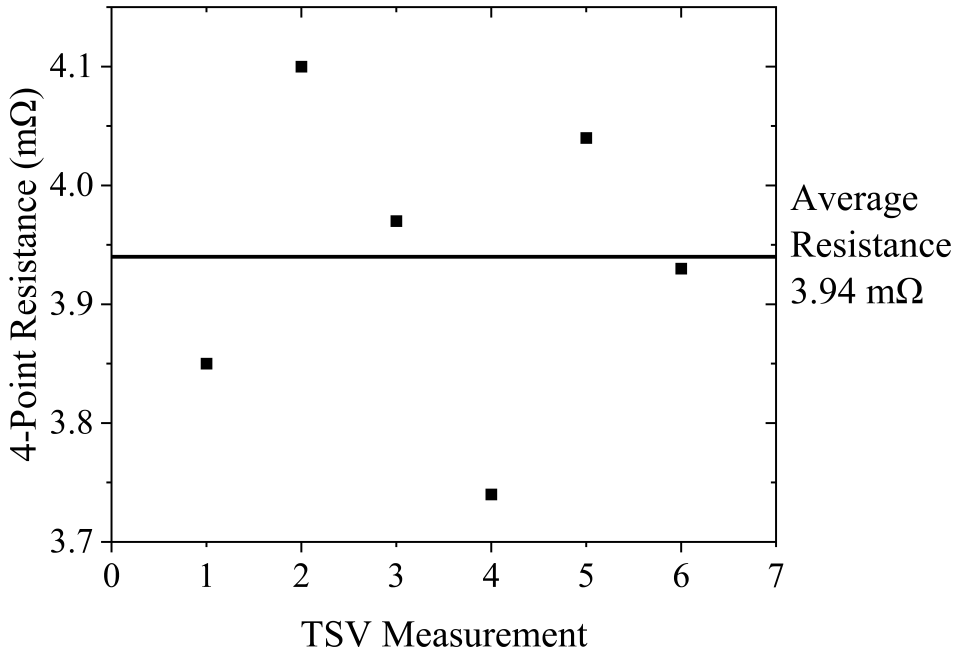


Figure 78. Four-point resistance measurements of six different BIM TSVs on the same sample.

4.3.2.2 Combined "PariPoser + TSV" four-point resistance

To test the "PariPoser + TSV" electrical interconnections, the BIM is self-aligned, assembled, and clamped onto the test die with the PariPoser interconnection system in place as seen in Figure 76 (b). The top of the BIM (non-pit side) is shorted electrically as in the case of the standalone TSV resistance measurement setup seen in Figure 77. The

overall four-point resistance measurement setup is identical to that of the BIM of CHAPTER 3 for MFIs as seen in Figure 69. The four-point resistance measurements of the "PariPoser + TSV" electrical interconnections are reported in Figure 79, where the "PariPoser + TSV" four-point resistance measurements vary from 0.8238 Ω to 1.1040 Ω with an average resistance of approximately 0.979 Ω. A larger compression force on the BIM would serve to decrease this resistance. Relative to the four-point resistance measurements of the TSVs as recorded in Figure 78, it is seen that the majority of the "PariPoser + TSV" resistance is comprised of the PariPoser itself and the PariPoser contact resistance. Part of the seen variation in the "PariPoser + TSV" resistance data may stem from the variability of the stub heights on the pit-side of the BIM sample. Recall that any over-electroplated Cu on the pit-side of the BIM wafer was left untouched to act as stubs for the PariPoser interconnection system. A polish on the pit-side followed by a patterning and plating of the stubs to equal thicknesses should create a more uniform resistance reading throughout the tested samples.

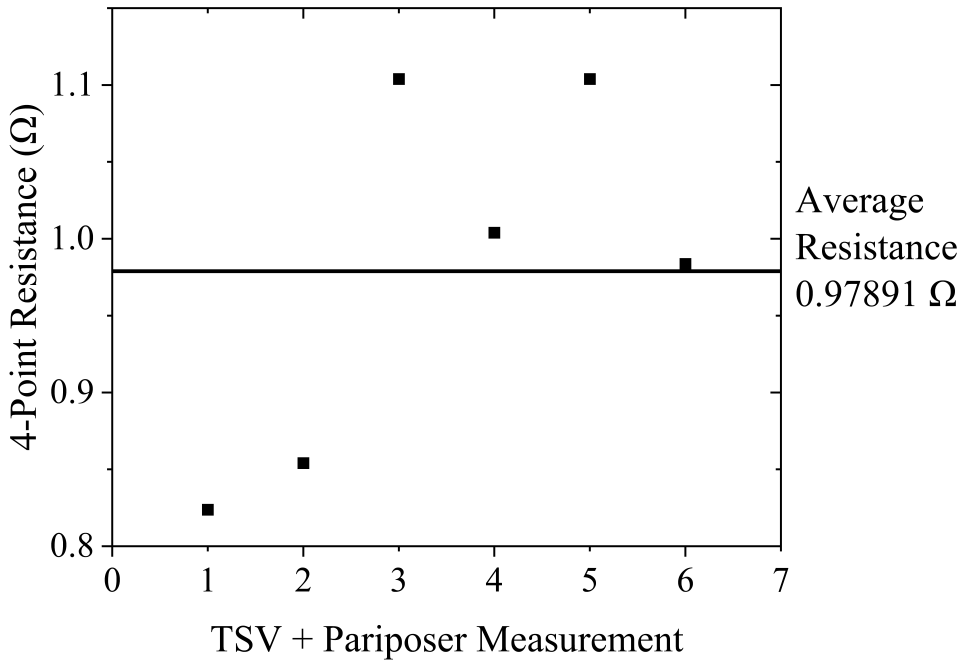


Figure 79. Four-point resistance measurements of six different BIM "TSV + PariPoser" electrical links on the same BIM sample.

These resistance measurements demonstrate that self-alignment is successfully achieved and that a sufficient assembly force is applied, hence an electrical connection can be formed and maintained (and removed at any time).

4.4 Fabrication Challenges and Potential Solutions

4.4.1 Fabrication Challenges

After the KOH-etching of the pits and the ICP etching of the through vias, the BIM wafer (being 300 μm thick) is relatively fragile and prone to cracking/breaking. Of the ten wafers from the first batch of wafers to undergo the TSV-based, PariPoser-based BIM fabrication process, only one survived until the end of the electroplating process; this one wafer also survived the final grinding and CMP process. The majority of these ten wafers (eight of

these wafers) survived until just before the electroplating step after careful handling of said wafers. However, the electroplating process requires the application of an adhesive tape as part of the overall plating process as described in Section 4.2.5.2. This tape has strong adhesive properties, which is desired to prevent electroplating solution from leaking in; however, this same strong adhesion requires sufficient force to peel off the tape from the BIM wafer. It is often the case that this strong force creates cracks throughout the BIM wafer, even if proceeding with very careful wafer handling. As the electroplating process must be checked at several different periods to ensure that plating is completed (and if not completed, said wafer must resume plating), the adhesive tape is often applied and removed during each of these periods as the adhesion of the tape weakens after the sample is removed, cleaned, and dried. Several applications and removals of the adhesive tape can cause (and have caused) the BIM wafer to break.

Even if the wafers do not break, but contain cracks, they must still undergo the grinding and CMP process. The BIM may also require additional steps after the CMP process for biocompatibility and SNR purposes (or for PariPoser stub purposes). Therefore, even non-broken (but cracked) wafers will be susceptible to breaking during one of these subsequent processes. Said fabrication process flow seems ultimately a high-risk process for the TSV-based BIMs. Hence, a blind-via approach, as seen in Figure 80, was conceived and partially attempted.

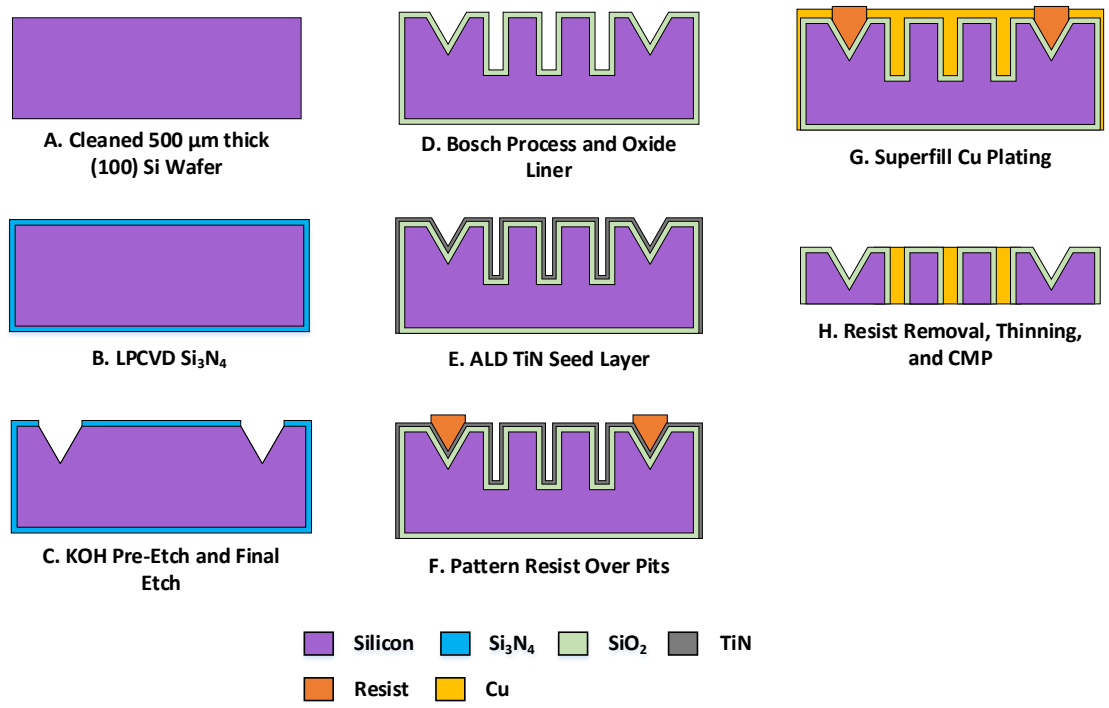


Figure 80. Fabrication process flow for a TSV-based BIM using a blind-via approach.

4.4.2 Blind-Via Potential Solution

This more robust approach replaces the 300 µm thick Si wafers with 500 µm thick Si wafers and it replaces the through via etching with blind via etching, as seen in Figure 81. The handling of these thicker and less fragile wafers is a much lower-risk approach to fabricating TSVs. Additionally, no adhesive tape is required during the fabrication process flow, which considerably lowers the risk of introducing cracks into the wafer. As blind vias are employed, a thinning process (in addition to a grinding and CMP process) must be performed to expose the other end of the TSVs. This thinning process (in addition to grinding and CMP process) is outsourced to Aptek Industries, Inc.

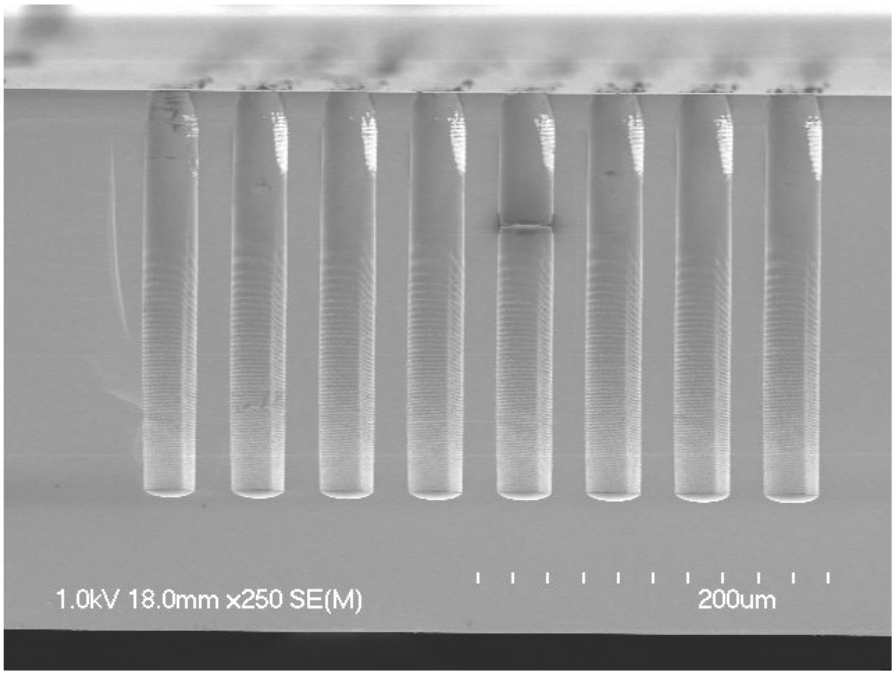


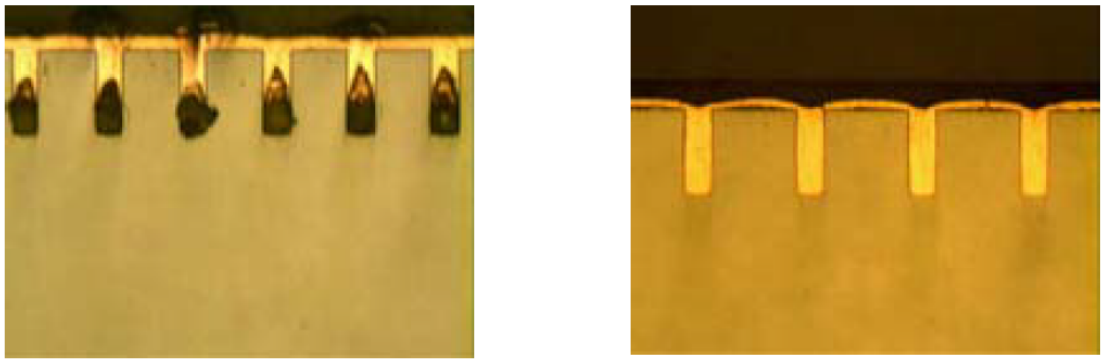
Figure 81. SEM of TSV-based BIM cross-section, showing ≈300 µm deep blind vias (30 µm via diameter) after the Bosch etching process.

The other advantage of employing blind vias (besides creating a much more robust wafer and not having to use an adhesive tape) is the ability to apply the thermally conductive cool grease (or crystal bonder) throughout the entire carrier wafer in preparation for the Bosch process of the BIM wafer. As aforementioned, for the previous 300 µm thick wafers, to prevent cool grease from being exposed to the ICP plasma (as the vias were etched completely through the BIM wafer), cool grease was only applied to the peripheral of the carrier wafer, which is not ideal.

However, a blind via approach requires several considerations that are not as critical in the case of the through-via approach used for the 300 µm thick BIM sample: 1) pre-wetting, 2) conformal seed layer deposition, 3) high aspect ratio (10:1) superfill plating.

4.4.2.1 Pre-wetting

During the electroplating process, it is essential that the plating solution gets inside the vias and that any air bubbles within these vias are removed. The replenishment of the copper ions and bath additives within the vias is also critical for a successful Cu electroplating process. Otherwise, plating will not successfully occur within these regions of the vias as seen in Figure 82. In the case of the through vias, the initial electroplating pinch-off step has both sides of the via open; hence, any air bubbles within the vias can more easily escape through the other end of the open via, and the needed ions and elements can also more easily arrive within the via from both open ends (the bottom-up plating step however does require a greater emphasis on pre-wetting).



(a) (b)

Figure 82. Filling a blind via (a) without pre-wetting and (b) with pre-wetting [165].

Several pre-wetting techniques are described in the literature including agitation [166], vacuum-based pre-wetting [165], [166], chemical [167], surface hydrophilicity modification based pre-wetting [168], ultrasonic agitation [169], and high pressure DI water based pre-wetting [170].

The vacuum-based pre-wetting method was used for the blind-via approach due to its simplicity and its ability to remove air from the BIM sample vias prior to being submerged inside the pre-wetting solution (e.g., DI water). Additionally, [166] demonstrated better success with vacuum-based pre-wetting versus agitation-based pre-wetting (i.e., less voids). To this end, a custom vacuum-based pre-wetting system was built to implement this vacuum-based pre-wetting process as seen in Figure 83.

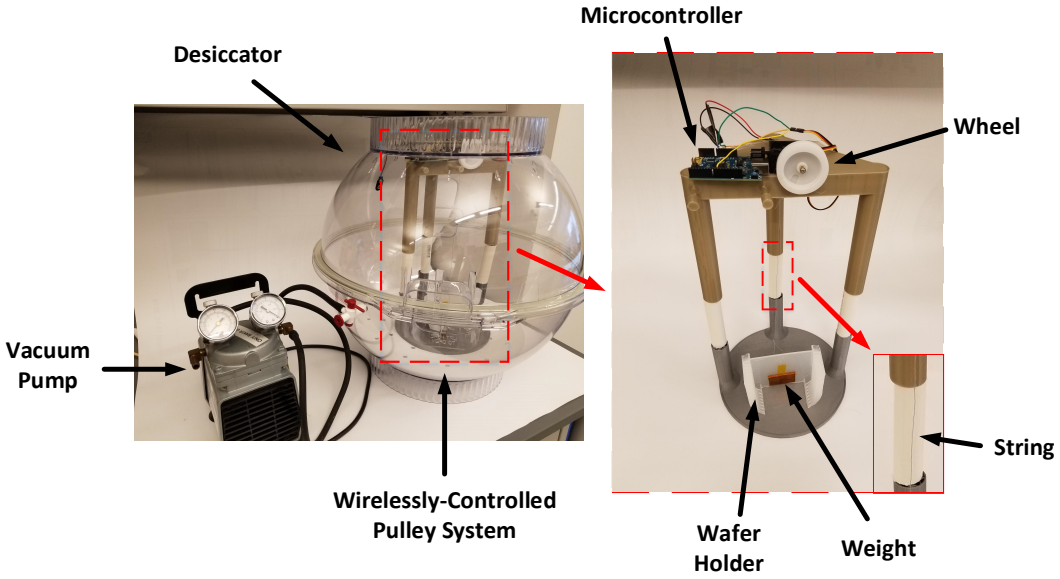


Figure 83. Wirelessly-controlled pulley system slowly lowers BIM wafer into beaker filled with pre-wetting solution under vacuum conditions.

This setup consists of a wirelessly-controlled pulley system (wirelessly controlled via a microcontroller), which lowers the BIM sample (which is held by a wafer holder) into a beaker filled with pre-wetting solution (e.g., DI water) under vacuum conditions. These vacuum conditions are created within a desiccator chamber attached to a vacuum pump, which pumps down the chamber. The BIM sample only enters the beaker after several

minutes of pumping down (to allow the air to pump out). As DI water is used as the pre-wetting solution, it is essential that the critical vaporization temperature (293 K) in vacuum pressure (2.3 KPa) is not exceeded. Otherwise, vapor bubbles from the DI water may form which is problematic for vias in much the same way as air bubbles are problematic.

4.4.2.2 Conformal Seed Layer Deposition

Due to the relatively high aspect ratio of the vias (10:1), depositing a conformal and high-conductivity seed layer within this via may be challenging given the current equipment housed by Georgia Tech's IEN microfabrication facilities. Atomic Layer Deposition (ALD) titanium nitride (TiN) was deposited to act as the electroplating seed layer given the high aspect ratio depositions provided by ALD. The resistivity of ALD TiN is approximately 72 μΩ·cm [171], which is relatively high compared to the bulk copper resistivity of 1.67 μΩ·cm. This relatively high resistivity can cause relatively high IR drops across the wafer and within the vias, which can create difficulties during the superfill plating process (e.g., the via may close near the top before the rest of the via can be plated). To address the IR drop across the wafer, copper was evaporated onto the BIM wafer (this step is omitted in Figure 80), which would help improve plating uniformity across the wafer. However, the local IR drop within the via would remain. Improving the conductivity of the seed layer would minimize this IR drop within the via and assist in the superfill plating process.

4.4.2.3 High-Aspect Ratio Superfill Plating

The additives used for the pinch-off superfill step in 4.2.5.1 is also used here. The electroplating current density, the deposition frequency, the deposition duty cycle, etc.

affect a wide variety of plating parameters including current efficiency, bottom-up filling ratio, side wall growth ratio, etc. [172]. These variables must be optimized for a successful superfill plating process. However, as aforementioned, a low-conductivity seed layer (which can cause a large IR drop within the via) can add to the challenges of a successful superfill plating process.

The continuation of this blind via potential solution is left for future work and will be discussed again in CHAPTER 7.

4.5 Conclusion

A TSV-based, PariPoser-based version of the BIM was microfabricated in this chapter. Four-point resistance of this BIM system was measured for both TSVs (standalone) and the "TSV + PariPoser" electrical link. An average of 0.979 Ω four-point resistance of the "TSV + PariPoser" electrical link was recorded. A larger compression force on the BIM would serve to decrease this resistance. The current TSV-based, PariPoser-based BIM undergoes a relatively high-risk fabrication process flow (i.e., thin wafer with many cavities from a large number of large pits and vias). The specific challenges associated with this high-risk process in addition to a potential blind-via solution have been discussed.

CHAPTER 5. PSAS-TO-PSAS SELF-ALIGNMENT MECHANISM WITH SUB-MICRON ACCURACY

5.1 Introduction

Two different mechanically-based self-alignment mechanisms have been used thus far throughout this thesis: 1) PSAS-to-Pits and 2) Ball-in-Pit. Both technologies were used in combination in CHAPTER 3 and CHAPTER 4. In this chapter, a novel mechanically-based self-alignment mechanism is introduced where lithographically-defined PSAS on one substrate self-aligns to lithographically-defined PSAS on another substrate; this self-alignment technology is termed PSAS-to-PSAS. This PSAS-to-PSAS self-alignment mechanism possesses two primary advantages:

1) It is non substrate invasive as no etching is required as is the case for PSAS-to-Pits and Ball-in-Pit. This non-invasiveness aids to consume less substrate real estate in addition to eliminating contact with potentially incompatible chemicals (e.g., KOH).
2) It is substrate agnostic as any substrate material may be used (surface roughness will affect PSAS size however due to lithography scaling limitations on rougher surface materials such as non-crystalline materials). As an anisotropic wet etch is avoided (unlike with the case of PSAS-to-Pits and Ball-in-Pit), the crystallographic orientation of the substrate materials is irrelevant (in regard to achieving an anisotropic etched profile as none is needed). Additionally, non-crystalline materials may be used.

Another advantage of the PSAS-to-PSAS technology is that the PSAS-to-PSAS can act as a temporary self-alignment mechanism that can later be removed (via acetone or a resist remover) if need be.

This chapter demonstrates: 1) PSAS-to-PSAS design and engineering to understand the relationship between PSAS width, height, and lateral spacing, and the inter-substrate gap, 2) self-alignment of two substrates containing only PSAS, which removes the need for an alignment/assembly placement tool, and corresponding alignment data, and 3) alignment repeatability data that demonstrates the potential for the PSAS-to-PSAS self-alignment technology as a viable self-alignment candidate when repeated use of one or both of the mating substrates is needed.

5.2 PSAS-to-PSAS Overview, Design, and Engineering

5.2.1 PSAS-to-PSAS Overview

PSAS-to-PSAS self-alignment can occur in several different configurations, as seen in Figure 84, where a 3-to-1 PSAS-to-PSAS configuration and a 4-to-1 PSAS-to-PSAS configuration are illustrated. A 3-to-1 PSAS-to-PSAS configuration is used throughout this chapter since the PSAS-to-PSAS lateral spacing (on the same substrate) is larger and hence the inter-substrate gap is less susceptible to change due to tolerance-induced changes in this lateral PSAS spacing (from the lithography process). The relationship between this inter-substrate gap and PSAS dimensions (and their definitions) is discussed in Section 5.2.2. However, a 4-to-1 (or greater) PSAS-to-PSAS configuration may provide more assembly robustness.

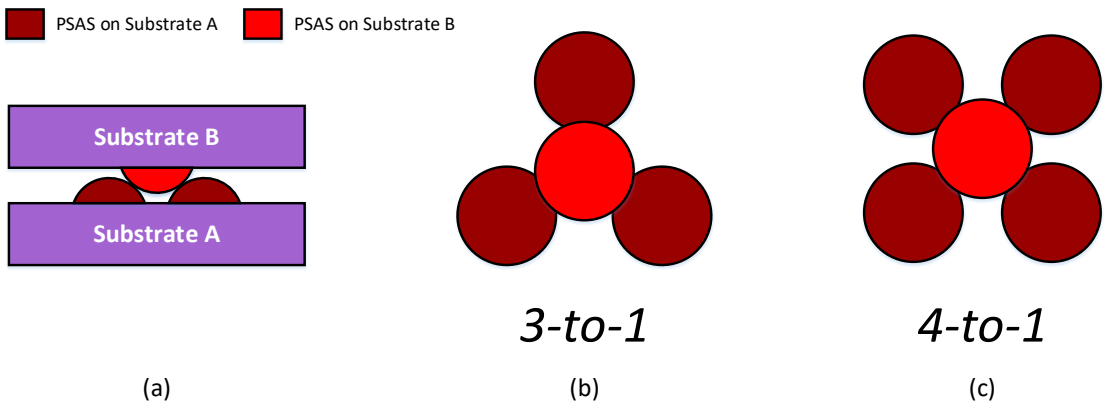


Figure 84. (a) Cross-section view of 1 PSAS on Substrate B aligning to a set of PSAS on Substrate A, which come in different configurations: (b) Overhead view of 3-to-1 PSAS-to-PSAS configuration where 1 PSAS on one substrate aligns to a 3-PSAS set on another substrate and (c) overhead view of 4-to-1 PSAS-to-PSAS configuration where 1 PSAS on one substrate aligns to a 4-PSAS set on another substrate.

5.2.2 PSAS-to-PSAS Design and Engineering

The dimensions of the PSAS (both height and width) and the lateral PSAS spacing affect the gap between mating substrates or the inter-substrate gap. To determine these relationships for design and engineering purposes, the PSAS-to-PSAS self-alignment configuration is first parametrized as illustrated in Figure 85. The highlighted geometrical parameters from Figure 85 include PSAS height (h), PSAS width (w), lateral PSAS spacing (s), and the inter-substate gap (g). For purposes of simplicity, the PSAS on both substrates are assumed to have the same height and width (h and w). Additionally, the PSAS is assumed to take the shape of a truncated sphere as was demonstrated in [128] and as seen in Figure 86.

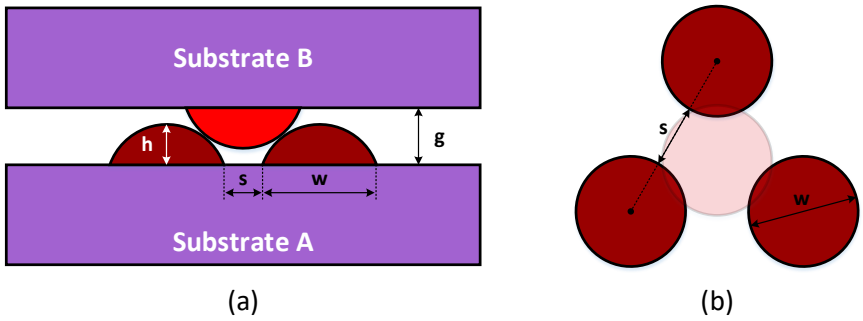


Figure 85. PSAS-to-PSAS geometry from (a) a cross-sectional view and (b) an overhead view. Highlighted geometrical parameters include PSAS height (*h*), PSAS width (*w*), lateral PSAS spacing (*s*), and inter-substrate gap (*g*). The PSAS on Substrate A and Substrate B are assumed to have the same PSAS dimensions (*h* and *w*).

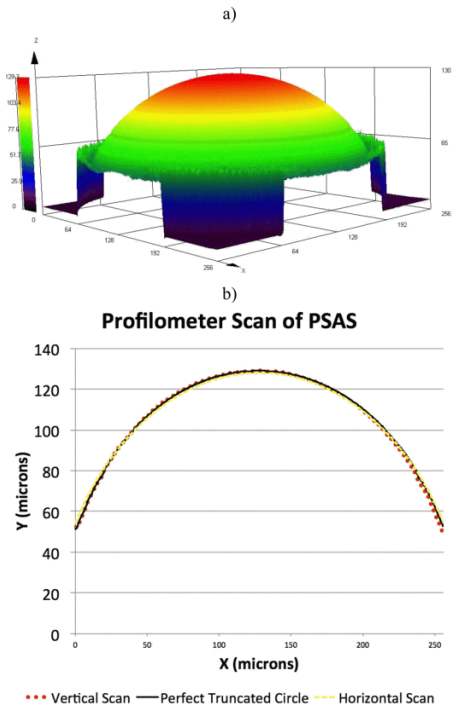


Figure 86. (a) A 3D image of a PSAS scanned by a confocal laser microscope and b) an extracted plot of the measured profile of the PSAS through its center both in the horizontal and vertical directions. Overlayed on this same extracted plot is a perfect truncated circle, which demonstrates a very close overlap between the PSAS profile and a perfect truncated circle/sphere [128].

For simplicity, we initially assume that the PSAS has their height equal to their half-width ($h = w/2$); in other words, the PSAS is initially considered a perfect half-sphere (or hemisphere). Afterwards, we consider the case of a truncated half-sphere. Figure 87 and Figure 88 illustrate the geometry involved in the PSAS-to-PSAS self-alignment calculations between the dimensions of the PSAS (assumed to be a perfect half-sphere here as aforementioned) and the inter-substrate gap. As is seen in Figure 87 and Figure 88, the 3-to-1 PSAS-to-PSAS configuration can be viewed as a tetrahedron with each vertex of the tetrahedron located at the center of the bottom of each PSAS (or the center of the PSAS sphere if the PSAS were a perfect sphere as opposed to a perfect half-sphere). In viewing this tetrahedron, it is desired to solve for the height of the tetrahedron, which in the case of the PSAS-to-PSAS configuration is the inter-substrate gap (g).

The tetrahedron can be split essentially into two 2D triangles for the purposes of determining the relationship between PSAS geometry and the inter-substrate gap, as seen in Figure 87 and Figure 88. The base of the tetrahedron, as seen in Figure 87, is an equilateral triangle in which a_1 must be determined in terms of the PSAS width (w, which is also equal to the PSAS diameter in this case) and the lateral PSAS spacing (s). Within this equilateral triangular base exists a 30-60-90 triangle, as seen in Figure 87. Solving for a_1 of this 30-60-90 triangle leads to:

$$a_1 = \frac{(w+s)}{2} \cdot \frac{2}{\sqrt{3}}$$

$$a_1 = \frac{(w+s) \cdot \sqrt{3}}{3} \tag{4}$$

where:

w = PSAS width

s = Lateral PSAS spacing

Now that a_1 is known in terms of PSAS geometrical parameters, we can solve for the inter-substrate gap (g) in the 2D right triangle seen in Figure 88:

$$a_2{}^2 = a_1{}^2 + g^2$$

$$w^2 = a_1{}^2 + g^2$$

$$g = \sqrt{w^2 - a_1{}^2} \tag{5}$$

Replacing a_1 in (5) with (4) gives:

$$g = \sqrt{\frac{2w^2 - 2w \cdot s - s^2}{3}}\ for\ PSAS\ hemisphere \tag{5}$$

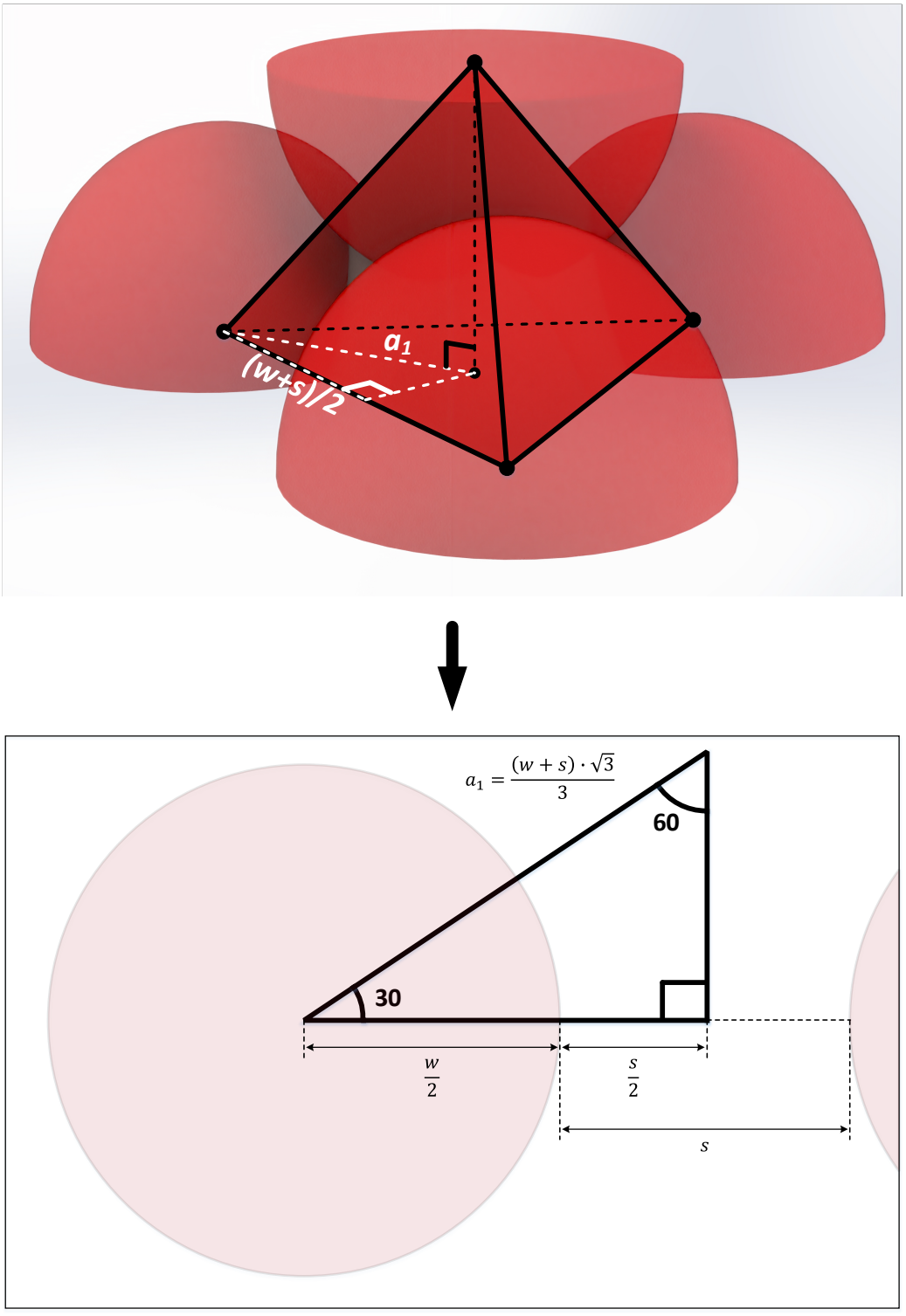


Figure 87. PSAS-to-PSAS self-alignment geometry for obtaining the relationship between PSAS dimensions and the inter-substrate gap. First breakdown of tetrahedron geometry for obtaining parameter a_1.

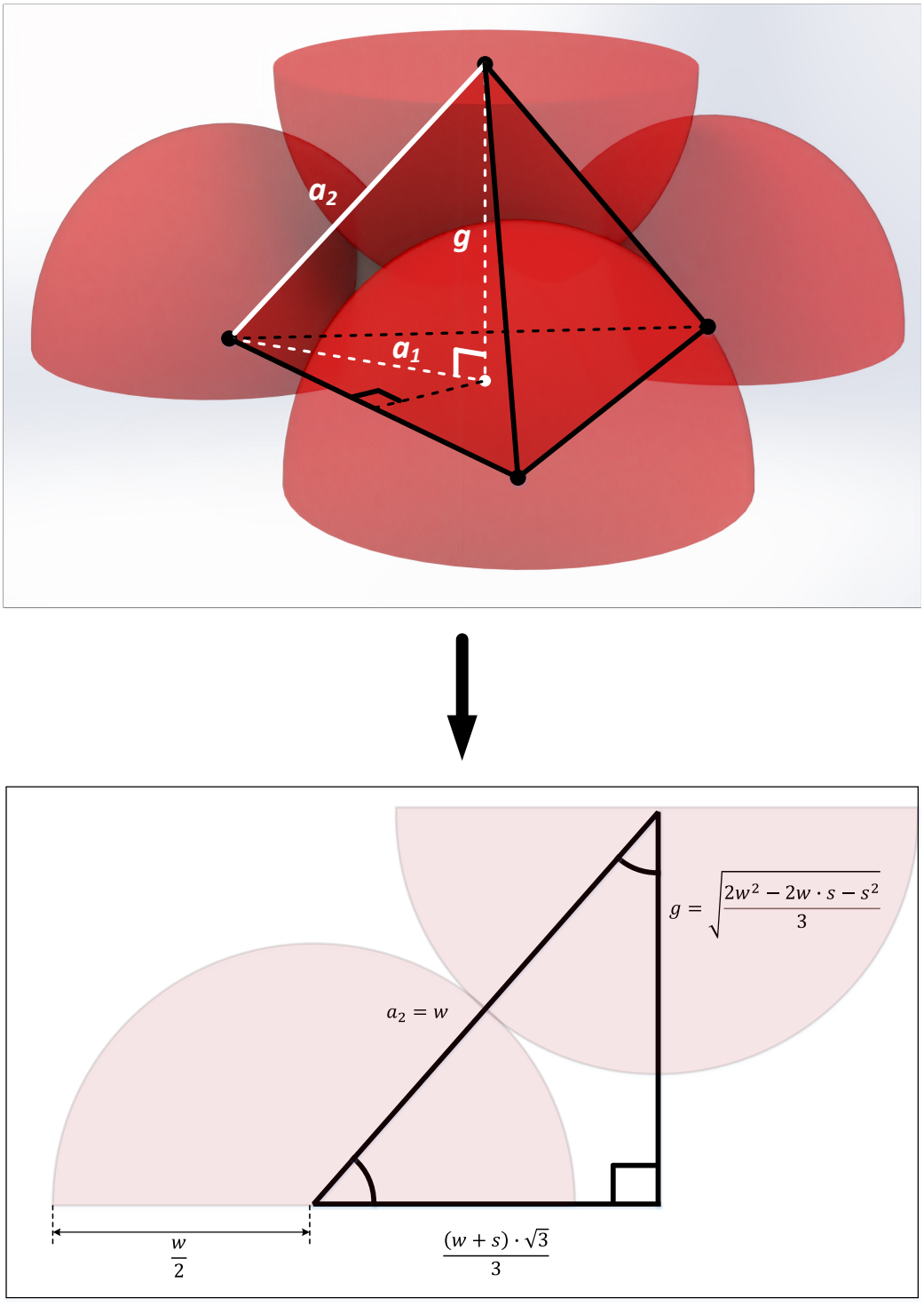


Figure 88. PSAS-to-PSAS self-alignment geometry for obtaining the relationship between PSAS dimensions and the inter-substrate gap. Second breakdown of tetrahedron geometry for obtaining inter-substrate gap parameter *g*.

Recall that Equation (5) is only for the specific case where the PSAS is a perfect hemisphere ($h = w/2$). In the event where the PSAS is a truncated hemisphere, $h \neq w/2$, the above equations need to be modified in order to take this more generalized geometry into account. The same tetrahedron geometrical approach is taken but with a modification, as seen in Figure 89: the truncated hemisphere PSAS is first assumed to be a complete hemisphere for mathematical simplification purposes. In other words, it is first assumed that the hemisphere is not truncated. The extra portion added to the truncated hemisphere height, h_{extra}, (so that it is a full hemisphere) is removed after the "full hemisphere" gap calculations have been completed. Thus, we first determine the radius of the "full PSAS hemisphere" (R) and the lateral PSAS spacing of the "full PSAS hemisphere" (S) from the dimensions of the truncated PSAS hemisphere (w, h, and s):

$$R = \frac{w^2}{8h} + \frac{h}{2} \tag{6}$$

$$D = 2R \tag{7}$$

$$S = s - 2\left(R - \frac{w}{2}\right) \tag{8}$$

where

R = the radius of the PSAS assuming that the PSAS is a full hemisphere

D = the diameter of the PSAS assuming that the PSAS is a full hemisphere

S = the lateral PSAS spacing assuming that the PSAS is a full hemisphere

D from (7) and *S* from (8) are plugged into (5) as *w* and *s*, respectively:

$$g_{pre} = \sqrt{\frac{2D^2 - 2D \cdot S - S^2}{3}} \tag{9}$$

where

g_{pre} = the inter-substrate "pre-gap" assuming that the PSAS are full hemispheres

The "extra" PSAS height (h_{extra}) added to the truncated PSAS hemisphere for the purposes of mathematical calculations is then removed. This "extra" PSAS height (h_{extra}) is calculated as follows:

$$h_{extra} = R - h \tag{10}$$

where

h_{extra} = the extra PSAS height added to the truncated hemisphere for "full PSAS hemisphere" calculations

As this extra height (h_{extra}) is added to both the PSAS on the top substrate and the PSAS on the bottom substrate as seen in Figure 89, two of these heights ($2h_{extra}$) must be removed from the pre-gap (g_{pre}) calculations:

$$g = g_{pre} - 2h_{extra} \tag{11}$$

$$g = \frac{1}{4}\sqrt{\frac{w^4}{h^2} + 16h^2 + \frac{8}{3}(-2s^2 - 4sw + w^2)} - \frac{w^2}{4h} + h \tag{11}$$

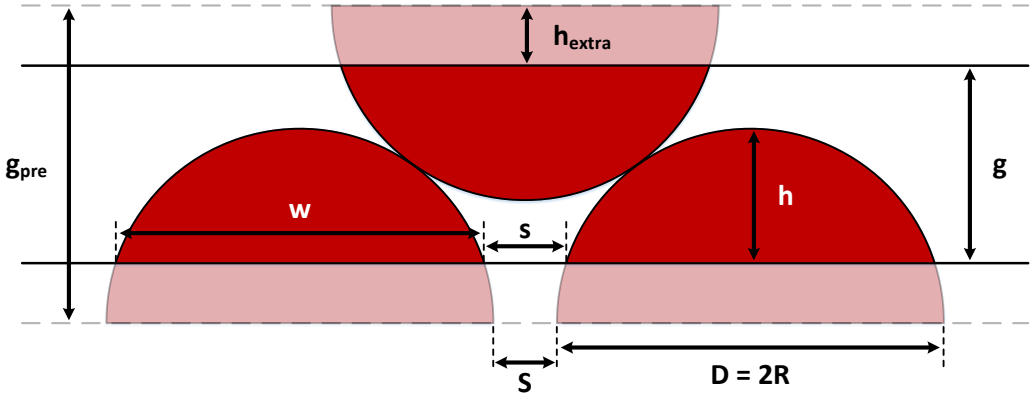


Figure 89. PSAS-to-PSAS self-alignment geometry for obtaining the inter-substrate gap of general PSAS geometries (including truncated hemisphere PSAS) from the more idealized relationship involving the inter-substrate gap of perfect hemisphere PSAS.

Equation (11) is the generalized equation for the inter-substrate gap for the 3-to-1 PSAS-to-PSAS configuration for both truncated and non-truncated PSAS hemispheres. Equation (11) simplifies to Equation (5) when the PSAS is a full hemisphere. Recall that these equations assume identical PSAS geometrical parameters (*h* and *w*) for both top and bottom mating substrates. Appendix A.2 contains MATLAB code for this generalized inter-substrate gap relationship (for both truncated and non-truncated PSAS hemispheres).

Figure 90, Figure 91, and Figure 92 illustrate the predicted inter-substrate gap as a function of lateral PSAS spacing for a 3-to-1 PSAS-to-PSAS configuration for different scenarios:

1) Figure 90 illustrates the inter-substrate gap as a function of lateral PSAS spacing for four different PSAS, each assumed to be perfect hemispheres (*h* = *w/2*). The minimum gap

curve is also plotted in Figure 90. The minimum gap for any PSAS-to-PSAS alignment configuration is equal to the PSAS height. For example, if the mating dice are completely misaligned, the top die will sit on top the bottom die, separated only by the PSAS themselves. At that point, the inter-substrate gap is equal to the PSAS height.

2) Figure 91 illustrates the inter-substrate gap as a function of lateral PSAS spacing when the PSAS height is fixed but the PSAS width varies. Specifically, for this illustration, the PSAS height is fixed at 30 μm and four different PSAS widths are examined. The minimum gap here for each PSAS pair is equal to 30 μm.

3) Figure 92 illustrates the inter-substrate gap as a function of lateral PSAS spacing when the PSAS width is fixed but the PSAS height varies. Specifically, for this illustration, the PSAS width is fixed at 120 μm and four different PSAS heights are examined. The minimum gap curve is also plotted in Figure 92.

The ability to control this inter-substrate gap is critical in general. For optical coupling for example, minimizing this inter-substrate gap is desired for maximizing the optical coupling efficiency [173]. Additionally, when compliant interconnects are used (such as MFIs or CMIs), the height of the interconnect in addition to the amount of deformation desired for said interconnect are important parameters when determining the inter-substrate gap. A gap smaller than the interconnect height is needed for the interconnect to mate with its corresponding mating pad. Additionally, it may be desirable to avoid a very small gap (e.g., much smaller than the interconnect height) as the induced stress within the interconnect may lead the interconnect to experience excessive plastic deformation, fracture, and/or

delamination. The PSAS-to-PSAS self-alignment mechanism is used in conjunction with CMIs in CHAPTER 6 where these considerations are taken into account.

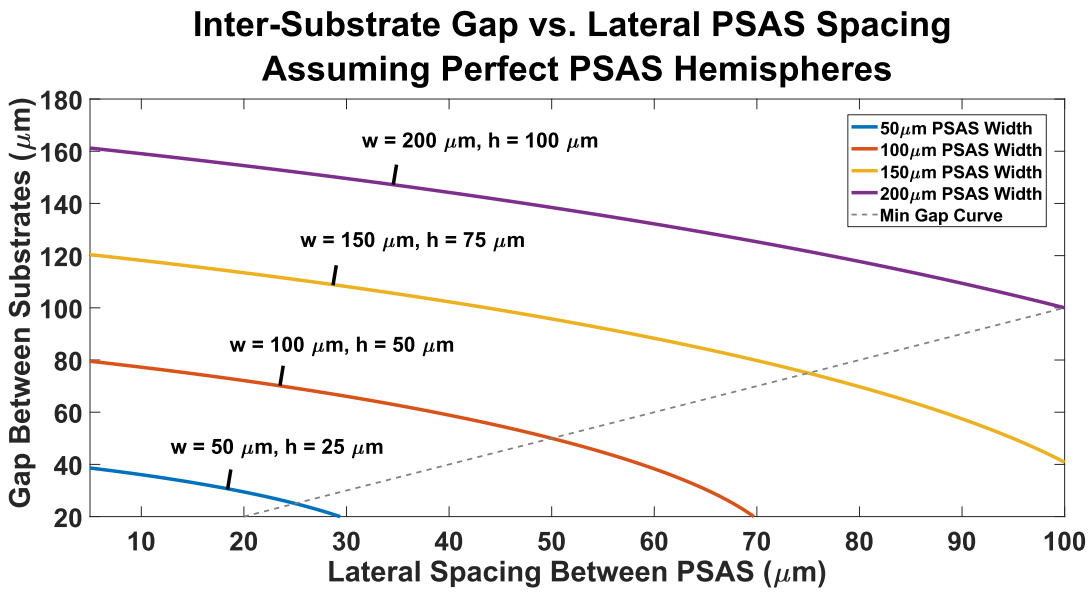


Figure 90. Graph of inter-substrate gap as a function of lateral PSAS spacing for a 3-to-1 PSAS-to-PSAS configuration involving four different PSAS, each assumed to be perfect hemispheres. The radius of these PSAS = 50 µm, 100 µm, 150 µm, 200 µm. The minimum gap curve is also plotted.

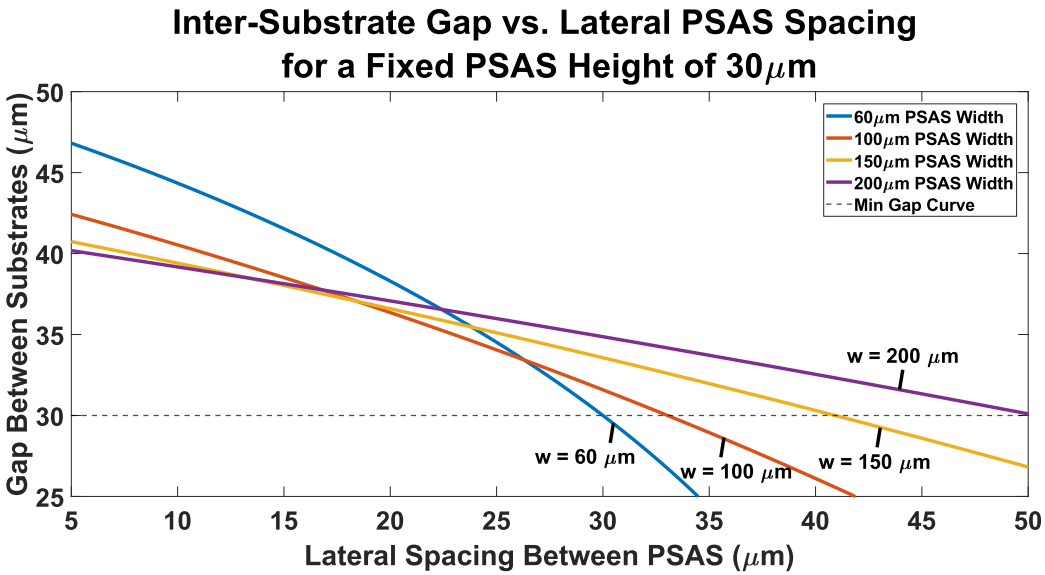


Figure 91. Graph of inter-substrate gap as a function of lateral PSAS spacing for a 3-to-1 PSAS-to-PSAS configuration involving four different PSAS each with height = 30 µm and widths = 60 µm, 100 µm, 150 µm, 200 µm. The minimum gap allowable is equal to the height of the all the PSAS = 30 µm.

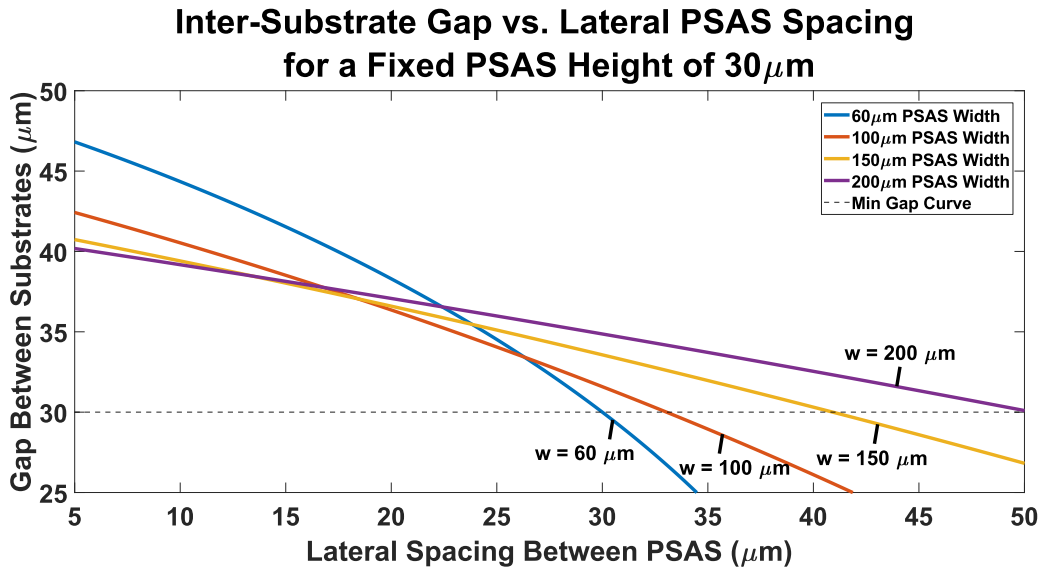


Figure 92. Graph of inter-substrate gap as a function of lateral PSAS spacing for a 3-to-1 PSAS-to-PSAS configuration involving four different PSAS each with width = 120 µm and heights = 30 µm, 40 µm, 50 µm, 60 µm. The minimum gap curve is also plotted.

5.3 Fabrication Process

Two separate wafers, as seen in Figure 93, were fabricated where one wafer contained Vernier scale patterns and one PSAS sets (termed the 1-PSAS wafer or the 1-PSAS die), and the other wafer contained complementary Vernier scale patterns and three PSAS sets that complement the one PSAS sets of the 1-PSAS wafer (termed the 3-PSAS wafer or the 3-PSAS die). The Vernier scales, as seen in Figure 94, are fabricated first on a cleaned glass wafer via a lift-off process where Ti/Cu/Au (20nm/300nm/100nm) are evaporated onto the patterned wafer, which is then placed into an acetone bath for lift-off. The resolution of these designed Vernier scale patterns is 1 μm. As a note, glass wafers are used as substrates during the fabrication process to demonstrate that silicon wafers are not needed for the PSAS-to-PSAS self-alignment mechanism to operate (unlike the case for PSAS-in-Pits and Ball-in-Pit self-alignment technologies). Additionally, glass wafers ease the process of alignment measurement characterization.

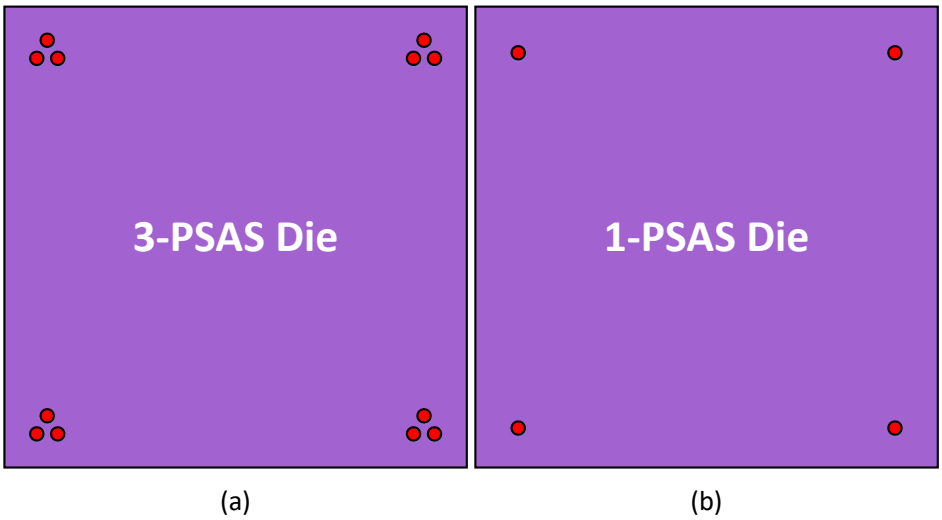


Figure 93. (a) 3-PSAS die from the 3-PSAS wafer showing 4 sets of 3-PSAS, 1 set at each die corner and (b) 1-PSAS die from the 1-PSAS wafer showing 4 sets of 1-PSAS, 1 set at each die corner. For simplicity, the Vernier scale patterns are not shown.

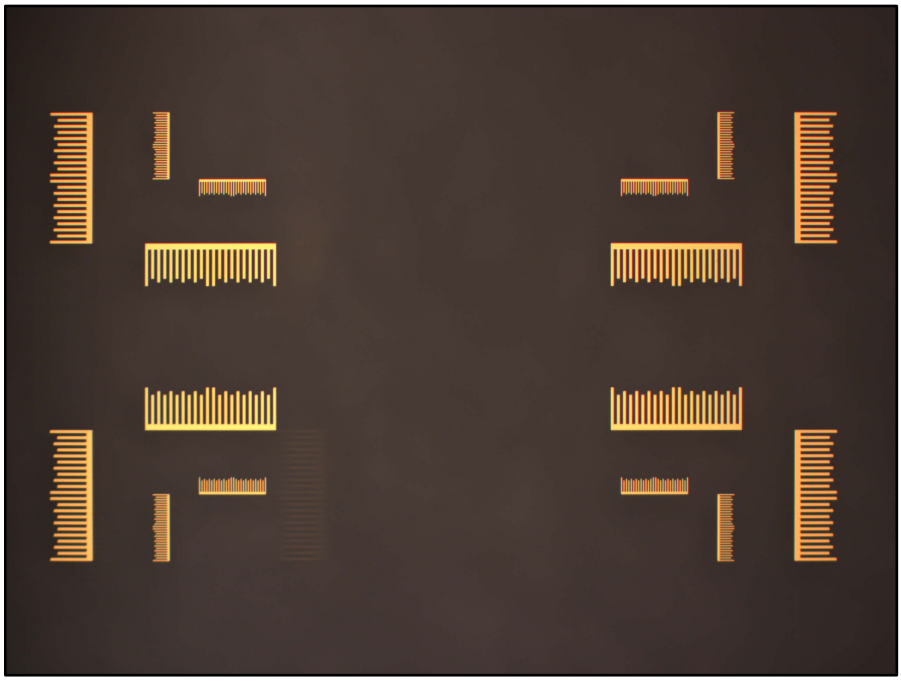


Figure 94. Optical image of fabricated Vernier scales used for alignment measurement characterization. The resolution of these Vernier scales is 1 µm.

After the lift-off process is completed, both the 1-PSAS wafer and the 3-PSAS wafer undergo a thick photoresist patterning (≈27 µm thick AZ40XT) followed by a reflow process at a temperature above the glass transition temperature (T_g) of the patterned photoresist (≈126°C for 3.5 minutes). A 1-PSAS wafer 1 PSAS set and a 3-PSAS wafer 3-PSAS set are shown in Figure 95. These PSAS both have the same width and height dimensions (width ≈ 80 µm, height ≈ 40 µm). The 3-PSAS sets have a lateral PSAS spacing of ≈ 20 µm. Each die of both wafers contains their respective PSAS sets at each corner of the die as illustrated in Figure 93. For example, the 1-PSAS die contains 4 PSAS with 1 PSAS located at each of the 4 corners. The targeted inter-substrate gap as calculated by Equation (11) for this specific PSAS-to-PSAS 3-to-1 self-alignment configuration is approximately 55 µm.

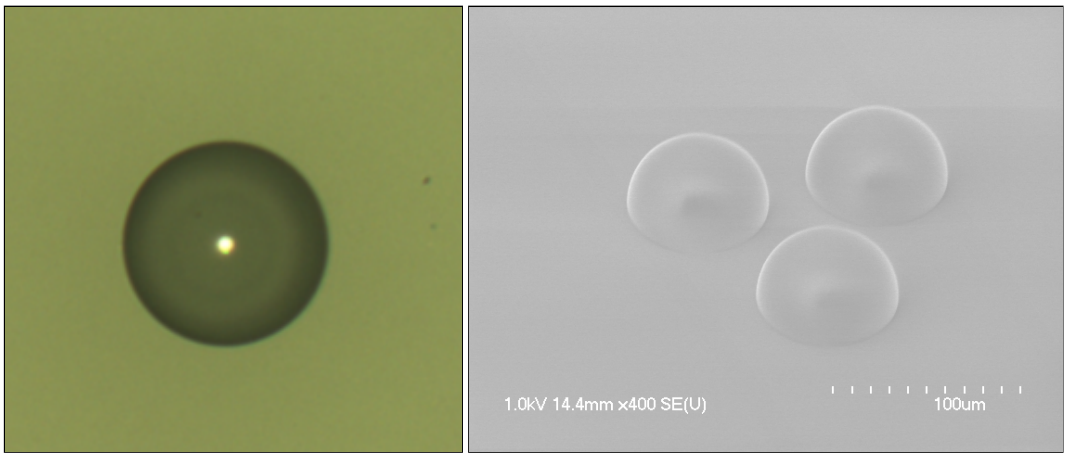


Figure 95. (a) An optical image of a single PSAS "set" on the 1-PSAS wafer and (b) an SEM image of a three PSAS set on the 3-PSAS wafer. These PSAS both have the same width and height dimensions (width ≈ 80 µm, height ≈ 40 µm). The lateral PSAS spacing is ≈ 20 µm.

5.4 Assembly and Alignment Accuracy Measurements

5.4.1 Assembly

The 1-PSAS die is manually aligned via the aid of an optical microscope to the sitting 3-PSAS die. The 3-PSAS sets are used as visual indicators of alignment accuracy during the manual alignment process. When the PSAS from the 1-PSAS die are visually within the alignment tolerance region of the corresponding 3-PSAS sets (as illustrated in Figure 96), the 1-PSAS die is gently dropped and self-alignment occurs as seen in Figure 97. This misalignment tolerance region is equal to an equilateral triangle with sides of length 100 µm (equal to PSAS width of 80 µm + lateral PSAS spacing of 20 µm).

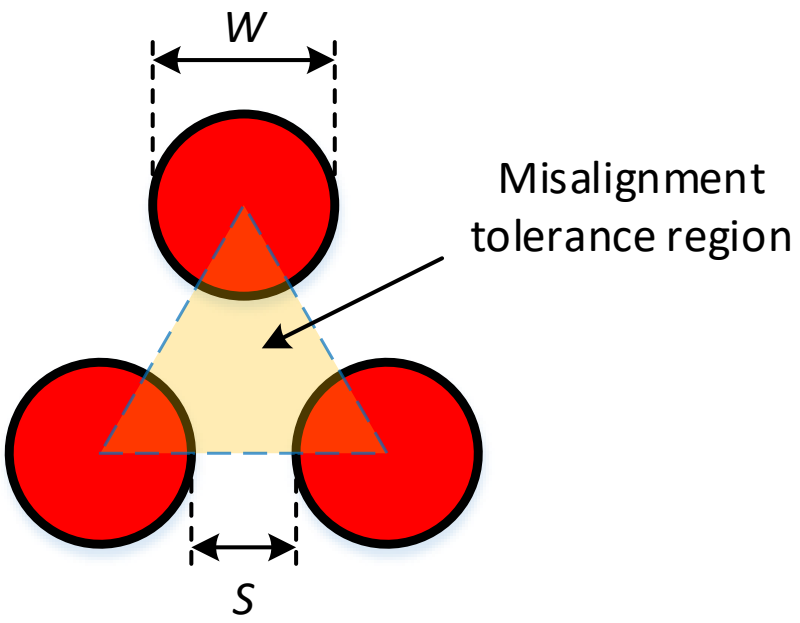


Figure 96. The misalignment tolerance region for the 3-to-1 PSAS-to-PSAS configuration, where *w* = PSAS width and *s* = lateral PSAS spacing.

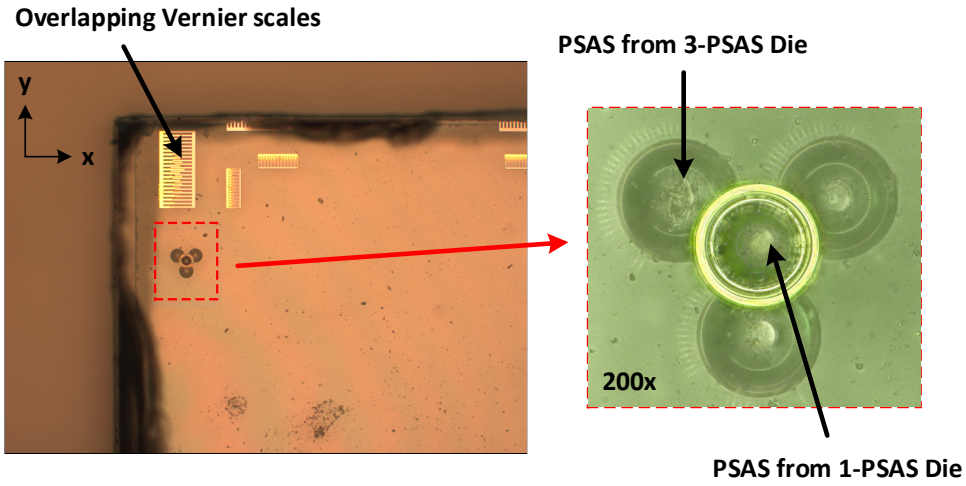


Figure 97. Optical image after the manual assembly of the 1-PSAS die onto the 3-PSAS die. Self-alignment is achieved as illustrated both by the complementary Vernier scales and the centering of the 1-PSAS from the 1-PSAS die within the 3-PSAS from the 3-PSAS die. As a note, both dice are glass and hence optically transparent.

5.4.2 Alignment and Alignment Repeatability Measurements

After both dice are assembled as seen in Figure 97, the alignment accuracy between the two dice are measured via examining the overlapping Vernier scale patterns using an optical microscope. Each corner of both dice contains complementary Vernier scale patterns (for both x- and y-directions, which are defined in Figure 97) and hence eight alignment measurements are performed, two for each corner of the mating dice (x- and y-alignment), as seen in Figure 98.

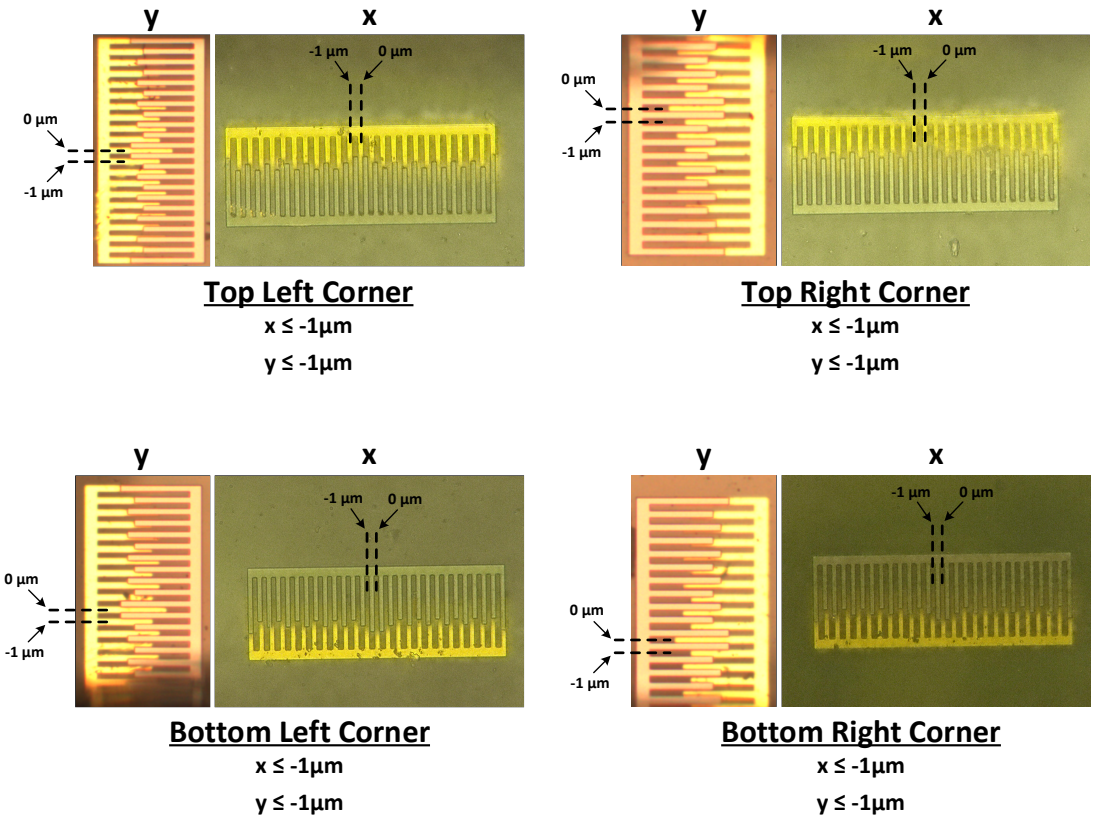


Figure 98. Overlapping Vernier scale patterns for each corner of the mating dice for both x- and y-directions.

For each corner of the die in Figure 98, submicron misalignment is measured for both the x- and y-directions. Alignment measurements were performed for a total of three mating die pairs from which the average is also computed (including the one in Figure 98); these measurements are reported in Table 12.

Table 12. Average alignment across three mating die pairs using the 3-to-1 PSAS-to-PSAS alignment configuration

Sample	Top Left (μm)		Bottom Left (μm)		Top Right (μm)		Bottom Right (μm)	
	x	***y***	***x***	***y***	***x***	***y***	***x***	***y***
1	<1	<1	<1	<1	<1	<1	<1	<1
2	<1	<1	<1	<1	<1	<1	<1	<1
3	<1	<1	<1	<1	<1	<1	<1	<1
Average	<1	<1	<1	<1	<1	<1	<1	<1

Each die demonstrates misalignment of less than 1 μm (where 1 μm is the resolution of the patterned Vernier scales). Recall that the misalignment tolerance region, as illustrated in Figure 96, is equal to an equilateral triangle with sides of length equal to 100 μm.

Since repeated use of one or both of the dice may be needed for certain applications (e.g., testing, replaceability), multiple manually placed assemblies were performed to test self-alignment repeatability. The results of these tests are shown in Table 13. Data recorded in Table 13 is with respect to any differences in alignment observed relative to the initial alignment measurement. As shown, 50 different manually placed assemblies are performed where the top substrate (1-PSAS die) is removed and then re-assembled onto the bottom substrate (3-PSAS die). Little difference is observed between each self-alignment measurement, which demonstrates that the self-alignment accuracy is consistent after repeated use.

Table 13. Self-alignment repeatability measurements up to 50 manual assemblies for a 3-to-1 PSAS-to-PSAS alignment configuration. Relative alignment differences are recorded with respect to the initial alignment measurement.

Assembly Count	Top Left (μm)		Bottom Left (μm)		Top Right (μm)		Bottom Right (μm)	
	Δx	***Δy***	***Δx***	***Δy***	***Δx***	***Δy***	***Δx***	***Δy***
5	≤1	≤1	≤1	≤1	≤1	≤1	≤1	≤1
10	≤1	≤1	≤1	≤1	≤1	≤1	≤1	≤1
20	≤2	≤1	≤1	≤1	≤2	≤2	≤1	≤2
50	≤1	≤1	≤1	≤1	≤1	≤1	≤1	≤1

5.5 Conclusion

A novel mechanically-based self-alignment technology was introduced in this chapter where PSAS on one substrate self-aligned to other PSAS on another substrate; this technology is hence termed PSAS-to-PSAS self-alignment. The mathematical relationship between the inter-substrate gap and the PSAS dimensions (width, height, and lateral spacing) for a 3-to-1 PSAS-to-PSAS self-alignment configuration was derived. To verify the alignment accuracy of this PSAS-to-PSAS technology, two sets of wafers were fabricated (one containing 1-PSAS sets and the other containing 3-PSAS sets). Alignment measurements were then performed after manual assembly, which demonstrated sub-micron alignment across all three pairs of dices characterized. Alignment repeatability measurements were also performed, demonstrating consistent alignment accuracy throughout 50 repeated manual assemblies.

CHAPTER 6. REPLACEABLE INTEGRATED CHIPLET ASSEMBLY USING COMPRESSIBLE MICROINTERCONNECTS AND PSAS-TO-PSAS FOR HETEROGENEOUS INTEGRATION

6.1 Introduction

A re**P**laceable, **IN**tegrated **CH**iplet assembly (PINCH) using Compressible MicroInterconnects (CMIs) as the non-permanent interconnection system and PSAS-to-PSAS as the self-alignment technology, as seen in Figure 99, is introduced in this chapter for use in heterogeneous integrated applications. Such a heterogeneous integrated approach can be of benefit to a wide variety of applications including mm-wave systems as this heterogeneity can aid to optimize system performance. As aforementioned in CHAPTER 1, certain material substrates are better suited to perform optimally versus other material substrates: GaN for power amplifiers to achieve higher power densities [10], GaAs pHEMTs for LNAs that require low noise figures (NFs) and a wide broadband performance [12], fused silica to provide a low-loss dielectric substrate for mm-wave applications including 5G [13], and InP photodiodes for high-performance DP-QPSK receivers [14].

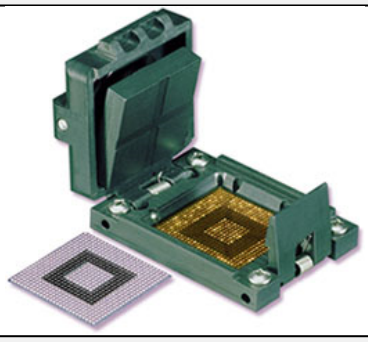
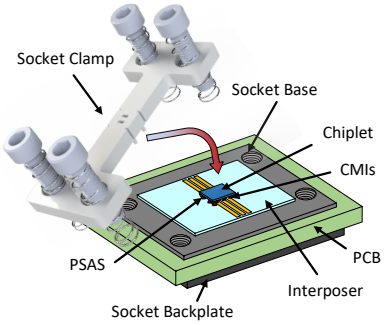
Socket Characteristics	Conventional IC Socket	PINCH Assembly
		
I/O Pitch	Down to 200 µm	Down to 20 µm ✓
Misalignment	> 100 µm	< 1 µm ✓
DC Resistance	< 300 mΩ	< 50 mΩ ✓
Insertion Loss	-1dB @ 9.9 GHz	-0.22dB @ 40 GHz ✓
Return Loss	-20dB @ 2.48 GHz	-20dB @ 23 GHz ✓
Loop Inductance	1.11 nH	0.106 nH ✓
Capacitance	0.17 pF	0.017 pF ✓
Device Under Test	Package	Die/Chiplet ✓

Figure 99. Comparison between a conventional IC socket [174] used for package testing and the PINCH assembly introduced in this chapter. The RF characteristics are from the CMIs employed by the PINCH assembly [175].

However, if a non-permanent setup is required (for replaceability, testing, prototyping, upgradeability, etc.), challenges arise in implementing the appropriate set of enabling technologies to achieve such a setup. This chapter implements the use of a non-permanent interconnection system via CMIs and a non-permanent self-alignment technology via PSAS-to-PSAS. As discussed in CHAPTER 5, one of the primary advantages of the PSAS-to-PSAS technology is that it is substrate agnostic as any substrate material may be used. For the case of heterogeneously integrated systems, which may incorporate a wide variety

of material substrates as aforementioned (GaN, GaAs, fused silica, InP, etc.), the PSAS-to-PSAS self-alignment technology can prove very valuable as it does not require any specific substrates involved as is the case for both the PSAS-in-Pits and Ball-in-Pit technologies. These latter technologies may therefore not prove suitable for this specific application (i.e., non-permanently integrated heterogeneous systems).

Additionally, the PINCH assembly is particularly important as chiplets become key to building ever complex systems. The PINCH assembly provides a means to testing or characterizing such systems in much the same way as conventional socket ICs test or characterize larger-pitch packages; however, the latter technology does not have the enabling technologies to interface with fine-pitch systems yet the PINCH assembly does as seen in Figure 99. The PINCH assembly also can address SiP yield challenges as was discussed in CHAPTER 1.

This chapter demonstrates: 1) the design considerations behind building a PINCH system, 2) design and manufacturing of the PINCH socket, 3) the micro-fabrication process flow for all the components of the PINCH system (e.g., interposer, chiplet), 4) four-point electrical resistance measurements of the CMIs within the PINCH system (when the socket has been secured), and 5) a discussion on assembly challenges and the corresponding future work involved.

6.2 PINCH System Overview

As seen in Figure 100, the PINCH system is composed of: an interposer, a chiplet of any material substrate (or set of chiplets), the socket, and a PCB. The glass interposer contains CMIs and 3-PSAS sets. The chiplet contains 1-PSAS sets that complement the 3-PSAS

sets on the interposer. The chiplet self-aligns to the interposer via the PSAS-to-PSAS technology as detailed in CHAPTER 5. If need be, the interposer can be wire bonded to the PCB. After the chiplet is self-aligned to the interposer, the socket clamp is inserted into its base so that the interposer CMIs can electrically connect to the mating chiplet (or chiplets).

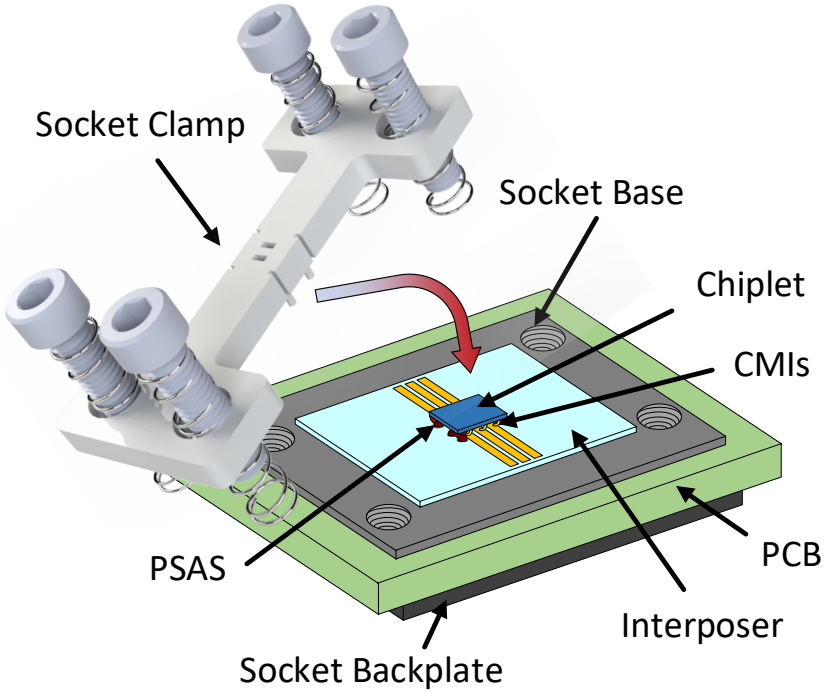


Figure 100. Overview of the re**P**laceable, **IN**tegrated **CH**iplet (PINCH) assembly.

For the specific PINCH system design fabricated and tested throughout this chapter, the geometrical parameters and their designed values are listed in Table 14. As a note, for the purposes of demonstration and yield, the CMIs were fabricated on the chiplet as the chiplets were smaller, which results in a great number of dice per wafer as opposed to the case of

the interposer wafer. This fabrication process will be discussed in more detail in Section 6.4. However, as aforementioned, the PINCH system, in theory, intentionally incorporates the CMIs on the interposer as the interposer may be freely designed and batch fabricated whereas the chiplets may be commercially available off-the-shelf (COTS) components in which we wish to impose minimal post-fabrication processes (for purposes of simplicity, cost reduction, time, and to minimize any potential damage to these COTS components as a result of the post-fabrication processes).

Table 14. The PINCH system geometric parameters and their corresponding designed values for the fabricated and assembled PINCH system

PINCH System Geometric Parameters	
CMI Height	40 μm
CMI Pitch	150/200 μm
Chiplet 1-PSAS Height	27 μm
Chiplet 1-PSAS Width	60 μm
Interposer 3-PSAS Height	27 μm
Interposer 3-PSAS Width	60 μm
Interposer 3-PSAS Lateral Spacing	19 μm
Targeted Inter-Substrate Gap	33.2 μm

6.3 PINCH System Design

6.3.1 Self-Alignment Engineering

In choosing the targeted inter-substrate gap, G_t, the PSAS geometric variations across the processing wafer are taken into account as seen in Figure 101, where:

$G_t\,(w, h, s)$ is the targeted inter-substrate gap with PSAS width, *w*, PSAS height, *h*, and PSAS lateral spacing, *s*.

G_{Max} is the maximum inter-substrate gap allowable.

G_{Min} is the minimum inter-substrate gap allowable.

$$\Delta G_{tU} = G_t\left(w + \frac{\Delta w}{2}, h + \frac{\Delta h}{2}, s - \frac{\Delta w}{2}\right) - G_t\,(w, h, s) \tag{12}$$

where:

ΔG_{tU} = The max increase in the inter-substrate gap due to the corresponding worst-case scenario PSAS variations

Δw = PSAS width total fabrication variation, centered on *w*

Δh = PSAS height total fabrication variation, centered on *h*

$$\Delta G_{tL} = G_t\,(w, h, s) - G_t\left(w - \frac{\Delta w}{2}, h - \frac{\Delta h}{2}, s + \frac{\Delta w}{2}\right) \tag{13}$$

where:

ΔG_{tL} = The max decrease in the inter-substrate gap due to the corresponding worst-case scenario PSAS variations

Note that there is no "PSAS lateral spacing variation" variable (Δs) in Equations (12) and (13) as $\Delta s = -\Delta w$. The equations and definitions seen in Figure 101 assume that all PSAS

have the same height and width. Therefore, if the PSAS width increases by a set amount, the lateral PSAS spacing decreases by this same set amount.

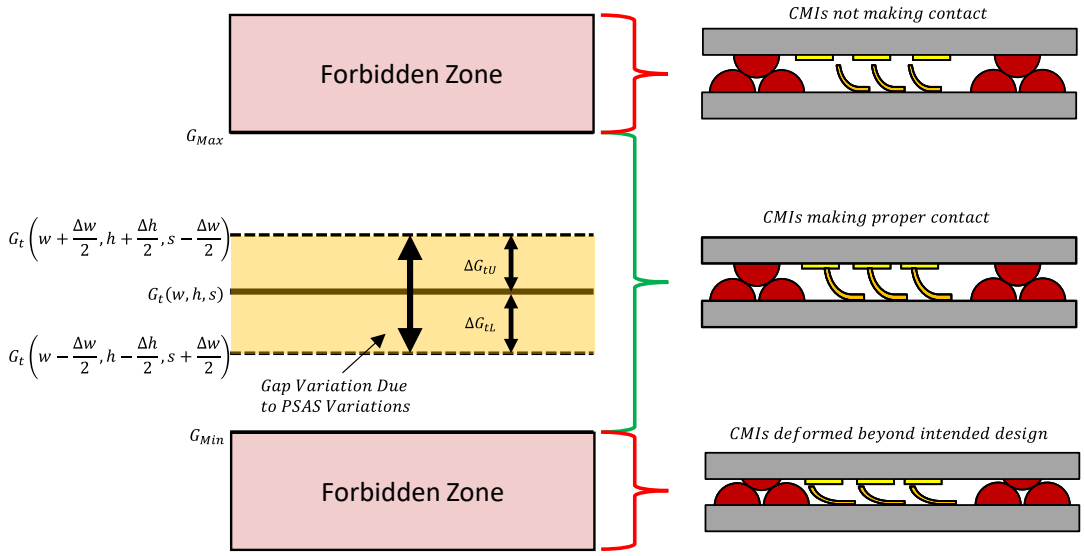


Figure 101. Variations in the inter-substrate gap relative to the targeted gap due to PSAS geometry fabrication variations. So long as this inter-substrate gap variation stays within the maximum allowed gap and the minimum allowed gap, the corresponding targeted inter-substrate gap is within tolerance.

The targeted inter-substrate gap must be selected such that:

$$G_t\,(w,h,s) + \Delta G_{tU} \leq G_{Max}$$

$$G_t\,(w,h,s) - \Delta G_{tL} \geq G_{Min}$$

or

$$G_{Min} + \Delta G_{tL} \leq G_t\,(w,h,s) \leq G_{Max} - \Delta G_{tU} \tag{14}$$

To apply the equations and definitions from Equations (12)-(14), it is first observed that, as seen in Table 14, that the designed CMI height is 40 μm. Therefore, the inter-substrate gap must be less than 40 μm so that the CMIs can come into contact with their respective mating pads; hence G_{Max} = 39 μm (a 1 μm buffer is provided). With regards to G_{Min} in general, the inter-substrate gap cannot be too small (e.g., g << 40 μm) as the needed pressure to force such a gap may lead the CMIs to experience excessive plastic deformation, fracture, and/or delamination (also, if the pressure is too excessive, it may also fracture or crack the chiplet/interposer). However, in this specific case with both a CMI pitch of 150 μm and 200 μm, as seen in Table 14, the CMIs do not experience plastic deformation (let alone fracture, etc.) even when deformed fully (40 μm). Hence, the main limiter for the minimum gap in this specific case is not the CMI but the PSAS height, which is equal to 27 μm. Therefore, G_{Min} = 28 μm (a 1 μm buffer is provided).

In regard to PSAS geometric variations, we first begin with the PSAS height variations across a 4-inch wafer. This variation is approximately ±1.1%, as seen in Table 15. For a targeted 27 μm height PSAS (which is the targeted PSAS height in this case as seen in Table 14), a ±1.1% PSAS height variation translates to a variation in the PSAS height from ≈26.7 μm to ≈ 27.3 μm. Therefore, $\Delta h \approx 0.6\mu m$.

Table 15. PSAS height variation across two separate wafers with two different targeted PSAS heights. PSAS heights were measured via a contact profilometer.

Wafer Portion	**PSAS Height (µm)**	
	Wafer 1	*Wafer 2*
Top Left (Average)	24.7	40.7
Top Right (Average)	24.9	40.4
Bottom Left (Average)	24.9	40.3
Bottom Right (Average)	24.4	39.8
Whole Wafer (Average)	24.7	40.3
PSAS Height Variation (relative to whole wafer average)	±1.0%	±1.1%

In regard to the PSAS width variations across a 4-inch wafer in the vicinity of the targeted PSAS width of 60 µm, this variation is approximately ±2.6%, as seen in Table 16. For a targeted 60 µm width PSAS (which is the targeted PSAS width in this case as seen in Table 14), a ±2.6% PSAS width variation translates to a variation in the PSAS width from ≈58.4 µm to ≈ 61.6 µm. Therefore, $\Delta w \approx 3.2$µm.

Table 16. PSAS width variation across two separate wafers. PSAS widths were measured under an optical microscope.

Wafer Portion	**PSAS Width (µm)**	
	Wafer 1	*Wafer 2*
Top Left (Average)	59.2	58.7
Top Right (Average)	58.5	60.4
Bottom Left (Average)	61.5	59.5
Bottom Right (Average)	60.9	61.8
Whole Wafer (Average)	60.0	60.1
PSAS Width Variation (relative to whole wafer average)	±2.5%	±2.6%

Hence, for this specific demonstration, we have:

$$G_{Max} = 39\ \mu m$$

$$G_{Min} = 28\ \mu m$$

$$\Delta h = 0.6\ \mu m$$

$$\Delta w = 3.2\ \mu m$$

If we evaluate Equation (11) from CHAPTER 5 with $g\left(w + \frac{\Delta w}{2}, h + \frac{\Delta h}{2}, s - \frac{\Delta w}{2}\right)$ for $G_{t(w,h,s)} + \Delta G_{tU}$ and $g\left(w - \frac{\Delta w}{2}, h - \frac{\Delta h}{2}, s + \frac{\Delta w}{2}\right)$ for $G_{t(w,h,s)} - \Delta G_{tL}$ with w, h, and s from Table 14, we obtain:

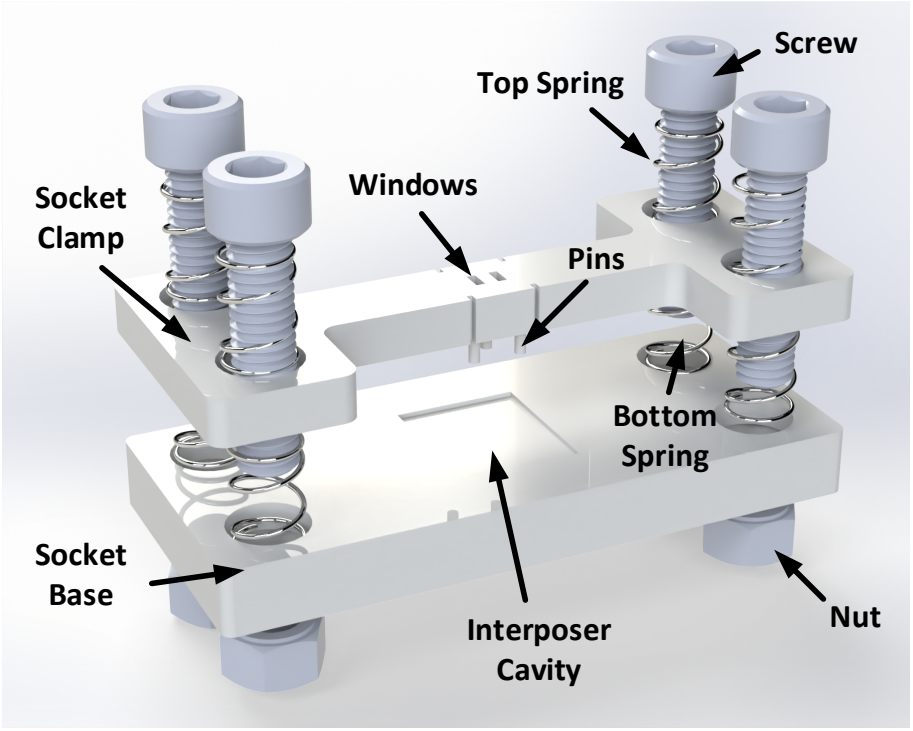
$$G_{t(w,h,s)} + \Delta G_{tU} = 34.6\ \mu m$$

$$G_{t(w,h,s)} - \Delta G_{tL} = 31.6\ \mu m$$

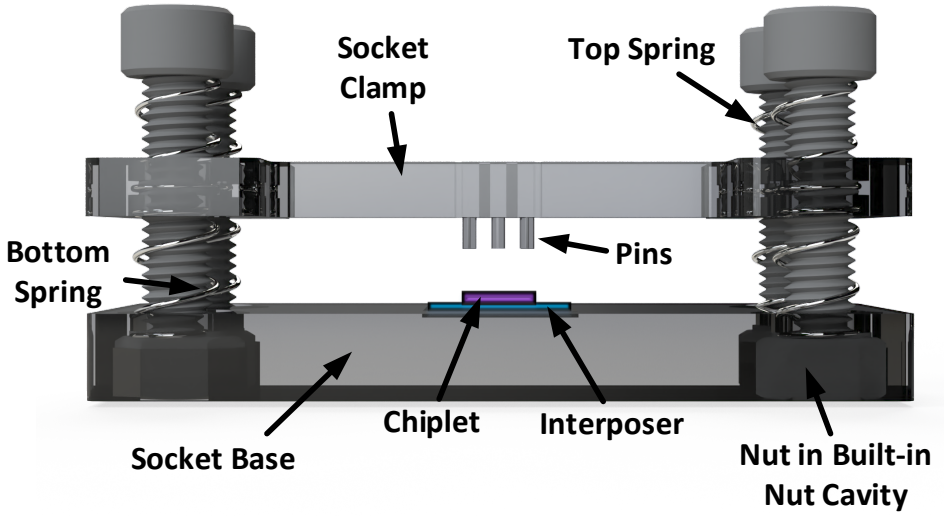
Therefore, the inter-substrate gap (with the designed PSAS geometry values listed in Table 14 and with the observed variation of the PSAS geometry values) varies from 31.6 µm to 34.6 µm, with the targeted inter-substrate gap being 33.2 µm (as also seen in Table 14). This inter-substrate gap variation falls between G_{Min} (28 µm)and G_{Max} (39 µm) and hence, the targeted inter-substrate gap of 33.2 µm is well within tolerance.

As a note, some design flexibility exists with regards to targeting an acceptable inter-substrate gap even after the initiation of the fabrication process. For instance, as will be discussed in Section 6.4.1, the CMIs are fabricated prior to the PSAS on the same wafer. Hence, if the measured height of the fabricated CMI is taller or shorter than expected, the targeted inter-substrate gap can be modified, which is achieved via modifying the PSAS-to-PSAS geometric dimensions (e.g., *w*, *h*, *s*).

There also exists variation in the CMI height (≈±5%). For a 40 µm tall CMI, the CMI height varies across a 4-inch wafer from ≈38 µm to ≈42 µm. In this specific demonstration, this alters G_{Max} to 37 µm (a 1 µm buffer is provided). G_{Min} is unchanged. Even when considering the CMI height variation, the targeted inter-substrate gap range (centered on 33.2 µm) is within tolerance.



(a)



(b)

Figure 102. Socket design used in the PINCH system: (a) Exploded view drawing and (b) side view after assembly with chiplet and interposer. The corner screws are inserted into the socket base to move down the socket clamp until the pins of the socket clamp make contact with the chiplet, providing force to the chiplet and hence the CMIs. CMIs and PSAS are not shown for simplicity.

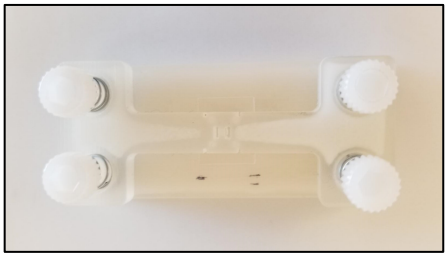
6.3.2 Socket Design, Operation, and Manufacturing

The socket design used for the PINCH system designed in this chapter is seen in Figure 102. The socket consists of several components: a socket clamp, pins protruding from the socket clamp, a socket base, several threaded holes for screws, and several built-in nut cavities in the socket base for the purposes of preserving the threaded-assisted motion of the screws (the socket is 3D printed, as will be discussed shortly, and hence the resolution and mechanical integrity of the threads may not be sufficient during the screw insertion and removal process). The pins on the socket clamp attempt to provide a uniform load distribution onto the underlying chiplet.

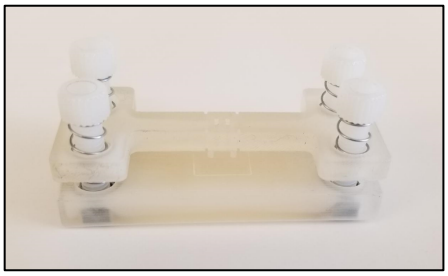
The socket base contains a cavity for the interposer to sit. As seen in Figure 102(b), after the chiplet is self-aligned to the interposer via PSAS-to-PSAS (while the interposer sits in the interposer cavity of the socket base), the socket clamp is clamped onto the socket base via securing the screws through both the clamp and the base at all four corners. Once the socket clamp is secured onto the socket base, the four screws at the corners may be further screwed into the base, which brings the socket clamp and hence the pins closer to the socket base. This motion downward continues until the pins of the socket clamp contacts the chiplet where it provides the needed pressure required by the CMIs to create and maintain a sufficient electrical connection, as illustrated in Figure 102(b). Also, note that the socket in Figure 102 contains “windows.” These “windows” are present for debugging purposes as it enables us to visually observe both the PSAS-to-PSAS alignment and the CMIs in contact with their respective mating pads after the socket clamp has been inserted.

The screws at the corners which secure the socket clamp onto the socket base are M5 x 0.8 mm screws. The embedded nuts within the socket base correspond to these specific screw dimensions.

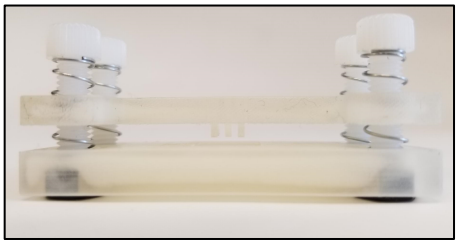
The socket was 3D printed using a Projet 3510 HD 3D printer at Ultra-High Definition (layer heights of 29 μm). The assembled socket (without chiplet and interposer) is seen in Figure 103.



(a)



(b)



(c)

Figure 103. 3D printed socket used for the PINCH system: a) overhead view, b) bird eye's view, and c) side view.

6.4 Microfabrication Process

Two different dice were fabricated for the PINCH system: 1) the chiplet and 2) the interposer. The process flows for each die will be described below.

6.4.1 Chiplet Fabrication Process Flow

Figure 104 illustrates the PINCH-system chiplet fabrication process flow. Fused quartz (glass) wafers were initially cleaned with a thorough AMI step. As the wafers are fused quartz, no passivation film is needed for electrical isolation purposes. CMIs are then fabricated onto the wafer as described in [118]. These CMI fabrication steps will be discussed here with perhaps slight modifications (e.g., descum process times). Recall that the PINCH-system, in theory, has the CMIs on the interposer; however, for purposes of demonstration and yield (as the chiplet dice are smaller than the interposer dice), CMIs are fabricated on the chiplet in this chapter. As a note, both 150 μm pitch and 200 μm pitch CMIs were fabricated on the chiplet wafer simultaneously.

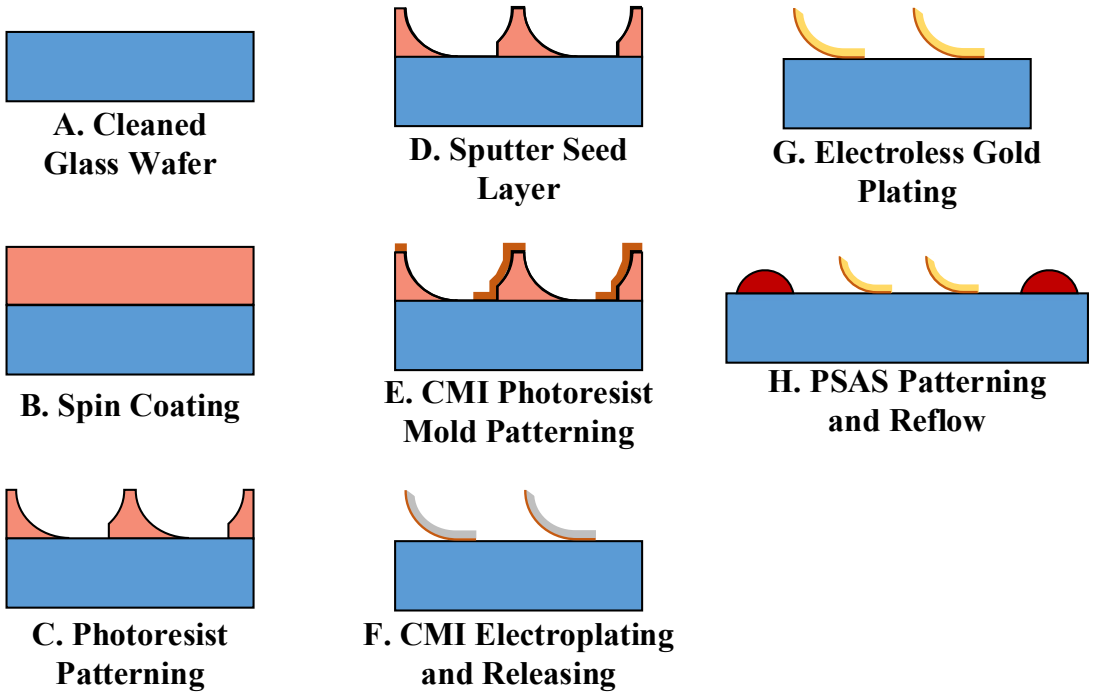


Figure 104. Fabrication process flow of the PINCH-system chiplet with CMIs and PSAS.

A thick photoresist (AZ40XT) is spin coated and patterned onto the glass wafer after the initial AMI cleaning process. This patterning results in a concave-shaped sidewall profile as seen in Step C of Figure 104. Afterwards, an electroplating seed layer is deposited. A 15 second descum process is initially performed. 30 nm Ti/500 nm Cu/30 nm Ti is then sputtered onto the patterned resist. As was the case for the MFIs, the top Ti layer is deposited to act as a lift-off layer to remove resist residue after development of the patterned CMI resist mold prior to electroplating (this step will be discussed in more detail shortly). Approximately 10 µm of AZ4620 is then spray coated onto the seed film-covered resist. The CMI mask is then patterned onto this resist.

After the removal of the top Ti layer (to remove any remaining resist residue after development), the CMIs are electroplated using a nickel sulfamate bath (Elevate Ni 5910

RTU from Technic). Sodium tungstate dihydrate and citric acid were added to this bath to provide a specific tungsten concentration that ultimately forms a NiW alloy electroplating solution. The bath was then heated to approximately 50°C prior to electroplating. The NiW deposition was then performed using pulsed current (PC) plating. The electroplated NiW thickness for the CMIs was measured to be approximately 5.5 μm.

After electroplating, the sample is washed thoroughly with DI water and then dried with a N_2 gun. The spray-coated photoresist (e.g., AZ4620 – a positive resist) is then flood exposed with UV light and then subsequently developed. BOE is then used to remove the top Ti layer. APS is used to remove the Cu layer. Then BOE is used again to remove the bottom Ti layer. The sample is then dipped into acetone to remove the thick patterned photoresist film. Finally, the CMIs are passivated via immersing the sample into an electroless gold plating solution such that all exposed CMI surfaces are coated with gold.

Finally, for the PSAS formation, another layer of thick photoresist (AZ40XT) is spin coated and patterned (the 1-PSAS mask is used here). This photoresist is then reflowed on a hot plate at 126°C for 3.5 minutes. The fabricated chiplet die (7mm x 7mm) with CMIs and PSAS is shown in Figure 105.

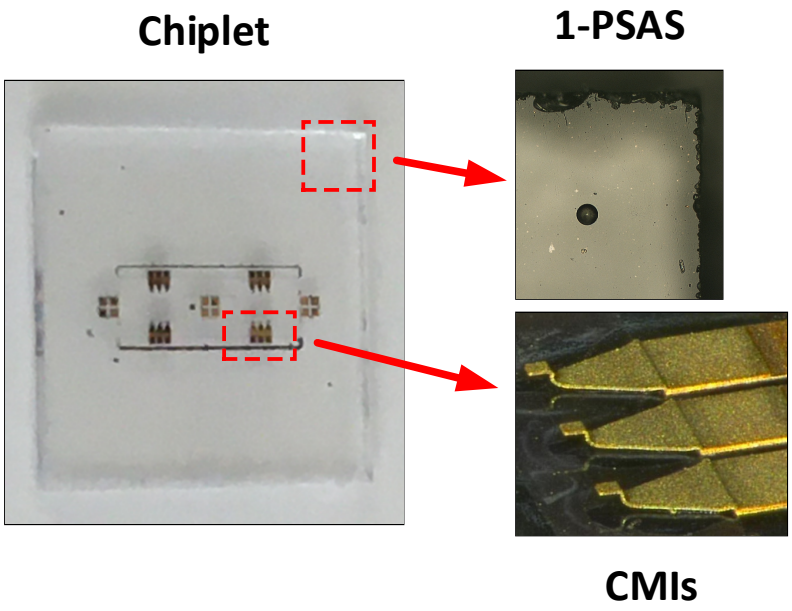


Figure 105. Fabricated chiplet die (7mm x 7mm) with both CMIs and 1-PSAS.

6.4.2 Interposer Fabrication Process Flow

Figure 106 illustrates the PINCH-system interposer fabrication process flow. Fused quartz (glass) wafers were initially cleaned with a thorough AMI step. For the lift-off step, SC1827 is spin coated and patterned. Prior to metallization, a 30 second descum is performed using an RIE process. E-beam evaporation is then used to deposit a 20 nm Ti adhesion layer, a 300 nm Cu layer, and a 100 nm Au layer. The sample is then placed into an acetone bath overnight for lift-off. Alternatively, a short ultra-sonic bath (e.g., few minutes) can be used to expedite the lift-off process.

After lift-off has been completed, the PSAS patterning and reflow process is implemented (same as in the case for the PINCH-system chiplet with the exception of the

3-PSAS mask being used in place of the 1-PSAS mask). The fabricated interposer die (12mm x 10mm; L x W) is shown in Figure 107.

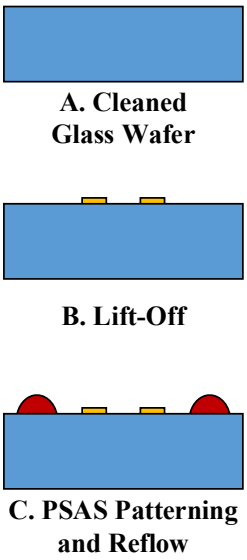


Figure 106. Fabrication process flow of the PINCH-system interposer.

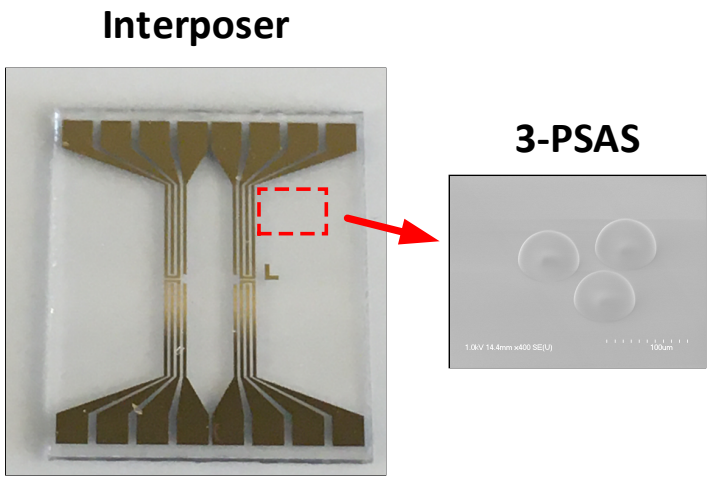


Figure 107. Fabricated interposer die (12mm x 10mm) with 3-PSAS.

6.5 Setup, Results, and Discussion

6.5.1 Assembly

The PINCH-system interposer is first placed within the interposer cavity of the socket base. The 1-PSAS on the PINCH-system chiplet is then manually aligned via the aid of an optical microscope to the 3-PSAS interposer. The 3-PSAS sets on the interposer are used as visual indicators of alignment accuracy during the manual alignment process. When the PSAS from the 1-PSAS chiplet are visually within the alignment tolerance region of the corresponding 3-PSAS sets (as illustrated in Figure 96), the 1-PSAS chiplet is gently dropped onto the 3-PSAS chiplet and self-alignment occurs.

After self-alignment between chiplet and interposer is completed, the socket clamp is secured to its base as described in Section 6.3.2. At this point, the four corner screws are inserted further into the socket base until the pins of the socket clamp come into contact with the underlying chiplet, which applies the needed pressure to the chiplet and hence the CMIs as also described in Section 6.3.2. Figure 108 shows the PINCH-system after assembly has been performed.

To ensure that the alignment does not change after the clamp socket is secured, the socket clamp "windows" as described in Section 6.3.2 and as seen in Figure 108 are used to visually observe both the PSAS-to-PSAS self-alignment, and the CMIs and their respective mating pads, as seen in Figure 109.

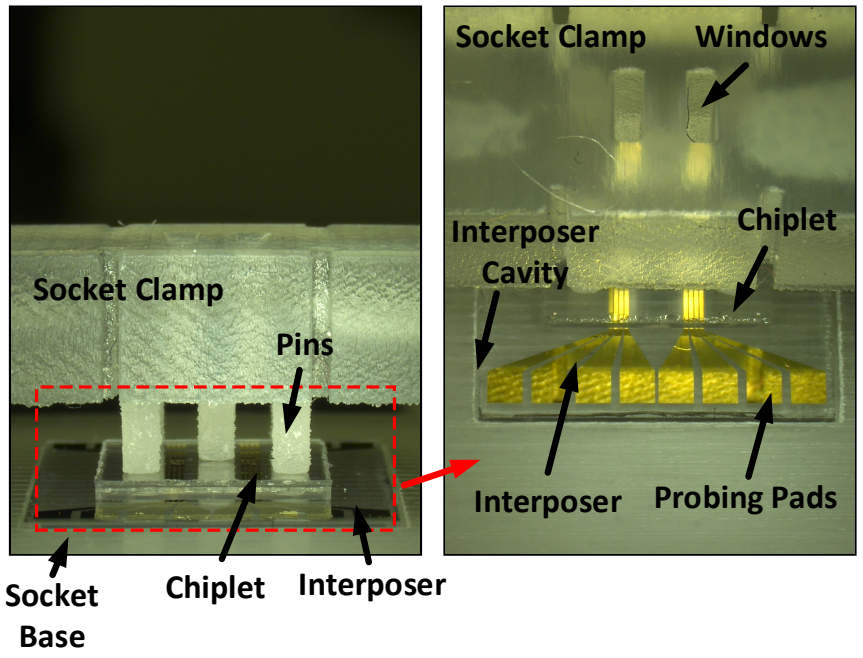


Figure 108. Optical side-view image of the PINCH-system after full assembly has been performed with the chiplet and interposer. The pins of the socket clamp come into contact with the underlyding chiplet to provide the needed pressure for the CMIs to create and mainatain electrical connections. These pins attempt to provide a uniform load across the chiplet.

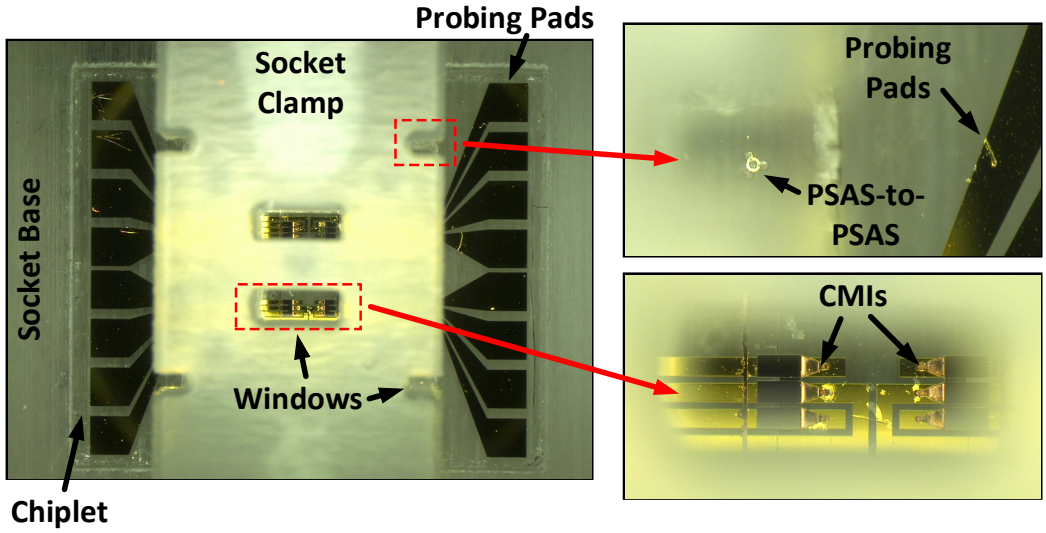


Figure 109. Optical image of the PINCH-system after full assembly has been performed. Windows within the socket clamp are used to visually observe both PSAS-to-PSAS, and CMIs and their respective mating pads to ensure that alignment is accurate and CMI contact is formed throughout the measurement process.

6.5.2 Setup and Four-Point Resistance Measurements

As seen in Figure 110, a probe station was used to measure the four-point resistance of the CMIs within the fully assembled PINCH-system. Six chiplet samples were measured for the 200 μm pitch CMIs and four chiplet samples were measured for the 150 μm pitch CMIs. As all probing pads were on the same side of the interposer, all four micro-manipulators of the probe station were moved to the same side as seen in Figure 110. After the probes were set in place (on the interposer probing pads), the microscope of the probe station was lifted so that each corner screw was accessible. These corner screws were slowly rotated with a screwdriver until a resistance reading was established (i.e., a non-open reading). At the very earliest stages of observing a resistance reading during the rotation of the corner screws, the CMI resistance fluctuated, indicating that perhaps only a weak electrical connection has been formed and that the CMI was still significantly subjected to noise (e.g., vibrations from the probe station, vibrations in the air). Upon further rotation of the screws, the CMI reading became stable and no longer fluctuated. Further rotation of the screws decreased the four-point resistance reading further until it eventually saturated. These steady, saturated four-point resistance readings were recorded and listed in Table 17. As a note, as the PINCH-system is non-permanent, several different chiplet samples were tested with the same system (e.g., same socket, same interposer).

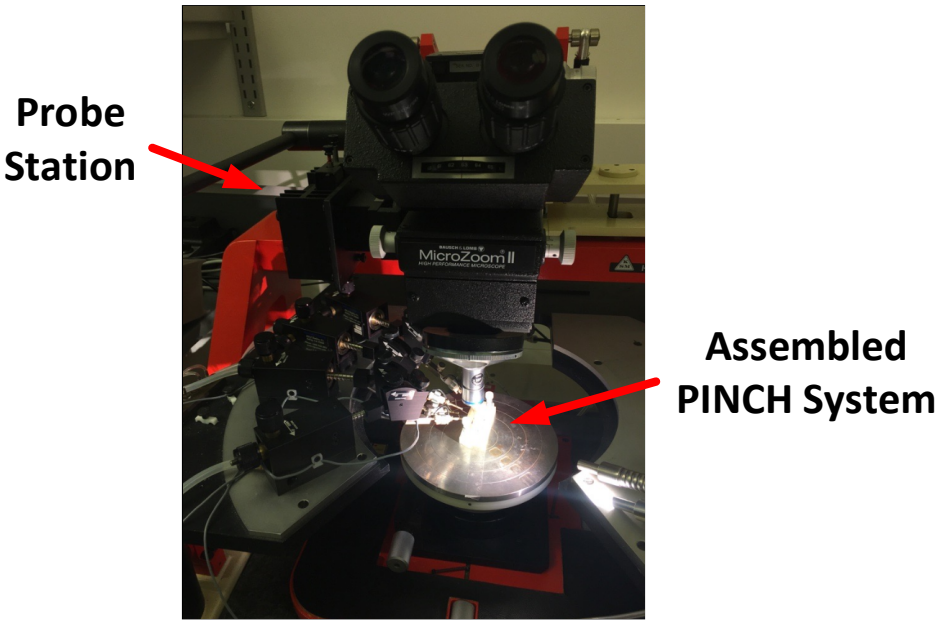


Figure 110. Measurement setup using a probe station for the four-point resistance measurements of the CMIs within the assembled PINCH-system.

As aforementioned, two sample sets were measured. The first sample set included CMIs with a 200 µm pitch. The second sample set included CMIs with a 150 µm pitch. In regards to the 200 µm CMI pitch set, six different CMI samples were measured with a computed four-point resistance average of 219.0 mΩ and a corresponding resistance standard deviation of 58.9 mΩ. In regards to the 150 µm CMI pitch set, four different CMI samples were measured with a computed four-point resistance average of 123.1 mΩ and a corresponding resistance standard deviation of 2.8 mΩ. Note that the difference in the standard deviation of the 200 µm CMI pitch and the 150 µm CMI pitch is likely due to differences in the assembly process and not the CMIs themselves. This matter is discussed in more detail in Section 6.5.3. Nevertheless, these resistance measurements demonstrate that self-alignment is successfully achieved and that a sufficient assembly force is applied, hence an electrical connection can be formed and maintained (and removed at any time).

Table 17. CMI four-point resistance measurements for 200 µm CMI pitch and 150 µm CMI pitch chiplets after the PINCH-system has been fully assembled

200 µm Pitch

CMI Sample No.	Four-Point Resistance (mΩ)
1	300.5
2	263.1
3	236.3
4	183.0
5	138.4
6	192.7
Avg.	219.0
Std. Dev.	58.9

150 µm Pitch

CMI Sample No.	Four-Point Resistance (mΩ)
1	126.4
2	123.4
3	119.6
4	123.1
Avg.	123.1
Std. Dev.	2.8

6.5.3 Discussion

6.5.3.1 Assembly Considerations

The targeted inter-substrate gap assumes that the PSAS holds its shape and is not distorted/deformed. However, if excessive force/pressure is applied, the PSAS does indeed deform, hence not only does the inter-substrate gap change, but the alignment changes as well. This PSAS shape deformation and change in alignment were initially observed during flip-chip bonding experiments when excessive forces were applied to the chiplet on interposer (the flip-chip bonder was only used here for force application purposes after alignment). As it is not known how much force is being applied (or how much force the PSAS can handle prior to deformation), it is certainly possible that during the aforementioned four-point resistance measurements that the PSAS did indeed deform, perhaps decreasing the inter-substrate gap and slightly moving the chiplet. Regarding the aforementioned saturated resistance readings, it is possible that the saturation also derived

(perhaps partially) from the PSAS preventing any further vertical motion of the chiplet. If so, excessive force may "overcome" this "PSAS barrier" and distort/deform the PSAS shape, which, in turn, may alter resistance readings. It is possible that such an excessive force was applied for some of the samples yet not the others. Or perhaps the degree of excessive force varied between measured samples. Additionally, if the misalignment created by this PSAS deformation slightly moved the CMIs partially off their mating pads (while still being partially in contact with these mating pads), this misalignment will also affect resistance (increasing resistance readings). These factors may potentially explain some of the variation in the resistance readings for the 200 μm CMI pitch case. The 150 μm pitch CMI resistance readings were performed subsequent to the 200 μm pitch CMI resistance readings; more familiarity with the assembly process likely assisted in being more consistent with subsequent assemblies, which may have resulted in less variation in the 150 μm pitch CMI resistance readings. A potential solution to minimize the distortion and/or deformation of the PSAS during the assembly process is to add microfabricated spacers (e.g., electroplated stubs with a thickness equal to slightly less than the targeted inter-substrate gap) onto the interposer to prevent the deformation/distortion of the PSAS and hence preserving the inter-substrate gap and alignment.

6.6 CMI RF Characterization

Figure 98 demonstrates several RF characteristics of the CMI. The derivation and measurement approach for these RF characteristics of CMIs are from [175] and are partially reproduced here for standalone purposes. To obtain these RF characteristics of the CMI, an L-2L de-embedding process is performed with CPW-based transmission lines. More specifically, as shown in Figure 111(a), a testbed is designed in ANSYS HFSS, which

emulates a fully assembled stitch-chip system using flip-chip bonding. A stitch-chip, as seen in Figure 112, is an electrical bridge that connects one chiplet to another chiplet in much the same manner as an interposer; such a bridge may be referred to as a TSV-less bridge-based interposer. Fused-silica is selected as the substrate material for the stitch-chip and the CMI-chip due to its low-loss attributes (low dielectric constant ~3.9 and low loss tangent ~0.0002 up to 30 GHz). Coplanar waveguides (CPWs) are formed on the stitch-chip, while two ground-signal-ground (G-S-G) pairs of gold-coated NiW CMIs with probing pads are formed on the CMI-chip. The CPWs and the CMIs are coated with electroless plated gold to prevent oxidation [115]. Note that this gold layer is also critical to reduce NiW CMI loss due to the higher conductivity and larger skin depth of gold at high frequencies. Figure 111(b) shows the device under test (DUT) in this testbed consisting of probing pads, CPW lines, and CMIs. Figure 111(c) demonstrates an illustration of CMIs with curved sidewalls, which enable their out-of-plane mechanical flexibility [118].

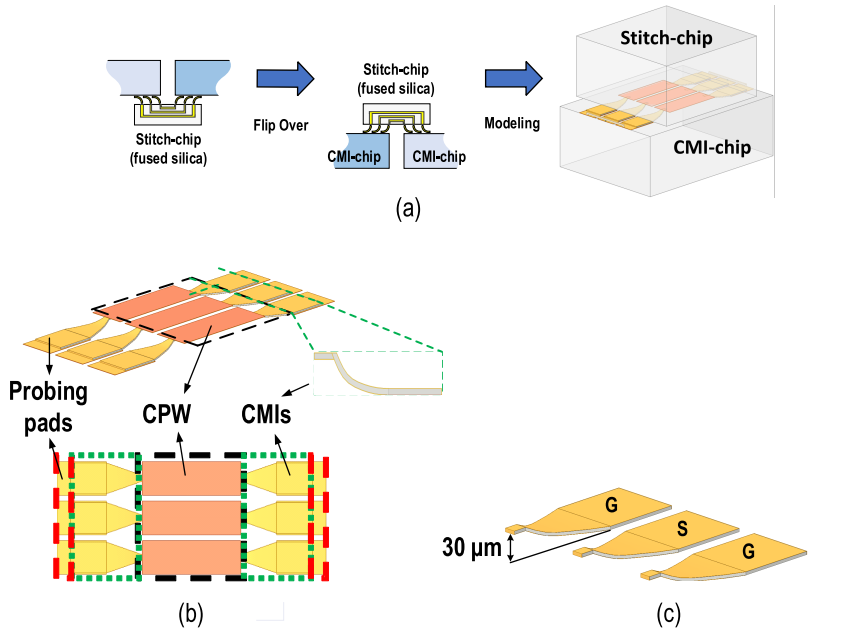


Figure 111. HFSS model for the testbed: (a) Modeling procedure, (b) schematic and top view of the device under test, and (c) schematic of G-S-G CMIs [175].

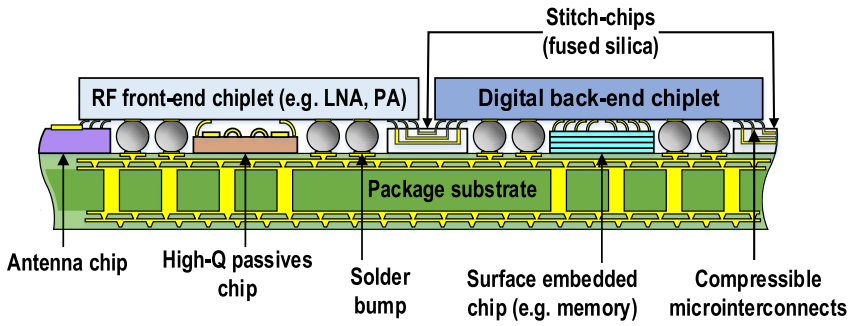


Figure 112. Polylithic integration using stitch-chips for RF/mm-wave applications [175].

The procedure of de-embedding involves two steps and uses ABCD-parameters converted from S-parameters. The first step is to remove the probing pad parasitics as shown in Figure 113(a), which can be summarized using the following matrix computations:

$$[Thrupads] = [Pad][Pad] \tag{15}$$

$$[DUT] = [Pad][Link][Pad] \tag{16}$$

$$[Link] = \sqrt{[Thrupads]}^{-1}[DUT]\sqrt{[Thrupads]}^{-1} \tag{17}$$

The probing pad parasitics are removed for two DUTs, one with L-length CPW and the other with 2L-length CPW. The results are denoted as [Link1] and [Link2], as shown in Figure 113(b). In Figure 113(b), [CMI] and [L] are the ABCD-parameters of the CMIs and L-length CPW, respectively. Next, L-2L de-embedding [176], [177] is utilized and can be described as follows:

$$[Link1] = [CMI][L][CMI] \tag{18}$$

$$[Link2] = [CMI][L][L][CMI] \tag{19}$$

$$[CMI] = \left(\sqrt{[Link1]^{-1}[Link2][Link1]^{-1}}\right)^{-1} \tag{20}$$

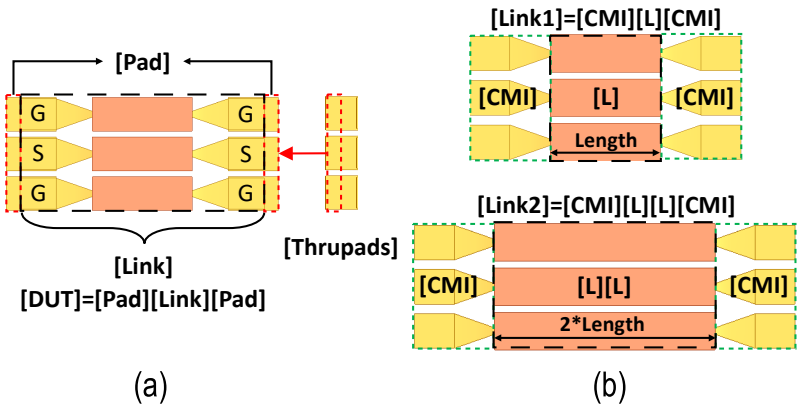


Figure 113. L-2L de-embedding procedure: (a) Top view of pad parasitics removal and (b) top view of L-2L de-embedding models [175].

These stitch-chips and CMI-chips can then be fabricated as described in [175]. After the fabrication process is completed and the assembly is performed, RF measurements up to 30 GHz are performed using Cascade Microtech 200 µm-pitch G-S-G IZI probes and a Keysight N5245A PNA-X network analyzer, which are housed in a Faraday cage. Short-open-load-thru (SOLT) calibration is used with a Cascade Microtech CSR-8 calibration substrate before RF measurements of the testbeds are performed. Next, L-sample, 2L-sample, and thru-pads structures are measured, from which the CMI RF characteristics are extracted. The CMI S-parameters after L-2L de-embedding are shown in Figure 114; these results are also recorded in Figure 99. More details on this process can be found in [175].

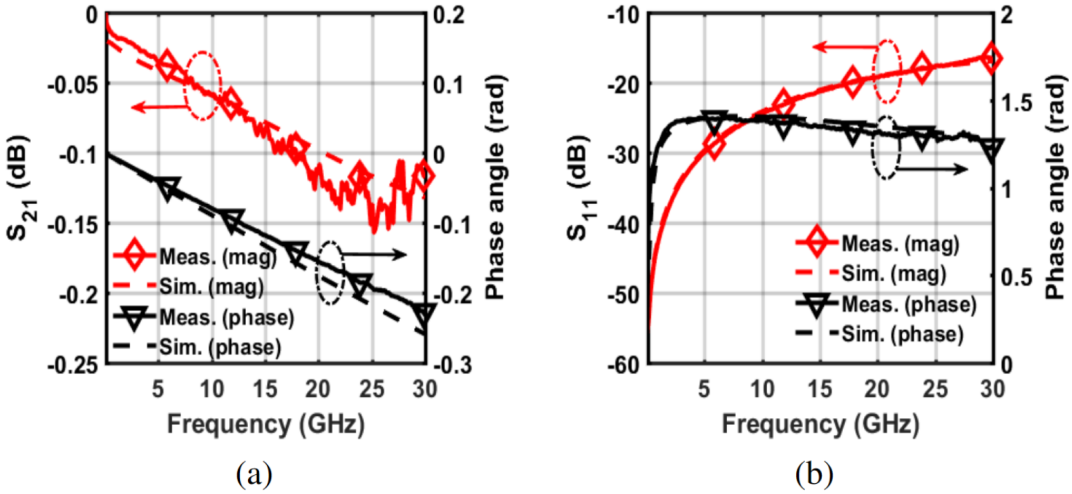


Figure 114. CMI S-parameters after L-2L de-embedding: (a) insertion loss and(b) return loss [175].

6.7 Conclusion

In this chapter, a re**P**laceable, **IN**tegrated **CH**iplet (PINCH) assembly using Compressible MicroInterconnects (CMIs) and PSAS-to-PSAS self-alignment technology is introduced for use in heterogeneous integrated applications. The PSAS-to-PSAS self-alignment technology is advantageous here and serves as an enabling technology for these applications given that it is substrate agnostic and given the wide variety of material substrates that can be incorporated into a heterogeneously integrated system. PINCH-system design considerations were discussed including achieving the targeted inter-substrate gap even with fabrication-based geometrical variations considered. The design, operation, and the fabrication of the PINCH-system socket, chiplet, and interposer were all described. Four-point resistance measurements of the CMIs after the PINCH-system was fully assembled were performed. A brief discussion on future work was also introduced.

CHAPTER 7. SUMMARY AND FUTURE WORK

7.1 Summary of the Thesis

In this thesis, non-permanent heterogeneous integrated systems, and several corresponding enabling technologies and toolsets were studied, analysed, and experimentally demonstrated.

7.1.1 Enabling Technologies and Toolsets

7.1.1.1 Optimization Methodology for the Improved Mechanical Performance of Compliant Interconnects

A novel optimization methodology for the improved mechanical performance of a wide variety of compliant interconnects was developed, simulated, and experimentally verified in CHAPTER 2. This optimization methodology provides a toolset to improve the reliability and the performance of the non-permanent heterogeneously integrated system via improving the mechanical performance of the compliant interconnect themselves. The key features of this optimization methodology include:

1. A generalized optimization process applicable to a wide variety of different compliant interconnects, each with unique fabrication process flows; this generalization of the optimization is enabled via optimizing only the photomask design of the interconnect.
2. The implementation of a spline-based parametrization for the interconnect geometry so that this optimization process is flexible enough to accommodate a

large variety of geometric designs while minimizing the formation of high-stress corners.

7.1.1.2 Non-Permanent Electrical Interconnect Technologies

Three different types of non-permanent electrical interconnect technologies were employed throughout this thesis:

1. Mechanically Flexible Interconnects (MFIs): A lithographically-defined, reflowed dome based fine-pitch compliant interconnect technology. MFIs were employed or studied in CHAPTER 2 and CHAPTER 3.
2. PariPoser: An anisotropic conductive film (ACF) where separated vertical columns of Ag-coated Ni balls within a matrix of silicone electrically connect corresponding mating pads on two mating substrates. PariPoser was employed in CHAPTER 4.
3. Compressible MicroInterconnects (CMIs): A lithographically-defined, concave-shaped fine-pitch compliant interconnect technology. CMIs were employed in CHAPTER 6.

As aforementioned in CHAPTER 1, the two general technologies to enable a tightly integrated non-permanent heterogeneous integrated system are: 1) a non-permanent off-chip, fine-pitch interconnect technology and 2) a non-permanent alignment technology. The first criterion is satisfied via all three non-permanent electrical interconnect technologies employed throughout this thesis. These interconnect technologies provide a non-permanent mechanism to create and maintain an electrical connection (via the application of pressure) while providing fine-pitch electrical connections (i.e., < 50 μm). The incorporation of these different interconnect technologies into non-permanent

integrated systems has been demonstrated repeatedly throughout this thesis (CHAPTER 3, CHAPTER 4, and CHAPTER 6).

7.1.1.3 Self-Alignment Technologies

Three different types of non-permanent alignment technologies were employed throughout this thesis. The non-permanent feature of these technologies satisfies the second criterion for non-permanent integrated systems as laid out in CHAPTER 1.

1. Ball-in-Pit: A self-alignment technology with sub-micron alignment that pairs precision balls and anisotropic-etched pits (usually etched via KOH or TMAH into (100) Si). Ball-in-Pit technology in conjunction with PSAS-in-Pits technology were employed in a novel double self-alignment configuration in CHAPTER 3 and CHAPTER 4.
2. PSAS-in-Pits: A self-alignment technology with sub-micron alignment that pairs Positive Self-Alignment Structures (PSAS), which are thermally-reflowed circularly patterned photoresist structures, and anisotropic-etched pits (same as in Ball-in-Pit technology). PSAS-in-Pits technology in conjunction with Ball-in-Pit technology were employed in a novel double self-alignment configuration CHAPTER 3 and CHAPTER 4.
3. PSAS-to-PSAS: A novel, self-alignment technology introduced for the first time that employs only PSAS structures on both mating substrates and that has been experimentally demonstrated in CHAPTER 5 to achieve sub-micron alignment. Two of the primary advantages that this self-alignment technology possesses are:

a. It is non substrate invasive as no etching is required as is the case for Ball-in-Pit and PSAS-to-Pits. This non-invasiveness aids to consume less substrate real estate in addition to eliminating contact with potentially incompatible chemicals (e.g., KOH).
b. It is substrate agnostic as any substrate material may be used. As an anisotropic wet etch is avoided (unlike with the case of Ball-in-Pit and PSAS-to-Pits), the crystallographic orientation of the substrate materials is irrelevant (in regard to achieving an anisotropic etched profile as none is needed). Additionally, non-crystalline materials may be used.

This second primary advantage (i.e., being substrate agnostic) is particularly useful for certain applications including heterogeneously integrated applications as said applications may employ systems which incorporate a wide variety of material substrates (GaN, GaAs, fused silica, InP, etc.) for the purposes of achieving optimal performance. Hence, this PSAS-to-PSAS self-alignment technology can prove very valuable as it does not require any specific substrates involved as is the case for both the Ball-in-Pit and PSAS-in-Pits technologies. This PSAS-to-PSAS technology was studied in depth in CHAPTER 5 and incorporated into a non-permanently integrated system in CHAPTER 6.

7.1.2 Non-Permanent Heterogeneous Integrated Systems

7.1.2.1 Bio-sensing Interface Module (BIM)

CHAPTER 3 introduced a novel disposable (hence non-permanent), self-aligned, and socketed biosensing-interface module (BIM) that serves to act as a 3D integrated interface

between an underlying CMOS biosensor and the cells grown atop the BIM surface. CHAPTER 4 extended this work via incorporating TSVs into the BIM in addition to also using PariPoser in place of MFIs as the interconnection system. The key features of this BIM technology include:

1. A novel double-self alignment mechanism, which incorporates both Ball-in-Pit and PSAS-in-Pits technologies in conjunction. This self-alignment mechanism facilitates non-permanent interconnections, increases testing throughput as alignment placement tools are avoided, and enables field-deployable applications as a simple manual placement of the BIM suffices for assembly.
2. Non-permanent MFI or PariPoser electrical interconnects that allow for the disposal of the BIM, which circumvents cross contamination, and hence leads to increased throughput as sterilization processes are avoided.
3. A socket to apply the needed pressure to the BIM and hence the MFIs or the PariPoser to create and maintain electrical connections between BIM and the biosensor (or test die).
4. The ability to circumvent a CMOS-only fabrication process if needed as the BIM does not contain any active devices, hence culture medium biocompatible materials and necessary surface treatments are easily incorporated into the overall fabrication process, which can potentially be performed at the wafer level, hence leading to decreased costs in accordance with economies of scale.

7.1.2.2 Replaceable Integrated Chiplet (PINCH) Assembly

A re**P**laceable, **IN**tegrated **CH**iplet (PINCH) assembly using CMIs and PSAS-to-PSAS self-alignment technology for use in heterogeneous integrated applications was introduced in CHAPTER 6. The key features of the PINCH assembly include:

1. The incorporation of the non-permanent PSAS-to-PSAS self-alignment technology. As aforementioned, this technology serves as a suitable enabling technology as it is substrate agnostic, which is needed in the case where multiple different substrate materials may be used as is the case for heterogeneous integrated systems. For purposes of demonstration, the PINCH system of CHAPTER 6 employed only glass material substrates (for both chiplet and interposer).
2. Non-permanent CMI compliant interconnections that allow for the removal or replacement of the PINCH-system chiplet, which can be useful for when chiplet removal/reuse/replacement is required (for replaceability, testing, prototyping, upgradeability, etc.).
3. A socket to apply the needed pressure to the chiplet and hence the CMIs to create and maintain electrical connections between chiplet and interposer.

7.2 Future Work

To further advance this dissertation work, several potential future works are discussed, some of which have already been introduced throughout the thesis.

7.2.1 Optimization Work

7.2.1.1 Minimizing stress concentrations and exploring non-ideal loads

It is important for future work to incorporate several factors into consideration not initially considered in the original optimization work of this thesis. Although it is observed that the maximum stress was minimized for the optimized design relative to the initial design for the specific ideal loading condition applied in the optimization work, it is certainly possible that in a more practical scenario where non-ideal loading conditions would be exerted that we may observe a higher maximum stress in the stress concentrations of the optimized design relative to the stress concentrations of the initial design, which would be the opposite of what is targeted. Future work should not only focus on minimizing maximum stress alone, but it should also potentially implement some geometric constraints to minimize stress concentrations as well since the removal of stress concentrations will aid to prevent unexpected failures. For example, such geometric constraints may force certain radii of portions of the MFI structure to exceed some specified radius minimum. In other words, the reduction of geometric stress concentrations is a useful metric to include in future studies so long as the compliance and strain constraints are met (or whatever other constraints may be present). Additionally, future work should incorporate not just a single ideal loading condition, but it should also explore the effect of non-ideal loads in an attempt to increase the mechanical performance (and non-mechanical performance if needed) of the MFI structure in a more realistic environment where different non-ideal loads may exist in practice (i.e., loads at angles to the z-axis not centered on the MFI head/pad).

7.2.1.2 Optimization process to also include electrical performance optimization

The optimization process introduced in CHAPTER 2 focused solely on the mechanical performance of compliant interconnects. However, the same process can be used to optimize electrical performance as well (both DC and high-frequency). In the case of

mechanical performance, a simulated indentation was performed where a load was applied at the tip of the MFI; from this simulated indentation, mechanical parameters including compliance and stress were evaluated. These parameters became the targets for optimization. An analogous simulation environment and corresponding parameters are needed for the case of DC and high-frequency compliant interconnect optimization. For the high-frequency case, an appropriate transmission line setup is likely needed. Such a setup should reflect what will be or what could be microfabricated (such as CPW lines). For the simultaneous optimization of both mechanical and electrical performance, several different simulation environments may need to be used. To capture the inter-play between both mechanical and electrical performance (e.g., electrical resistance of the compliant interconnect as it is deflected), a multi-physics simulation setup may be required.

7.2.2 Biosensing-Interface Module (BIM)

7.2.2.1 MFI-based BIM

As was discussed in CHAPTER 3, the MFI fabrication process experienced several challenges, all of which were addressed with the exception of the "reflection off the domes." Recall that due to the relatively close spatial distance between the relatively tall reflowed domes, it was observed that during one of the exposure steps that the UV light reflected off the domes and into the region between the domes. However, part of this region is not intended for exposure; the consequence of this undesired exposure created shorts between the back-to-back MFIs. A bottom anti-reflective coating (BARC) process development was initiated to address this problem but it was never completed. Spin-coating this BARC film proved unsuccessful. Spray-coating this BARC film was attempted;

however, the spray-coating mixture for viscosity purposes had not been properly developed. There are several possible directions as to how to proceed forward:

1. Continue the process development with the BARC film. Optimize the spray coating resist with BARC. The intent here is that a conformal deposition of the BARC film on the reflowed domes will prevent the observed undesired reflection. However, the BARC film works via two means: (1) destructive interference and (2) absorption. As the domes are non-planar in addition to the conformally deposited BARC film, minimizing reflection due to destructive interference of the reflected incidences of light is unlikely to work. However, the absorption of the light within the BARC may prove useful in minimizing said reflection.
2. Develop a different MFI array configuration. The corresponding domes were relatively tall as two MFIs shared one dome (double-dome approach). This was intentionally done as discussed in CHAPTER 3 to increase the height of the MFIs for compliance purposes. The single-dome MFI approach may circumvent this reflection problem; however, the compliance of these single-dome MFIs may become too low, which may create other challenges (e.g., MFI fracture, substrate fracture, MFI delamination). Perhaps another MFI array configuration can both maintain a relatively high compliance while circumventing the reflection problem.
3. Another technology may be used in place of MFIs (CMIs, PariPoser, etc.). As mentioned in CHAPTER 1, one of the primary criteria for non-permanent heterogeneous integrated systems is a non-permanent off-chip, fine-pitch interconnect technology. Although MFIs meet these requirements, it is not the only interconnect technology that meets these requirements. Two other interconnect

technologies (CMIs and PariPoser) that meet these requirements were employed in this thesis.

7.2.2.2 TSV process for BIM (or other systems)

As described in CHAPTER 4, the standard TSV-based BIM fabrication process flow is relatively high-risk due to the large number of pits and vias within the 300 μm thick BIM wafer; these large number of cavities create the potential for cracks and fractures to occur throughout the wafer. A new process was initiated to address these challenges, as discussed in Section 4.4. The continuation of the development of this process can prove useful not only for the reliability of subsequent BIM wafers during processing, but it can also prove useful for any process that requires TSVs.

7.2.2.3 BIM with an active biosensor

The BIM has been demonstrated and characterized in CHAPTER 3 and CHAPTER 4. A next natural step for the BIM is to integrate the BIM with an active biosensor. In this process, the BIM surface requires biocompatibility. Additionally, in clinical and *in-vivo* applications, the BIM surface electrode material and shape are critical for maximizing SNR for electrical signal recording. Gold, platinum bright, platinum black, and titanium nitride have been studied as potential biocompatible materials that result in a low electrode-cell impedance [178]. These materials (or more) can be potentially implemented as the BIM surface electrode material. Furthermore, many of the 3D processes employed throughout this thesis (e.g., dome for MFIs, concave-pattern shape for CMIs) may be employed to increase the surface area of the electrodes and hence minimize the electrode-cell impedance. Multiple studies can be performed on these different electrode materials and

shapes. Finally, integration of an active biosensor with the BIM and subsequent bio-testing would demonstrate a much fuller potential of the BIM to be used in a wide variety of biosensing applications while facilitating these testing and characterization processes due to its non-permanently integrated nature and the separation between sensing sites and biosensor while maintaining a very fine-pitch interconnectivity between BIM and biosensor.

7.2.3 PSAS-to-PSAS additional characterization

Several additional PSAS-to-PSAS characterizations include:

1. A means to determine the inter-substrate gap experimentally: The mathematical relationship between inter-substrate gap and PSAS geometrical dimensions, as derived in CHAPTER 5, is critical for the design and engineering of systems that employ the PSAS-to-PSAS technology. However, to ensure that these relationships are as accurate as possible, experimentally determining these inter-substrate gaps is important. Applying epoxy to an assembled die pair and examining the side-view of this pair in an SEM can provide data on this inter-substrate gap. However, the application of the epoxy may move the dice in the process of curing, hence affecting the inter-substrate gap. Applying pressure to the die pair during the epoxy curing process may help secure the dice in place; however, if this pressure is not enough, the inter-substrate gap may still slightly change. If the pressure is too large, it may deform the PSAS and again affect the inter-substrate gap. Furthermore, the SEM measurement process requires that the SEM measurement tool be calibrated and that the dice pair be perfectly (or near perfectly) viewed at its side. As the

measurement capture process is manual, there is also the introduction of potential human error. A more accurate means to experimentally measuring the inter-substrate gap may be via capacitive-sensing measurements that directly measure coupling capacitance while rejecting parasitic capacitances [179].

2. Determining the amount of pressure/force needed for the PSAS to change shape (height, width, etc.): The deformation of the PSAS should be minimized as such deformation may lead to changes in both the inter-substrate gap and the alignment. As described in Section 6.5.3.1, electroplated stubs with a thickness equal to slightly less than the targeted inter-substrate gap were introduced as a possible solution to this undesired PSAS deformation. The reasoning behind the thickness of the stub to be slightly less than the targeted inter-substrate gap is to ensure that the PSAS fully couples with its mating PSAS. However, some deformation of the PSAS will occur here upon the electroplated stubs being reached. If this deformation is minimal and does not affect the alignment nor inter-substrate gap by much, then perhaps such a deformation may be considered acceptable. Such deformation characterization of the PSAS should be performed for overall engineering and design purposes as it is critical to understand the challenges associated with corresponding systems (such as the PINCH system).
3. Determining potential alignment changes due to thermal cycling conditions: The PSAS is potentially susceptible to further reflow during heated conditions. Excessive baking of the PSAS may also cause it to become brittle and to potentially delaminate. Additionally, the PSAS may more easily deform when heated and when pressure is applied. Hence, for system reliability purposes, it is important to

understand the effects of temperature in regard to alignment and PSAS mechanical integrity. Future work should analyze such situations.

7.2.4 PINCH-system (or general non-permanent SiP systems)

7.2.4.1 Additional characterizations

Further characterization of the PINCH-system is critical for determining its full potential. RF characterization is particularly critical for the PINCH-system given that one of its potential uses is for mm-wave applications. The appropriate testbed and measurement setup will be needed; these include setting up the appropriate de-embedding techniques (e.g., L-2L) to de-embed the probing pads (and perhaps the on-chip traces) in order to isolate the high-frequency characterization of the CMIs when fully assembled within the PINCH-system.

Additionally, characterization of the CMI electrical performance (both DC and high-frequency) as a function of force (or CMI deformation) is also critical to understanding the dynamic nature of an adjustable and non-permanent integrated system (e.g., PINCH-system). These DC and high-frequency parameters are expected to change as a function of force and this can assist in the design and engineering of these systems. As discussed in CHAPTER 6, during the four-point resistance measurements, it was observed that after the very initial contact of the small screw against the chiplet that a continual rotation of the screw would further decrease resistance until this resistance reading eventually saturated. A finer control of the applied load (in addition to perhaps a pressure sensor on the chiplet) will prove useful in implementing the force measurement setup and the corresponding force measurement characterizations.

7.2.4.2 Integration with active dice

Upon further development and characterization of the PINCH-system, integration of the PINCH-system with active dice will further assist to demonstrate the full potential of the PINCH-system for a variety of applications (e.g., testing, prototyping, applications that require reuse or upgradeability). The PINCH-system interposer can be expanded to integrate multiple dice, not just a single die. As an example, we can envision the integration of a small transmit/receive RF system that integrates together an antenna die, a GaN PA MMIC, a pHEMT LNA die, and an SOI switch die all on a common low-loss interposer, all of which is part of the overall PINCH-system.

7.2.4.3 PINCH assembly reliability

The PINCH assembly reliability is, in part, dependent on the reliability of the PINCH assembly enabling technologies. Future work regarding the reliability of the PSAS-to-PSAS technology has been discussed in Section 7.2.3. Also, a more robust means to improving the performance of off-chip flexible interconnects has been discussed in Section 7.2.1. The reliability of the PINCH assembly can be explored via several tests: thermal cycling and the consistency of both DC and RF connections, vibration tests (electrical characterization measured before and after), repeatability tests (electrical characterization over multiple testing cycles), shock tests (electrical characterization before and after), different loading (measure electrical characteristics of CMIs vs. assembly force), humidity tests (electrical characterization before and after), etc. The repeatability of the flexible interconnects themselves (>100,000 cycles) will also prove useful in the reliability of the PINCH assembly. As the PINCH assembly is novel and incorporates many different

enabling technologies, future work should explore such reliability tests. A similar reliability focus should also be adapted for the BIM system in future work.

APPENDIX A. MATLAB CODE FOR SELF-ALIGNMENT DESIGN AND ENGINEERING CALCULATIONS

A.1 Ball-in-Pit and PSAS-in-Pits Design and Engineering Calculations

full_sphere_w

```
function [w,rmin,rmax,etch_depth,radius_depth,opening] =
full_sphere_w(r,g)

%all parameters in um
%assuming no Si 111 etching occurs (Si 111 etch rate = 0)

B = atand(1/sqrt(2));   %in degrees
w = r*secd(B) - (g/2)*tand(B); %half the total pit width

alpha = 90-B;  %in degrees
rmin = w*tand(alpha/2);
rmax = w/sind(alpha);

if r < rmin
    fprintf('Invalid radius for proper fitting. Too small!')
elseif r > rmax
    fprintf('Invalid radius for proper fitting. Too large!')
else
    fprintf('Valid radius!!!')
end


etch_depth = w/tand(B);
radius_depth = r - ((r/sind(B))-etch_depth);

if etch_depth > 300
    opening = 2*((etch_depth - 300)/tand(alpha));
else
    opening = 'no opening since etch depth does not exceed Si thickness
of 300um';
end

end
```

full_sphere_rad

```
function [r,r_max_gap,etch_depth,radius_depth,opening] =
full_sphere_rad(full_width,g)

%all parameters in um
%assuming no Si 111 etching occurs (Si 111 etch rate = 0)
```

```
w = full_width/2; %where w is half the total width
B = atand(1/sqrt(2));   %in degrees
r = w*cosd(B) + (g/2)*sind(B);


alpha = 90-B;  %in degrees


r_max_gap = w/sind(alpha);

gmax = (2*r_max_gap)/sind(B) - (2*w)/tand(B);

if g == 0 && full_width >= 0
    fprintf('Gap is 0. Therefore, given radius is max. Therefore any
values lesser than or equal to given radius are valid')
elseif g > gmax && g > 0 && full_width >= 0
    fprintf('Invalid width for targeted gap. Targeted gap too
large/width too small!')
elseif g > 0 && full_width >=0
    fprintf('Valid gap/width combination!!!')
else
    fprintf('Invalid input(s). Non-physical numbers.')
end

etch_depth = w/tand(B);
radius_depth = r - ((r/sind(B))-etch_depth);

if etch_depth > 300
    opening = 2*((etch_depth - 500)/tand(alpha));
else
    opening = 'no opening since etch depth does not exceed Si thickness
of 300um';
end

if g > gmax || g < 0 || full_width < 0
    r = 'N/A';
    r_max_gap = 'N/A';
    etch_depth = 'N/A';
    radius_depth = 'N/A';
    opening = 'N/A';
end

end
```

full_sphere_gap

```
function g = full_sphere_gap(full_width,r)

%all parameters in um
%assuming no Si 111 etching occurs (Si 111 etch rate = 0)

w = full_width/2; %where w is half the total width
B = atand(1/sqrt(2));   %in degrees
```

```
g=2*((r/sind(B))-w/tand(B));

end
```

trunc_half_sphere_w

```
function [w,rmin,rmax,etch_depth,radius_depth] =
trunc_half_sphere_w(r,g,t)

%all parameters in um
%assuming no Si 111 etching occurs (Si 111 etch rate = 0)

B = atand(1/sqrt(2));   %in degrees
w = tand(B)*((r/sind(B))-t-g);  %half the total width

alpha = 90-B;  %in degrees
rmin = t*cosd(alpha) + w*sind(alpha);
rmax = w/sind(alpha);

if (r < rmin) || (r > rmax)
    fprintf('Invalid radius for proper fitting')
else
    fprintf('Valid radius!!!')
end

etch_depth = w/tand(B);
radius_depth = r - ((r/sind(B))-etch_depth);

end
```

trunc_half_sphere_rad

```
function [r,r_max_gap,etch_depth,radius_depth] =
trunc_half_sphere_rad(full_width,g,t)

%all parameters in um
%assuming no Si 111 etching occurs (Si 111 etch rate = 0)

w = full_width/2;   %half the total width
B = atand(1/sqrt(2));   %in degrees
r = sind(B)*(g+(w/tand(B))+t);

alpha = 90-B;  %in degrees

r_max_gap = w/sind(alpha);

gmax = r_max_gap/sind(B) - w/tand(B) - t;   %should t be here or is t
inherently assumed to be 0 in r_max_gap

if g == 0 && full_width >= 0 && t < r && t>=0
    fprintf('Gap is 0. Therefore, given radius is max. Therefore any
values lesser than or equal to given radius are valid')
    etch_depth = w/tand(B);
```

```
    radius_depth = r - ((r/sind(B))-etch_depth);
elseif g > gmax && g > 0 && full_width >= 0 && t < r && t>=0
    fprintf('Invalid width for targeted gap. Targeted gap too
large/width too small!')
    r = 'N/A';
    r_max_gap = 'N/A';
    etch_depth = 'N/A';
    radius_depth = 'N/A';
elseif g > 0 && full_width >=0 && t < r && t>=0
    fprintf('Valid gap/width combination!!!')
    etch_depth = w/tand(B);
    radius_depth = r - ((r/sind(B))-etch_depth);
elseif g < 0 || full_width < 0 || t < 0
    fprintf('Invalid input(s). Non-physical numbers.')
    r = 'N/A';
    r_max_gap = 'N/A';
    etch_depth = 'N/A';
    radius_depth = 'N/A';
elseif t >= r && t >= 0
    fprintf('Invalid truncated geometry. Truncation cannot be equal to
or more than radius of PSAS.')
    r_max_gap = 'N/A';
    etch_depth = 'N/A';
    radius_depth = 'N/A';

end

end
```

trunc_half_sphere_trunc2

```
function [hhh,gmax,r] = trunc_half_sphere_trunc2(full_width,g,a)

%Author: Joe L. Gonzalez

%1) all parameters are in um (micrometers)
%2) assuming no Si 111 etching occurs (Si 111 etch rate = 0) so pit
width
%('full_width') is assumed unchanged. In reality however, the desired
pit
%width (in the mask pattern) would be wider after fabrication since KOH
%etches Si 111 (very slowly) so we will obtain some undercut. This
undercut
%effectively widens the pit width. This should be considered when
%determining what PSAS height is needed.
%3) For partial reference, please see James Yang's paper titled
%"Self-Alignment Structures for Heterogeneous 3D Integration." Also,
please
%google "radius as a function of chord length." Wolfram MathWorld has a
%link describing relations between variables of a circular segment.
%Specifically, it decribes the relationship between the radius of a
circle
%(r), its chord length (a), and the height of the arced portion (h).
The
```

```
%height equation in this function ('hhh') was derived from the
following
%equation:
% a = 2*sqrt(h*(2r-h))
%where 'a' is the chord length, 'h' is the height of the arced portion,
and
%'r' is the radius of the circle.
%4)Also see the ANSYS WB file,
%"PSAS_inverted_pyramid_pits_dimensions_UPDATED_FIXED" for a visual
aid.
%File might be located on the shared storage drive.


%-------------INPUTS----------------
%'full_width' is the full width of the pit
%'g' is the gap between substrates
%'a' is the full width of the PSAS (or the chord length of the PSAS
%"circle" where the PSAS meets the substrate)

%-------------OUTPUTS----------------
%'r' is the radius of the PSAS (not necessarily the PSAS width)
%'gmax' is the maximum gap achieveavble by the pit width and PSAS
%width. A non-truncated PSAS would be at maximum gap for that
combination
%of pit width and PSAS width.
%'hhh' is the required height of the PSAS to achieve the desired gap
for
%the given pit width and PSAS width

%-----------FUNCTION DESCRIPTION----------------------
%This function determines what PSAS height ('hhh') you need for
%a given PSAS width ('a'), a pit width ('full_width'), and a desired
gap
%('g').

%NOTE_1: The PSAS height is obtained via spin coating the appropriate
%thickness of photoresist (i.e., AZ40XT) and then reflowing this
resist.
%Typically, we assume the width of the PSAS/resist doesn't change. We
also
%assume the volume of the PSAS/resist doesn't change. This is how we
can
%back calculate the initial photoresist thickness needed. The PSAS
height
%given here is the height of the REFLOWED photoresist, not the initial
%photoresist.

%NOTE_2: The aforementioned assumptions (width of PSAS/resist does not
change
%and volume of PSAS/resist does not change) may not be entirely
accurate.
%In fact, the width may vary during reflow. Also, the volume during
reflow
%is likely to decrease as solvent evaporates. A shorter reflow (at a
given
%temp.) may decrease this solvent evaporation.
```

```
%NOTE_3: Code needs to be updated to tell users about any mathematical,
%physical, or fab violations. However, this code still works and still
%provides correct outputs but caution must be taken to ensure that all
%physical and fab requirements are met. I know what these constraints
are.
%I just have not written them into the code yet.


w = full_width/2;   %half the total width
B = atand(1/sqrt(2));   %in degrees
syms h;
eqn = h^2*(-4-4/sind(B)) + h*(8*w/tand(B) + 8*g) + (a^2 - a^2/sind(B))
== 0;
solh = solve(eqn,h);
num_sol = vpa(solh);

r = num_sol(2)/2+a^2/(8*num_sol(2));
t=r-num_sol(2);
hhh=num_sol;
% Two solutions come from solving "eqn" and are stored in hhh. One
solution
% is what we likely expect. The other solution is not what we want.

alpha = 90-B;  %in degrees

gmax = vpa(r/sind(B) - w/tand(B));

end
```

A.2 PSAS-to-PSAS Design and Engineering Calculations

psas to psas truncated psas

```
function [g, R, S, msg] = psas_to_psas_truncated_psas(w,s,h)

%This program finds the gap between substrates having PSAS for
%self-alignment purposes.
%One substrate has 3 PSAS. The other substrate has one PSAS.
%All PSAS all identical in size
%PSAS width and height are not necessarily the same. PSAS is assumed to
be
%a truncated sphere. That is, it is a portion of a perfect sphere (or
%perfect half-sphere). Only when the PSAS is a half-sphere is its half-
width
%and height the same (which would be the radius of the PSAS)

%all parameters in um
%w is the width of the PSAS (or the chord length of the truncated
circle)
%s is spacing between PSAS
%h is the height of the PSAS (or height of the arced portion)
%g is the gap between substrates containing PSAS for self-alignment
```

```
 R = (w.^2)/(8*h) + h/2; %R is the radius of the PSAS (assuming we had
a half-sphere).
 D=2*R;
 S = s - 2*(R-w/2); %S is the theoretical spacing between PSAS if the
PSAS were half-spheres.


num = (2*D.^2 - 2*D*S - S.^2);
pre_g = sqrt(num/3);

r = R-h; %r is the difference between PSAS radius (if full half-sphere)
and current PSAS height
g = pre_g - 2*r;

if g<h
    msg = 'Invalid gap as calculated gap is less than PSAS height';
    g = ['Invalid gap! Calculated gap = ' num2str(g)];
else
    msg = 'Valid gap';
end

end
```

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