THREE-DIMENSIONAL MICROFABRICATION TECHNOLOGIES FOR ELECTRONIC AND LAB-ON-CHIP APPLICATIONS

A Dissertation
Presented to
The Academic Faculty

by

Reza Abbaspour

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
Electrical and Computer Engineering

Georgia Institute of Technology
December 2018

THREE-DIMENSIONAL MICROFABRICATION TECHNOLOGIES FOR ELECTRONIC AND LAB-ON-CHIP APPLICATIONS

Approved by:

Dr. Muhannad S. Bakir, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Albert B. Frazier
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Yogendra K. Joshi
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Azad J. Naeemi
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 10/30/2018

To my wife, my son, and my parents

ACKNOWLEDGEMENTS

I would like to sincerely thank my advisor Dr. Muhannad S. Bakir for his unbounded support and endless guidance throughout my Ph.D. research, and my technical committee for their kind effort. It has been a great pleasure to working with Integrated 3D Systems (I3DS) Group current and previous members Joe Gonzalez, Thomas Sarvey, Sreejith Kochupurackal Rajan, William Wahby, Paul Kim, Hanju Oh, Xuchen Zhang, Paragkumar Thadesar, Chaoqi Zhang, Yue Zhang, Li Zheng, Yang Zhang, Muneeb Zia, Md Obaidul Hossen, and Congshan Wan. Moreover, I thank to Dr. Wilbur A. Lam, Dr. Jordan C. Ciciliano, and Dr. Hommood Alrowais for their productive collaboration at Georgia Tech. I also wish to thank the Institute for Electronics and Nanotechnology (IEN) staffs at Georgia Tech: Gary Spinner, Vinh Nguyen, Charlie Suh, John Pham, Thomas Averette, Mikkel Thomas, Chris Yang, Todd Walters, Eric Woods, Hang Chen, Dean Sutter, Bob Rose, and Paul Turgeon for their help inside and outside of the cleanroom. Last but not least, I wish to thank my wife for being patient and supportive in all these years, and my parents, for their endless encouragement.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATIONS

3D	Three-Dimensional
3D-IC	Three-Dimensional Integrated Circuits
3DI	Three-Dimensional Integration
ABS	Acrylonitrile Butadiene Styrene
ALD	Atomic Layer Deposition
AMI	Acetone-Methanol-Isopropanol
ATP	Adenosine triphosphate
Au	Gold
BGA	Ball Grid Array
BSA	Bovine Serum Albumin
CCC	Current-Carrying-Capacity
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical-Mechanical-Planarization
CNC	Computer Numerical Control
DC	Direct Current
DIC	Disseminated Intravascular Coagulation
DIW	Deionized Water
DRAM	Dynamic Random-Access Memory
EBL	Electron Beam Lithography
HMDS	Hexamethyldisiloxane

I/O	Input/Output
IC	Integrated Circuits
ILD	Inter-Level Dielectric
ITRS	International Technology Roadmap for Semiconductors
IoT	Internet of Things
LAP	Laser Assisted Photoreduction
MPO	Myeloperoxidase
MCM	Multi-Chip-Module
MEMS	Micro-Electro-Mechanical Systems
PBS	Phosphate-buffered saline
PCB	Printed Circuit Boards
PDMS	Polydimethylsiloxane
PECVD	Plasma-Enhanced-Chemical-Vapor
PoP	Package-On-Package
Pt	Platinum
PVD	Physical Vapor Deposition
RDL	Redistribution Layer
RIE	Reactive Ion Etching
RF	Radio Frequency
RPP	Reverse Pulse Plating
SCD	Sickle Cell Disease
SiN	Silicon-Nitride

SiP	System-in-Package
SLA	Stereolithography
SoC	System-on-Chip
TDMAT	[Tetrakis(dimethylamido)Titanium(IV)]
TDP	Thermal Design Power
Ti	Titanium
TiN	Titanium Nitride
TSV	Through Silicon Via
WLCSP	Fan-in Wafer-Level Chip-Scale-Package

SUMMARY

The density of heterogeneous three-dimensional integrated circuits (3D-ICs) is significantly limited by through-silicon-via (TSV) dimensions and cooling challenges. To enable fine-grained 3D-ICs, high aspect-ratio sub-micron diameter (~920 nm) TSV technology is demonstrated. The key processes used to form the sub-micron TSVs include: (1) Electron-beam-lithography (EBL) of the vias and fine resolution plasma etching of a hard-mask, (2) deep silicon etching of sub-micron features with a low-roughness sidewall profile, and (3) void-free metallization of TSVs through the electrodeposition of copper onto a diffusion barrier layer. Moreover, a testbed is designed and microfabricated to characterize the electrical resistance of the TSV, extract the copper resistivity of the core material, and measure the maximum achievable current-carrying capacity of the scaled TSVs. Possible failure mechanisms under current stressing are discussed.

To address cooling challenges and pronounced thermal wall limits in high-density integrated electronics and 3D-IC technology, a monolithic microfluidic cooling strategy is explored. Specifically, a thermal testbed with non-uniform power map and integrated microfluidics is microfabricated. The testbed features two independent fluid streams for cooling very high heat flux density hotspots separately from the background heat dissipation. To remove 100 W/cm^2 of background power dissipation and large heat fluxes generated by hotspots (up to 6 kW/cm^2) on the developed thermal testbed, microfluidics are etched into the back side of the silicon die and 3D printed microfluidic ports are integrated into the package. While the proposed silicon-based microfluidic cooling is shown to provide thermal benefits, the

silicon Bosch process introduces a number of challenges on a fully processed CMOS wafer, in particular introducing crystalline defects, reducing silicon volume and thus increasing wafer warpage. As an alternative, a novel metal additive manufacturing technology is developed as a key enabler for microfabricating a metallic microfluidic heatsink at the die-level and wafer-level. As a result, we demonstrate additively manufactured 200 µm diameter copper (Cu) pillars as the key heat dissipating elements for monolithically integrated microfluidic heatsinks. The material composition of the printed pillars is measured, and the Young's modulus, hardness, and Cu resistivity of the printed structure's material are characterized.

Lastly, it is discovered that there is a wide need for the silicon etching process that was developed for the high-density 3D-IC project. This sub-micron silicon etching process exhibits a scallop-free profile that is an essential feature for high resolution soft lithography. Thus, fabrication of aggressively scaled structures made from optically transparent bio-compatible polymers (e.g., PDMS) is enabled for bio-characterization applications. By leveraging this fine-grain soft lithography technology, for the first time, bio-physical interactions of red-blood-cells (RBCs) with their surrounding environment is visually studied in vitro.

CHAPTER 1. 3D MICROFABRICATION TECHNOLOGIES, APPLICATIONS, CHALLENGES, AND BOTTLENECKS

Denser integration of electronics has been a driving motivation for developing scaling technologies since the invention of the integrated circuit due to the ever-present demand for faster computational processing, more functionality, all at a lower cost. Innovative microelectronic packaging schemes have provided a complementary approach to the ongoing scaling efforts (More than Moore) and has hence gained significant attention for their ability to achieve an even higher density of integration [1]. Among all, the 3D integration of electronics seems to offer a promising approach to reduce the total cost of technology development for future generations of microelectronics in addition to providing the means to further integration [2]. One form of 3D-IC is enabled by the through-silicon via (TSV), which is the fundamental building block of heterogeneous 3D integrated systems. We therefore in this thesis demonstrate technologies that provide the capability to scale TSV dimensions to facilitate the development of fine grain 3D-IC technology. However, as with many technologies that provide benefits, there are certain tradeoffs that must also be considered. Specifically, in this case, denser 3D-ICs are increasingly facing thermal challenges as the power wall limit in 3D systems is becoming pronounced. To mitigate the dissipation of large heat fluxes generated across all silicon stacks in addition to enabling thermal isolation between heterogeneously 3D

stacked silicon tiers, this thesis also explores monolithic microfluidic cooling. Lastly, a nano-scale, deep silicon etching technique that was primarily developed for the scaling of TSV technology was found to exhibit a low roughness and scallop-free profile on etched nano-scale features. This etching process therefore further provides a 3D microfabrication capability by enabling a fine resolution soft lithography technology for specifically the microfabrication of a wide range of lab-on-chip devices. The following sections under this chapter will explore the motivations behind the conducted research presented in this Ph.D. dissertation.

1.1 The Ever-Growing Need for Denser Integration

The relentless need for high bandwidth communication [3], lower power consumption, and higher density of integration continues to drive the development of scaling technologies [4] and fueling the increasingly growing demand for innovative microelectronic packages [1]. Moreover, achieving a smaller form factor is essential for many emerging applications such as point-of-care, internet-of-things (IoT), and so forth. This necessitates employing diverse integration schemes which are often challenging to mix and match due to inherent incompatibilities between manufacturing processes. For example, leading-edge CMOS technology is mostly incompatible with MEMS technology, photonics, and III-V enabled optoelectronics [5]. However, the idea of "monolithic integration of everything" led the technology trend towards the concept of system-on-chip (SoC). After decades of advancements in the microelectronic industry, eventually integration of different microfabrication processes lead to the realization of SoC technology in late 1990s [6]. This paved the

way towards monolithic integration of multiple functions including DRAM, analog circuits, RF blocks, and logics all on a single silicon die [7]. However, emerging technologies such as lab-on-a-chip, silicon photonics, mm-wavelength, high-density memories, and MEMS created increasingly advanced challenges for implementing the concept of SoC. Hence, innovative heterogenous integration schemes such as system-in-package (SiP), package-on-package (PoP), and multi-chip-module (MCM) technologies were introduced [8] that aimed to reduce the manufacturability challenges of SoC devices (i.e. cost and time to market) while mitigating the limitations with the growing system complexity as illustrated in Figure 1 [9].

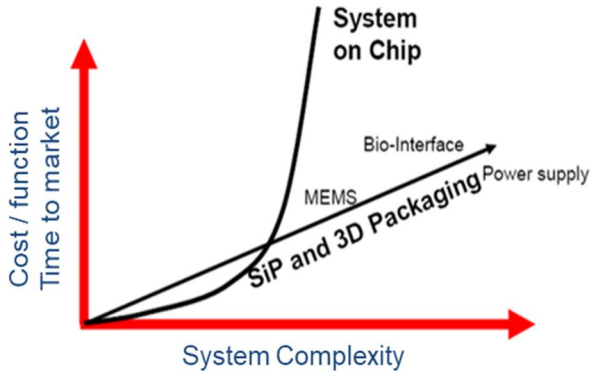


Figure 1 – System level integration. More than Moore, white paper, ITRS [9]

Application driven electronic packaging is a complex landscape which requires technology development in various directions. For many applications, manufacturing limitations still justify the building of electronic systems using discrete components and interconnecting on conventional PCBs. However, there are significant ongoing research efforts to address these manufacturing limitations by developing cost

effective, reliable, and smaller SiP-inspired microelectronic packages. For instance, WLCSP technology has been introduced for single-die chips to eliminate the package substrates and wirebonds [10], resulting in smaller package parasitics, higher reliability, and lower production cost [11]. This approach converts the wirebond pads at the perimeter of the silicon die to the solder BGA arrangement by redistributing (i.e. fan-in) I/Os at the center of the silicon chip [10]. In contrast, fan-out arrangement of I/Os became a feasible packaging scheme (i.e. fan-out wafer-level package—FOWLP) by exploiting the package mold encapsulation for implementing the die-to-package RDL [12]. Therefore, flexibility of package design increased as the RDL is no longer limited by the size of the silicon die [13]. Figure 2 illustrates a relatively broad range of different microelectronic packages that are introduced for different levels of integration. Among all, heterogenous 3D integration is being explored as an innovative technology to address the increasing need for denser integration, smaller latency, and lower energy dissipation through shortening of the length of interconnects. One form of 3D integration is enabled by vertically stacked silicon tiers and interconnecting using TSVs. This approach represents a promising technology to keep pace with Moore's law [14] and incorporates the modular design benefits of a heterogeneous architecture [15], [16]. TSV geometry, especially diameter, largely determines not only the electrical attributes and mechanical reliability of the interconnects but also that of the entire 3D stack and therefore scaling TSV dimensions is found to be critical for further advancement in the field of heterogenous 3D integration. Thus, a chapter of this Ph.D. thesis primarily focuses on technologies that enable the scaling of TSV dimensions.

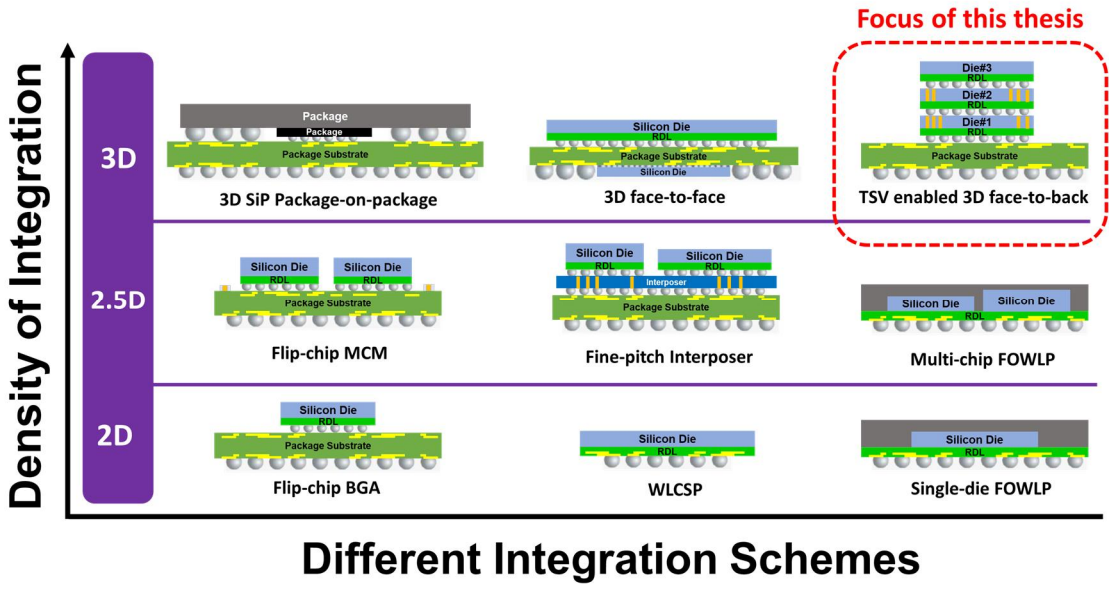


Figure 2 – Developed microelectronic packaging technologies with different integration density

1.2 Thermal Challenges in ICs

While keeping the temperature of devices below the specified operating temperature (preferably lower than 85 ℃ [17] but below the maximum junction temperature 150 ℃ [18]) has been satisfied with sufficient passive cooling techniques [19], thermal challenges in power demanding ICs impose limitations and concerns to the package integrity [20], performance [21], and density of integration [22]. Thus, the power wall (see Figure 3) and thermal challenges in 2D-ICs maintain the power density below approximately 100 W/cm^2 [23], which has become an evident outcome in designing modern CPUs [24].

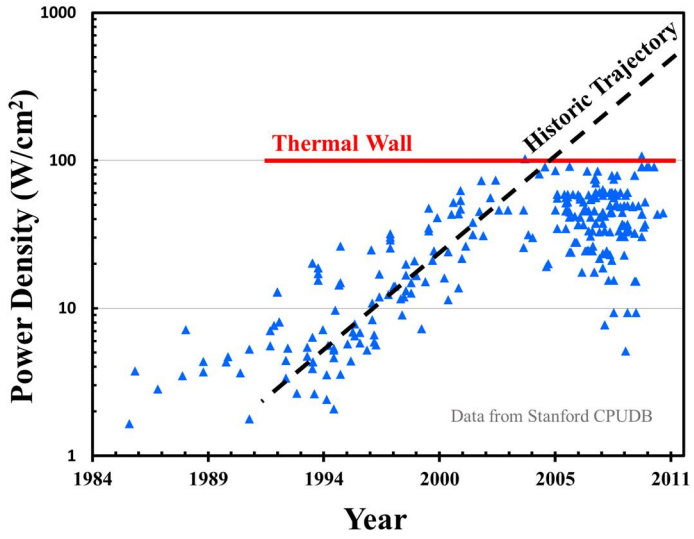


Figure 3 – Thermal wall limit dictates the power density to not increase as expected by the historic trajectory [23]

Higher power dissipation and the resulting larger temperature variations across the silicon die increases the leakage power [25],[26],[27] that undoubtedly contributes to the cost of system operation [21]. Thus, more effective cooling technologies such as fluidic cooling not only lead to lower leakage power, and hence saving energy [28], but also could overcome the thermal wall issue to achieve higher power density in CPUs and GPUs. Furthermore, it is challenging to adopt and scale the conventional air-cooling approaches for emerging high-density 2.5D and 3D technologies as they are bulky cooling solutions that are limiting at high heat power densities. As plotted in Figure 4, an air-cooling based heat removal system with a thermal resistance of 0.2 ℃/W is 1 kilogram in weight and 0.5 liter in volume. These measures are challenging to adopt for high density packaging schemes which

necessitates alternative cooling technologies with significantly smaller form factor and lower thermal resistance.

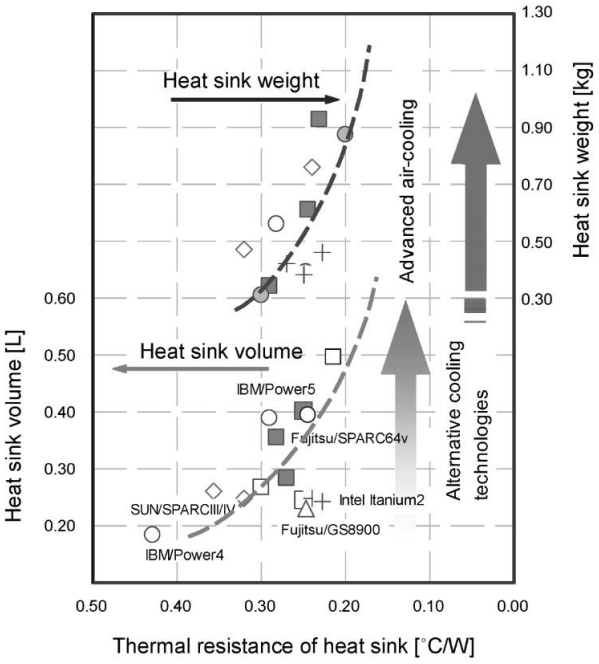


Figure 4 – Heatsink characteristic vs. thermal resistance [19]

As shown in Figure 5, more compact cooling techniques are enabled by exploiting the promising performance of fluid-based cooling. Cold-plates are non-monolithic fluidic heatsinks that currently are used in desktop computers and high-performance computing systems. While a better thermal performance is achieved by the cold-plates, the inherent thermal challenges in power hungry 2D-ICs (e.g. hardware accelerators and CPUs) and 2.5D architectures still need to be sufficiently addressed [29]. However, the demand for a higher heat removal rate and smaller form-factor requires the tighter integration of microfluidics. Thus, monolithically integrated microfluidics at the die level seems to offer the best performance in class and the smallest achievable form-factor compared to the existing alternatives.

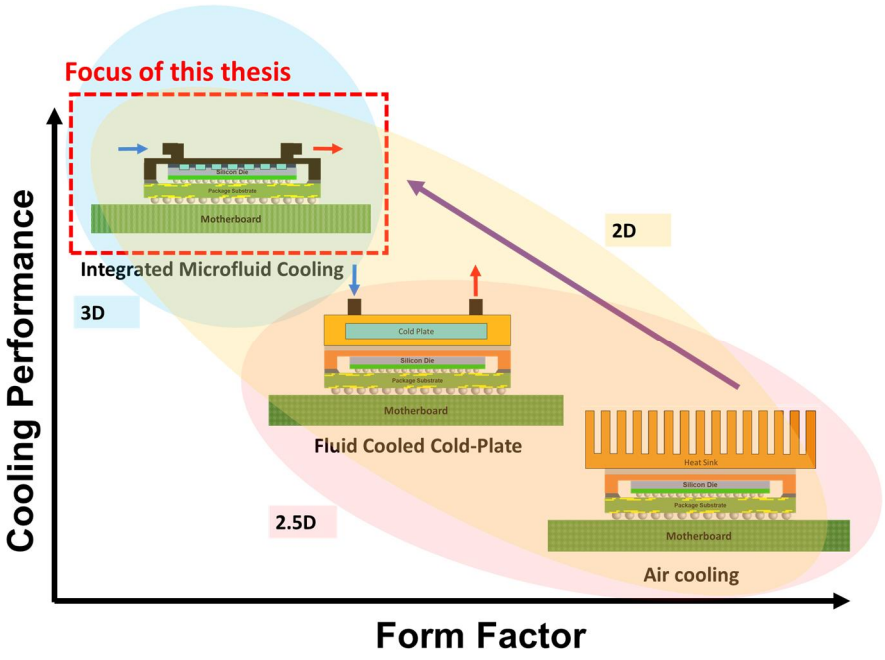


Figure 5 – Form factor vs. cooling performance for 1) air cooling, 2) fluid cooled cold-plate, and 3) integrated microfluidic cooling

Further, monolithically integrated microfluidic heatsinks have more to offer as they enable intra-stack heat removal in 3D-ICs [30]. This is increasingly beneficial since emerging fine-grain 3D-IC technologies face even worse thermal challenges due to the more pronounced power wall limits in denser 3D-ICs [31]. To mitigate the dissipation of large heat fluxes generated across the entire silicon die in addition to enabling thermal isolation between heterogeneously 3D stacked silicon tiers [32], monolithic microfluidic cooling is explored. The schematic of Figure 6 illustrates stacks of silicon tiers with monolithically integrated microfluidics. Hotspot heat dissipation is performed through a shallow micro-gap (10 µm deep) and sub-micron pin-fins. This cooling architecture demands scaled 3D interconnects to pass through the hotspot microgap and micropin-fins to provide signal- and power-based electrical

connections, which are required for dense and power-demanding circuitry in the hotspot region. The scaled TSV technology developed in this Ph.D. research has the potential to address the need with the hotspot.

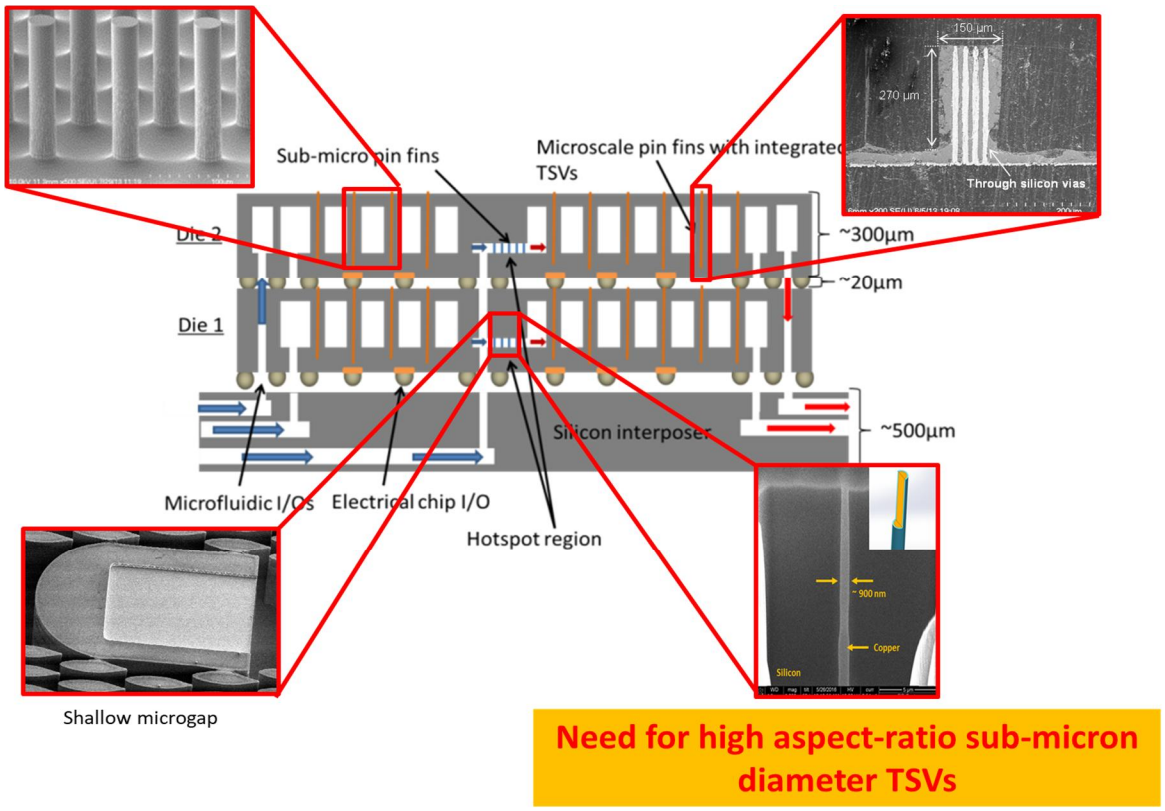


Figure 6 – Schematic of 3D stacked tiers with monolithically integrated microfluidic cooling and the need for sub-micron TSV technology.

1.3 Additive Manufacturing for Next Generation Integrated Circuits

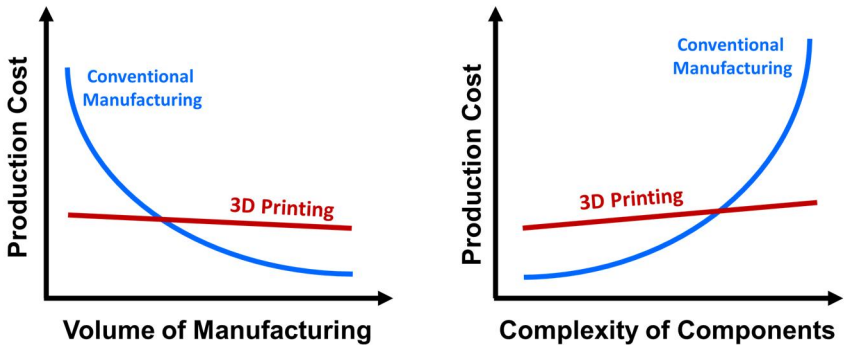


Figure 7 – High-level production cost comparison between 3D printing and conventional manufacturing.

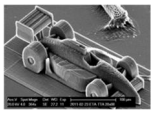
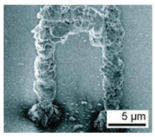
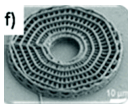
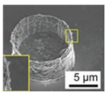
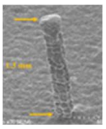
In the previous research topic, we presented motivations for developing the microfluidic cooling technology to mitigate thermal challenges in high power dissipating 2D and 3D ICs, enabled by conventional subtractive (i.e. silicon Bosch process) microfabrication techniques. While the proposed silicon-based microfluidic cooling is shown to provide thermal benefits, the silicon Bosch process introduces a number of challenges on a fully processed CMOS wafer, in particular introducing crystalline defects, reducing silicon volume and thus increasing warpage, among others. As a result, we also explore in this thesis the possibility of employing additive manufacturing technology as an enabler for fabricating a microfluidic heatsink at the die-level and wafer-level.

Additive manufacturing technology has gained significant attention as it enables cost-effective manufacturing of complex designs with fairly short production time. Figure 7 illustrates a high-level comparison between the conventional manufacturing technologies (e.g. CNC machining) and 3D printing technology.

Unlike conventional manufacturing processes, cost of additively manufactured products is insignificantly influenced neither by structural complexity of manufactured components nor by volume of production, making the 3D printing technology a viable solution for rapid prototyping and low volume production scheme. However, the increasing demand for inexpensive high-volume production of goods keeps the conventional manufacturing processes mainstream over additive fabrication technologies. Nevertheless, continuous research efforts in this field have lead to the development of multiple 3D printing technologies to address the need for different applications.

Table 1 shows a comparison between various additive fabrication technologies that each leverage a different core process for 3D printing. Despite all the advancements in this field, additive fabrication faces challenges with the use of metals. For many applications, metals are the materials of interest but are challenging to precisely deposit at the micron-scale in most 3D printing methods. Thus, we aim to address this challenge by developing a novel 3D printing process to overcome the lack of microscale deposition of metals in conventional additive manufacturing techniques. This allows us to utilize the best of additive manufacturing for heterogeneous integration of microfluidic cooling elements in the IC or package and to provide flexibility in IC fabrication as well as to provide reduced development time, improved yield, and hence a reduction in cost of manufacturing.

Table 1 – Comparing different additive manufacturing technologies

Process	Laser Enabled			Thermal Extrusion	Material Jetting	Electro-chemical Reduction	
	Polymerization	Sintering	Photo-Chemical Reduction				The presented work
Technology	SLA	SLS	LAP	FDM	BPM		
	BIS	SLM			ELP		
	HIS	DMLS			3DP		
	LTP	DMD					
	SGC	LPD					
Sample							
Multi-Material	No	No	No	Yes	Yes	No	Yes
Batch Fab	Yes	Yes	Yes	No	No	No	Yes
System Complexity	High	High	High	Medium	Medium	Medium	Low
Scale	Macro, micro, and Nano	Macro	Micro, and Nano	Macro	Micro	Micro, and Nano	Micro
Base Material Type	Liquid	Solid/solid -like	Powder				

1.4 Advanced Silicon Etching: Lab-on-Chip Applications

Additional novel applications are explored based on the 3D-IC silicon etching process that was developed in the prior sections. The sub-micron silicon etching process exhibits a scallop-free profile that is an essential feature for high resolution soft lithography. This enables fabrication of aggressively scaled structures made of

optically transparent polymers (e.g. PDMS) for bio characterization which has found an attractive lab-on-chip application. We launched a collaborative project and leveraged our fine-grain, soft lithography technology to study a long-standing research problem on the bio-physical interaction of blood cells with their surroundings.

Cardiovascular systems are dynamic and sophisticated microfluidic environments [33] in which the blood cells circulate. This fluidic system under different conditions exhibits physical changes through the introduction of platelets and fibrin matrices. Thus, the physical environment with which the blood cells bio-physically interact can be altered. This is found to be critical as the blood cells during hematologic processes, such as thrombosis [34] and hemostasis, exhibit bio-physical interactions with a myriad of vascular matrices. Although this has been well documented in the literature, how the cells respond to the underlying matrices having different mechanical properties remains a long-standing research problem. Studying these bio-physical interactions directly impacts our understanding from the context of clotting in which many parallel mechanisms are involved [35]. As shown in Figure 8, red blood cells (RBCs), activated platelet, and fibrin matrix, among others contribute to the formation of a clot [36]-[37], making it complicated to decouple all attributes. Although, the involved biochemical processes implicated in pathological clotting are well studied, the expected bio-physical interactions have previously been technologically infeasible to characterize. Thus, we sought to recreate the physical geometry of a fibrin network [38],[39] in a controlled, non-biological, in vitro microfluidic system using advanced microfabrication techniques.

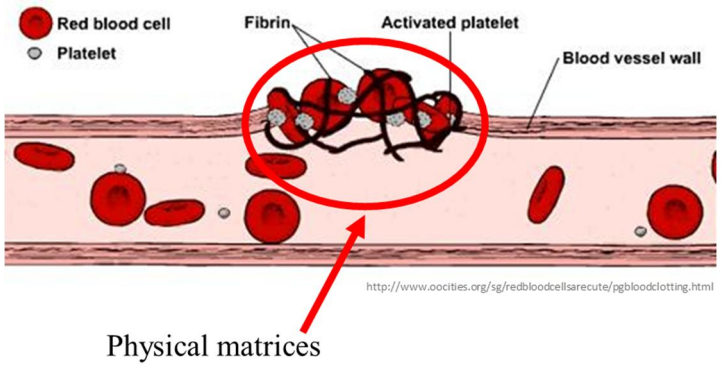


Figure 8 – Blood clots form by fibrin matrices, RBCs, and activated platelet [40]

To enable real-time visualization of single cell bio-physical interactions with its environment, a microsystem emulating a cardiovascular system needs to be fabricated from bio-compatible optically transparent polymer (e.g. PDMS). The vascular matrices that blood cells transit through are sub-micron feature sizes. Building these features from PDMS is non-trivial as it demands a sub-micron mold. This necessitates a microfabrication process with tight tolerances such that any imperfections and defects are avoided. Thus, a silicon-based fabrication process is developed to leverage the capabilities that have been created by the microelectronic industry. To form the silicon-based mold, silicon is deep etched, which creates a template into which PDMS will be directly poured. However, deep silicon etching (i.e. Bosch process) involves sequential etching and passivation cycles that tend to introduce sidewall scallops.

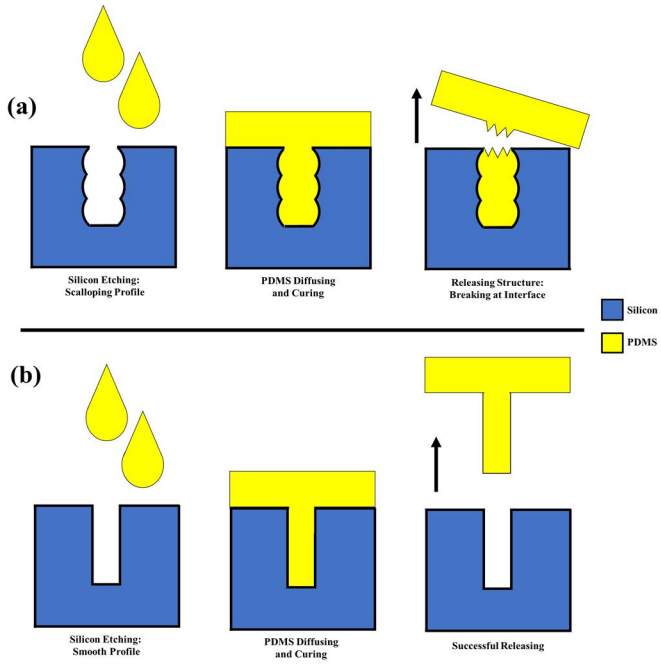


Figure 9 – Fine-resolution soft lithography: (a) failure due to scalloping on sidewall of etched feature vs. (b) smooth sidewall profile

As illustrated in Figure 9, scalloping is a fatal defect that will result in total failure as the cured PDMS may become stuck inside the mold during the releasing step. To address this issue, a scallop-free, low roughness silicon etching process is developed for nano-scale features. This process is the key enabling fabrication module for fine-grain soft lithography that allows for fabricating a wide range of nano-scale devices specifically for lab-on-chip applications.

1.5 Organization of the Thesis

Figure 10 illustrates the developed key microfabrication modules as enabling technologies for the demonstrated applications. The thesis focus will principally be

around 3D integration technologies and application driven enabling microfabrication techniques.

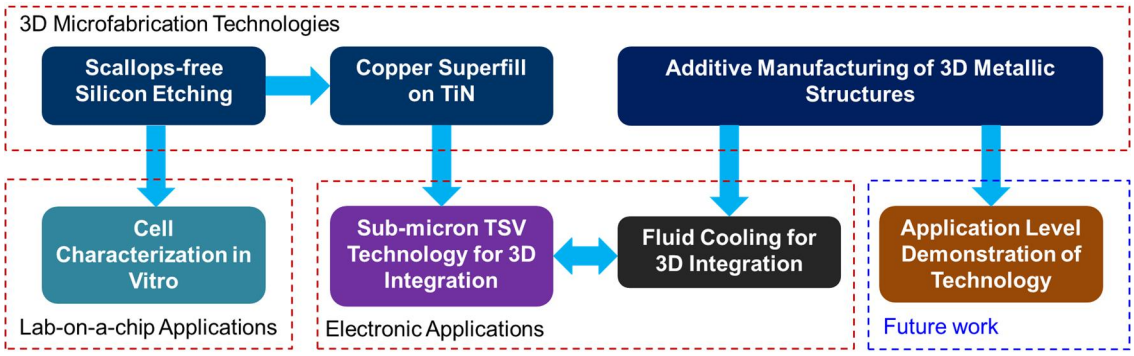


Figure 10 – Enabling technologies developed in this Ph.D. research

The first chapter outlines challenges and limitations associated with emerging 3D-IC technologies along with the solutions that are studied in this Ph.D. thesis. We discuss technology bottlenecks in the semiconductor industry that are the driving motivations for the continuous research efforts in the field and outline the developed solutions that would address not only those challenges but also benefit other areas such as the life sciences. Chapter 2 explores a sub-micron deep silicon etching process that features a scallop-free profile as an enabler not only for scaling TSV technology but also for fine resolution soft lithography of nano-structures. Chapter 3 presents a demonstration of sub-micron TSV technology using a novel copper electrodeposition technique on titanium nitride film. Chapter 4 addresses thermal challenges in integrated systems by presenting an intra-stack heat removal solution using a developed monolithic fluid cooling system. We utilize subtractive microfabrication techniques for building a monolithic fluidic heatsink. However, Chapter 5 tackles the possibility of integrating heat dissipating microstructures on a silicon die via a novel

metal 3D printing technology that could potentially replace the core microfabrication techniques employed in Chapter 4. Accordingly, Chapter 6 proposes to leverage the developed 3D printing technology to demonstrate the additive manufacturing of fluid-cooled heatsinks on silicon. In the last chapter, we discuss technology trends and propose envisioned applications and potential extensions of the presented research in this Ph.D. dissertation.

1.6 Research Contributions

1.6.1 Fluid Cooling Solution for Very High Heat Flux Density Hotspot

Cooling of large heat fluxes generated across the entire silicon die as well as concentrated hotspots necessitates an active cooling solution. In this presented research, we demonstrated a novel cooling strategy that 1) enables hotspot heat removal independent from background cooling, 2) significantly reduces the need for a chilled coolant, 3) provides independent and flexible control over two inlets in terms of coolant temperature and flow rates. Moreover, we have demonstrated a very large heat dissipation of 6.175 kW/cm^2 on a hotspot with the coolant at room temperature.

1.6.2 Sub-Micron TSV Technology

We demonstrated void-free fabrication of sub-micron diameter TSVs for dense 3D interconnections. Scaling TSVs is challenging as the fabrication of smaller diameters using conventional processes faces limitations. In this presented research,

TSVs with a sub-micron diameter and a 16:1 aspect-ratio in bulk silicon are fabricated and characterized. The demonstrated sub-micron TSV technology presented in this work was enabled by two newly developed key fabrication modules: 1) demonstration of low roughness scallop-free nano-Bosch silicon etching, and 2) demonstration of void-free Cu electrodeposition directly on a TiN diffusion barrier film.

1.6.3 Lab on Chip: In Vitro Characterization

For the first time, we have visually characterized the interaction of blood cells with their surrounding environment. We developed a microfabrication process that enables fine resolution soft lithography. This allowed us to fabricate optically transparent sub-micron devices integrated with microfluidics for the real-time characterization of the bio-physical behavior of blood cells under different physical environments.

1.6.4 Metal 3D Printing of Copper at the Micron-Scale

All existing metal 3D printing technologies primarily rely on either 1) the dispensing of material, 2) operating in liquid phase, or 3) high temperature processes. Unlike available metal 3D printing techniques, in this Ph.D. thesis, a new approach based on electro-brush plating is developed for the additive microfabrication of copper (Cu) features. Moreover, low Cu resistivity (6.34 μΩ-cm) from our metal 3D printer is achieved and when compared to other metal 3D printers for feature sizes on the order of hundreds of microns, our measured Cu resistivity is at least 2 times

lower than what is reported in the literature. This enables a path towards many electronic and thermal applications that would greatly benefit from micron-scale metal 3D printing technologies.

CHAPTER 2. SCALLOP-FREE SILICON ETCHING: ENABLING 3D MICROFABRICATION TECHNOLOGY

The ever-growing microelectronic industry is based upon micro-fabrication and nano-fabrication processes that are mainly developed for silicon. The exponential growth of microelectronics in manufacturing complexity, applications, and cost refinement of production since the 1960s provides a new opportunity for emerging technologies to leverage and utilize well-developed micro/nano fabrication techniques. Thus, it is likely inevitable to use silicon as the core material for developing essential building-blocks of emerging applications. In this chapter, a sub-micron etching process is presented as a key fabrication module for processing silicon for two distinct applications. The presented silicon etching process exhibits high etching selectivity and a scallop-free profile that allow fabrication of high aspect-ratio sub-micron TSVs 1) for heterogenous 3D integration of electronics and 2) high-resolution soft lithography of bio-compatible polymers for lab-on-chip applications, respectively. In this chapter, 1) details of the etching process will be discussed, and 2) a lab-on-chip application that leverages this etching technology along with other advanced fabrication techniques— electron-beam-lithography (EBL), photolithography, and so forth— will be elaborated upon. It is important to mention that the bio characterization of the fabricated lab-on-chip device is made possible through collaboration with Dr. Wilbur A. Lam and Dr. Jordan C. Ciciliano at Georgia Tech, Biomedical Engineering Department.

2.1 Deep Silicon Etching: Bosch Process

Plasma enhanced RIE etching of silicon is extensively used in precision shallow etching of silicon as the key enabler for cost-effective fabrication of 3D tri-gate FinFET transistors in bulk silicon [41]. This new generation of transistors paved the way for further scaling of transistor dimensions as predicted by Moore's law while keeping the leakage current small at low threshold voltages. However, RIE is inherently an isotropic etching process which is not suited for deep silicon etching since anisotropic performance is needed for minimum unwanted lateral etching (i.e. undercut and tapered etching) [42].

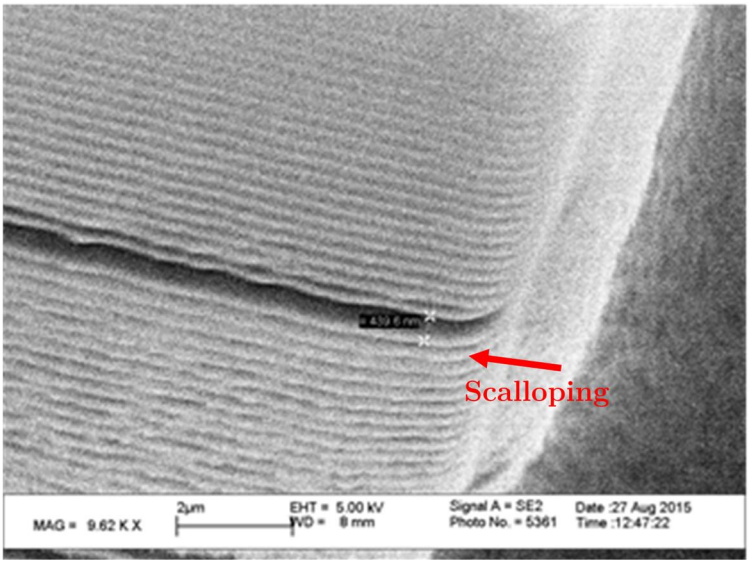


Figure 11 – SEM image of sidewall scalloping resulting from the standard Bosch silicon etching process

To achieve anisotropic dry etching of silicon, passivation cycles are added to the RIE process. The passivation mechanism is based on the chemical formation of a thin layer of etch-resistant polymer on the silicon surface by introducing

fluorocarbon gases (e.g. C_4F_8) in distinctive process cycles. This passivation step follows every etching cycle to protect the sidewall of an etched trench against the isotropic RIE etching process and hence makes it possible to achieve nearly anisotropic etching performance. This deep silicon etching process is named after German company Robert Bosch GmbH which developed this process. However, the Bosch process typically exhibits a sidewall scalloping profile (see Figure 11) as a result of the alternating etching and passivating cycles [43]. Moreover, the Bosch process is dependent upon the geometry of features being etched. Figure 14 shows excessive undercut, poor selectivity, and pronounced sidewall roughness resulting from the Bosch etching of sub-micron features (baseline process parameters are employed). To minimize undercut, achieve smooth sidewall, and increase silicon-to-mask etch selectivity, the process parameters should be adjusted accordingly. The Bosch process involves sequential etching and passivation cycles with different process parameters such as cycle duration, plasma power, chamber pressure, gases' flow rates, and silicon substrate temperature. These process parameters non-linearly influence the overall etching performance, which makes the optimization procedure challenging to model. Therefore, there is significant effort in this space to address deep silicon etching challenges [43], [44], [45], [46]. These solutions for etching sub-micron size features, however, still exhibit limitations [47], [48], [49], [50], hence necessitating further development. [47], [48], [49], [50], hence necessitating further development.

2.1.1 Patterning and hard-mask etching

As patterning of sub-micron features using traditional photolithography is non-trivial, EBL is used. However, EBL photoresist exhibits poor selectivity for the deep silicon etching step. This necessitates transferring the pattern from the photoresist to a hard-mask. Thus, approximately 200 nm of PECVD SiO_2 deposited onto the silicon wafer is used as the hard-mask. Next, a 900 nm thick ZEP520A photoresist is spin-coated on the SiO_2 layer at 500 rpm for 60 seconds followed by a pre-exposure bake of 180 ℃ for 2 min using a hotplate. Arrays of square-shaped features are exposed with different doses to experimentally determine the proper base exposure dose.

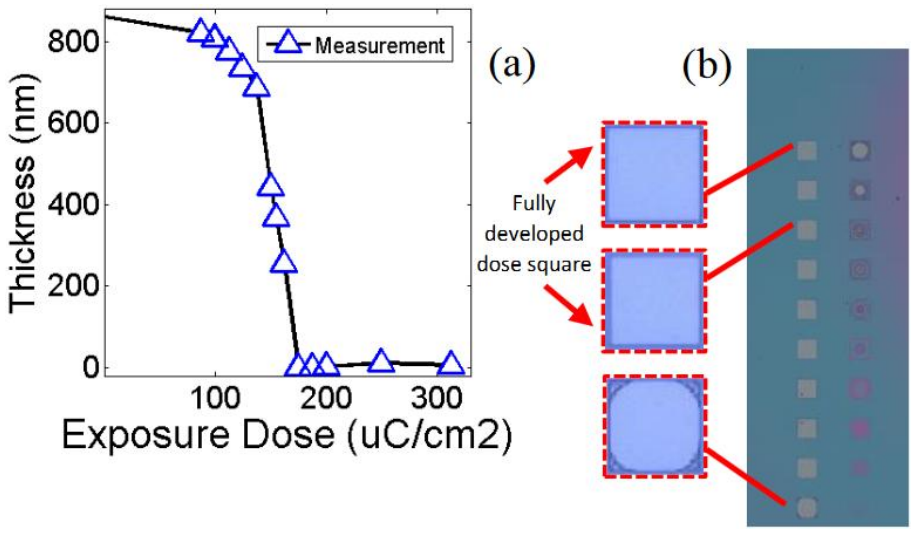


Figure 12 – (a) Different exposure doses vs. remaining thickness of photoresist after development step (b) Optical image from remaining

photoresist after development as a control procedure for monitoring required exposure dose.

Figure 12(a) shows exposure dose versus the remaining thickness of photoresist in 75 × 75 µm squared-shape features after developing in Amyl Acetate for 2 min. These control features (i.e. dose squares) are designed to monitor photoresist thickness variations and required adjustments on the exposure dose. The optimum base dose is estimated to be 200 µC/cm^2 considering the first fully developed dose square with sharp corners, as shown in Figure 12(b).

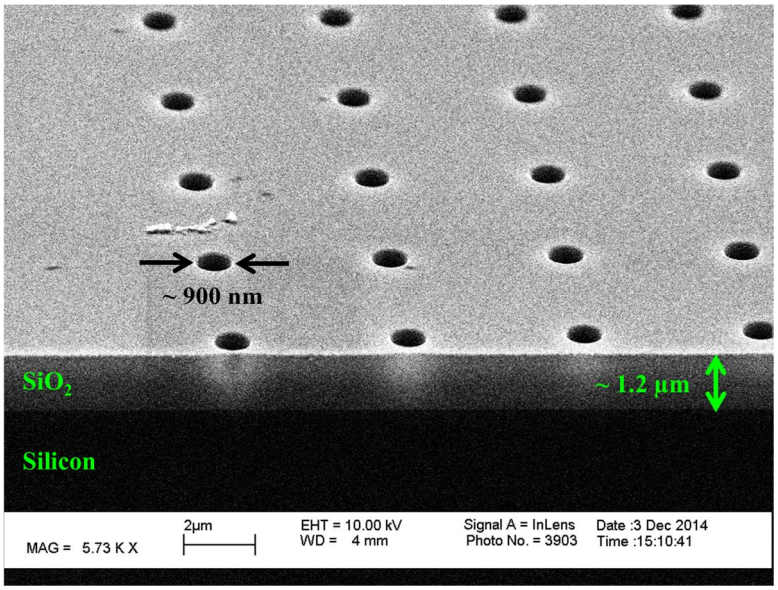


Figure 13 – The 900 nm diameter features are etched into the dielectric stacks.

Next, the hard-mask is dry etched using a mixture of fluorocarbon gases (C_4F_8 and CF_4), and O_2 in an ICP system [51] to transfer the patterned features from the photoresist to the hard-mask. Figure 13 shows the SEM image of the etched pattern

into the hard-mask after stripping off the photoresist and cleaning the sample. The silicon wafer is now ready for a deep silicon etching step.

2.1.2 Experimental Exploration: Etching Process Optimization

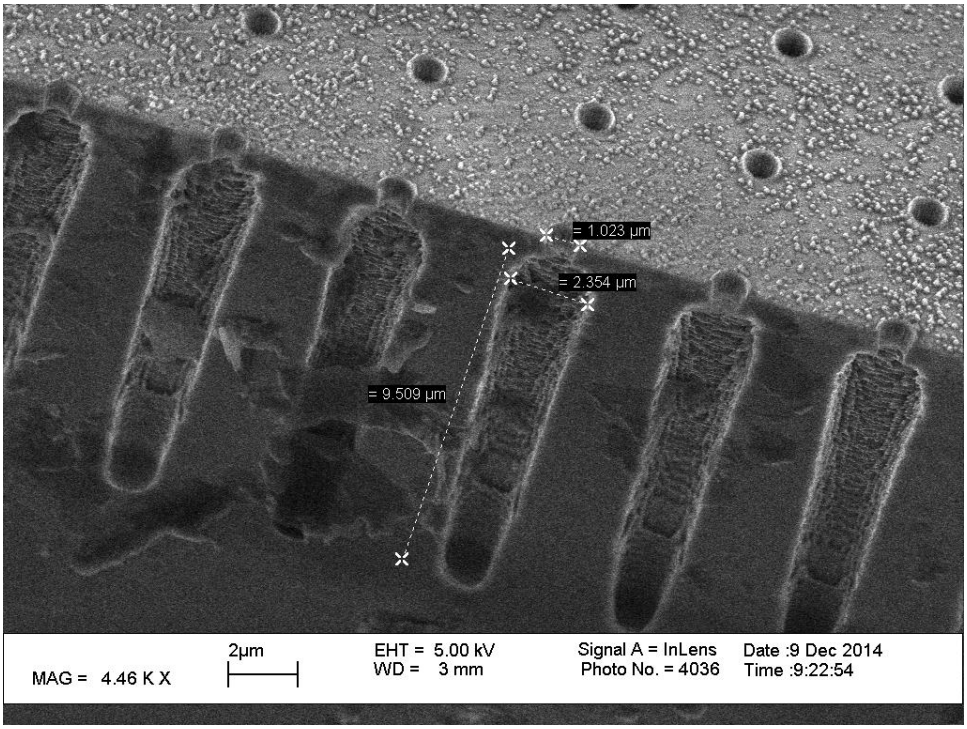


Figure 14 – Cross-sectional SEM image of etched sub-micron features using Bosch etching at baseline process parameters

In this work, an experimental approach is adopted for achieving reasonable etch results for the target application. To limit the possible number of different combinations with the process parameters, only the effects of the passivation cycle duration, the etching cycle duration, and O_2 flow rate are explored in this effort. Adding O_2 to SF_6 in the etching cycle forms a thin SiO_xF_y passivation film that

improves anisotropic etching [52], which is believed to result in smaller undercut and a smoother sidewall [53]. Thus, two different flow rate ratios for SF_6 to O_2 are explored (as a function of etch-to-passivation cycle ratio) to observe undercut and selectivity behavior with all other process variables (ICP power, chuck power, chamber pressure, and chuck temperature) kept constant at the base conditions.

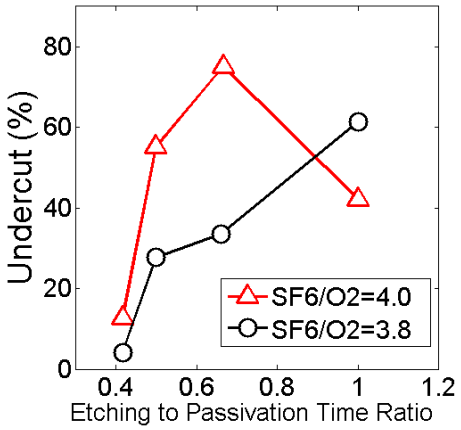


Figure 15 – Undercut (lateral distance etched under mask from mask opening) vs. etching/passivation ratio

Figure 15 shows that the smallest undercut (lateral distance etched under mask from mask opening) is achieved at higher O_2 flow rates but the corresponding data point on the selectivity (the ratio of the to-be-etched material etching rate to the mask etching rate) graph (Figure 16) does not demonstrate the highest achievable selectivity. However, minimizing undercut is a more critical objective since poor selectivity could be mitigated by depositing a thicker hard-mask layer. Indeed, this indicates a strong non-linearity between the process parameters, necessitating an experimental optimization for different feature sizes.

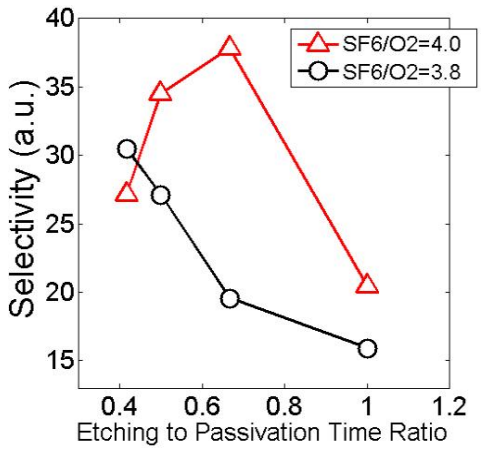


Figure 16 – Selectivity (the ratio of the to-be-etched material etching rate to the mask etching rate) vs. etching/passivation ratio

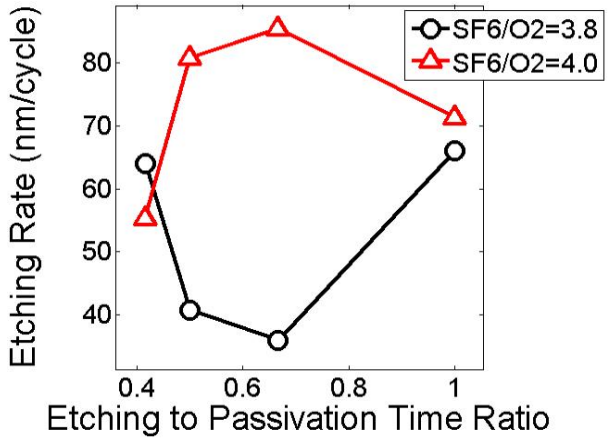


Figure 17 – silicon etching rate vs. etching/passivation ratio

Sidewall scalloping and etch rate (see Figure 17) are simultaneously monitored for each experiment by cross-sectional SEM imaging. Figure 18 shows an etched silicon via that corresponds to the minimum undercut data-point in Figure 15 and a 31:1 selectivity. This reasonable selectivity and undercut results from a

longer passivation cycle and an etch cycle with a higher O_2 content. Table 2 compares the Bosch process parameters at baseline with optimized etching recipe.

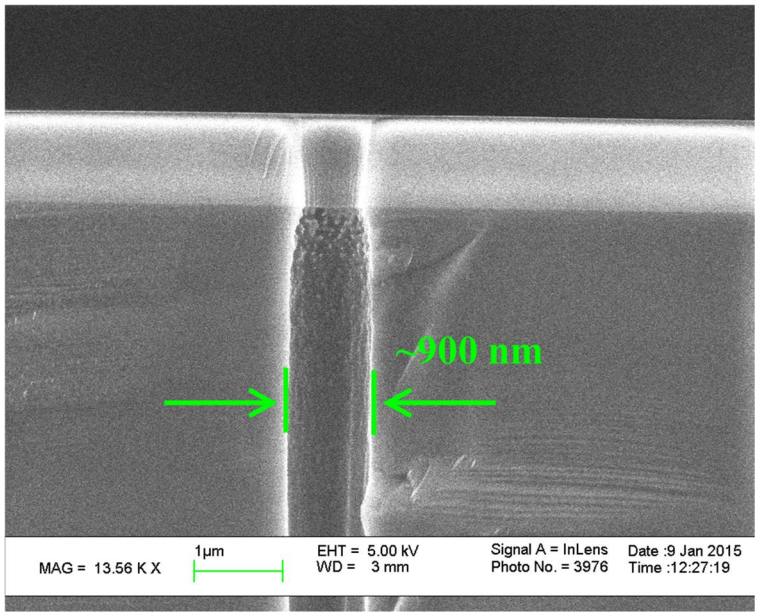


Figure 18 –SEM image of the etched feature exhibits smooth sidewall with no scalloping

Table 2 – The Bosch process parameters at baseline vs. optimized etching recipe

Process Parameter	Baseline Parameters	Optimized Parameters for Minimum Undercut
Etching Time	11 sec	5 sec
Passivation Time	8 sec	12 sec
C_4F_8 flow rate	100 sccm	100 sccm
SF_6 flow rate	130 sccm	35.0 sccm
O_2 flow rate	13.0 sccm	9.0 sccm
Etch-Cycle ICP RF power	600.0 W	600.0 W
Passivation-Cycle ICP RF power	600.0 W	600.0 W
Etch-Cycle ICP RF power	11.0 W	11.0 W
Passivation-Cycle ICP RF power	0.0 W	0.0 W
Helium Cooling Flow Rate	40 sccm	40.0 sccm

2.2 Scaling Bio-compatible Polymeric Structures Using Fine-Resolution Silicon Etching and Soft Lithography Technique

Using soft lithography technique and a fine resolution silicon etching process, we demonstrated arrays of sub-micron diameter Polymeric pillars that are integrated within a microfluidic system. The pillars resemble physical features that allow to recapitulate, at the single cell level, bio-physical interactions between vascular matrices and blood cells. Soft lithography technology is widely employed to microfabricate 3D structures using the molding-embossing approach [54]. This process allows utilizing of a wide range of materials to caste or emboss a mold with good level of controllability over process conditions [55]. Even the material property could be tailored using different chemistries [56], for example, to achieve biocompatibility for biological applications. Moreover, mold reusability enables cost effective mass manufacturing of micro/nano structures that is specifically beneficial for cost-sensitive applications. It is worth to mention that the top-down processing (e.g. etching) of polymers is challenging due to the lack of an anisotropic etching process for etching polymers [57]. Scaling soft lithography technology, however, is increasingly challenging since the very first step of this process, which is microfabricating a template or elastomeric stamp, exhibits limitations. For instance, processing silicon to microfabricate a mold comes with number of imperfections such as surface roughness, undercuts, and scalloping, among others that directly impact the quality of the over casted polymer. For smaller feature sizes, these fabrication imperfections are even more pronounced as the size of patterned features are comparable to the size of scallops, undercuts, and even the roughness profile. Thus, the low-roughness scallop-free deep silicon etching process that was developed under

this Ph.D. thesis was also discovered to be well-suited to fabricate the soft lithography mold template with sub-micron feature sizes. The following section elaborates on details of a microfabricated lab-on-chip device, based on this fine-grain soft lithography technology, that enables the study of bio-physical interactions of blood cells with their surrounding environment *in vitro*.

2.3 Motivation for Studying Blood Cells

The role of bio-physical cues in regulating cell activity has been recently studied in the field of cell mechanics. There is limited knowledge about effects of physical matrices on the three types of blood cells—red blood cells (RBCs), platelets, and neutrophils and how a cell's morphology is altered under different microenvironments. Decoupling bio-physical cues of physical matrices from biochemical cues paves the way to a better understanding of blood diseases. For instance, the presence of schistocytes (i.e. fragmented RBCs) is known as the sign of disseminated intravascular coagulation (DIC) disease. Although the clinical existence of schistocytes has been studied in vitro and well documented, fragmentation mechanism of RBCs is poorly understood [58]. Thus, studying the bio-physical parameter space to improve our understanding of RBC damage, fragmentation, and destruction is of great interest to the development of diagnostics for different states of diseases. Furthermore, the cells in a cardiovascular system circulate under a variety of shear stress and strain; the dynamic mechanical pressures that blood cells are exposed to would cause the cells' reactions. For example, blood clotting is connected to the platelets activation and aggregation of vascular matrices such as

fibrin clots [35], [59]. However, contributing mechanisms for blood clotting are not observed in real-time. Our goal is to conduct in-vitro studies on: 1) RBCs' deformation under stress/strain forces resulting from a controlled environment consisting of vascular matrices and microfluidics, and 2) visually observing a response of platelets to controlled shear stresses.

2.3.1 Fabrication of Sub-Micron diameter PDMS Pillars, and Micro-Canals

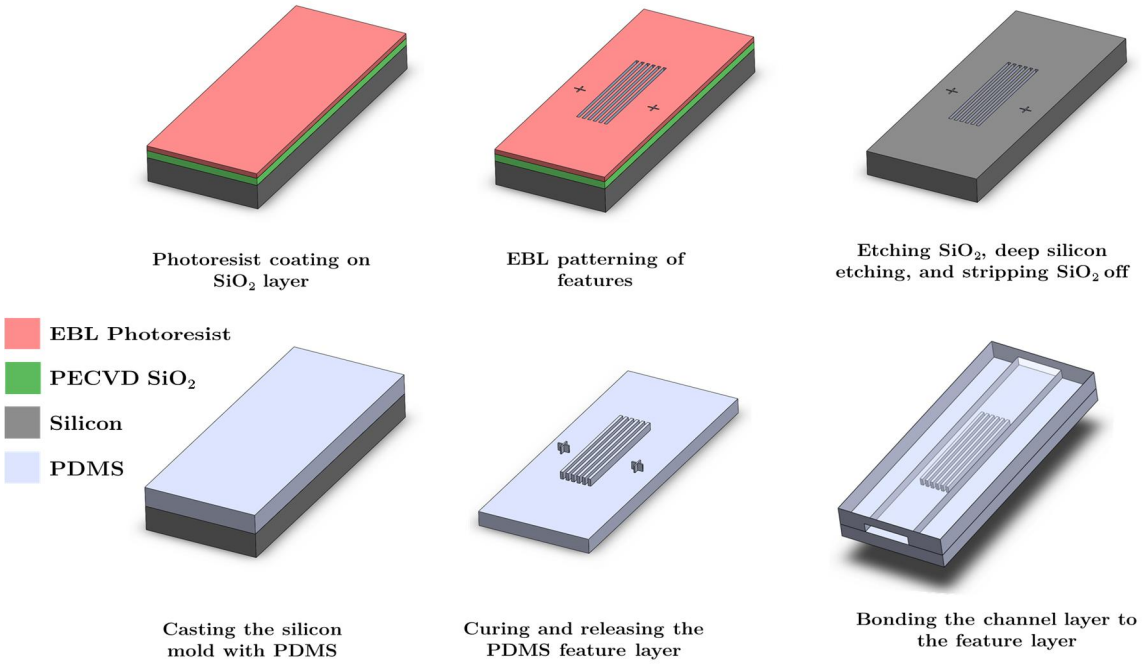


Figure 19 – PDMS micropillar and micro-canal fabrication process flow

To mimic the vascular matrices, devices are microfabricated with features on the order of biologically relevant dimension, which is at a single-digit micron scale. Creating high-fidelity features of this dimension demand a silicon wafer template microfabricated using the developed fine-resolution silicon etching process. Figure 19

illustrates the simplified fabrication process flow of the devices; hard-mask etching, and silicon etching steps are similar to what is discussed in sections 2.1.1 and 2.1.2.

Two sperate silicon molds are microfabricated to create two different feature layers from PDMS. The first feature layer contains 900 nm diameter and 3 µm height pillars, and the second one has micro-canals of 2 µm width and 3 µm height at different lengths (varying from 2-90 µm). Prior to the casting step, the silicon mold needs to chemically be treated to become hydrophobic as it further facilitates releasing of the cured polymer from the mold. Therefore, the silicon mold after multiple cleaning steps in an Acetone bath is vapor treated with HMDS. A 10:1 ratio of elastomer to curing agent is employed for preparing the PDMS mixture. Next, the mixture is poured over the treated silicon mold and immediately the sample is transferred to a vacuum chamber and kept under very low-pressure environment (approximately 10^{-3} bar) for approximately 1 hour. This ensures that no void-defect occurs—due to gas trapping— since the polymer can diffuse into the micron-sized features without seeing any resistance from the ambient gases. Next, the PDMS is cured overnight at 60 ℃ in an oven. The SEM images shown in Figure 20, and Figure 21 confirm that the PDMS micro-canals and pillars are of the expected dimensions and fidelity.

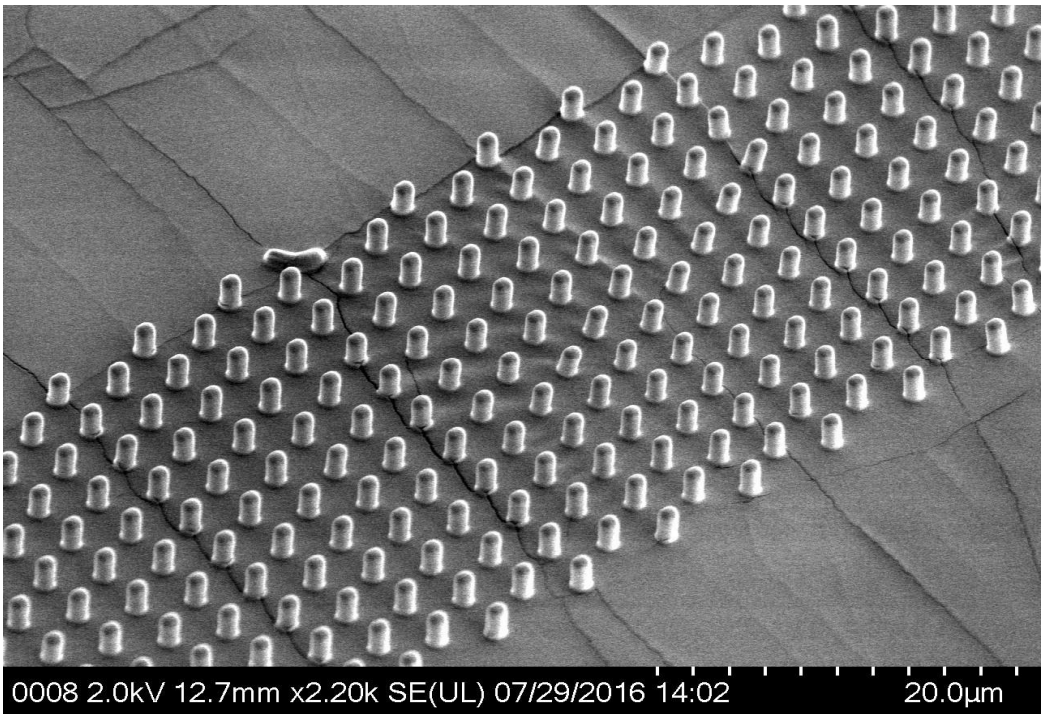


Figure 20 – SEM image of the PDMS pillars

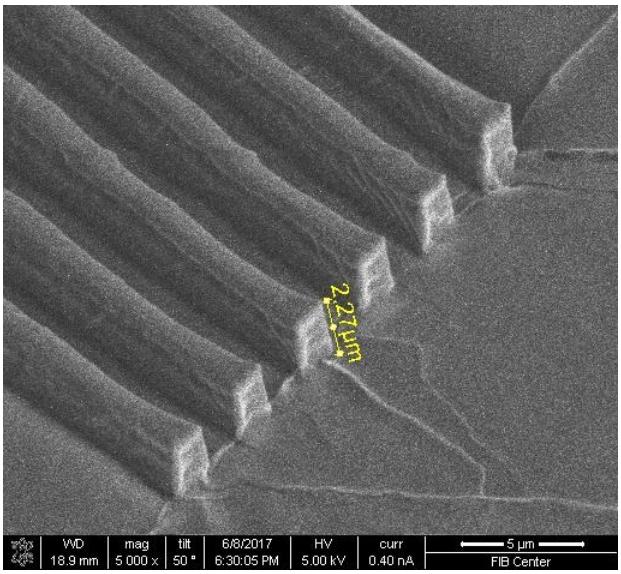


Figure 21 – SEM image of the PDMS micro-canals

To create the microfluidics (i.e. channel layer), 150 µm wide channels are templated by patterning SU-8 photoresist on a silicon wafer using optical lithography and casting over with PDMS. To cap the channel layer, the feature layer is flipped and bonded to the channel layer. This is accomplished by activating both PDMS layers—feature and channel (using the handheld Corona Treater), aligning under an optical microscope, and pressure bonded together. Finally, to achieve stronger bonds between the layers, the sample is thermally treated on a hotplate at 80 ℃ for 10 minutes. Having two separate layers to build the structure allows us to study various bio-physical systems by creating different combinations of micron-sized features and channels.

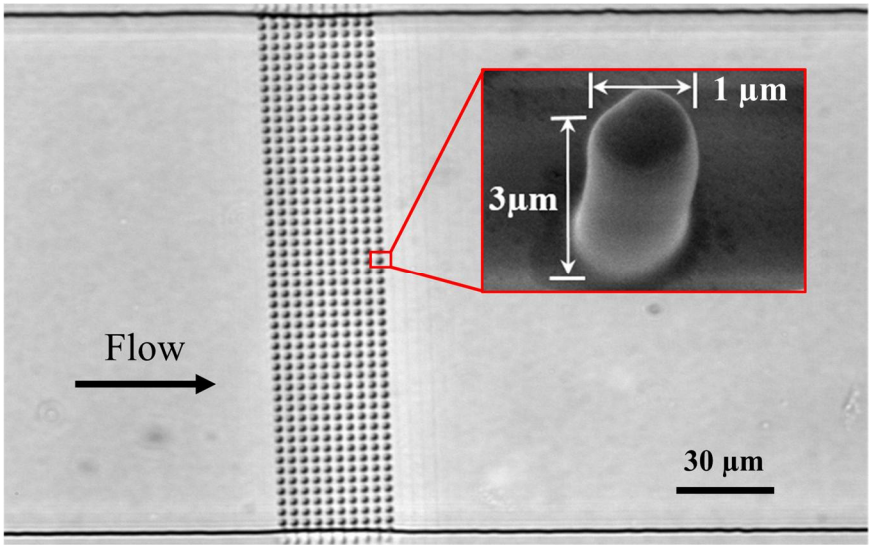


Figure 22 – Optical image from bonded channel layer to the feature layer that contains the PDMS micropillars

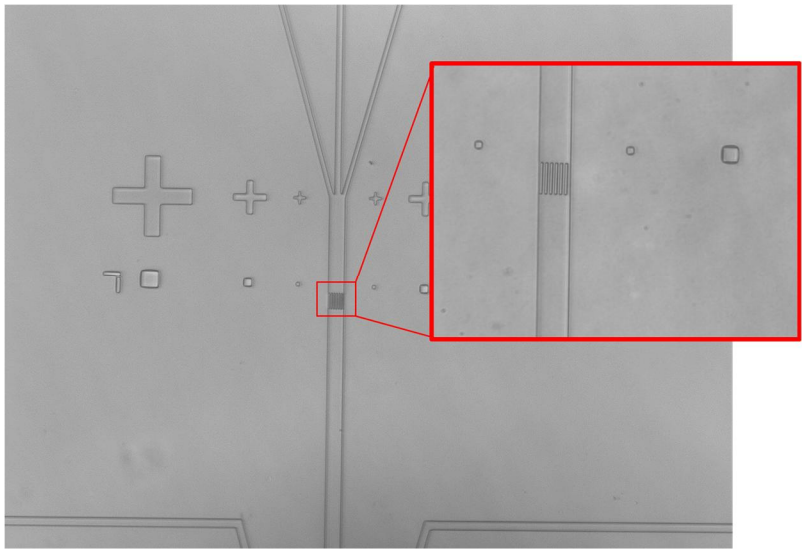


Figure 23 – Optical image from bonded channel layer to the feature layer that contains the PDMS micro-canals

To study platelet, the micropillar feature layer is bonded to a 6 µm tall channel with 150 µm width. The pillar array is placed perpendicular to the flow direction, as shown in Figure 22. To study RBCs, however, the channel is shallower (3 µm tall) which results in higher shear/strain forces necessary for stressing RBCs. The experiments conducted with the micro-canal device employ 26 µm wide and 3 µm tall channels while each canal is approximately centered between inlet and outlet ports (see Figure 23).

2.4 Device Characterization

The physical presence of fibers introduces shear stress on blood cells [58]. The shear/strain forces are identified as a bio-physical activator of platelets [60], [61], [62]. It has been shown that platelet activity depends on the magnitude of shear

forces and the size of a shear microgradient [63]. The PDMS pillars, therefore, create controlled regions of high shear as well as stagnant zones to observe bio-physical interaction of platelets with a PDMS matrix while the biological factors are absent.

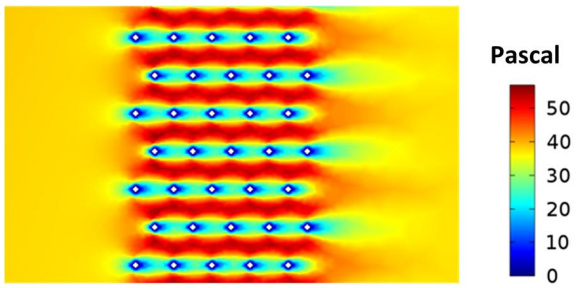


Figure 24 – Simulated shear stress created by the PDMS pillars at 0.2 µL/min

To properly emulate this shear stress in the experiments in order to observe the effect of stress/strain forces on a single cell, the flow rate of fluid in the channel should accordingly be chosen. Thus, COMSOL modeling is carried out to estimate the required flow rate through numerical simulations for the laminar flow of an incompressible Newtonian fluid, assuming a constant inlet flow rate and atmospheric pressure at the outlet. For the pillar device, it is found that a flow rate of 0.2 µL/min creates a maximum shear stress of 55 Pa between the rows of pillars while there are notable dead zones behind the pillars as illustrated in Figure 24. The micro-canal device, however, exhibits constant shear stress throughout the canal at 2,000 Pa independent of canal length, with a flow rate of 0.5 µL/min. It is worthwhile to mention that the length of the canal only influences the pressure drop from the inlet to the outlet.

2.4.1 Platelets and Clump Formation

As shown in Figure 25, an extensive platelet aggregation and the consequent formation of an occlusive mass that extends to the edges of the micropillar array has been recorded. This in *vitro* study confirms that the shear microenvironment created by the physical presence of fibers is the exclusive reason (if not the only) for the activation of platelets in the absence of biological ligands and platelet agonists [58].

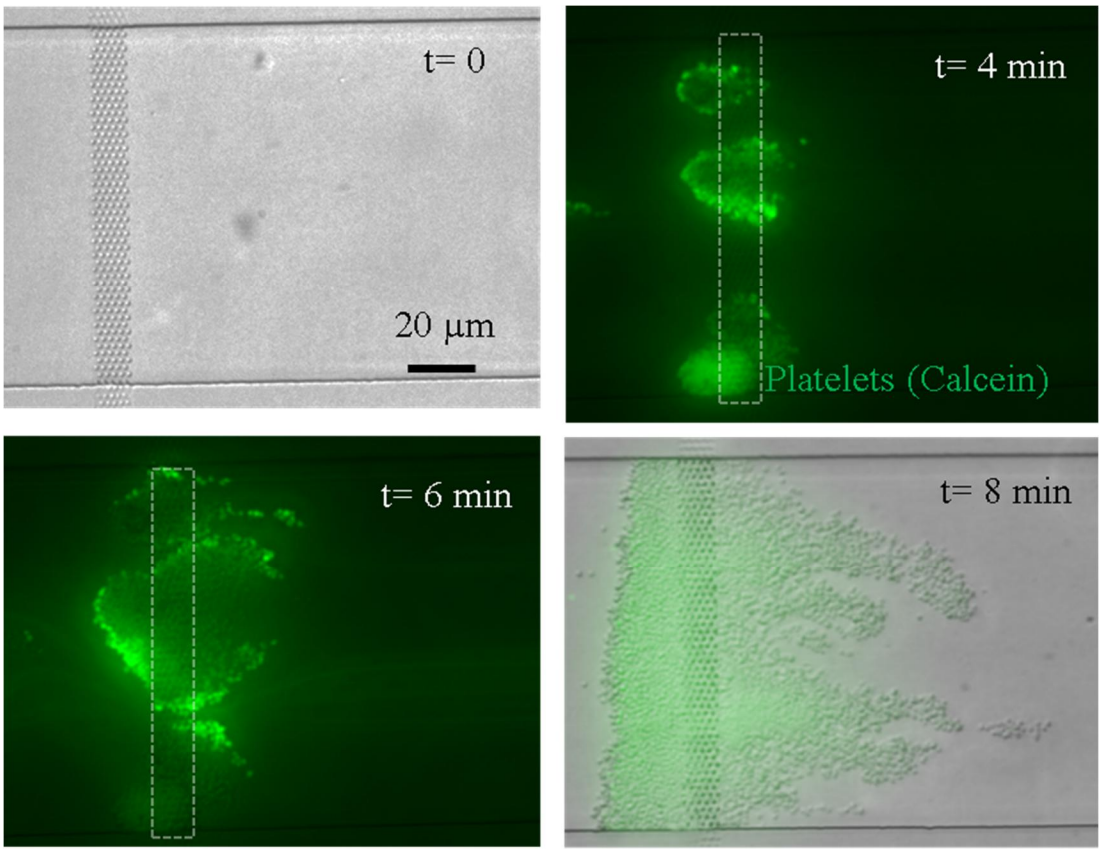


Figure 25 – Platelet aggregation due to shear stress as a bio-physical activator

2.4.2 Red Blood Cells Deformation

A high level of deformability is observed in RBCs even at large shear forces. Mechanical properties of RBCs have been extensively reported in the literature and their deformation capability is widely studied [64], [65], [66]. However, the RBC's mechanical deformability could be disrupted (e.g. due to presence of heart valve implants), which results in altering the cell membrane, causing RBCs to severely fragment. Thus, different aberrant RBC morphologies such as schistocytes, tear drop shaped cells, bite cells, dacrocytes, and echinocytes are believed to be linked to the mechanical disruptions [59].

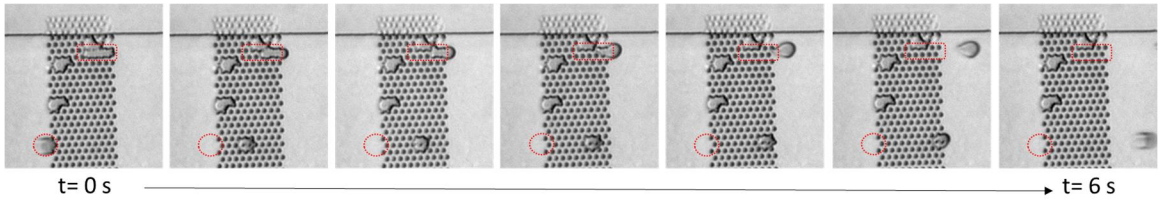


Figure 26 – RBCs transit through the PDMS pillars while showing no morphological changes.

Figure 26 shows that RBCs exhibit no morphology changes while transiting through the PDMS pillar array. This is because the shear force elastically deforms the cells and not enough to rupture them. This outcome is an expected result as the COMSOL simulation suggests the maximum shear stress in between of the micropillars is 55 Pa while the literatures suggest the required shear force for fragmenting the RBCs is between 150 to 300 Pa.

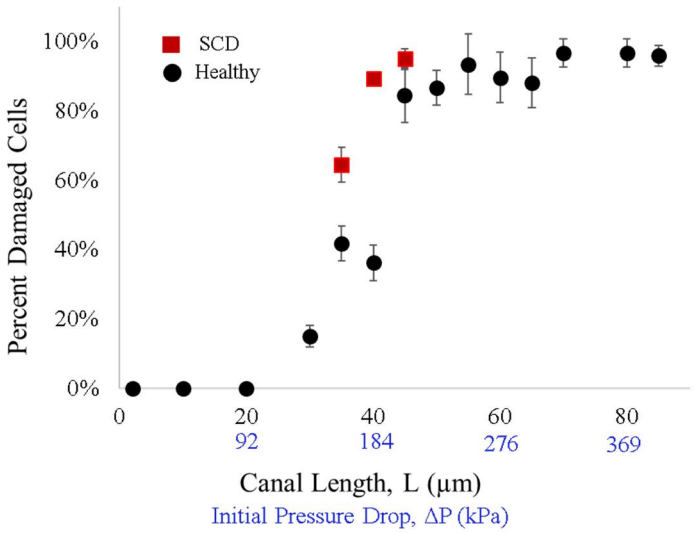


Figure 27 – As canal length increases, percent of damaged cells increases

To increase the shear force, the micro-canal devices are designed to stress RBCs over various lengths, ranging from 10 µm to 80 µm. As the results of the experiments in Figure 27 suggest, the critical length for the micro-canal is ~30 µm in order to start exposing the cells to a level of destructive shear stress. Interestingly, the result of our study finds preliminary evidence that RBCs from a patient with SCD are more sensitive to shear stress, fragmenting more readily than RBCs from a healthy donor (see Figure 27). Figure 28 shows a time lapse of sickle RBCs emerging from 40 µm long micro-canals, exhibiting various morphological abnormalities, including microspherocytes (black arrows), ghosts (white arrows), and schistocytes (green arrows). This observation implies that RBCs fragmentation profile shifts as they are under different pathologic conditions.

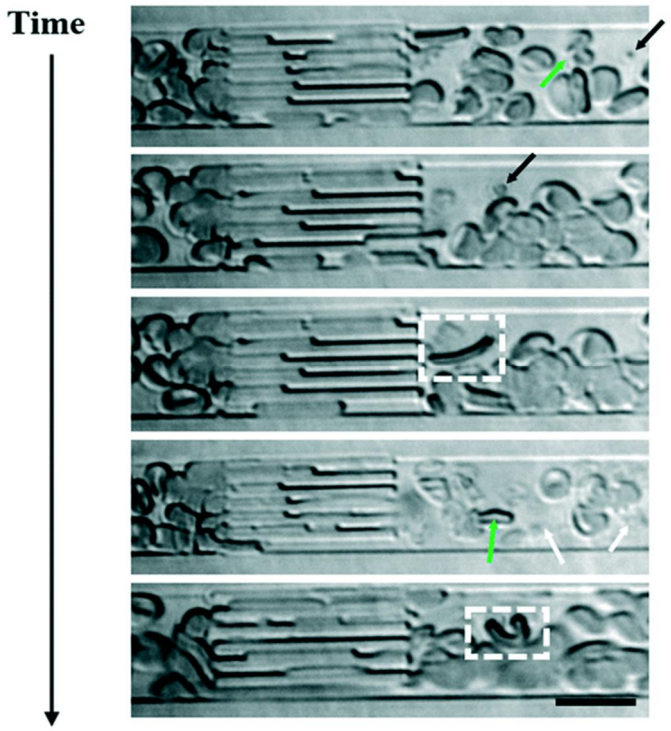


Figure 28 – A cell appears to be sickled after transit (white dotted box).

CHAPTER 3. FINE-GRAIN 3D INTEGRATION OF ELECTRONICS

The continuous demand for denser integration, lower power consumption, and higher-bandwidth density requires developing increasingly complex interconnect technologies [67]. For instance, three-dimensional integrated circuits (3D-ICs) are being explored as an innovative approach [68] to address the relentless need for dense interconnects with lower latency and energy dissipation through shortening the interconnect length [69], [8]. One form of 3D-IC is enabled by vertically stacking silicon tiers and interconnecting these tiers using TSVs. This approach represents a promising technology to keep pace with Moore's law [14] and incorporates the modular design benefits of a heterogeneous architecture [1]. TSV geometry, especially diameter, largely determines the electrical attributes and mechanical reliability of the interconnects as well as the 3D stack and motivates the need for scaling TSV dimensions. For example, a 10 µm long on-chip wire with a 10 µm diameter TSV exhibits a 30 ps delay while the same length on-chip wire with a 5 µm diameter TSV exhibits an approximate latency of 10 ps [70]. Moreover, reducing the TSV diameter can significantly mitigate the stresses related to copper (Cu) expansion as the mechanical stress is proportional to the square of the TSV radius. Relieving the mechanical stress is further beneficial as it results in a smaller keep-out-zone (KoZ) [71]— which is designed to guard active devices against the adverse proximity effects of TSVs [72]. Scaling TSVs is challenging as the fabrication of smaller diameters using conventional processes faces limitations [73]. This is due to the strong

dependency of both the via etch rate and metallization processes on the via aspect-ratio (AR) and diameter. A diffusion-barrier and conductive seed-layer deposition as the first steps of metallization are typically preformed using magnetron sputtering deposition [74], [75]. However, this method of material deposition is not effective for the fabrication of high aspect-ratio scaled TSVs as it may cause the TSV opening diameter to decrease before the via sidewall is fully coated [73]. This issue is caused by prolonged sputter deposition time, which is necessary to ensure continuous film formation as the material flux density at the bottom of TSV is limited.

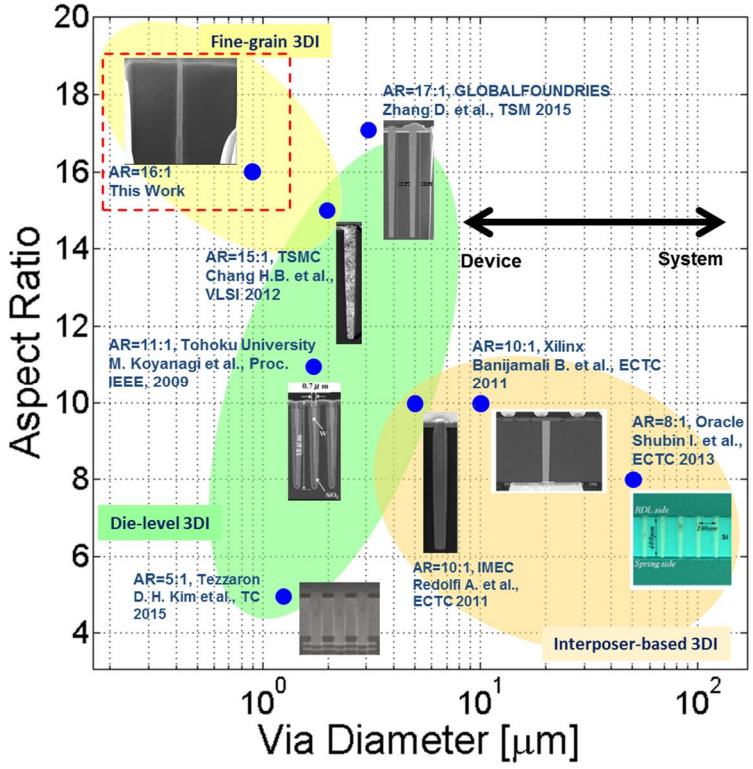


Figure 29 – TSV aspect ratio versus diameter for TSVs in the literature

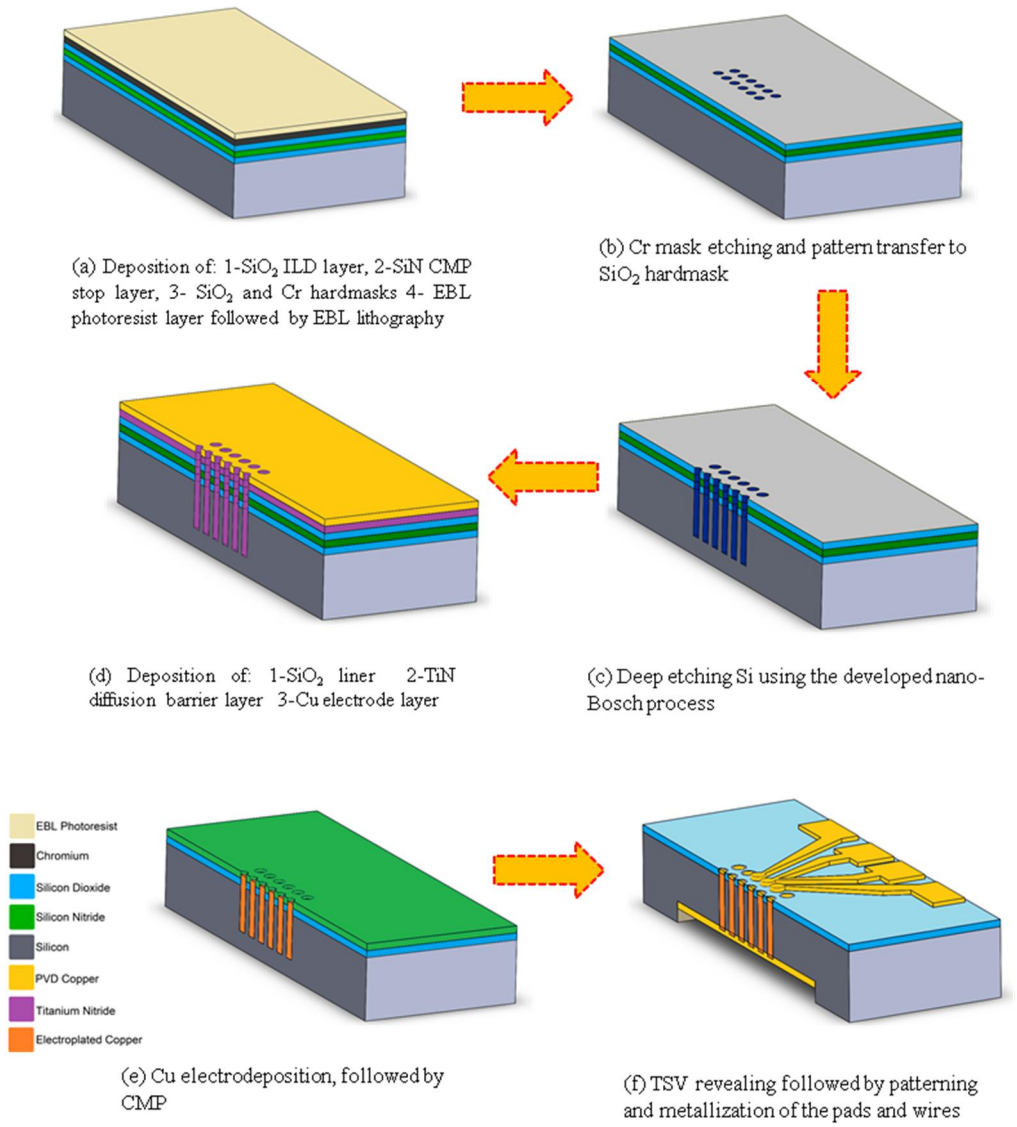


Figure 30 – Fabrication process flow

Despite the relentless efforts to reduce TSV footprint [76], [77], [78], [69], [79], [80], [81], virtually no results have been reported for high aspect-ratio (greater than 10:1) Cu TSVs (based on superfilling) in bulk silicon with total diameters below one micron, as shown in Figure 29. In this chapter, TSVs with sub-micron diameter and 16:1 aspect-ratio are fabricated and characterized. The fabrication process

presented in the next section discusses the key enabling modules developed for scaling TSV technology. This includes: 1- development of low roughness and scallop-free nano-Bosch silicon etching, and 2- a demonstration of void-free Cu electrodeposition directly on a titanium nitride (TiN) diffusion barrier film. Lastly, the electrical resistance and ampacity of the fabricated sub-micron TSVs are measured using the 4-wire Kelvin probe technique.

3.1 Surface Preparation and Electron Beam Lithography

The simplified fabrication process outlined in this section is illustrated in Figure 30. A 300 nm thick SiO_2 inter-dielectric layer (ILD) is thermally grown at 1050ºC using a wet oxidation furnace. To protect the ILD layer during the Chemical mechanical planarization (CMP) step, approximately 500 nm thick Si_3N_4 layer is deposited using plasma-enhanced-chemical-vapor-deposition (PECVD) as the CMP stop layer. Next, a 500 nm thick PECVD SiO_2 layer is deposited as the dielectric hard-mask followed by deposition of a 100 nm thick Chromium (Cr) as the metal mask. The Cr mask is a transition hard-mask used for etching 1.3 to 1.5 µm thick dielectric layers and for transferring the pattern from the softmask (EBL photoresist) to the dielectric hard-mask. Next, a 900 nm thick ZEP520A photoresist is spin-coated on the Cr layer at 500 rpm for 60 seconds followed by a pre-exposure bake of 180 ºC for 2 min using a hotplate (see Figure 30(a)). Next, arrays of circular features are patterned on ZEP520A photoresist using EBL at 200 µC/cm² exposure dose and then developed in Amyl Acetate for 2 min.

3.2 Hard-mask Etching: Chromium and SiO_2

The Cr mask enables etching of the 1.5 µm thick dielectric layers since EBL photoresist is not thick enough to etch the dielectric layers (based on its etch selectivity). Fine resolution Cr mask dry etching (step (b) in Figure 30) is performed using Chlorine (Cl_2), Oxygen (O_2), and Hydrogen (H_2) gases in an inductively coupled plasma (ICP) system [82] and Table 3 shows the process parameters. Figure 31 shows Cr etch rate characterization for the dose squares using a contact profilometer with respect to DC bias of the chuck RF coil.

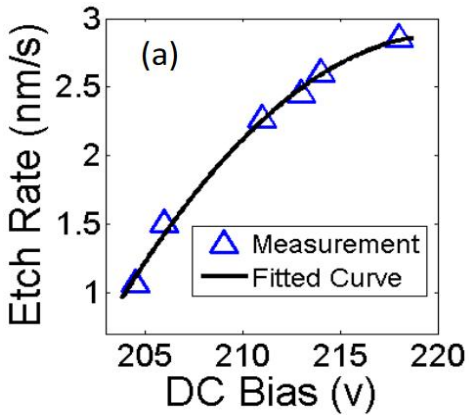


Figure 31 – Cr etching rate variation indicated by DC bias fluctuation

Table 3 – Process parameters for etching Chromium hard-mask

Process Parameter	Setpoint
Chamber pressure	10 mTorr
Cl_2 flow rate	80 sccm
H_2 flow rate	18 sccm
O_2 flow rate	26 sccm
ICP RF power	50.0 W
Chuck RF power	500 W
Helium cooling	Yes

Since the etch rate of the sub-micron features is slower than a control sample that contains larger feature sizes, 10% over etching is performed to ensure that the sub-micron features are fully etched, as shown in Figure 32(b). Next, the remaining ZEP520A on the Cr mask is stripped off in 1165 solvent at 80 ºC for 45 min prior to etching the SiO_2 mask. Eventually, the SiO_2 hard-mask is dry etched using a mixture of fluorocarbon gases (C_4F_8 and CF_4), and O_2 in an ICP system [51]. Table 4 summarizes SiO_2 etching process parameters.

Table 4 – Process parameters for etching SiO_2 hard-mask

Process Parameter	Setpoint
Chamber pressure	5 mTorr
Ar flow rate	4.0 sccm
CF_4 flow rate	15.0 sccm
O_2 flow rate	4.0 sccm
C_4F_8 flow rate	16.0 sccm
ICP RF power	400.0 W
Chuck RF power	400.0 W
Helium cooling	Yes

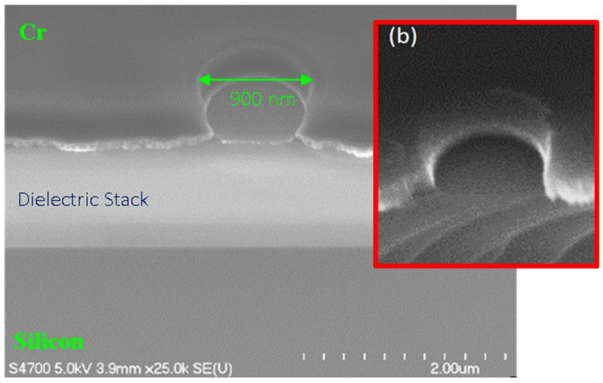


Figure 32 – SEM cross-section from dry etched features on the Cr hard-mask

3.3 Deep Silicon Etching

Details of silicon etching process are discussed in CHAPTER 2. The process is developed to minimize undercut and maximize etching selectivity as key enabling modules for microfabricating sub-micron 3D structures. The relatively smooth sidewall that is achieved through the developed etching process could be crucial for high aspect-ratio TSVs as modeling shows that excessive scalloping on the TSV sidewall negatively impacts TSV reliability and electrical characteristics [83], [84]. Figure 33 illustrates an SEM cross-section image of deep-etched TSVs in silicon and, as seen, no scalloping is observed on the TSV's sidewall.

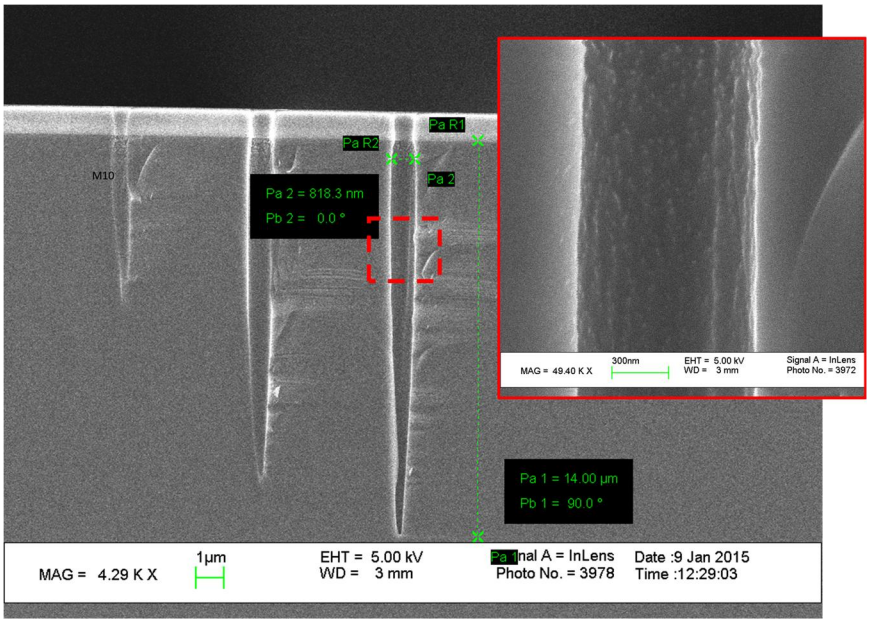


Figure 33 – SEM cross-section image of deep etched trenches in silicon; No scalloping is observed on the sidewall.

3.4 Metallization: Copper Superfill Process

Void defects in the Cu core of the TSVs are a major manufacturing reliability concern, and thus, must be explored for the TSV under consideration. Depositing a diffusion-barrier layer along with a conductive seed-layer on the TSV sidewalls are the very first steps of the metallization process that significantly impact the subsequent Cu electrodeposition. Defect-free coverage of the seed-layer on the TSV sidewalls is important since any discontinuity of the film from the top to the bottom of the TSV could result in voids. Conventional PVD methods, such as sputtering, exhibit limitations for the conformal deposition of the diffusion-barrier film (e.g. TiN) and seed-layer (e.g. Cu) due to strong dependency of material deposition upon the via AR and diameter [73]. To address this issue, ALD is an attractive alternative for conformal film deposition in high AR trenches. Deposition of TiN—diffusion-barrier layer—using ALD for interconnects has been explored previously [85], [86], [87]. TiN is electrically conductive, which opens the possibility for using it as ***both a diffusion barrier and a seed layer***. However, the resistivity of TiN is large and thus forms a large series resistance over a large surface area which makes it challenging for use as a seed-layer on a large diameter wafer. Because the series resistance causes a non-uniform current density distribution over a large surface area, (e.g. 4-inch diameter silicon wafer) non-uniform electroplating results across the wafer. To address this limitation, ***a thin layer of Cu (approximately 100 nm) is evaporated on the TiN*** coated substrate (Figure 30(d)). It is important to emphasize that this Cu layer does not cover the TiN film on the TSV sidewalls but mostly only coats the top surface of the wafer. This not only bypasses the series resistance of TiN film, but also makes the subsequent Cu electrodeposition less dependent upon the thickness

of the TiN layer. In this effort, ALD TiN is deposited on an SiO_2 liner using Cambridge NanoTech Plasma ALD tool (step (d) in Figure 30). The employed precursors used in the aforementioned ALD tool are TDMAT and NH_3 [86] processed at 250 ℃. The thickness of the TiN film is measured to be approximately 45 nm using a Woollam M2000 Ellipsometer.

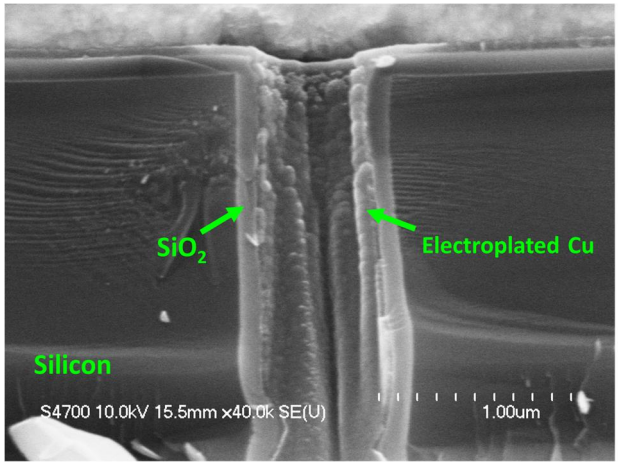


Figure 34 – SEM cross-section image from reduction of cupric ions on the TiN film on the TSV sidewall

To prove the concept, a test sample is partially electroplated for 10 minutes and cleaved for cross-sectional inspection. Figure 34 shows that cupric ions are reduced on the TiN film and form a layer of Cu on the TSV sidewall. This proves that the use of TiN is a feasible approach for metallizing scaled TSVs. Next, electrodeposition is performed on the sample (see Figure 30(e)) using super-filling and reverse pulse plating (RPP) techniques [88], [89], [90].

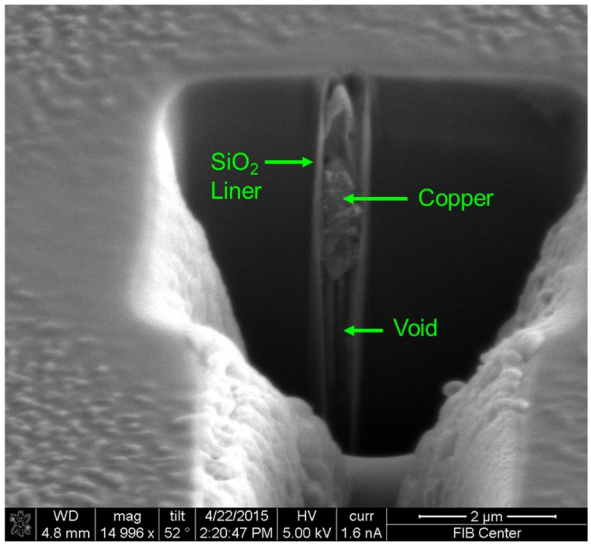


Figure 35 – SEM cross-section from the electroplated TSV using MICROFAB DVF 200 plating bath.

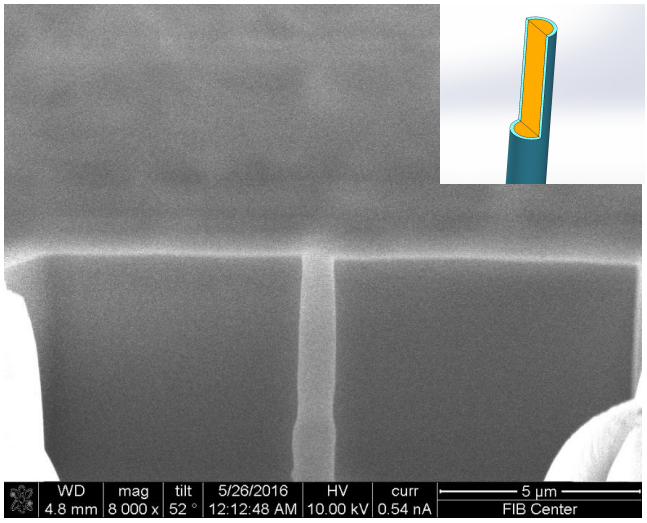


Figure 36 – FIB cross-section at 50% depth from the void-free TSV

The super-filling technique employs special additives in the electroplating electrolyte that accelerates Cu deposition in the bottom of the TSV while decreases

Cu growth rate at the top. However, there are different electroplating bath chemistries and additives [91] that makes the experimental design space large. Thus, an electroplating bath (MICROFAB DVF 200) specialized for TSV processing [92] with two additive compounds, accelerator (Part "B") and suppressor (Part "C"), is employed as a starting point and the end result is shown in Figure 35. It is believed that the bottom voids are formed due to large grain growth close to the TSV opening, causing pinching. This coarse Cu grain growth might be because of the bath chemistry and additives concentration that are optimized for fast electroplating of TSVs with diameter ranging from 5 µm to 20 µm [93], [94]. To test this hypothesis, another electroplating bath (TECHNIPULSE 5300) that is designed for finer grain deposition of Cu [95] was explored using the electroplating parameters shown in Table 5.

Table 5 – Reverse pulse electroplating parameters

Process Parameter	Value	Unit
Reverse cycle duration	2	millisecond
Reverse pulse duty cycle	50	%
Reverse pulse frequency	1000	Hz
Reverse current	Approx. 25	mA
Forward pulse duty cycle	50	%
Forward pulse frequency	200	Hz
Forward cycle duration	25	millisecond
Forward current	Approx. 15	mA
Agitation	200	RPM
Bath Temperature	Approx. 23	℃

The cross-sectional TSV FIB image shown in Figure 36 resulting from this bath chemistry exhibits no Cu voids and is a significant improvement. To ensure the

tested sample is defect free, polishing is continued to the deeper regions, as shown in Figure 37. It is important to note there were a number of challenges associated with the cross-sectioning of high AR TSVs; for instance, the sample should be perfectly perpendicular to the ion-beam and any small stage misalignment causes non-uniform FIB milling.

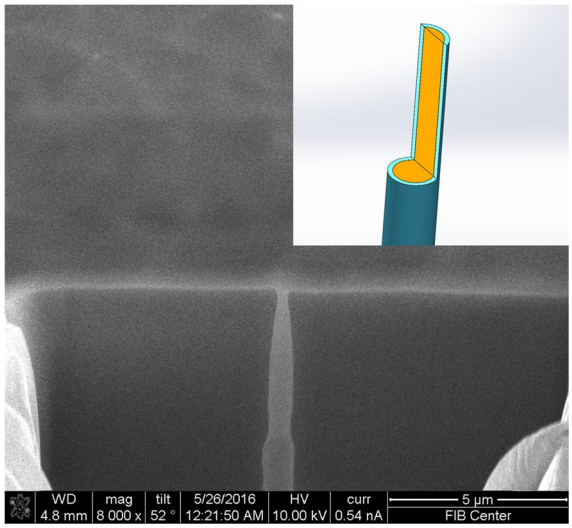


Figure 37 – FIB cross-section at 70% depth from the void-free TSV

In Figure 38, it is shown that the cross-section of the Cu core resembles a needle due to a higher removal rate at the top. Moreover, simultaneous milling of 3 different materials (silicon, SiO2, and Cu) is complex as they have different hardness. Although no voids are observed in the cross-sectioned samples regardless of these imaging challenges, we are aware that a significantly larger visual data set is needed to demonstrate the manufacturing yield.

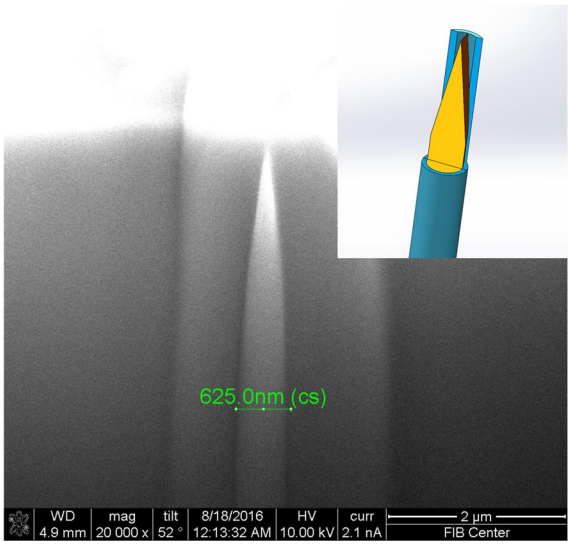


Figure 38 – SEM cross-section from a sample resembling a needle due to FIB stage misalignment

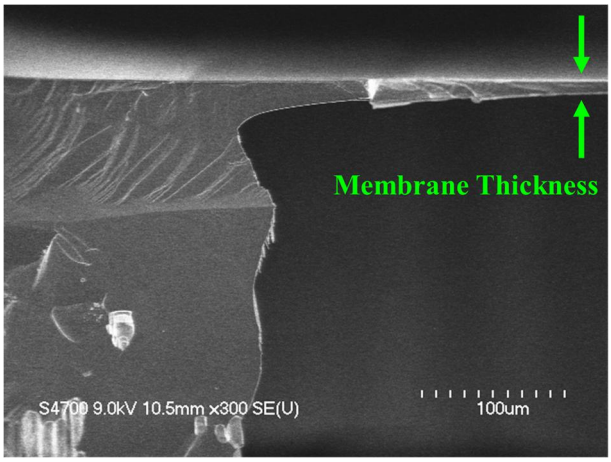


Figure 39 – SEM cross-section from the backside etched silicon substrate that shows 285 µm deep cavity

3.5 Electrical Characterization: Parasitic Resistance

To characterize electrical resistance (R_{TSV}) of the fabricated TSVs in section II, the back side of the silicon substrate is aligned with the topside features (e.g. TSVs) and patterned using optical lithography. Next, the patterned features (i.e. openings) on the back side are dry etched (see Figure 30(f)) to reveal the blind end of the TSVs. This creates a cavity with approximately 285 µm depth (for a 300 µm thick silicon wafer), as shown in Figure 39.

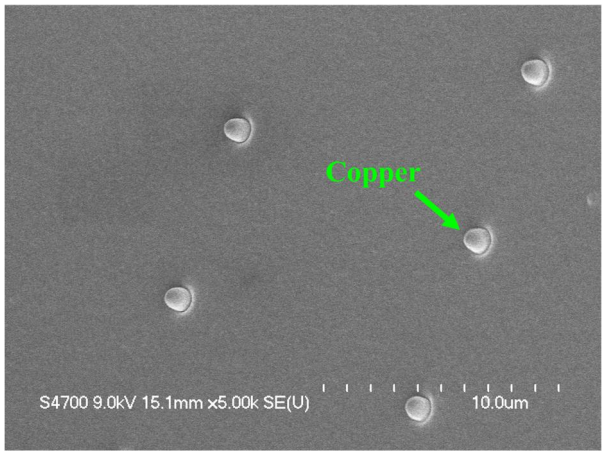


Figure 40 – SEM image from the revealed end of TSVs after backside etching shows the Cu core of TSVs.

Figure 40 shows the TSV Cu core revealed after backside etching. Next, the closed electrical loop is formed by shorting the revealed end of the TSVs by sputtering a layer of Cu into the cavity. The probing pads and wires for electrical characterization are patterned using EBL and the metal layers— Ti/Cu/Au (30 nm Ti, 1 µm Cu, and 350 nm Au)— are deposited using a sputtering tool for good step coverage. Next, R_{TSV} of 15 µm deep TSVs with approximately 680 nm diameter Cu core is measured using the four-wire Kelvin probe technique as the test setup

schematic, and the result of measurements are shown in Figure 41, and Figure 42, respectively. Figure 43 illustrates a Gaussian distribution of the measured R_{TSV} for different DUTs. The average measured R_{TSV} is calculated to be approximately 1.2 Ω. Furthermore, R_{TSV} for 2, 3, 4, and 8 parallel TSVs is measured and plotted in Figure 44. The slope of the fitted curve suggests that the extracted average R_{TSV} for a single TSV is 1.216 Ω which agrees with the measured R_{TSV}.

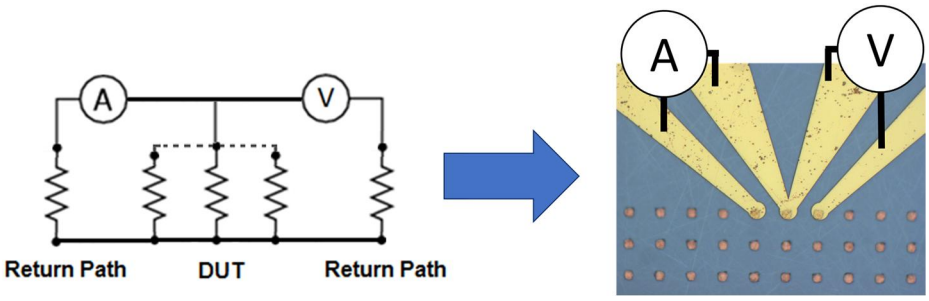


Figure 41 – Schematic of the 4-wire Kelvin probe technique for characterizing the DUT in the test-vehicle

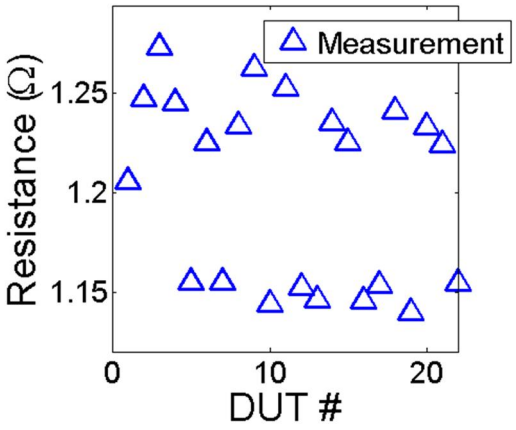


Figure 42 – Measured R_{TSV} of DUTs approximately ranging from 1.14 Ω to 1.27 Ω

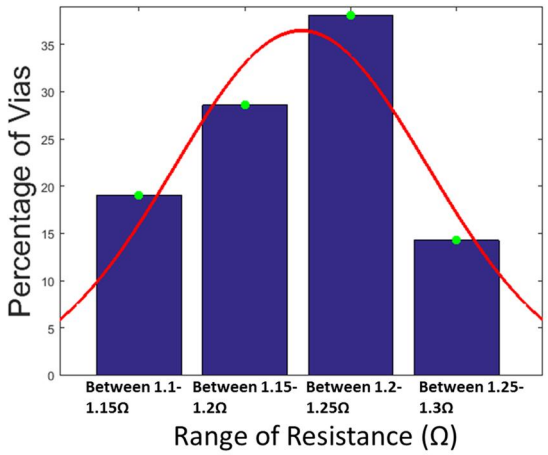


Figure 43 – Gaussian distribution of the measured R_{TSV} for different DUTs

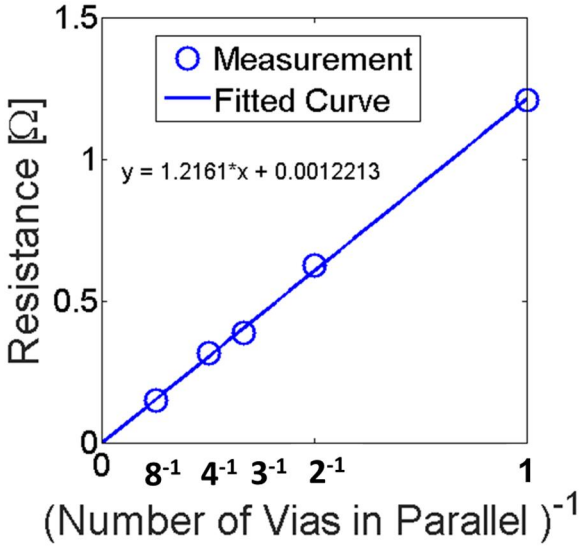


Figure 44 – R_{TSV} measured for 2, 3, 4, and 8 parallel TSVs

Given the fabricated TSV dimensions, Cu resistivity of the metal core is extracted to be approximately 2.95 μΩ-cm. It is shown by Chang et al. [96] that the use of the chosen additives in the electroplating bath chemistry increases Cu

resistivity from 2 μΩ-cm to 2.9 μΩ-cm. This agrees with the measurements presented in this work.

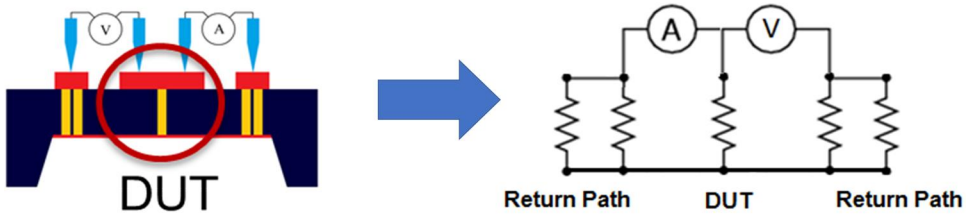


Figure 45 – Schematic of the test-vehicle designed for measuring CCC

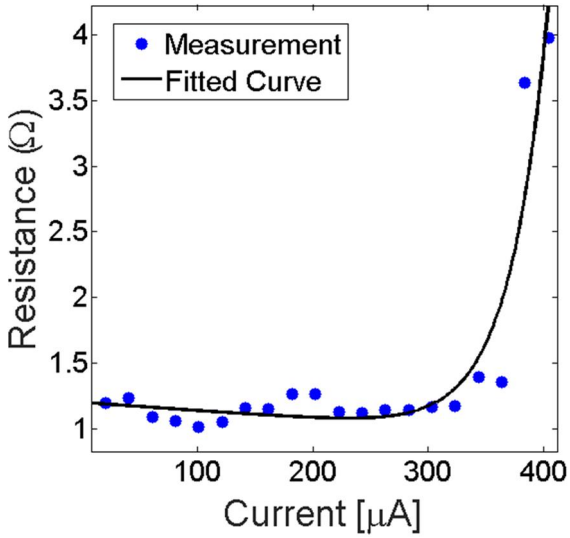


Figure 46 – Current-carrying-capacity is measured for sub-micron TSVs

3.6 Electrical Characterization: Current-Carrying Capacity

Figure 45 illustrates the schematic of the test vehicle that is designed to measure the (current-carrying-capacity) CCC of the fabricated sub-micron diameter

TSVs. The CCC measurement is conducted by monitoring R_{TSV} while DC current is pumped into a single TSV (i.e. DUT). To decrease the return path electrical resistance, eight TSVs are connected in parallel for this experiment. This ensures that the current flow is not limited in the return path. Next, the DC current is increased until R_{TSV} exhibits a rapid change ($\Delta R_{TSV}/R_{TSV} \geq 20\%$), indicating that the DUT has reached its maximum CCC (i.e. ampacity). The measurements shown in Figure 46 suggest that the ampacity of the DUT is 360 µA, or 105 kA/cm^2 given the TSV dimensions.

3.7 Conclusion

In this chapter, we showed enabling fabrication processes for sub-micron TSVs to gain the most from the connectivity benefits (e.g. low parasitic capacitance) of fine-grain 3DI. The presented sub-micron TSV technology enables heterogeneous 3D ICs using vertically stacked thin silicon tiers. The demonstrated approximately 900 nm diameter TSVs are 15 µm deep with 680 nm Cu core. To address the challenges in fabricating these TSVs, nano-Bosch silicon etching with no scalloping and direct Cu super-filling on a TiN diffusion barrier layer have been developed as the two key enabling modules. Furthermore, using the test-vehicle, the average electrical resistance of these sub-micron vias is measured to be approximately 1.2 Ω. Furthermore, maximum CCC of the scaled TSVs is characterized to be approximately 360 µA. Given the TSV dimensions, the current density at maximum CCC and Cu resistivity are extracted to be approximately 105 kA/cm^2 and 2.95 µΩ-cm, respectively.

CHAPTER 4. NON-UNIFORM FLUID COOLING FOR 3D INTEGRATED CIRCUITS

Higher density of integration continues to show unprecedented benefits for addressing the ever growing need for energy efficient high performance computing (HPC) [14]. Thermal challenges, however, in power demanding HPC systems impose limitations and concerns to the package integrity of CPUs and GPUs [20] that necessitate innovative heat removal solutions. Emerging heat dissipation technologies aim to address the current thermal management needs for high density ICs while they could potentially pave the way to mitigate the pronounced power wall limit [97], [31] in 3D-ICs [98]. Integrated microfluidic cooling is believed to be a promising heat removal technique that can offer a low thermal resistance at the die level [99] and enable thermal isolation in 2.5D architectures and 3D-ICs [100]. The resulting thermal cross-talk reduction between background power dissipation and temperature-sensitive devices (e.g., photonics) enables integration of different functions in very small form factors. In addition to the background heat generation, non-uniform power dissipation across the silicon die in modern ICs produces hotspots (i.e., high temperature islands) that demand a heatsink architecture for adequately cooling them. Since a cooling system often is limited by the worst-case temperature imposed by hotspot power dissipation profile, it may be beneficial to provide non-uniform cooling in order to prevent overdesigning the entire heatsink. The enabling microfluidic cooling technique explored in this chapter addresses non-uniform temperature distribution across the silicon die and virtually mitigates the power wall

limit imposed by high heat dissipative elements and hotspots, which paves a way to the 3D integration of electronics.

In this work, we demonstrate a non-uniform integrated microfluidic heatsink with two independent fluid streams in order to adequately cool very high heat flux density hotspots separately from the background. This approach eliminates the need for refrigeration of the background coolant below outside atmospheric temperatures, hence saving energy. The promising benefits of non-uniform heatsinks were motivated by several different efforts in this field; C. Green et. al. [101] proposed a water-cooled cold-plate in which two separate fluid streams are used to remove heat from the background and hotspot regions. Their experimental demonstration used deionized water-based jet impingement on the hotspot, and a separate coolant stream through a pin-fin array for the background cooling. Fluid-cooled background using a staggered micropin-fins based heatsink is shown by J. Dirner et. al. [102] for a uniform power-map across a chip. This approach has also been employed in other works to address a non-uniform power dissipation through a single fluid inlet system and non-uniform density of pin-fins for the entire heatsink [103], [104], [105]. Several other hotspot cooling methods have been demonstrated, including jet impingement as aforementioned [106], [107] thermoelectric coolers [99], [108], and thin film evaporation [109]. Nasr et al. [110] demonstrated a dedicated hotspot cooler, consisting of a 10 µm tall microgap with high heat flux removal of approximately 5 kW/cm^2. Such a small microgap would produce prohibited high pressure drops if used across the entire chip but can produce high heat transfer coefficients across a small area. Thus, these extremely shallow microgaps could be employed to selectively cool hotspot regions where cooling of a small surface area is required.

The work presented consists of: 1) design of a thermal testbed that emulates a high power dissipating hotspot with a maximum flux density of 6.175 kW/cm^2 and 100 W/cm^2 uniform background heat generation, 2) microfabrication of a silicon testbed, package, and integration of fluid delivery ports within the package, 3) performance characterization of microfluidic cooling at different hotspot flux densities, and 4) a comparison between the experimental data and simulations.

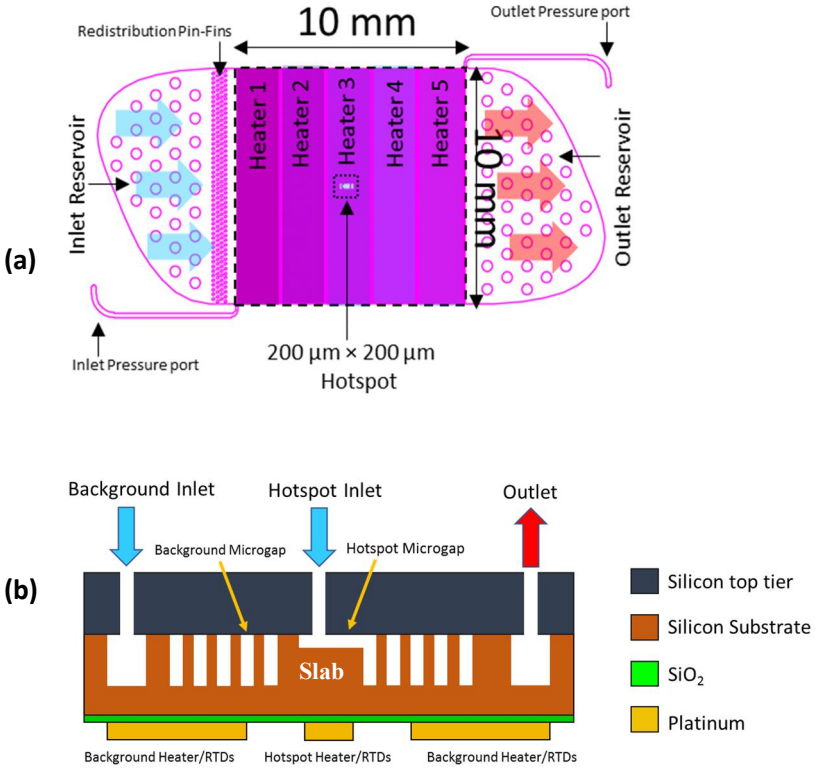


Figure 47 – (a) Top-view schematic of the testbed showing the position of heaters/RTDs and fluidic ports across the chip. (b) Side-view schematic of hotspot and background microgap integrated at the back side of the silicon substrate.

4.1 Silicon Testbed Structure

Top-view schematic of the thermal testbed is outlined in Figure 47(a)-(b). There are five 1.95 mm × 10 mm heaters across the chip that generate a total "background" power density of 100 W/cm^2 (20 W/cm^2 per heater). A 200 µm × 200 µm high-power density heater is located at the center of the chip to represent the hotspot region and generates a higher power density than the background [111]. The heatsink design is primarily built upon the dedicated microgap approach such that a high heat flux is transferred to the coolant in the single-phase regime. To create a large surface area that enhances heat removal for dissipating the background heat, an array of micro-hydrofoils is etched over the aforementioned 10 mm × 10 mm background area into the back side of the base silicon to a height of 200 µm (see Figure 48).

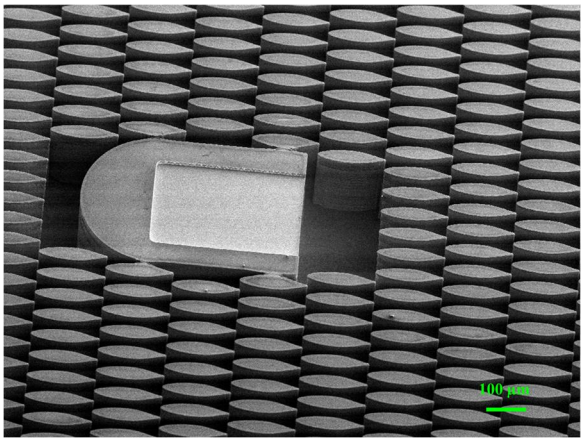


Figure 48 – Top-view SEM image of the hydrofoil micropin-fin array that is etched into the back side of the base silicon to a height of 200 µm along with a 200 µm × 200 µm hotspot microgap.

These 150 µm wide micro-hydrofoils have transverse and longitudinal pitches of 225 µm and 642.5 µm, respectively. The hotspot microgap, however, is extremely shallower and is only 10 µm deep. To enable direct coolant injection atop the hotspot microgap at a high flow rate, a 200 µm × 90 µm fluidic via is etched through the capping silicon tier. This allows independent power dissipation for the hotspots at a higher heat flux removal rate than the background.

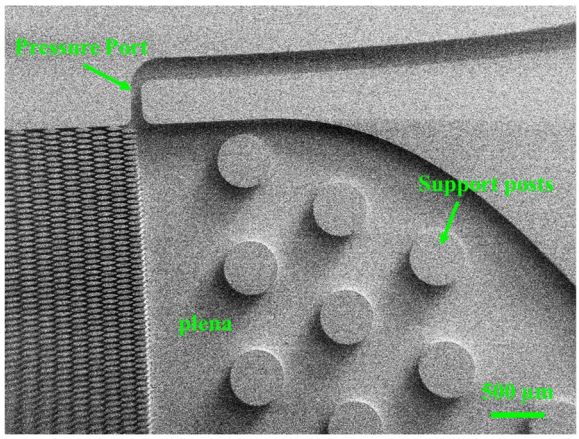


Figure 49 – SEM image of the outlet plena, pressure port, and support posts

The hotspot and background have combined return flows and share one outlet. Two plena are designed at the background inlet and outlet to regulate and buffer the fluid flow (see Figure 49). As shown in Figure 50, the staggered redistribution pin-fins are placed close to the inlet plenum to uniformly redistribute the background coolant inside the heatsink but at the expense of increased pressure drop. That is why the inlet pressure port is located next to the redistribution pin-fins and behind the micropin-fin array (see Figure 49) to exclude the effect of redistribution pin-fins on pressure drop measurements. Moreover, these on-chip

pressure ports help to accurately measure pressure-drop across the background heatsink by being located outside of the flow path. Additionally, the pressure drop on the hotspot inlet is separately measured using an off-chip pressure port since the coolant flow rate is low and the pressure drop through the hotspot tubing is minimal. The temperature of the die is measured using resistance temperature detectors (RTDs) that also function as heat sources (see Figure 51). The background and hotspot heat fluxes are characterized using five RTDs/heaters across the die and the dedicated hotspot RTD/heater, respectively. This distributed floor plan enables adjusting a power map for different thermal scenarios. However, a uniform background power density of 100 W/cm^2 across the 10 mm $\times$ 10 mm chip is applied and the hotspot power density is accordingly chosen for different experiments. The fabrication process and packaging of the testbed will be discussed the following sections.

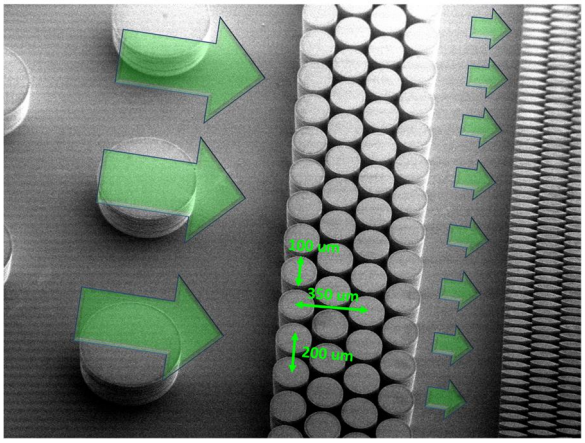


Figure 50 – SEM image of the redistribution pin-fin array for regulating the fluid flow from inlet to hydrofoil micropin-fin array

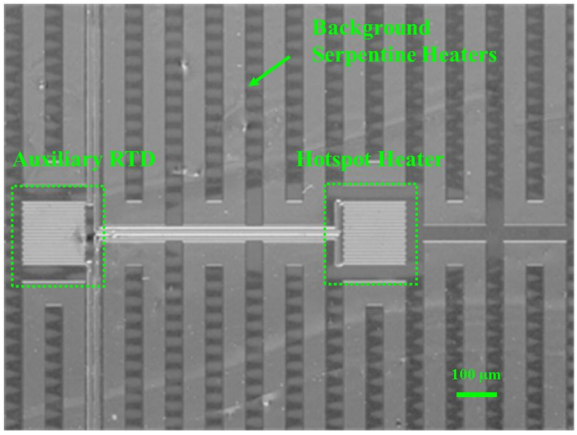


Figure 51 – Top-view Infrared image of background and hotspot heaters/RTDs

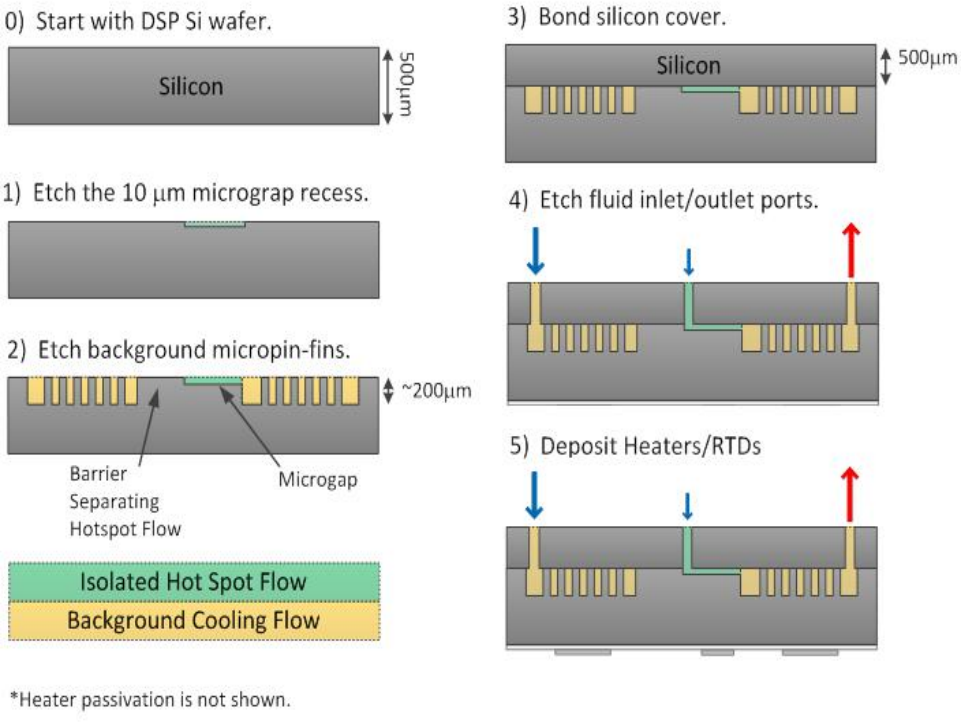


Figure 52 – Testbed fabrication process flow

4.2 Microfabrication of Silicon Chip

The simplified fabrication process flow is illustrated in Figure 52. A double-side polished (DSP) 500 µm thick silicon wafer is used as the substrate. Standard AMI pre-cleaning steps under a class 100 cleanroom environment is implemented on the bare silicon substrate. Further, the silicon wafer is cleaned in 120 ℃ piranha solution for 10 min followed by deionized water rinsing for 2 min (i.e., step 0 in Figure 52). Next, the hotspot microgaps are patterned through a bright-field fused-silica mask and UV lithography at 365 nm wavelength. The sample is exposed to a gentle oxygen plasma for 45 sec (i.e., descum) in an RIE tool to ensure the developed features are not masked with any possible thin photoresist residue [112]. Next, the hotspot microgap is dry etched [113] to a depth of 10 µm into the silicon substrate through an optimized Bosch process using an STS-ICP tool (i.e., step 1 Figure 52). Since the microgap is shallow (i.e., 10 µm), conventional Bosch etching recipes that are designed for deep silicon etching introduce surface roughness. Therefore, the passivation time, etching time, and oxygen gas flow rate are optimized to achieve smooth shallow silicon etching [114] as stated in Table 6. To prepare the silicon substrate for patterning the background micropin-fins, the initial photoresist layer is stripped off using oxygen-plasma cleaning. This procedure ensures that no photoresist residue is left on the substrate to distort subsequent fabrication steps. The next step of fabrication is etching the background microgaps. The background hydro-foil pin-fins are patterned and aligned with hotspot microgaps using a Karl Suss TSA MA-6 mask-aligner. Next, the hydro-foil pin-fins are etched to a depth of 200 µm in the silicon substrate through an optimized Bosch process (i.e., step 2 in Figure 52). The third step of fabrication is capping the etched features with a silicon

wafer using an activated surface silicon-to-silicon bonding technique. To achieve high strength bonding, it is important to keep the surface of both silicon substrates undamaged and clean in all fabrication steps. After aligning the substrate with the cap, pressure is applied to the sample to enhance surface bonds. Annealing cycles are employed to strengthen the bonds and prevent mechanical failure during high pressure operation. The 500 µm diameter micropin-fins shown in Figure 49 are designed as mechanical support structures to increase the surface area between the substrate and the cap for strengthening silicon-to-silicon bonding. Next, the fluid inlet and outlet ports are etched through the silicon cap, connecting the background, and hotspot ports to the plena and hotspot microgap, respectively. The mask for these fluid vias (i.e., background, and hotspot ports) is backside aligned with the etched hotspot microgap using the Karl Suss MA-6 mask-aligner. The background ports (1.2 mm diameter) and the hotspot inlet (90 µm diameter) are simultaneously etched through the silicon cap using STS-ICP. Since the hotspot port is 13-times smaller than background ports, the etch rate for hotspot inlet is lower and therefore, the etch end-point is based on the smaller feature. After forming the ports, 2 µm of SiO_2 is deposited on the top side of the sample using a PECVD tool. This dielectric layer electrically isolates the heaters and RTDs from the silicon substrate. The RTDs and heaters are firstly patterned by backside alignment with the inlet ports, and secondly metallized by evaporating 30 nm of Ti (the adhesion layer) prior to the deposition of 200 nm of Pt using a CHA metal evaporator. Eventually, the metallization step is completed by patterning on-chip wires, and wire-bonding pads and depositing Au using an evaporator. In all metallization steps, liftoff technique is utilized.

Since the Au wires are formed on top of the Pt heaters/RTDs, the parasitic resistance of the Pt heaters is reduced to mitigate an unwanted voltage drop over the transmission lines. Moreover, it is found that passivating the Pt elements with a 1 µm thick SiO_2 layer increases the lifetime of the heaters. This dictates an additional step which reveals the buried Au pads by etching the SiO_2 passivation layer.

Table 6 – Bosch process parameters for micro-scale etching

Process Parameter	Value	Unit
Passivation Time	7	second
Etching Time	7	second
Process Mode	Discrete	-
APC Setting	68.4	%
Base Pressure	0.1	mTorr
Pressure Trip	94.0	mTorr
C_4F_8	100	Sccm
SF_6	60	Sccm
O_2	15	Sccm
Coil Passivation Power	600	W
Coil Etch Power	600	W
Platen Passivation Power	0	W
Platen Etch Power	11	W
Platen Frequency	13.56	MHz

4.2.1 Testbed Packaging

The schematic shown in Figure 53 illustrates the structural design of the package. The 4-inch silicon wafer that contains the fabricated devices, is diced into individual dice. A package-level fan-out is implemented on an FR4 substrate and the signal pads on the silicon die are wire bonded to the package substrate as shown in Figure 53.

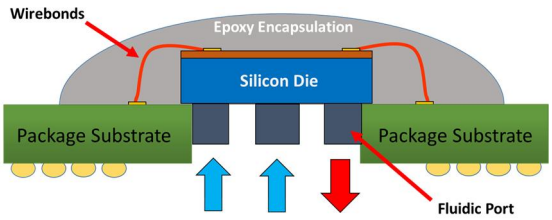


Figure 53 – Schematic of the package structure

The off-chip fluid connections are embedded into the package to enable full encapsulation of the device. Thus, package to die fluid ports are designed and 3D printed using Stereolithography (SLA) technology as shown in Figure 54. Next, the fluid connections are encapsulated and bonded to the backside of the silicon die where the fluid vias are located, using heat-resistant bonding epoxy resin. The fully packaged device with embedded fluid ports is shown in Figure 55.

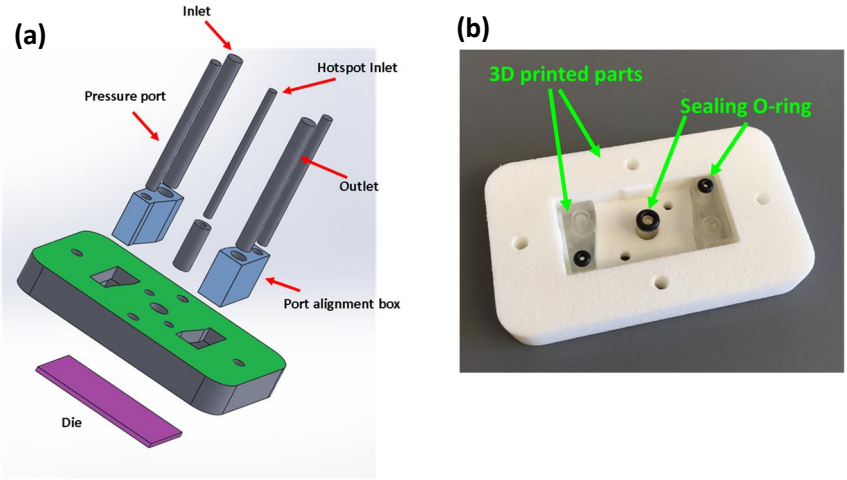


Figure 54 – (a) 3D design of the fluid ports illustrating the package encapsulation and assembly. (b) 3D printed fluid ports using SLA 3D printing technology

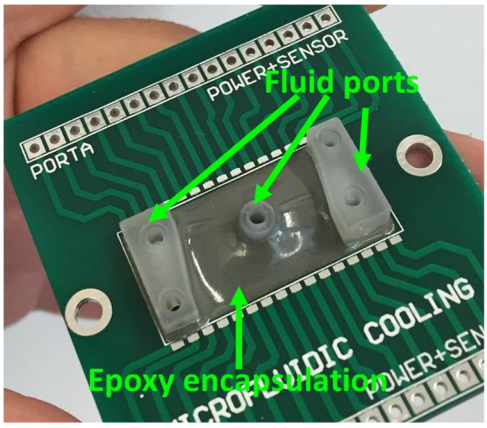


Figure 55 – Fluid ports through the packaging substrate attached to the die and epoxy encapsulated

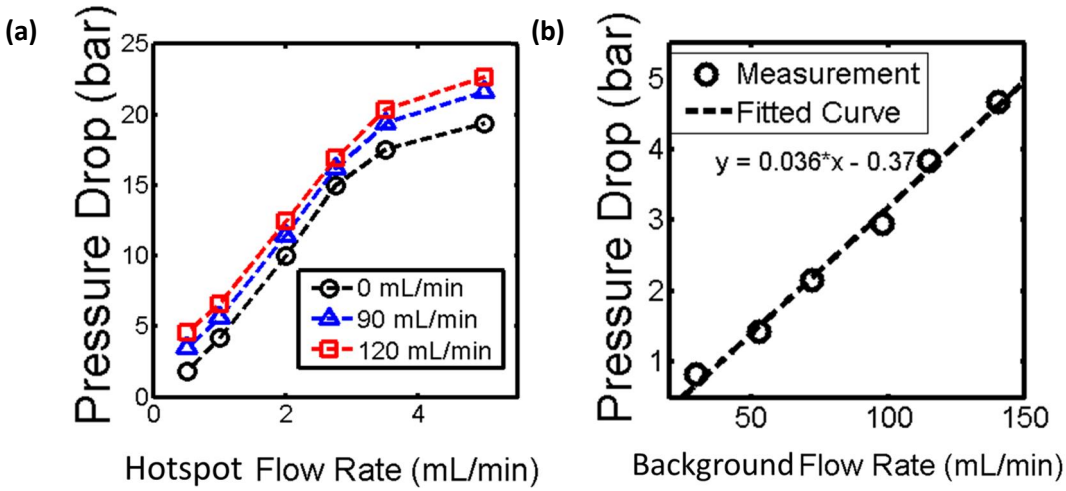


Figure 56 – (a) Pressure drop vs. flow rate on hotspot microgap at three different background flow rates and (b) pressure drop vs. flow rate on the background microgap while no loading on the hotspot.

4.3 Pressure Drop and Heat Removal Rate

The cooling loop is driven by a gear-pump and a syringe-pump dedicated to the background and hotspot, respectively. Independent operation of these two pumps enables adjusting coolant flow rates to the hotspot and the background independently. The measured pressure-drop over the background microgap is a function of the micropin-fin density. A denser array of micropin-fins is beneficial as it creates a larger surface area and potentially improves heat dissipation. However, it leads to a higher pressure drop which necessities a larger pump to maintain the required flow rate. Thus, the geometry design of the background and hotspot microgaps directly determines not only the cooling performance but also the pump size. The size and pitch of the fabricated features in Section II are accordingly chosen [101], [104] to ensure the background pressure drop can feasibly be handled by a small gear pump. This design implementation exhibits approximately 2.96 bar pressure drop at 100 mL/min, which is the fluid flow rate of interest. Pressure drop for the hotspot and the background microgaps at different flow rates can be seen in Figure 56(a) and Figure 56(b), respectively. It is important to note that the differential pressure drop shown in Figure 56(a) is from the hotspot inlet to the end of the micropin-fin array. The experiments imply that the hotspot pressure drop is influenced by the background flow rate as there is a shift in the hotspot pressure drop while the background flow rate is increased to 90 mL/min and 120 mL/min. This is due to a back pressure created by the background coolant flow on the hotspot outlet. Thus, a larger pressure drop across the hotspot micro-gap is observed as the background flow rate increases.

4.4 Hotspot Coolant Temperature and Heat Sink Performance

The measurements reported in Figure 57 are conducted at the 20.1 ^{o}C inlet temperature under a constant flow rate of 100 mL/min and 1.5 mL/min for the background and hotspot, respectively. At 100 W/cm^2 flux density, the temperature gradient is shown to be linearly increasing across the chip. The slope of the fitted curve implies approximately 1.5 ^{o}C/mm temperature elevation in the x-direction for the respective coolant flow rate, which is an expected result since the background coolant flow rate is constant. This is a consistent observation in all the measurements shown in Figure 57(a)-(f) as the slope of the fitted curve remains the same and the apparent spatial temperature of the heaters from the fluid inlet towards the outlet port exhibits a linear increase. Additionally, the difference between hotspot temperature and inlet temperature (T_j- T_{in}), and the hotspot temperature difference from the background temperature ($\Delta T_{H\text{-}B}$) are both plotted on each graph of Figure 57(a)-(f). The hotspot temperature is shown to be approximately 8.35 ^{o}C cooler than the neighboring background RTD (see Figure 57(a)) while both the background and the hotspot regions are loaded with the same heat flux density (100 W/cm^2). To further study the heatsink performance, the hotspot heat flux density is increased from 100 W/cm^2 up to 6.175 kW/cm^2 and Figure 58 illustrates the hotspot RTDs temperature with respect to the background temperature (T_j-T_{BKG}). The fitted curve demonstrates a linear trend while the hotspot flux density is increased, indicating that there is sufficient cooling provided by the presented heatsink design. It is important to note that the hotspot power dissipation at a very high heat flux density (Figure 57(f)) is proven to be sustainable using no refrigerant below room temperature.

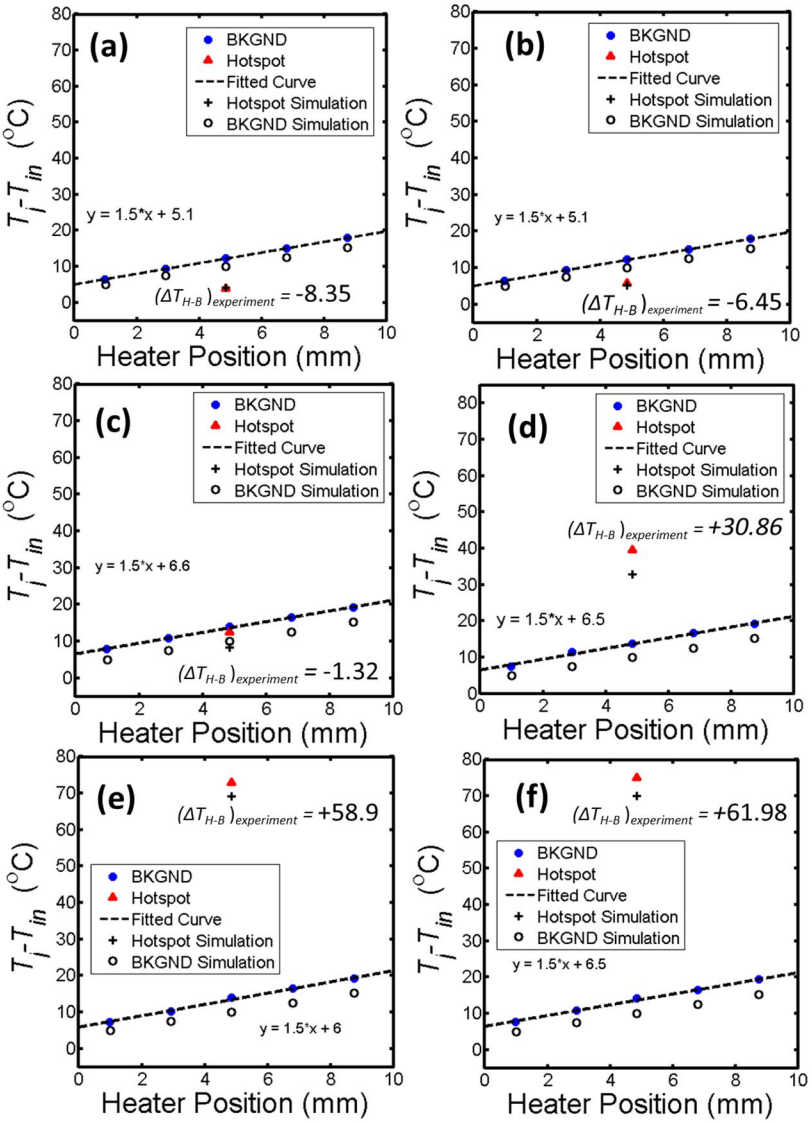


Figure 57 – The hotspot and the background RTDs temperatures (T_j)— simulation and experiment— with respect to the coolant temperature at the inlet (T_{in}) vs. RTDs position on the silicon substrate while the hotspot power density is: (a) 100 W/cm² (b) 200 W/cm² (c) 500 W/cm² (d) 2.75 kW/cm² (e) 6.1 kW/cm² (f) 6.175 kW/cm²

To confirm the experiments, thermal performance of the testbed is evaluated using a 3D multi-physics finite element simulator (COMSOL Multiphysics 5.3) and

the results are compared with experimental data. The simulated model employs the non-isothermal fluid flow module and the modeled structure is simplified to half the micropin-fin area to reduce numerical complexity. As illustrated in Figure 59(a), temperature increases across the silicon chip in the direction of the fluid flow and the simulation results show the same linear trend with an approximately similar slope as compared to the measurement data in Figure 57. The simulated temperature profile of the heatsink surface is shown in Figure 59(b) while the average hotspot temperatures under various heat flux densities are compared with the experiments and demonstrate a close match (see Figure 58).

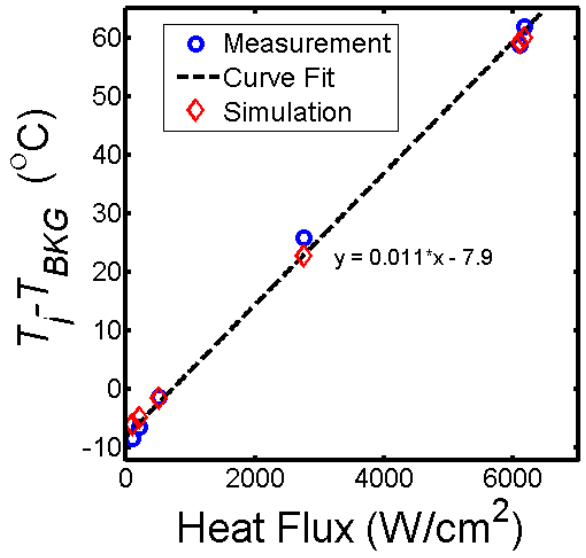


Figure 58 – Simulated and experimental hotspot RTDs temperature (T_j) with respect to the background temperature (T_{BKG}) vs. heat flux.

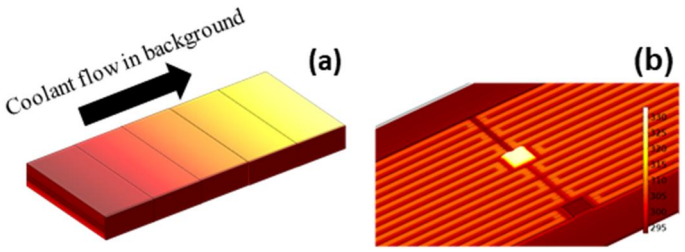


Figure 59 – (a) Temperature profile increases across the top of the thermal testbed. (b) Temperature distribution along the hotspot and background heaters.

It was observed from the experiments that the hotspot heat dissipation performance was minimally impacted by higher flow rates of the room temperature coolant— data not shown— and therefore a numerical simulation is carried out to study this observation. As illustrated in Figure 60(a), the cross-sectional temperature profile shows a large lateral heat spreading across the silicon substrate, which implies that a notable portion of the heat flux is laterally spreading.

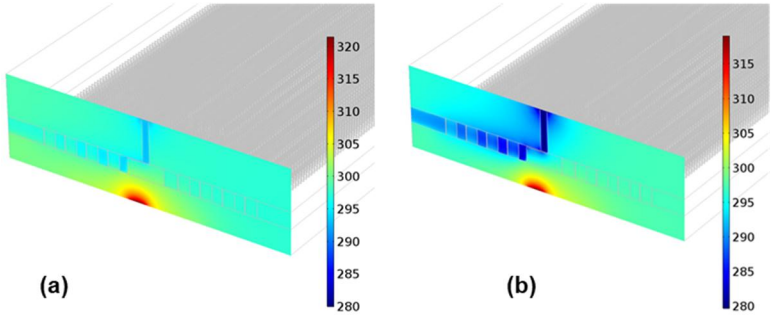


Figure 60 – (a) Temperature profile increases across the top of the thermal testbed. (b) Temperature distribution along the hotspot and background heaters.

The simulation outcome at the elevated hotspot flow rates (up to 3.5 µL/min) validates the experiments; the heatsink temperature profile (the hotspot and the neighboring background) is not changing even as the inlet flow rate is increased and thus, negligible cooling performance improvement results. Since heat spreading plays a considerable role in the power dissipation [110], it is believed that the hotspot heat flux is dissipated less through the fluid cooling mechanism and more through its spreading into the base silicon. Therefore, it is expected that decreasing the base silicon temperature using a chilled coolant would result in a better cooling performance.

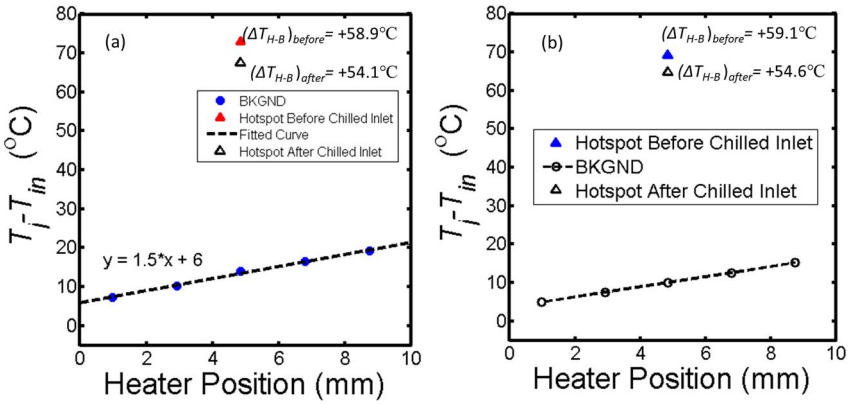


Figure 61 – Approximately 10% temperature drop on the hotspot at 6.1 kW/cm² due to use of chilled water (a) experiment, (b) simulation.

Moreover, the impact of the chilled coolant is assumed to be more noticeable while the hotspot is loaded at the highest achievable heat flux density (i.e., > 6 kW/cm²). Accordingly, a numerical model in COMSOL is set up to study this hypothesis. The simulation results suggest that the hotspot region largely increases the temperature of the silicon slab close to the hotspot microgap (see the schematic

in Figure 47). Thus, decreasing the temperature of the silicon slab and the adjacent bulk silicon impacts the hotspot temperature as the simulation result shows in Figure 60(b); it suggests that the chilled hotspot inlet lowers hotspot temperature. An experiment parallel to the simulation is conducted by chilling the hotspot coolant down to approximately 5 ^{o}C while injecting this coolant at a high flow-rate of 5 mL/min into the hotspot microgap. The measured hotspot temperature drops by 4.8 ^{o}C (10%) at a high-power density of 6.1 kW/cm^{2}. The measurements for these experiments have been recorded in steady-state conditions. Thus, the fluid flow rate is assumed to be constant from the syringe pump outlet to the hotspot inlet and therefore the flow rate displayed by the pump is recorded as the flow rate reading. Furthermore, the coolant temperature is measured close to the hotspot inlet using a k-type thermocouple and shows 2.4 ^{o}C above the 5 ^{o}C syringe temperature (i.e., the coolant temperature at the hotspot inlet is 7.4 ^{o}C). It is important to note that the background heat flux and the background coolant flow rate are kept constant in order to obtain a consistent comparison between the experiments. Figure 61(a) and Figure 61(b) show results of the measurement and simulation, respectively. The hotspot temperature drops by approximately 10% from 58.9 ^{o}C to 54.1 ^{o}C which agrees with the simulated model that exhibits a temperature reduction from 59.1 ^{o}C to 54.6 ^{o}C.

4.5 Conclusion

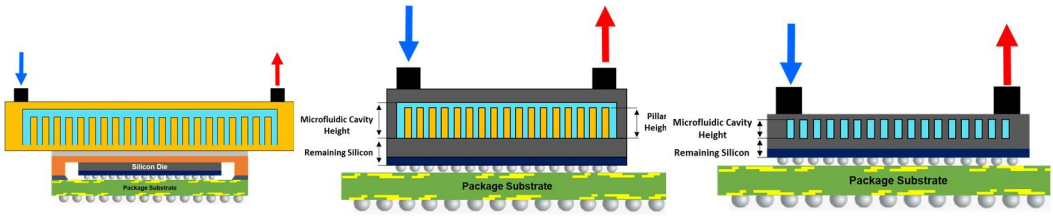
This chapter presented a monolithically integrated microfluidic heatsink solution for the simultaneous cooling of hotspot and background in power demanding ICs with non-

uniform power-maps. The cooling strategy employs two microgaps in addition to dedicated coolant inlets for the hotspot and background. Splitting the fluid ports: 1) eliminates the need for high volume refrigerated coolant for cooling the entire chip, hence saving energy, 2) enables adjusting the background and hotspot fluid flow rates independently for different thermal management scenarios, 3) since the narrow microgap is only designed for the hotspot, the background region exhibits low pressure drop and therefore a smaller pump could be employed. To evaluate this cooling strategy, a thermal testbed is designed and microfabricated, consisting of hydrofoil shaped micropin-fins and a shallow microgap. The fluid ports are 3D printed using SLA technology, integrated onto the silicon die and the package substrate, and the entire testbed is encapsulated to emulate a commercial IC package. With a nominal background heat flux of 100 W/cm^2 and flow rate of 100 mL/min, the average temperature across the entire chip is measured only to be increasing by approximately 1.5 ^{o}C/mm above room temperature from the fluid inlet to the outlet. The hotspot power density is swept over a wide range to study heatsink performance for low, moderate, and high heat fluxes. The hotspot temperature appears to have a relatively linear increase versus heat flux variations which indicates no degradation of the hotspot heater even at very high heat fluxes. This stability demonstrates that the cooling mechanism is sufficiently dissipating the power. A maximum of 6.175 kW/cm^2 flux density loaded on the hotspot is reported and the hotspot temperature is measured to be approximately 62 ^{o}C above room temperature which is well below the maximum allowable junction temperature (150 ^{o}C [18]). The numerical and experimental measurements imply that the heatsink performance could be further enhanced by chilling the hotspot coolant. Thus, the hotspot heat dissipation is experimentally demonstrated to be improved by 10% if the coolant is chilled down to 7.4 ^{o}C coolant.

CHAPTER 5. ENABLING METAL 3D PRINTING AT THE MICRON-SCALE FOR ADDITIVELY INTEGRATED MICROFLUIDIC HEATSINKS

The growing trend of higher power dissipation at a smaller form factor motivates the development of miniaturized high-performance cooling systems. Unlike conventional air-cooling solutions, microfluidic heatsinks have shown very high thermal performance; however, commercially available microfluidic solutions (i.e., cold-plates) do not offer significant miniaturization. Monolithic microfluidic cooling technology (see CHAPTER 4), on the other hand, exhibits the smallest form factor and best thermal performance but has integration complexities that may impose manufacturing challenges. For example, monolithic integration of microfluidics requires post-processing of a CMOS wafer for etching, capping, and sealing microfluidics; these steps introduce a number of challenges, in particular reducing silicon volume and thus increasing warpage, exposing the fully processed wafer to high power plasma, and bonding silicon layers through applying a large mechanical force. As an alternative, a novel metal additive manufacturing technology is developed in this thesis as a key enabler for fabricating a metallic microfluidic heatsink at the die and wafer levels.

Table 7. Cooling solutions



Technology	Cold-plate heatsink	Additively integrated heatsink	Monolithic silicon heatsink
Form Factor	Large	Compact	Very compact
TIM Layer	Yes	No	No
Pressure-drop	Very low	Low	High
Heat Dissipation	Medium	High	High
Silicon Substrate	Entire die	Entire die	Partially etched
Warpage	Minimal	Minimal	Maybe large

Table 7 compares three cooling solutions and highlights the benefits of the 3D printed metal heatsink. Using additive microfabrication technology, a novel manufacturing method is envisioned to address the following issues:

- Thermal-Interface-Material (TIM): To ensure having a proper thermal contact (without an air-gap) between the silicon die and a heatsink, a TIM layer is applied; however, this TIM largely increases thermal resistance and therefore, eliminating the TIM layer is highly beneficial

- Silicon Etching: deep silicon etching of known-good dice is a high-risk procedure that exposes fully-processed CMOS dice to high-power plasmas. Thus, a manufacturing scheme that does not require silicon etching could

significantly reduce manufacturing barriers for integrating microfluidic heatsinks.

- Warpage and Reliability: minimizing warpage due to a thinned silicon die that results from the deep silicon etching step is beneficial

Additive microfabrication could potentially mitigate all the above manufacturing issues while addressing other fundamental shortcomings of subtractive manufacturing schemes. For example, the building of sophisticated geometries and hollow objects using subtractive fabrication techniques (e.g. CNC machining) faces intrinsic restrictions including inaccessible construction planes [115]. The restrictions with subtractive manufacturing techniques, however, are the driving motivation behind the development of additive manufacturing schemes [116] that enable the fabrication of complex structures, even with multiple materials involved (i.e., two or more types of polymers). Currently, rapid prototyping and low volume production are considered as mainstream for 3D printing technologies as they offer flexible and relatively quick manufacturing with reasonable total cost of ownership [117]. However, these advantages are limited by the range of materials that can be implemented in additive fabrication [118]. For instance, metals are often materials of interest for many applications but they are challenging to precisely deposit layer by layer in constructing a 3D structure [119] due to the high melting temperatures required both for the deposition itself and for the bonding between deposited adjacent layers. Nonetheless, commercially available metal 3D printers rely on a form of high temperature metal processing technique which is based on pulsed-laser sintering and heat confinement within the area of the laser spot [120] where

the metal locally melts and solidifies to form fused layers [121] (i.e. direct-metal-laser-sintering (DMLS) process). These printers exhibit macro-scale capability (minimum feature sizes in the order of millimeters [122]) and have found a wide range of applications in defense and aerospace industries (e.g. for making aircraft parts such as titanium jet-turbine blades [123]). Nonetheless, the need for additively microfabricating metal structures in different domains (e.g. MEMS and cell-probing) motivates the development of novel 3D printing technologies. However, it is non-trivial to construct microdevices based on high temperature material processing techniques. To address this issue, low melting temperature metals such as gallium alloys could be employed to decrease process temperatures, hence enabling 3D printing of metal features with smaller dimensions [124] but this technique is material limited. To achieve micron-scale feature sizes, another approach employs a laser beam for localizing electrophoretic deposition through the trapping, confining, and stacking of metal nano-particles that are suspended within a liquid solution [125], [126]. Unlike these 3D printing techniques that rely on a form of physical deposition techniques, localized electrochemical deposition was shown to be a feasible approach for metal processing with nano-scale precision at room temperature [127]. This 3D printing scheme relies on electrodeposition confinement within a droplet of an aqueous electrolytic solution that is precisely dispensed through a nano-pipet to an area where the metal deposition is confined [128], [129] [130], [131]. Since this technique primarily relies on a pico-liter meniscus of a liquid electrolyte, it is challenging to control against evaporation [132], capillary forces [133], and the adverse effect of a surface hydrophobicity profile [133] but very fine feature sizes are impressively demonstrated. Moreover, the meniscus of the electrolyte solution has a

large surface area to volume ratio that amplifies the negative impact of ambient evaporation. Therefore, the water content of the electrolyte rapidly decreases [132], which not only causes a higher ion concentration at the interface of the meniscus [134] (hence different electrodeposition rate [132]) but also results in frequent clogging of the nano-pipet's opening [128]. To minimize the effect of ambient evaporation, environmental humidity is significantly raised in the printing chamber; however, a high humid environment could accelerate the oxidation of 3D printed Cu features and it is possible that the reported high Cu electrical resistivity (68 μΩ-cm [131], 39 μΩ-cm [130]) seen in some publications is due to possible oxidation in this humid environment. Table 8 summarizes all micron-scale additive microfabrication techniques reported in open literature for Cu.

Table 8. Comparing different metal 3D printing techniques

Printing Technology	Technique	Challenge	Confirmed Material Composition	Electrical Resistivity	Feature Size Range	Deposition Method
This work	Electro-brush plating	Dendrite Buildup	Copper (EDS)	6.34 μΩ-cm	~200 μm	Electro-chemical
FluidFM[135]	Dispensing Ions in Liquid	Precision pumping[136]	Not Reported	Not Reported	100 nm-1 μm	Electro-chemical
Meniscus-Confinement	Dispensing Aqueous Electrolyte [129]	Pipet Clogging [128]	Not Reported	5.3[data not shown] [129], 39 [130], and 63.6 [131] μΩ-cm	100 nm-10 μm	Electro-chemical
Assisted Laser Sintering Ink-Jet	Annealed Ink-Jet Printing	Porosity	Copper (XRD)	17.4 μΩ-cm[137]	~20 μm	Physical
Electroless-Plating Enhanced LIFT	Laser assisted photo reduction	Porosity	Copper (XRD)	12.9 μΩ-cm[138]	~250 μm	Physical

The work presented in this chapter, demonstrates the early success from a metal additive microfabrication technology that 1) is non-submersing approach, 2) is less sensitive to ambient humidity (based on preliminary observations), 3) employs dispense-free localized electrochemical deposition using electro-brush plating, and 4) exhibits 3D printed Cu with reasonable electrical resistivity (6.34 µΩ-cm) which is an important figure of merit for many electronic and thermal applications. The simplicity of demonstrated printing technique allows the realization of a multi-tip printing architecture which is a practical approach for parallel 3D printing, hence enabling additive batch microfabrication concept.

The presented 3D printing technology can be complementary to conventional microfabrication technologies particularly when high-aspect ratio metal structures are needed. Especially for the demonstrated micropillars, in the area of monolithic microfluidic cooling, integration of structures on the back side of high-power chips could be performed without the need for cleanroom processing. Additive microfabrication of Cu pillars at proper dimensions (100 to 200 µm diameter and 5:1 aspect ratio) is well-suited for integrated microfluidic cooling of electronics since no high-risk subtracting post-processing steps (e.g. plasma etching) need to be performed on a known-good electronic chip [103]. Moreover, the demonstrated tall Cu pillars (1.3 mm) enables larger cooling microfluidic cavities than what is possible to achieve with a 500 µm thick silicon substrate (300 to 400 µm tall cavity), hence resulting in a lower fluid pressure drop (8 times) as the modeling simulation shows in Figure 62 (for both cases, all parameters including friction coefficient, micropillar density, etc. are the same except for the channel height). The lower pressure drop results in the higher reliability (the lower risk of fluid leakage), the smaller circulation

pump, and the higher power dissipation performance. Thus, the presented metal 3D printing technology not only lowers the manufacturing barriers for integration of microfluidics but also improves thermal performance and addresses system level integration challenges.

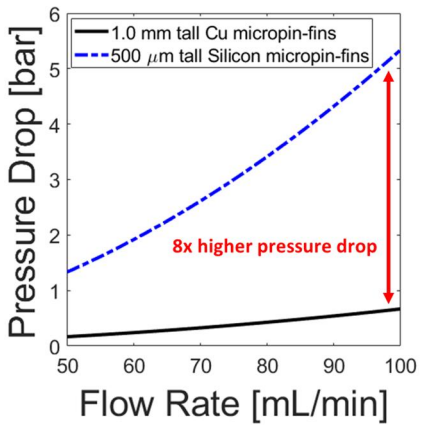


Figure 62 – Simulation of pressure drop in 1 mm and 500 µm tall microfluidic heatsinks.

In this chapter, we present the design of a feedback-driven micron-scale metal 3D printer in addition to a successful proof-of-concept demonstration of 3D printed Cu pillars at the micron-scale. The presented technology is a novel variant of localized electrodeposition-based 3D printing that enables additive manufacturing of 200 µm and potentially larger feature sizes. The size of the 3D printed features is a proper fit for thermal applications, which are envisioned to be a major use for the demonstrated technology. Moreover, the electrical and mechanical properties of the 3D printed Cu features (i.e. micropillars) are also characterized.

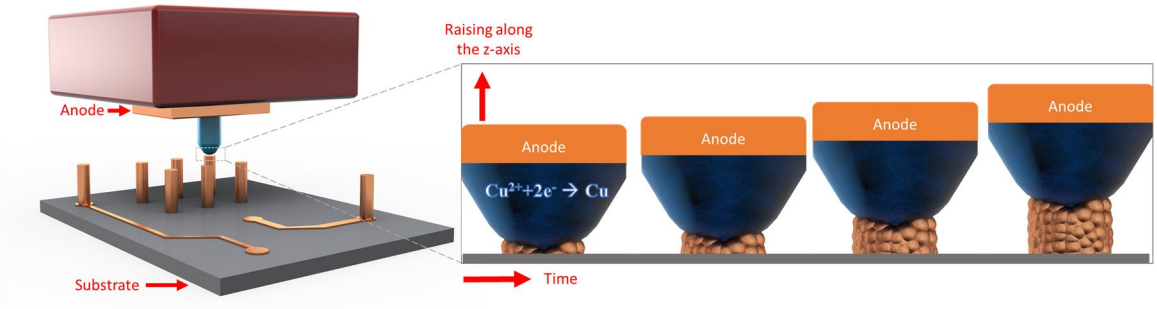


Figure 63 – Schematic of the 3D printer nozzle.

5.1 Basics of Operation:

5.1.1 Localization and Feedback Driven Electrodeposition

To enable localized electrodeposition, we use an electrolyte-containing medium (i.e. the printing-tip) to electroplate layers of Cu only within the area where the tip makes contact with the substrate, as illustrated in Figure 63. To form this ionic conductive medium, a commercial electro-brush plating pen plater is used to absorb an aqueous solution containing Cu(II) sulfate pentahydrate ($CuSO_4 \cdot 5H_2O$). As such, Cu^{2+} species within the electrolyte are reduced at the substrate surface (cathode) upon application of an electric field (E_{dep}) between the anode above the tip and the cathode, hence forming solid Cu layers. The E_{dep} is created through applying a potential and results in a Faradic electrodeposition current, i_{tip}, flowing from the anode electrode (i.e. positive polarity), via the electrolyte-containing tip towards the substrate, which is biased to a negative polarity. This performs an oxidation at the anode and electrodeposition on the substrate as is illustrated in Figure 63—the

electro-brush plating mechanism for different metals and materials is extensively documented in the literature [139], [140], [141], [142], [143], [144] and details of various processes involved in electrochemical deposition are well studied in prior efforts [145], [146], [147], [148].

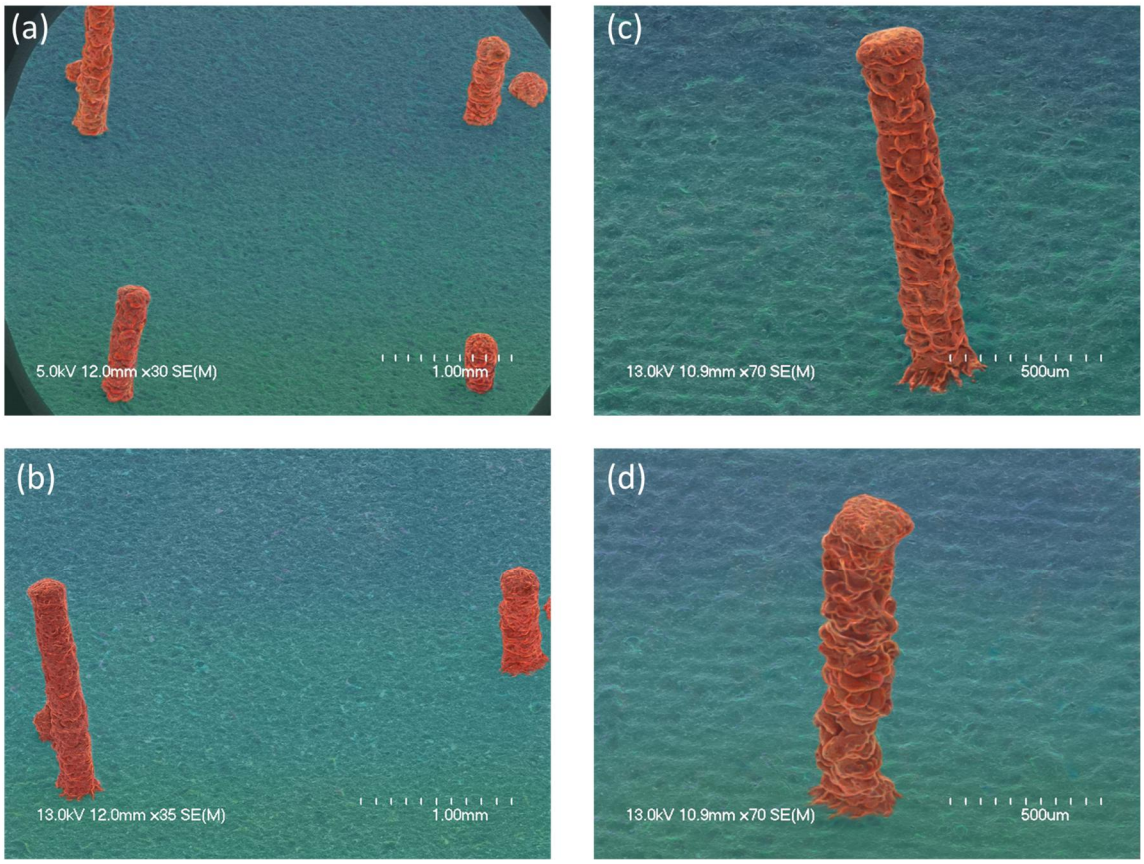


Figure 64 – (a) Side-view SEM image of 3D printed Cu pillars in 2x2 array. (b) Side-view SEM image of multi-height 3D printed Cu pillars. (c)-(d) SEM image of Cu pillar with 7:1 aspect-ratio.

The use of electro-brush plating enables localized electrodeposition without the need to submerse the substrate in a liquid electrolyte. When the tip forms an electrical contact with the substrate, cupric ions are reduced only within this region

of contact; using this approach, Cu growth above the substrate can occur as the tip is gradually raised during electrodeposition. To demonstrate this approach, Cu micropillars, which can be used for various electronic applications including microfluidic cooling [111], of various heights were printed. Side-view SEM image of Figure 64(a) shows multi-height Cu micropillars of 230 µm diameter in an array with approximately 2.5 mm pitch; height ranges from 300 µm to 1.4 mm. Figure 64(b), Figure 64(c), and Figure 64(d) illustrate high magnification SEM images of 3D printed features.

5.1.2 Details of System Configuration

These Cu micropillars are printed with a relatively inexpensive in-house developed hardware system (see Figure 65(a)) that contains all functions required for the presented additive microfabrication technology including precision linear stage, printing-head, and a feedback control loop. The precision linear stage with micropositioning capabilities is required throughout the process; printing micropillars requires steady and continuous mechanical movement at a very low speed— order of microns per minute. A high-resolution 16-bit position encoder and precision mechanical mechanisms are utilized to enable moving the printing-head linearly in the z-direction with a resolution to 33.5 nm while the substrate is independently actuated in the x-y plane (see Figure 65(b))— all the employed parts for building this setup including screws, servo motors, ICs, sensors, etc. are purchased as off-the-shelf commercial components.

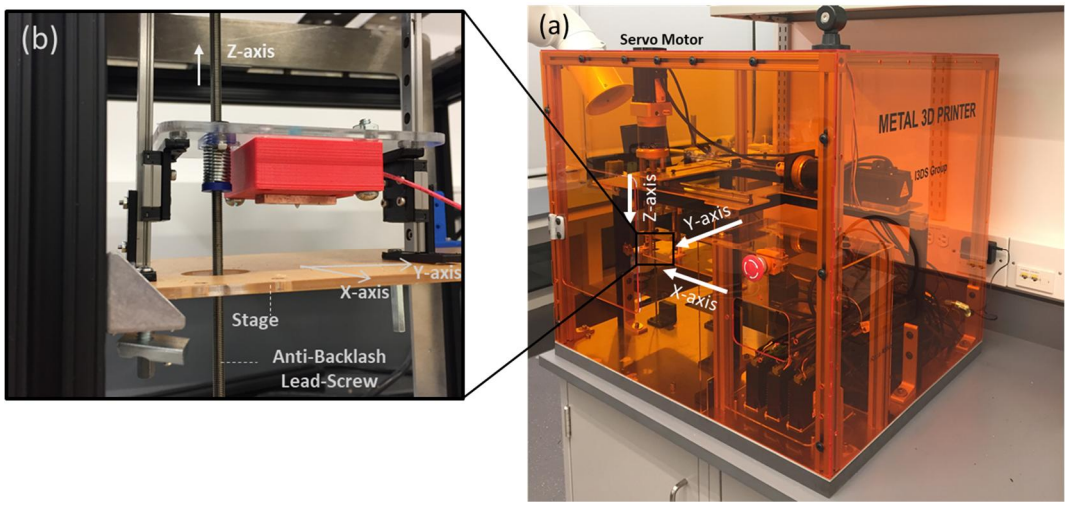


Figure 65 – (a) In-house developed 3D Printer. (b) Printer stage and the nozzle tip.

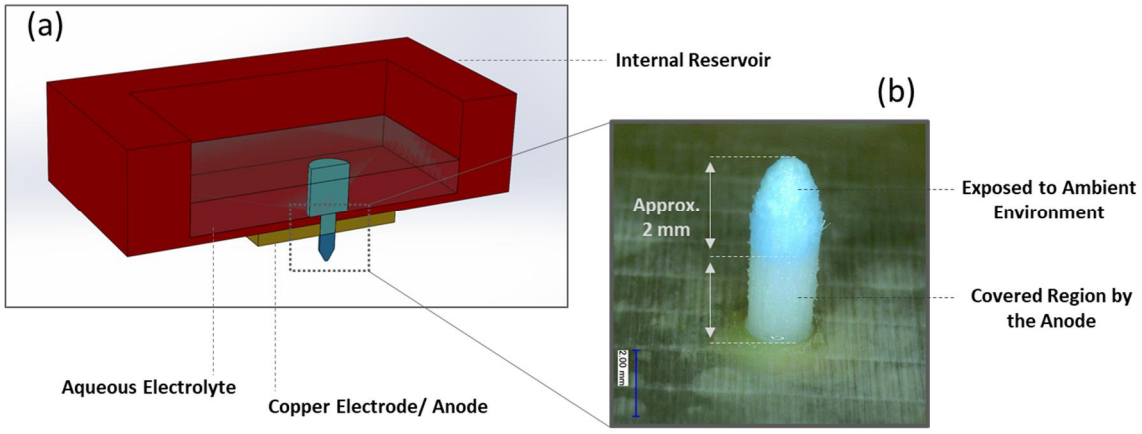


Figure 66 – (a) cross-sectional schematic of the printing-head. (b) Printing-tip

As the printing-head moves at a constant speed, the electrolyte reaches the tip through capillary action from an internal reservoir that contains the aqueous solution of $CuSO_4 \cdot 5H_2O$. Figure 66(a) illustrates details of the printing-head

structure and the reservoir where the tail of the printing-tip is inserted. This design allows and forms a medium that maintains electrolyte throughout the printing process and reducing the adverse effect of evaporation through capillary action.

As shown in Figure 67, the employed electro-brush pen plater (composed of 20 µm thick ultra-fine cotton fibers) has an approximately 175 µm wide tip which localizes electrodeposition in a region close to the diameter of the printing-tip; tip diameter of other specimens varies and up to 320 µm. Thus, the expected diameter of the printed micropillars is approximately similar to the diameter of the tip. Figure 68(a) shows the printed micropillars' diameters from 4 different experiments.

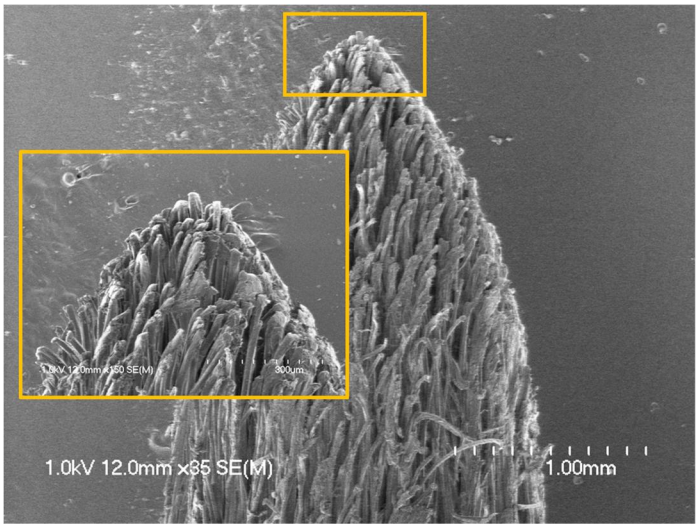


Figure 67 – SEM image of the printing-tip dimensions.

The difference between each of the experiments is the use of a new printing-tip to decouple a possible effect from a used tip of previous experiments on printed features. Table 9 shows relevant yield data of the printed micropillars; the dimensions of all printed micropillars are SEM imaged and measured. From the data, it is found

that the average micropillar diameter is approximately 40 to 50 µm larger than the printing-tip diameter.

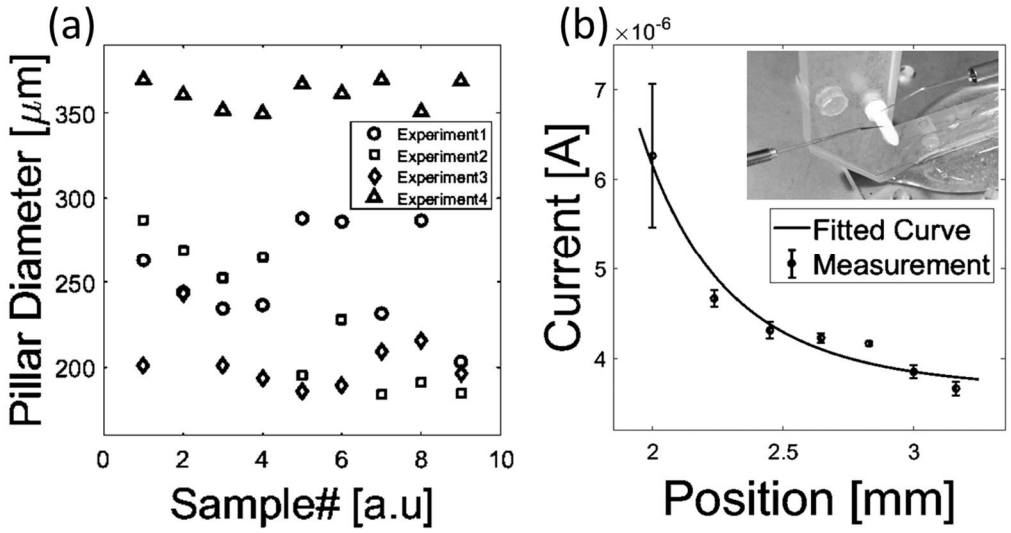


Figure 68 – (a) Diameters of 3D printed pillars per experiments. (b) Current drop vs distance from the anode connection.

Table 9. Result of the diameter characterization of 3D printed micropillars

Sample#	Number of Micropillars	Average Diameter	Standard Deviation	Average Tip Diameter
1	10	253.67 µm	26.95 µm	213 µm
2	9	228.55 µm	38.43 µm	175 µm
3	9	203.93 µm	16.39 µm	148 µm
4	11	362.73 µm	8.29 µm	320 µm

As shown in Figure 68(b), through a control experiment, i_{tip} is measured to rapidly drop as distance increases and therefore, the anode electrode needs to be positioned as close as possible to the tip to minimize electrical losses; this relates to

the ionic conductivity of the medium and higher equivalent electrical resistance further away from the anode. The anode-to-tip resistance determines the minimum required potential, V_{on}, for creating E_{dep}. To find V_{on}, cyclic voltammetry (CV) characterization of the electroplating medium is conducted, and the threshold voltage is measured to be approximately 0.35 V as shown in Figure 69(a). This implies that the electrodeposition occurs above a threshold of 0.35 V which corresponds to a minimum Faradic current.

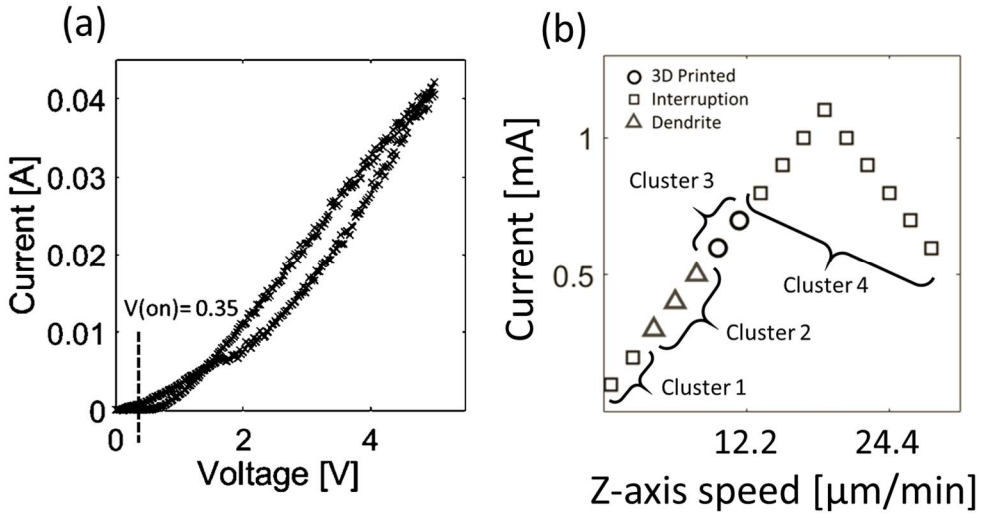


Figure 69 – (a) Cyclic voltammetry of electroplating medium. (b) Result of experiments for different z-axis speeds and electroplating current.

Generally, all variants of localized electrodeposition-based 3D printing technologies (e.g., meniscus confinement) demand a feedback loop to control and stabilize the printing process; the electronic feedback from the electroplating current and voltage drop across the electroplating circuit are the only possible parameters that could be monitored for the regulation of the electrodeposition rate (similar to

bulk electroplating but at different precision). To implement the required electronic feedback loop, an instrument amplifier converts the measured i_{tip} to an electric voltage (as indicated by node δ in Figure 70) that is monitored and compared against a threshold value; this indicator is a measure to stop the tip while substrate surface is detected. Once the measured i_{tip} becomes non-zero (greater than a minimum threshold), the z-axis stops to avoid excessive force and consequent tip deformation. This measurement is critical as the tip is formed using a relatively soft material (cotton fibers) and it could be mechanically deformed by up to 3.6 mm (tip's compliance is approximately 0.5 mm/N) if excessive force is applied by the servo-motor's maximum torque. Upon detecting the substrate, a buffer amplifier samples the voltage-drop on the tip, V_{tip}, that represents the contact resistance and compares it with a digital reference value. This reference value is an average measured of V_{tip} from 15 substrate detection control experiments. A change in contact resistance reflects contact area variation per experiment (all other process parameters are kept unchanged in each experiment), and therefore the sampled V_{tip} upon detecting the substrate represents this variation. The standard deviation of measured V_{tip} is found to be ±10% of the reference value. Thus, the i_{tip} is linearly adjusted within ±10% of an electroplating current setpoint to account for a contact area variation. This feedback loop ensures that i_{tip} is regulated and stabilized per experiment by considering contact area variations. It is important to note that the voltage source is disconnected right after sampling the contact resistance in order to prevent any unwanted electrodeposition while the tip is idle on the substrate.

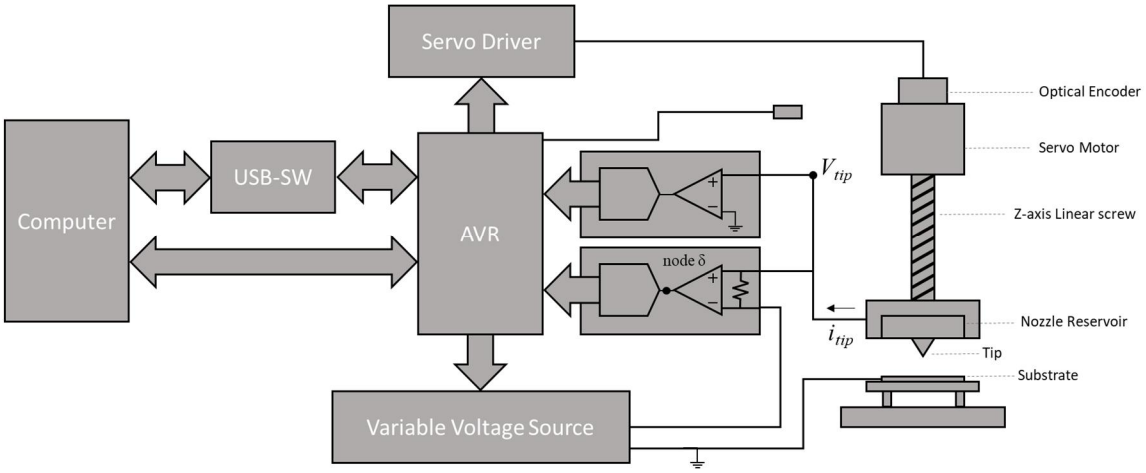


Figure 70 – Schematic diagram of the presented metal 3D printer.

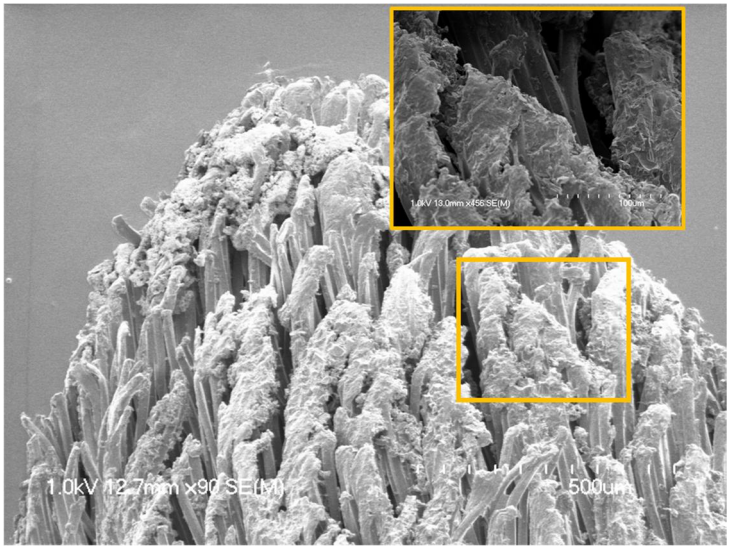


Figure 71 – Cu buildup into the printing-tip.

Electrodeposition rate and speed of the axis motion are two major parameters that primarily determine the outcome of the 3D printing process. Specifically, there were two failure modes that were observed: 1) excessive Cu buildup into the tip and 2) printing interruption. In order to mitigate Cu buildup inside the nozzle tip, the

feedback-driven system continuously regulates i_{tip} based on V_{tip} variations. Despite this feedback driven process, gradual Cu buildup inside the tip, as Figure 71, is observed to occur frequently, which results in a short circuit between the anode and the cathode electrodes; hence, measures are required to prevent such shorting.

In this work, it is found that the combination of reverse pulse plating (RPP) and the use of the electroplating current feedback control loop when tuned appropriately mitigate Cu buildup into the printing-tip. It is important to note that a deposition rate higher than the z-axis travel speed will result, however, in a rapid Cu buildup despite the use of RPP and the control feedback loop. In contrast, if the deposition rate is slower than the z-axis travel speed, an interruption (i.e., a gap) between the printing-tip and the contact area will occur, hence resulting in an open circuit. Thus, it is essential to maintain i_{tip} at an appropriate current-to-travel-speed ratio (CSR). Through a design of experiments, various CSRs were experimentally explored to identify most promising parameters. As shown in Figure 69(b), the data points of cluster 1 all yielded an interruption failure. The travel speed and plating current are set at very low rate resulting in an unsustainable printing process and a consequent interruption. In contrast, data points in cluster 2 represent a condition in which the printing-tip moves slowly in the z-axis relative to the Cu electrodeposition growth, which results in Cu build-up into the tip. It is found that the Cu buildup within the tip is most severe at slower travel speeds (i.e. lower left data points in cluster 2) than at higher ones (i.e. upper right data points in cluster 2). Therefore, increasing the travel speed may potentially mitigate this problem; however, an interruption in the electroplating may occur due to a faster z-axis movement than the electrodeposition rate. Indeed, there is a narrow process window

to achieve a balance between i_{tip} and z-axis travel speed, which is believed to be dependent upon the printing-tip material composition and geometry (i.e., different commercial brands might require different process parameters). Through experiments, the process parameters of data points in cluster 3, results in achieving continuous material deposition without experiencing an interruption nor a significant Cu buildup inside the nozzle. All the presented successful 3D printed Cu micropillars are based on the process parameters of cluster 3. It is noted that a further increase in travel-speed despite increasing i_{tip} unavoidably leads to interruption failure (cluster 4). Suitable mass deposition rate for faster growing micropillars, through the experiments of cluster 4, is found to be limited at z-axis travel speeds; moving the z-axis faster than a certain velocity will also cause interruption failure.

5.2 Characterization of 3D Printed Features

5.2.1 Material Composition

To evaluate the material composition of the printed features, an energy dispersive X-ray spectroscopy (EDS) technique was used. The high-resolution SEM image in Figure 72(a) shows grain-like texture of the printed Cu and pinpoints the location of where the EDS measurement is performed. The highest energy count in the spectrum corresponds to the Cu element as illustrated in Figure 72(b), demonstrating that the pillar is mainly composed of Cu. The other smaller energy peaks represent carbon and sulfur residues.

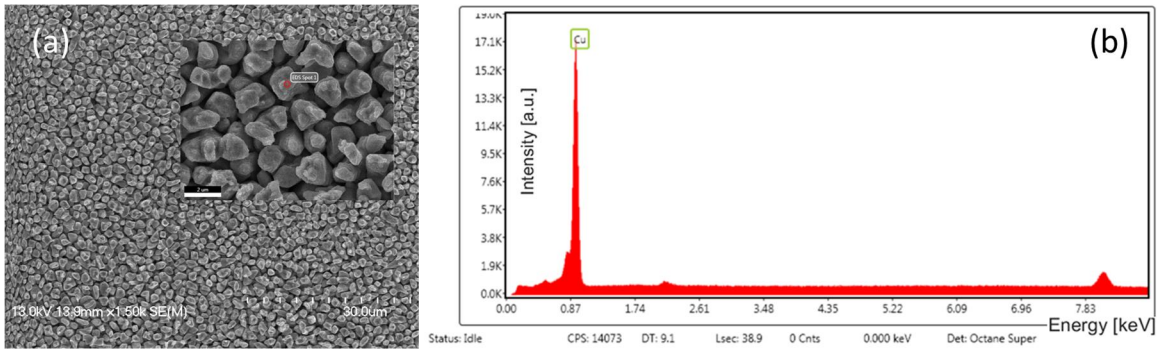


Figure 72 – (a) High-resolution SEM image of Cu grain-like texture. (b) EDS measurement from the deposited Cu.

Since the presented 3D printing scheme relies on electrochemical deposition, this implies that even metal alloys [149] could be deposited via this technology and therefore used for a variety of applications in which different material properties are needed. In this work, Cu is the material of interest due to its high electrical conductivity and low thermal resistance, hence making it a proper choice for many thermal and electrical applications. For example, microfluidic cooling of high-power dissipation ICs is commonly explored using silicon micropin-fins, which requires a series of microfabrication steps, including deep silicon etching [111]. This approach to microfluidic cooling, however, can be significantly simplified by replacing silicon-based micropin-fins with the additive microfabricated copper micropillars reported in this Ph.D. dissertation, as shown in the schematic of Figure 73; the thermal performance of such a microfluidic cooling system is expected to improve as Cu has a thermal conductivity three times larger than that of silicon [150] and making tall micropin-fins can improve thermal resistance and significantly reduce pressure drop.

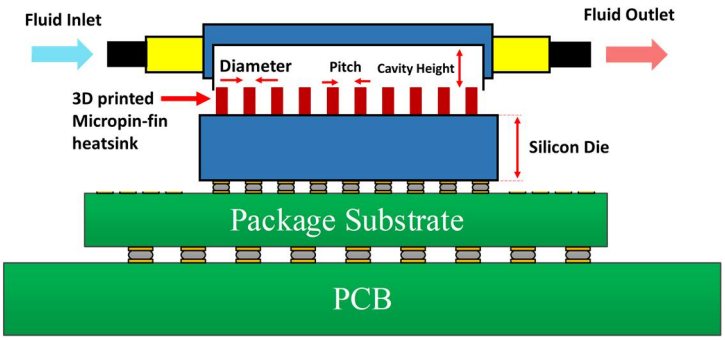


Figure 73 – Schematic of additively microfabricated Cu micropin-fins for integrated microfluidic based heatsinks.

5.2.2 Electrical Properties

The electrical properties of the 3D printed pillars, which includes DC resistance and current-carrying-capacity (CCC), are characterized by pumping electrical current (I) through the pillar from 10 mA to 100 mA. Simultaneously, the voltage-drop (V) across the pillar is measured using a 4-point Kelvin method and the results are shown in Figure 74. The measured I-V curve of the device-under-test (DUT) exhibits a linear behavior at all currents. This implies that the achievable CCC for the DUT is at least 100 mA (3.18 MA/m^2 current density given 200 µm diameter for the DUT) since the voltage drop stays in a linear regime. Table 10 shows the measured electrical resistance (R) of a few micropillars (DUTs) along with their dimensions (see Figure 75) and extracted Cu resistivity. The average electrical resistivity of Cu is 6.34±1 µΩ-cm, which is higher than that of bulk Cu (1.67 µΩ-cm) but falls within the range of reported electroplated Cu resistivity values in the literature, as shown in Table 11.

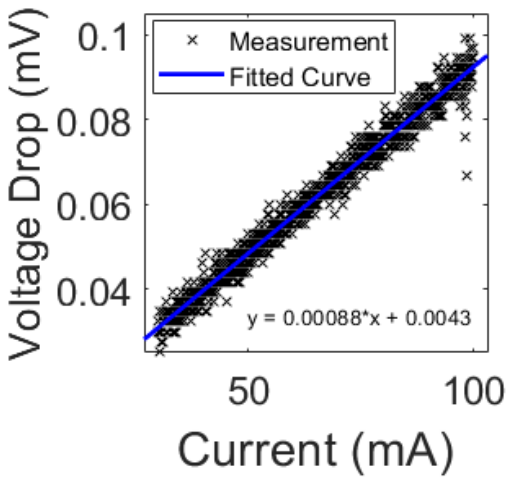


Figure 74 – I-V measurement conducted on the 3D printed micropillar.

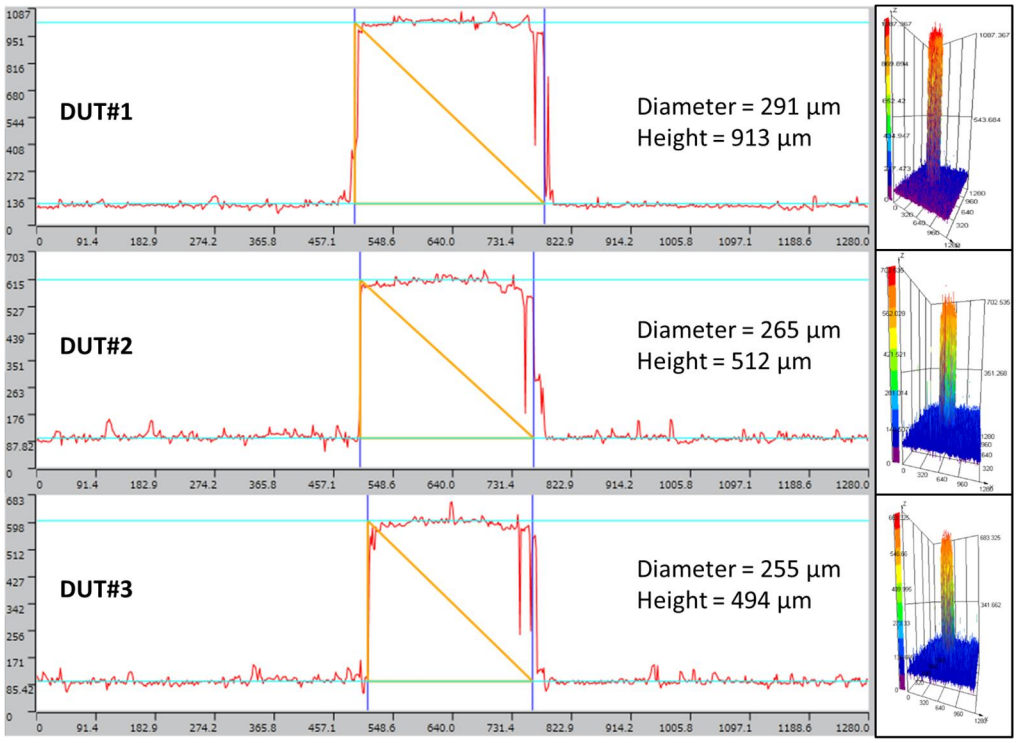


Figure 75 – Measured diameter and height of DUTs using optical profilometery.

Table 10 Electrical resistance measurement and extraction of Cu resistivity

DUT#	Measured Resistance [mΩ]	Diameter [μm]	Height [μm]	Resistivity [μΩ-cm]
1	0.88	291	913	6.41
2	0.49	265	512	5.28
3	0.71	255	494	7.34

5.2.3 Mechanical Characteristics

The mechanical properties of the printed Cu layer are studied by characterizing hardness (H) and Young's modulus (E). The reduced Young's modulus (E_r) and H for the sample are measured using a nano-indentation tool. The indentation tool is firstly calibrated with a known reference material (quartz) in order to parametrize an area function that models a Berkovich indenter tip while simultaneously compensating for thermal drift to achieve higher accuracy [151]. Next, the surface of the sample is loaded with a perpendicular force that ramps up to 7000 μN in 5 seconds in order to generate a loading-unloading vs. displacement curve as shown in Figure 76(a). H and E_r are both extracted from the unloading curve by the tool's software, as shown in Figure 76(b), and Figure 76(c), respectively. E, however, is calculated to be approximately 71.54 GPa using the method discussed by W. Oliver et al. [160] from the average measured E_r (80.89 GPa), assuming that the Cu Poisson's ratio is 0.34 [161].

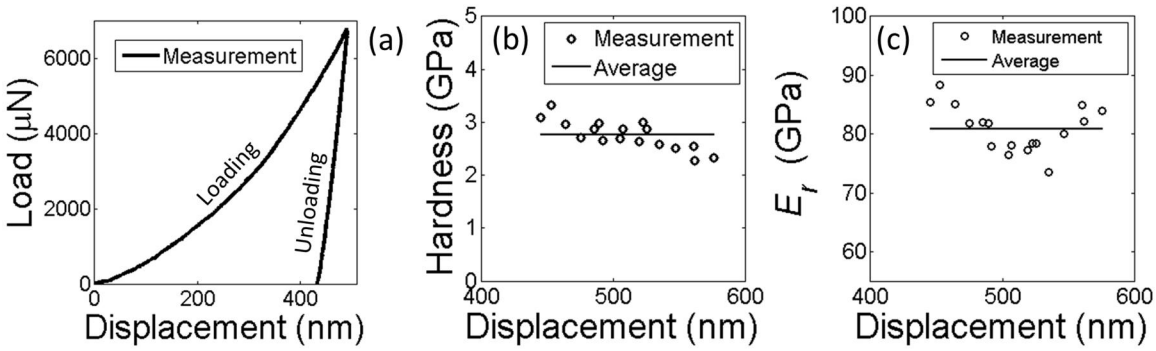


Figure 76 – (a) Nanoindentation load vs. displacement curve. (b) Extracted hardness vs. displacement for multiple measurements. (c) Extracted reduced Young's modulus (E_r) vs. displacement from unloading curve for multiple measurements.

The measured E is relatively close to the average reported value in the literature (see Table 11) for Cu electroplated via pulse-plating and RPP. The characterization results summarized in Table 11 imply that the localized electroplating technique employed in this 3D printing technology yields metal films that are comparable to conventional electroplating.

Table 11 Characterization results compared with reported measurements in literature

Characteristic	Measured Value	Reported in Literature
Cu Resistivity	6.34 μΩ-cm	1.6 to 68 μΩ-cm [152] [96] [131]
Young's Modulus	71.54 GPa	73 to 115 GPa [153] [154] [155] [156]
Cu Hardness	2.758 GPa	1 to 3.7 GPa [157] [158] [159]

5.3 Scalability of Density: Considerations

For thermal applications, a heatsink based on a denser array of 3D printed Cu micropillars is expected to exhibit better thermal attributes as the surface area increases proportionally with the micropillar density. Since the pitch of micropillars determines density, achieving a smaller pitch is beneficial. As shown in Figure 77 , the tip geometry impacts the pitch; choosing a smaller α allows a tighter pitch as the printing-tip could operate at a closer proximity to a printed pillar without damaging it or coming into contact with it. From Figure 77, it is noted that a tighter pitch could also be achieved for a given α if shorter micropillars are 3D printed (i.e., smaller aspect-ratios—2:1 vs. 7:1). This simply implies that the pitch is an inverse function of the micropillar's height.

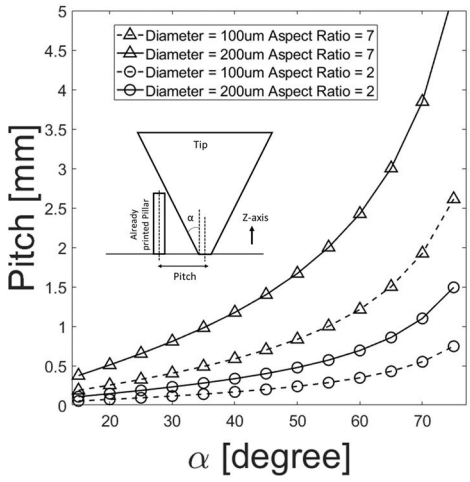


Figure 77 – Simulated pitch of 3D printed micropillars vs. tip geometry

From the SEM image of Figure 67, the α is measured to be approximately 50 to 55° for the employed electro-brush. Given the measured α, through geometry modeling, the plot in Figure 78 estimates that the smallest achievable pitch is 350

µm for 100 µm tall micropillars. As the micropillars are 3D printed taller, the minimum achievable pitch becomes coarser; the pitch is approximately 2 mm for the tallest micropillars (1.3 mm) demonstrated in Figure 64. This pitch-to-height dependency imposes two possible scenarios for the additive manufacturing of integrated microfluidic heatinks using the presented 3D printer:

1) A heatsink based on fine pitch and short Cu micropin-fins (which is comparable to monolithic silicon heatsinks).

2) A heatsink based on coarse pitch and tall Cu micropin-fins (which is comparable to commercial high-performance pinfin cold-plates [162] as shown in Figure 79).

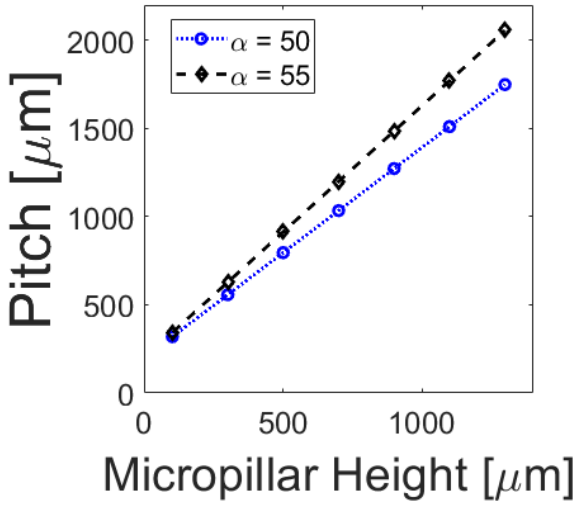


Figure 78 – Simulated pitch of 3D printed pillars vs. height of micropillar

Each of the abovementioned manufacturing scenarios that can potentially be implemented with the current capability of the 3D printer eliminates the need for a

TIM layer (unlike the cold-plate technology that requires a TIM layer). Therefore, a lower thermal resistance and better heatsink performance could be achieved. However, the necessary conductive layer that is initially formed on the silicon die (i.e., Ti adhesion layer and Cu seed-layer) creates multiple interfaces that could possibly impact the thermal resistance. Further investigation is necessary to evaluate these effects.

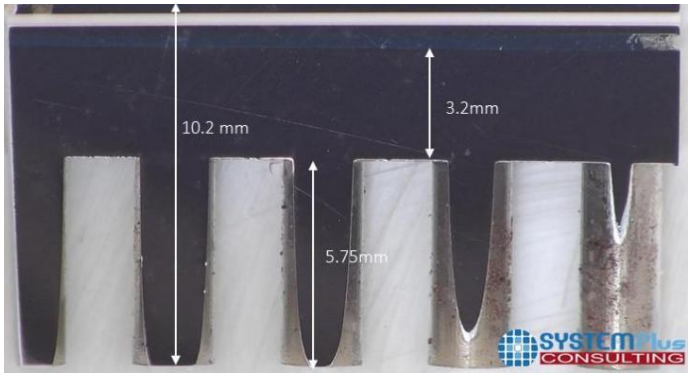


Figure 79 – Cross-section image of a commercial pinfin cold-plate [162].

5.4 Conclusion

In summary, we presented a proof-of-concept demonstration of a metal 3D printing technology that exploits localized electrodeposition for the additive manufacturing of Cu micropillars. Unlike conventional 3D printers that employ a laser beam for sintering or use a form of a dispensing nozzle either for the deposition of a material or the dispensing of a precursor (i.e. electrolyte), the technology demonstrated in this chapter utilizes a dispense-free mechanism for material deposition through an electro-brush plating technique. Using this technology, Cu micropillars are additively microfabricated with an average diameter of

approximately 200 µm and a height of 100 µm to 1.4 mm. Moreover, material composition of the printed pillars is analyzed and demonstrated to be almost entriely Cu. Mechanical and electrical properties of 3D printed Cu are characterized and compared against reported values in the literature. It is demonstrated that the material properties achieved by this technology are comparable to that of electroplated Cu.

CHAPTER 6. TECHNOLOGY TREND AND FUTURE WORKS

6.1 Additive Manufacturing and Future Applications: Electronic Packaging

Unlike conventional manufacturing processes, the cost of additively manufactured parts is insignificantly influenced by the structural complexity of the printed product or by the volume of production, making the 3D printing technology a viable solution for rapid prototyping and low volume production. These advantages establish additive fabrication as the chosen technology for the future of many different applications in industries such as aerospace, defense, and so forth. However, the fundamental limitations for high-precision, micron-scale 3D printing of non-polymeric materials make additive manufacturing challenging and even an inapplicable approach in the microelectronics industry. Nonetheless, continuous research in this field has led to the development of ink-jet printing of passives (e.g., in-package antennas and inductors) to address the need for incorporating metals into future printed electronics. Despite these recent advancements, subtractive microfabrication techniques are yet the only feasible path to process metals for building on-chip and in-package interconnects. Thus, the ongoing research and development efforts are primarily focused on improving production yield and scaling conventional microfabrication technologies. These manufacturing schemes, however, are essentially developed for building 2D microdevices and are challenging to employ for constructing 3D microstructures. For instance, complex fabrication processes such

as silicon etching, seed-layer deposition, electrochemical deposition, CMP, and so on are required to implement vertical interconnections (e.g. TSVs) for the 3D integration of electronics while all these microfabrication processes are specifically developed for 2D platforms. To address this issue, we envision utilizing 3D printing technology— that is primarily developed for making 3D structures— for constructing lateral and vertical interconnects for both 2D and 3D electronic applications (see Figure 80(a)). Furthermore, through-mold-vias could be implemented using the Cu 3D printing technique (see Figure 80(b)) for emerging stacked multi-chip FOWLP technology by allowing to vertically interconnect the top die to the package through the additive microfabrication of high aspect-ratio copper pillars.

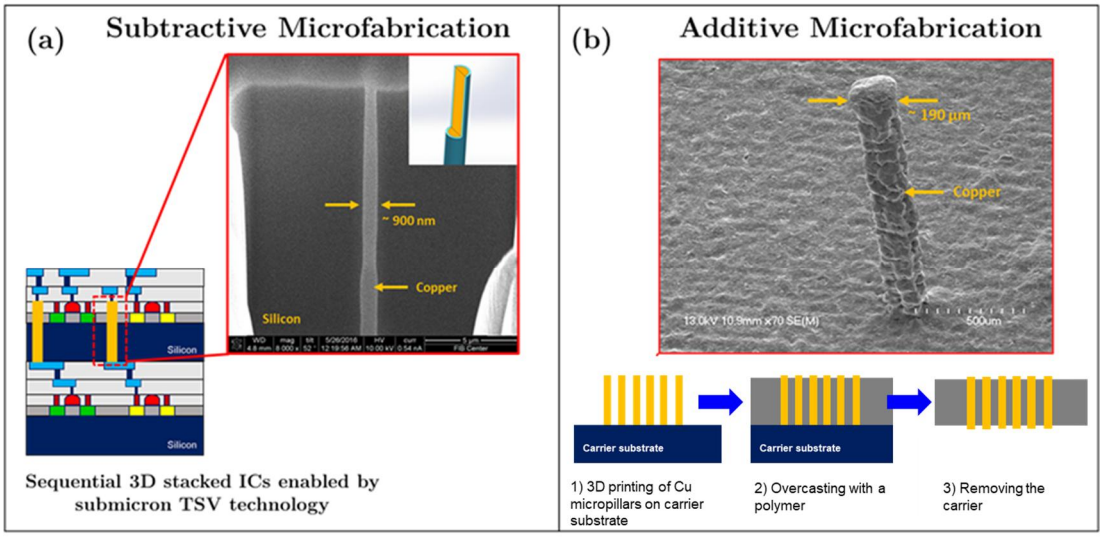


Figure 80 – (a) Microfabricated TSV through subtractive techniques. (b) Envisioned microfabrication of TSVs using the proposed 3D Printing technology.

6.2 Metal 3D Printing: Improving the Technology

6.2.1 Scaling Printing-Tip: Trimming Dimensions

As discussed in section 5.3, the pillar dimensions primarily depend on the printing-tip geometry. Thus, trimming the printing-tip dimensions could be a viable solution for achieving finer pillar diameter and pitch. For instance, the printing of 200 µm diameter pillars with 500 µm pitch is achievable if the tip diameter is approximately smaller than 500 µm as illustrated in schematic Figure 81. However, it could be challenging to modify the tip geometry due to its material composition (organic fibers).

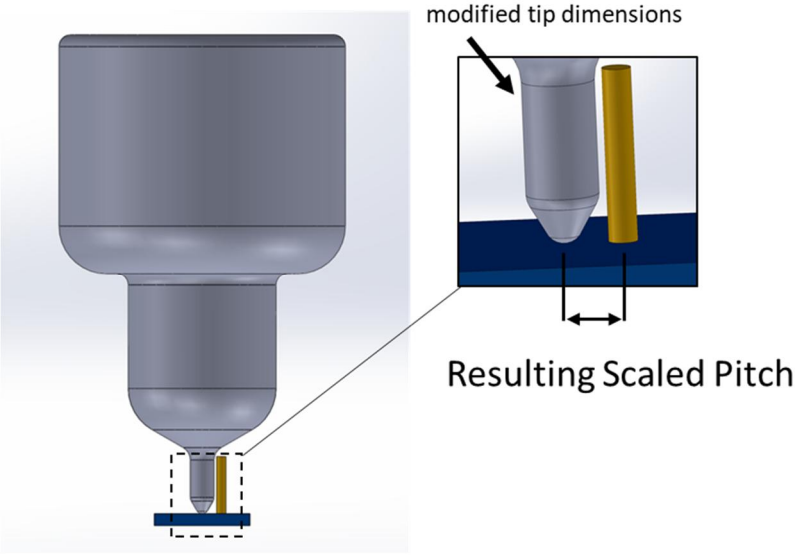


Figure 81 – Envisioned a scaled electro-brush plating tip

The commercial electro-brushes are manufactured through hot-pressing organic fibers in a mold. Thus, a finer tip could potentially be manufactured using a

custom-made mold; the mold will require aggressive dimensions which could be achieved by micro-machining techniques and silicon processing technologies. Moreover, laser trimming of the brush is another possible solution that could be implemented by exposing the brush tip to high energy laser pulses using a CO_2 laser micro-machining tool. This technique could be invasive and precision control is necessary since the organic fibers could violently burn due to the thermal energy of the laser beam.

6.2.2 Parallel Printing

The presented nozzle structure in Figure 63 is actuation-free and it only consists of two components which allows for the realization of a multi-tip nozzle architecture, enabling the concept of parallel 3D printing for mass manufacturing. The envisioned multi-tip design will consist of an ASIC chip that allows for the independent control of each individual tip. Thus, each tip resembles a pixel in an array that could be turned on/off for selective metal deposition and hence create a pattern. The tips will directly be built on top of the ASIC die per each pixel. The ASIC chip receives serial data from a microprocessor and multiplexes the data over the pixels accordingly. Moreover, the chip monitors the voltage drop over each pixel in order to regulate electroplating current density. This feedback control loop locally equalizes the metal deposition rate for each tip, ensuring that the pattern of interest is being 3D printed without dead pixels.

REFERENCES

[1] S. S. Iyer, "Heterogeneous Integration for Performance and Scaling," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 7, pp. 975–984, Jul. 2016.

[2] A. W. Topol *et al.*, "Three-dimensional integrated circuits," *IBM J. Res. Dev.*, vol. 50, no. 4.5, pp. 491–506, Jul. 2006.

[3] K. Kim, "1.1 Silicon technologies and solutions for the data-driven world," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–7.

[4] M. Horowitz, "1.1 Computing's energy problem (and what we can do about it)," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 10–14.

[5] T. Tekin, "Review of Packaging of Optoelectronic, Photonic, and MEMS Components," *IEEE J. Sel. Top. Quantum Electron.*, vol. 17, no. 3, pp. 704–719, May 2011.

[6] J. U. Knickerbocker *et al.*, "Three-dimensional silicon integration," *IBM J. Res. Dev.*, vol. 52, no. 6, pp. 553–569, Nov. 2008.

[7] R. Saleh *et al.*, "System-on-Chip: Reuse and Integration," *Proc. IEEE*, vol. 94, no. 6, pp. 1050–1069, Jun. 2006.

[8] J. U. Knickerbocker *et al.*, "Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch chip interconnection," *IBM J. Res. Dev.*, vol. 49, no. 4.5, pp. 725–753, Jul. 2005.

[9] S. Adamson *et al.*, " • This Roadmap Process presentation was prepared by these members of the IMAPS Global Business Council & National Technology Council:," p. 54.

[10] S. Qu and Y. Liu, "Fan-In Wafer-Level Chip-Scale Package," in *Wafer-Level Chip-Scale Packaging*, Springer, New York, NY, 2015, pp. 15–38.

[11] P. Garrou, "Wafer level chip scale packaging (WL-CSP): an overview," *IEEE Trans. Adv. Packag.*, vol. 23, no. 2, pp. 198–205, May 2000.

[12] Y. Liu, "Trends of power semiconductor wafer level packaging," *Microelectron. Reliab.*, vol. 50, no. 4, pp. 514–521, Apr. 2010.

[13] P. Liu, J. Wang, L. Tong, and Y. Tao, "Advances in the Fabrication Processes and Applications of Wafer Level Packaging," *J. Electron. Packag.*, vol. 136, no. 2, pp. 024002-024002–7, Apr. 2014.

[14] G. E. Moore, "Cramming More Components Onto Integrated Circuits," *Electronics*, vol. 38, no. 8, pp. 114–117, Apr. 1965.

[15] A. Papanikolaou, D. Soudris, and R. Radojcic, *Three Dimensional System Integration: IC Stacking Process and Design*. Springer Science & Business Media, 2010.

[16] M. Bohr, "The evolution of scaling from the homogeneous era to the heterogeneous era," in *2011 International Electron Devices Meeting*, 2011, pp. 1.1.1-1.1.6.

[17] S. P. Gurrum, S. K. Suman, Y. K. Joshi, and A. G. Fedorov, "Thermal issues in next-generation integrated circuits," *IEEE Trans. Device Mater. Reliab.*, vol. 4, no. 4, pp. 709–714, Dec. 2004.

[18] B. Chambers, T.-Y. T. Lee, and W. Blood, "Steady state and transient thermal analysis of chip scale packages," *J. Electron. Manuf.*, vol. 09, no. 02, pp. 131–139, Jun. 1999.

[19] J. Wei, "Challenges in Cooling Design of CPU Packages for High-Performance Servers," *Heat Transf. Eng.*, vol. 29, no. 2, pp. 178–187, Feb. 2008.

[20] V. Tiwari, D. Singh, S. Rajgopal, G. Mehta, R. Patel, and F. Baez, "Reducing Power in High-performance Microprocessors," in *Proceedings of the 35th Annual Design Automation Conference*, New York, NY, USA, 1998, pp. 732–737.

[21] I. L. Markov, "Limits on fundamental limits to computation," *Nature*, vol. 512, no. 7513, pp. 147–154, Aug. 2014.

[22] P. Coudrain *et al.*, "Experimental Insights Into Thermal Dissipation in TSV-Based 3-D Integrated Circuits," *IEEE Des. Test*, vol. 33, no. 3, pp. 21–36, Jun. 2016.

[23] A. Danowitz, K. Kelley, J. Mao, J. P. Stevenson, and M. Horowitz, "CPU DB: Recording Microprocessor History," *Commun ACM*, vol. 55, no. 4, pp. 55–63, Apr. 2012.

[24] W. Huang, K. Rajamani, M. R. Stan, and K. Skadron, "Scaling with Design Constraints: Predicting the Future of Big Chips," *IEEE Micro*, vol. 31, no. 4, pp. 16–29, Jul. 2011.

[25] Y. Liu, R. P. Dick, L. Shang, and H. Yang, "Accurate Temperature-dependent Integrated Circuit Leakage Power Estimation is Easy," in *Proceedings of the Conference on Design, Automation and Test in Europe*, San Jose, CA, USA, 2007, pp. 1526–1531.

[26] H. Su, F. Liu, A. Devgan, E. Acar, and S. Nassif, "Full Chip Leakage Estimation Considering Power Supply and Temperature Variations," in *Proceedings of the 2003 International Symposium on Low Power Electronics and Design*, New York, NY, USA, 2003, pp. 78–83.

[27] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[28] T. J. Breen *et al.*, "From Chip to Cooling Tower Data Center Modeling: Chip Leakage Power and Its Impact on Cooling Infrastructure Energy Efficiency," *J. Electron. Packag.*, vol. 134, no. 4, pp. 041009-041009–8, Nov. 2012.

[29] C. C. Lee *et al.*, "An Overview of the Development of a GPU with Integrated HBM on Silicon Interposer," in *2016 IEEE 66th Electronic Components and Technology Conference (ECTC)*, 2016, pp. 1439–1444.

[30] M. M. Sabry, A. K. Coskun, D. Atienza, T. Š. Rosing, and T. Brunschwiler, "Energy-Efficient Multiobjective Thermal Control for Liquid-Cooled 3-D Stacked Architectures," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 30, no. 12, pp. 1883–1896, Dec. 2011.

[31] W. Wahby, L. Zheng, Y. Zhang, and M. S. Bakir, "A Simulation Tool for Rapid Investigation of Trends in 3-DIC Performance and Power Consumption," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 6, no. 2, pp. 192–199, Feb. 2016.

[32] J.-M. Koo, S. Im, L. Jiang, and K. E. Goodson, "Integrated Microchannel Cooling for Three-Dimensional Electronic Circuit Architectures," *J. Heat Transf.*, vol. 127, no. 1, pp. 49–58, Feb. 2005.

[33] D. M. Wootton and D. N. Ku, "Fluid Mechanics of Vascular Systems, Diseases, and Thrombosis," *Annu. Rev. Biomed. Eng.*, vol. 1, no. 1, pp. 299–329, 1999.

[34] J. J. Hathcock, "Flow Effects on Coagulation and Thrombosis," *Arterioscler. Thromb. Vasc. Biol.*, vol. 26, no. 8, pp. 1729–1737, Aug. 2006.

[35] K. L. Berkner, "Blood Clotting: General Pathway," in *eLS*, John Wiley & Sons, Ltd, 2001.

[36] A. Bonnefoy, Q. Liu, C. Legrand, and M. M. Frojmovic, "Efficiency of Platelet Adhesion to Fibrinogen Depends on both Cell Activation and Flow," *Biophys. J.*, vol. 78, no. 6, pp. 2834–2843, Jun. 2000.

[37] A. L. Fogelson and K. B. Neeves, "Fluid Mechanics of Blood Clot Formation," *Annu. Rev. Fluid Mech.*, vol. 47, no. 1, pp. 377–403, 2015.

[38] M. Okada, B. Blombäck, M. D. Chang, and B. Horowitz, "Fibronectin and fibrin gel structure.," *J. Biol. Chem.*, vol. 260, no. 3, pp. 1811–1820, Feb. 1985.

[39] I. V. Pivkin, Z. Peng, G. E. Karniadakis, P. A. Buffet, M. Dao, and S. Suresh, "Biomechanics of red blood cells in human spleen and consequences for physiology and disease," *Proc. Natl. Acad. Sci.*, vol. 113, no. 28, pp. 7804–7809, Jul. 2016.

[40] "Schematic of blood cells clotting." [Online]. Available: http://www.oocities.org/sg/redbloodcellsarecute/pgbloodclotting.html. [Accessed: 10-Oct-2018].

[41] J. Kavalieros *et al.*, "Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering," in *2006 Symposium on VLSI Technology, 2006. Digest of Technical Papers.*, 2006, pp. 50–51.

[42] R. Li, Y. Lamy, W. F. A. Besling, F. Roozeboom, and P. M. Sarro, "Continuous deep reactive ion etching of tapered via holes for three-dimensional integration," *J. Micromechanics Microengineering*, vol. 18, no. 12, p. 125023, 2008.

[43] S. A. McAuley *et al.*, "Silicon micromachining using a high-density plasma source," *J. Phys. Appl. Phys.*, vol. 34, no. 18, p. 2769, 2001.

[44] K. W. Kok, W. J. Yoo, K. Sooriakumar, J. S. Pan, and E. Y. Lee, "Investigation of in situ trench etching process and Bosch process for fabricating high-aspect-ratio beams for microelectromechanical systems," *J. Vac. Sci. Technol. B*, vol. 20, no. 5, pp. 1878–1883, Sep. 2002.

[45] H. V. Jansen, M. J. de Boer, S. Unnikrishnan, M. C. Louwerse, and M. C. Elwenspoek, "Black silicon method X: a review on high speed and selective plasma etching of silicon with profile control: an in-depth comparison between Bosch and cryostat DRIE processes as a roadmap to next generation equipment," *J. Micromechanics Microengineering*, vol. 19, no. 3, p. 033001, 2009.

[46] B. Wu, A. Kumar, and S. Pamarthy, "High aspect ratio silicon etch: A review," *J. Appl. Phys.*, vol. 108, no. 5, p. 051101, Sep. 2010.

[47] F. Marty *et al.*, "Advanced etching of silicon based on deep reactive ion etching for silicon high aspect ratio microstructures and three-dimensional micro- and nanostructures," *Microelectron. J.*, vol. 36, no. 7, pp. 673–677, Jul. 2005.

[48] M. W. Pruessner, W. S. Rabinovich, T. H. Stievater, D. Park, and J. W. Baldwin, "Cryogenic etch process development for profile control of high aspect-ratio submicron silicon trenches," *J. Vac. Sci. Technol. B*, vol. 25, no. 1, pp. 21–28, Jan. 2007.

[49] X. Wang, W. Zeng, G. Lu, O. L. Russo, and E. Eisenbraun, "High aspect ratio Bosch etching of sub-0.25μm trenches for hyperintegration applications," *J. Vac. Sci. Technol. B*, vol. 25, no. 4, pp. 1376–1381, Jul. 2007.

[50] C. Chang *et al.*, "Etching submicrometer trenches by using the Bosch process and its application to the fabrication of antireflection structures," *J. Micromechanics Microengineering*, vol. 15, no. 3, p. 580, 2005.

[51] H.-H. Doh, J.-H. Kim, S.-H. Lee, and K.-W. Whang, "Mechanism of selective SiO2/Si etching with fluorocarbon gases (CF4, C4F8) and hydrogen mixture in electron cyclotron resonance plasma etching system," *J. Vac. Sci. Technol. A*, vol. 14, no. 5, pp. 2827–2834, Sep. 1996.

[52] T. Syau, B. J. Baliga, and R. W. Hamaker, "Reactive Ion Etching of Silicon Trenches Using SF 6 / O 2 Gas Mixtures," *J. Electrochem. Soc.*, vol. 138, no. 10, pp. 3076–3081, Oct. 1991.

[53] R. J. Belen, S. Gomez, D. Cooperberg, M. Kiehlbauch, and E. S. Aydil, "Feature-scale model of Si etching in SF6O2 plasma and comparison with experiments," *J. Vac. Sci. Technol. A*, vol. 23, no. 5, pp. 1430–1439, Sep. 2005.

[54] D. Qin, Y. Xia, and G. M. Whitesides, "Soft lithography for micro- and nanoscale patterning," *Nat. Protoc. Lond.*, vol. 5, no. 3, pp. 491–502, Mar. 2010.

[55] M. E. Wilson *et al.*, "Fabrication of circular microfluidic channels by combining mechanical micromilling and soft lithography," *Lab. Chip*, vol. 11, no. 8, pp. 1550–1555, 2011.

[56] J. G. Fernandez *et al.*, "Micro- and nanostructuring of freestanding, biodegradable, thin sheets of chitosan via soft lithography," *J. Biomed. Mater. Res. A*, vol. 85A, no. 1, pp. 242–247, Apr. 2008.

[57] B. Balakrisnan, S. Patil, and E. Smela, "Patterning PDMS using a combination of wet and dry etching," *J. Micromechanics Microengineering*, vol. 19, no. 4, p. 047002, 2009.

[58] J. C. Ciciliano, R. Abbaspour, J. Woodall, C. Wu, M. S. Bakir, and W. A. Lam, "Probing blood cell mechanics of hematologic processes at the single micron level," *Lab. Chip*, vol. 17, no. 22, pp. 3804–3816, 2017.

[59] B. J. Bain, *Blood Cells: A Practical Guide*. John Wiley & Sons, 2014.

[60] T. A. Doggett *et al.*, "Selectin-Like Kinetics and Biomechanics Promote Rapid Platelet Adhesion in Flow: The GPIbα-vWF Tether Bond," *Biophys. J.*, vol. 83, no. 1, pp. 194–205, Jul. 2002.

[61] N. A. Mody and M. R. King, "Platelet Adhesive Dynamics. Part II: High Shear-Induced Transient Aggregation via GPIbα-vWF-GPIbα Bridging," *Biophys. J.*, vol. 95, no. 5, pp. 2556–2574, Sep. 2008.

[62] Z. S. Kaplan and S. P. Jackson, "The Role of Platelets in Atherothrombosis," *ASH Educ. Program Book*, vol. 2011, no. 1, pp. 51–61, Dec. 2011.

[63] W. S. Nesbitt *et al.*, "A shear gradient–dependent platelet aggregation mechanism drives thrombus formation," *Nat. Med.*, vol. 15, no. 6, pp. 665–673, Jun. 2009.

[64] Q. Guo, S. P. Duffy, K. Matthews, A. T. Santoso, M. D. Scott, and H. Ma, "Microfluidic analysis of red blood cell deformability," *J. Biomech.*, vol. 47, no. 8, pp. 1767–1776, Jun. 2014.

[65] G. Deplaine *et al.*, "The sensing of poorly deformable red blood cells by the human spleen can be mimicked in vitro," *Blood*, vol. 117, no. 8, pp. e88–e95, Feb. 2011.

[66] S. Salehyar and Q. Zhu, "Effects of stiffness and volume on the transit time of an erythrocyte through a slit," *Biomech. Model. Mechanobiol.*, vol. 16, no. 3, pp. 921–931, Jun. 2017.

[67] M. S. Bakir and J. D. Meindl, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*, 1st ed. Norwood, MA, USA: Artech House, Inc., 2008.

[68] S. S. Iyer and T. Kirihata, "Three-Dimensional Integration: A Tutorial for Designers," *IEEE Solid-State Circuits Mag.*, vol. 7, no. 4, pp. 63–74, Fall 2015.

[69] D. H. Kim *et al.*, "Design and Analysis of 3D-MAPS (3D Massively Parallel Processor with Stacked Memory)," *IEEE Trans. Comput.*, vol. 64, no. 1, pp. 112–125, Jan. 2015.

[70] X. Zhang *et al.*, "Impact of On-Chip Interconnect on the Performance of 3-D Integrated Circuits With Through-Silicon Vias: Part II," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2510–2516, Jun. 2016.

[71] W. Guo *et al.*, "Copper through silicon via induced keep out zone for 10nm node bulk FinFET CMOS technology," in *2013 IEEE International Electron Devices Meeting*, 2013, pp. 12.8.1-12.8.4.

[72] A. Mercha *et al.*, "Comprehensive analysis of the impact of single and arrays of through silicon vias induced stress on high-k / metal gate CMOS performance," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 2.2.1-2.2.4.

[73] S. V. Huylenbroeck *et al.*, "Advanced Metallization Scheme for 3x50µm Via Middle TSV and Beyond," in *Electronic Components and Technology Conference (ECTC) , 2015 IEEE 65th*, 2015, pp. 66–72.

[74] P. J. Kelly and R. D. Arnell, "Magnetron sputtering: a review of recent developments and applications," *Vacuum*, vol. 56, no. 3, pp. 159–172, Mar. 2000.

[75] C. A. Nichols, S. M. Rossnagel, and S. Hamaguchi, "Ionized physical vapor deposition of Cu for high aspect ratio damascene trench fill applications," *J. Vac. Sci. Technol. B*, vol. 14, no. 5, pp. 3270–3275, Sep. 1996.

[76] A. Redolfi *et al.*, "Implementation of an industry compliant, 5×50µm, via-middle TSV technology on 300mm wafers," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 1384–1388.

[77] I. Shubin *et al.*, "Package demonstration of an interposer with integrated TSVs and flexible compliant interconnects," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 329–333.

[78] R. Chaware, K. Nagarajan, and S. Ramalingam, "Assembly and reliability challenges in 3D integration of 28nm FPGA die on a large high density 65nm passive interposer," in *Electronic Components and Technology Conference (ECTC), 2012 IEEE 62nd*, 2012, pp. 279–283.

[79] H. B. Chang *et al.*, "High-aspect ratio through silicon via (TSV) technology," in *2012 Symposium on VLSI Technology (VLSIT)*, 2012, pp. 173–174.

[80] M. Koyanagi, T. Fukushima, and T. Tanaka, "High-Density Through Silicon Vias for 3-D LSIs," *Proc. IEEE*, vol. 97, no. 1, pp. 49–59, Jan. 2009.

[81] G. V. der Plas *et al.*, "Design Issues and Considerations for Low-Cost 3-D TSV IC Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 293–307, Jan. 2011.

[82] S. Aoyama *et al.*, "Advanced Cr dry etching process," 1999, vol. 3748, pp. 137–146.

[83] M. A. Ehsan, Z. Zhou, L. Liu, and Y. Yi, "An Analytical Through Silicon Via (TSV) Surface Roughness Model Applied to a Millimeter Wave 3-D IC," *IEEE Trans. Electromagn. Compat.*, vol. 57, no. 4, pp. 815–826, Aug. 2015.

[84] L. Filipovic, R. L. de Orio, and S. Selberherr, "Effects of sidewall scallops on the performance and reliability of filled copper and open tungsten TSVs," in *Proceedings of the 21th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA)*, 2014, pp. 321–326.

[85] S. M. Rossnagel, A. Sherman, and F. Turner, "Plasma-enhanced atomic layer deposition of Ta and Ti for interconnect diffusion barriers," *J. Vac. Sci. Technol. B*, vol. 18, no. 4, pp. 2016–2020, Jul. 2000.

[86] J. W. Elam, M. Schuisky, J. D. Ferguson, and S. M. George, "Surface chemistry and film growth during TiN atomic layer deposition using TDMAT and NH3," *Thin Solid Films*, vol. 436, no. 2, pp. 145–156, Jul. 2003.

[87] I.-S. Jeon, S.-B. Kang, H.-S. Lim, and G. Choi, "Method of manufacturing a barrier metal layer using atomic layer deposition," US6399491 B2, 04-Jun-2002.

[88] Y. Feng, G. E. McGuire, O. A. Shenderova, H. Ke, and S. L. Burkett, "Fabrication of copper/carbon nanotube composite thin films by periodic pulse reverse electroplating using nanodiamond as a dispersing agent," *Thin Solid Films*, vol. 615, pp. 116–121, Sep. 2016.

[89] Y. Feng and S. L. Burkett, "Fabrication and electrical performance of through silicon via interconnects filled with a copper/carbon nanotube composite," *J. Vac. Sci. Technol. B*, vol. 33, no. 2, p. 022004, Mar. 2015.

[90] M. S. Chandrasekar and M. Pushpavanam, "Pulse and pulse reverse plating—Conceptual, advantages and applications," *Electrochimica Acta*, vol. 53, no. 8, pp. 3313–3322, Mar. 2008.

[91] R. Akolkar and U. Landau, "Mechanistic Analysis of the 'Bottom-Up' Fill in Copper Interconnect Metallization," *J. Electrochem. Soc.*, vol. 156, no. 9, pp. D351–D359, Sep. 2009.

[92] T. B. Richardson *et al.*, "Copper metallization of through silicon via," US7670950 B2, 02-Mar-2010.

[93] "Enthone - MICROFAB® DVF 200." [Online]. Available: http://enthone.com/Industries/Electronics_Solutions/Technology_Selector/Products/MICROFAB_DVF_200.aspx. [Accessed: 20-Sep-2016].

[94] Y. Zhang, G. Ding, H. Wang, and P. Cheng, "Microstructure of Electrodeposited Cu Micro-cylinders in High-Aspect-Ratio Blind Holes and Crystallographic Texture of the Cu Overburden Film," *J. Mater. Sci. Technol.*, vol. 32, no. 4, pp. 355–361, Apr. 2016.

[95] "electrolytic-copper-and-tin | technic.com." [Online]. Available: http://www.technic.com/apac/applications/pcb/chemistry/electrolytic-copper-and-tin. [Accessed: 20-Sep-2016].

[96] S.-C. Chang *et al.*, "Wetting effect on gap filling submicron damascene by an electrolyte free of levelers," *J. Vac. Sci. Technol. B*, vol. 20, no. 4, pp. 1311–1316, Jul. 2002.

[97] J. Xie and M. Swaminathan, "Electrical-Thermal Co-Simulation of 3D Integrated Systems With Micro-Fluidic Cooling and Joule Heating Effects," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 2, pp. 234–246, Feb. 2011.

[98] R. Abbaspour, D. K. Brown, and M. S. Bakir, "Fabrication and electrical characterization of sub-micron diameter through-silicon via for heterogeneous three-dimensional integrated circuits," *J. Micromechanics Microengineering*, vol. 27, no. 2, p. 025011, 2017.

[99] A. Bar-Cohen and P. Wang, "Thermal Management of On-Chip Hot Spot," *J. Heat Transf.*, vol. 134, no. 5, pp. 051017-051017–11, Apr. 2012.

[100] Y. Zhang, L. Zheng, and M. S. Bakir, "3-D Stacked Tier-Specific Microfluidic Cooling for Heterogeneous 3-D ICs," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 3, no. 11, pp. 1811–1819, Nov. 2013.

[101] C. Green, A. G. Fedorov, and Y. K. Joshi, "Fluid-to-Fluid Spot-to-Spreader (F2/S2) Hybrid Heat Sink for Integrated Chip-Level and Hot Spot-Level Thermal Management," *J. Electron. Packag.*, vol. 131, no. 2, pp. 025002-025002–10, Apr. 2009.

[102] R. S. Prasher *et al.*, "Nusselt Number and Friction Factor of Staggered Arrays of Low Aspect Ratio Micropin-Fins Under Cross Flow for Water as Fluid," *J. Heat Transf.*, vol. 129, no. 2, pp. 141–153, Apr. 2006.

[103] T. E. Sarvey *et al.*, "Integrated Circuit Cooling Using Heterogeneous Micropin-Fin Arrays for Nonuniform Power Maps," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. PP, no. 99, pp. 1–11, 2017.

[104] C. E. Green, P. A. Kottke, T. E. Sarvey, A. G. Fedorov, Y. Joshi, and M. S. Bakir, "Performance and Integration Implications of Addressing Localized Hotspots Through Two Approaches: Clustering of Micro Pin-Fins and Dedicated Microgap Coolers," p. V001T09A056, Jul. 2015.

[105] D. Lorenzini *et al.*, "Embedded single phase microfluidic thermal management for non-uniform heating and hotspots using microgaps with variable pin fin clustering," *Int. J. Heat Mass Transf.*, vol. 103, pp. 1359–1370, Dec. 2016.

[106] D. Nikolic, M. Hutchison, P. T. Sapin, and A. J. Robinson, "Hot spot targeting with a liquid impinging jet array waterblock," in *2009 15th International Workshop on Thermal Investigations of ICs and Systems*, 2009, pp. 168–173.

[107] Y. Han, B. L. Lau, and X. Zhang, "Package-Level Microjet-Based Hotspot Cooling Solution for Microelectronic Devices," *IEEE Electron Device Lett.*, vol. 36, no. 5, pp. 502–504, May 2015.

[108] I. Chowdhury *et al.*, "On-chip cooling by superlattice-based thin-film thermoelectrics," *Nat. Nanotechnol.*, vol. 4, no. 4, pp. 235–238, Apr. 2009.

[109] S. Narayanan, A. G. Fedorov, and Y. K. Joshi, "On-chip thermal management of hotspots using a perspiration nanopatch," *J. Micromechanics Microengineering*, vol. 20, no. 7, p. 075010, 2010.

[110] M. H. H. Nasr, "Extreme microgap based hotspot thermal management with convective boiling of refrigerant," Thesis, Georgia Institute of Technology, 2016.

[111] R. Abbaspour *et al.*, "Combined finned microgap with dedicated extreme-microgap hotspot flow for high performance thermal management," in *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2016, pp. 1388–1392.

[112] G. H. Wong, L. Ding, and W. L. Loh, "Evaluation of de-scum methodology for through silicon via (TSV) etch to improve TSV defects performance," in *Electronics Packaging Technology Conference (EPTC 2013), 2013 IEEE 15th*, 2013, pp. 771–774.

[113] F. Laerme, A. Schilp, K. Funk, and M. Offenberg, "Bosch deep silicon etching: improving uniformity and etch rate for advanced MEMS applications," in *Twelfth IEEE International Conference on Micro Electro Mechanical Systems, 1999. MEMS '99*, 1999, pp. 211–216.

[114] B. M. A., "Deep anisotropic dry etching of silicon microstructures by high-density plasmas," Department of Applied Science, Delft University of Technology, 2004.

[115] H. Bikas, P. Stavropoulos, and G. Chryssolouris, "Additive manufacturing methods and modelling approaches: a critical review," *Int. J. Adv. Manuf. Technol.*, vol. 83, no. 1–4, pp. 389–405, Mar. 2016.

[116] I. Gibson, D. Rosen, and B. Stucker, "Applications for Additive Manufacture," in *Additive Manufacturing Technologies*, Springer New York, 2015, pp. 451–474.

[117] Y. Huang, M. C. Leu, J. Mazumder, and A. Donmez, "Additive Manufacturing: Current State, Future Potential, Gaps and Needs, and Recommendations," *J. Manuf. Sci. Eng.*, vol. 137, no. 1, pp. 014001-014001–10, Feb. 2015.

[118] M. Vaezi, H. Seitz, and S. Yang, "A review on 3D micro-additive manufacturing technologies," *Int. J. Adv. Manuf. Technol.*, vol. 67, no. 5–8, pp. 1721–1754, Jul. 2013.

[119] L. Hirt, A. Reiser, R. Spolenak, and T. Zambelli, "Additive Manufacturing of Metal Structures at the Micrometer Scale," *Adv. Mater.*, p. n/a-n/a, Jan. 2017.

[120] M. Zenou, A. Sa'ar, and Z. Kotler, "Laser jetting of femto-liter metal droplets for high resolution 3D printed structures," *Sci. Rep.*, vol. 5, p. 17265, Nov. 2015.

[121] K. Maeda and T. H. C. Childs, "Laser sintering (SLS) of hard metal powders for abrasion resistant coatings," *J. Mater. Process. Technol.*, vol. 149, no. 1, pp. 609–615, Jun. 2004.

[122] W. E. Frazier, "Metal Additive Manufacturing: A Review," *J. Mater. Eng. Perform.*, vol. 23, no. 6, pp. 1917–1928, Jun. 2014.

[123] B. Dutta and F. H. (Sam) Froes, "The Additive Manufacturing (AM) of titanium alloys," *Met. Powder Rep.*, vol. 72, no. 2, pp. 96–106, Mar. 2017.

[124] Y. Zheng, Z. He, Y. Gao, and J. Liu, "Direct Desktop Printed-Circuits-on-Paper Flexible Electronics," *Sci. Rep.*, vol. 3, p. 1786, May 2013.

[125] T. Takai, H. Nakao, and F. Iwata, "Three-dimensional microfabrication using local electrophoresis deposition and a laser trapping technique," *Opt. Express*, vol. 22, no. 23, pp. 28109–28117, Nov. 2014.

[126] F. Iwata and J. Metoki, "Microelectrophoresis deposition using a nanopipette for three-dimensional structures," in *2014 International Conference on Manipulation, Manufacturing and Measurement on the Nanoscale (3M-NANO)*, 2014, pp. 304–307.

[127] A. P. Suryavanshi and M.-F. Yu, "Probe-based electrochemical fabrication of freestanding Cu nanowire array," *Appl. Phys. Lett.*, vol. 88, no. 8, p. 083103, Feb. 2006.

[128] S. K. Seol, D. Kim, S. Lee, J. H. Kim, W. S. Chang, and J. T. Kim, "Electrodeposition-based 3D Printing of Metallic Microarchitectures with Controlled Internal Structures," *Small*, vol. 11, no. 32, pp. 3896–3902, Aug. 2015.

[129] J. Hu and M.-F. Yu, "Meniscus-Confined Three-Dimensional Electrodeposition for Direct Writing of Wire Bonds," *Science*, vol. 329, no. 5989, pp. 313–316, Jul. 2010.

[130] A. Behroozfar *et al.*, "Microscale 3D Printing of Nanotwinned Copper," *Adv. Mater.*, vol. 30, no. 4, p. 1705107, Jan. 2018.

[131] Y. Lei *et al.*, "Dynamic 'Scanning-Mode' Meniscus Confined Electrodepositing and Micropatterning of Individually Addressable Ultraconductive Copper Line Arrays," *J. Phys. Chem. Lett.*, vol. 9, no. 9, pp. 2380–2387, May 2018.

[132] S. Morsali, S. Daryadel, Z. Zhou, A. Behroozfar, D. Qian, and M. Minary-Jolandan, "Multi-physics simulation of metal printing at micro/nanoscale using meniscus-confined electrodeposition: Effect of environmental humidity," *J. Appl. Phys.*, vol. 121, no. 2, p. 024903, Jan. 2017.

[133] A. Assy and S. Gomès, "Temperature-dependent capillary forces at nano-contacts for estimating the heat conduction through a water meniscus," *Nanotechnology*, vol. 26, no. 35, p. 355401, 2015.

[134] S. Morsali *et al.*, "Multi-physics simulation of metal printing at micro/nanoscale using meniscus-confined electrodeposition: Effect of nozzle speed and diameter," *J. Appl. Phys.*, vol. 121, no. 21, p. 214305, Jun. 2017.

[135] L. Hirt, R. R. Grüter, T. Berthelot, R. Cornut, J. Vörös, and T. Zambelli, "Local surface modification via confined electrochemical deposition with FluidFM," *RSC Adv.*, vol. 5, no. 103, pp. 84517–84522, 2015.

[136] L. Hirt *et al.*, "Template-Free 3D Microprinting of Metals Using a Force-Controlled Nanopipette for Layer-by-Layer Electrodeposition," *Adv. Mater.*, vol. 28, no. 12, pp. 2311–2315, Mar. 2016.

[137] H. Min, B. Lee, S. Jeong, and M. Lee, "Laser-direct process of Cu nano-ink to coat highly conductive and adhesive metallization patterns on plastic substrate," *Opt. Lasers Eng.*, vol. 80, pp. 12–16, May 2016.

[138] W. K. C. Yung *et al.*, "Additive and Photochemical Manufacturing of Copper," *Sci. Rep.*, vol. 6, p. srep39584, Dec. 2016.

[139] W. Wang, X. Liu, and Z. Shi, "Mechanisms and influences of electro-brush plating micro-force on coatings performances," *J. Mater. Res.*, vol. 31, no. 15, pp. 2337–2346, Aug. 2016.

[140] B. Wu, B. Xu, B. Zhang, X. Jing, and C. Liu, "Automatic brush plating: An update on brush plating," *Mater. Lett.*, vol. 60, no. 13, pp. 1673–1677, Jun. 2006.

[141] D. Vanek, "An update on brush plating," *Met. Finish.*, vol. 100, no. 7, pp. 18–20, Jul. 2002.

[142] L. Isern, S. Impey, H. Almond, S. J. Clouser, and J. L. Endrino, "Structure zone diagram and particle incorporation of nickel brush plated composite coatings," *Sci. Rep.*, vol. 7, p. 44561, Mar. 2017.

[143] S. Qi, X. Li, Z. Zhang, and H. Dong, "Fabrication and characterisation of electro-brush plated nickel-graphene oxide nano-composite coatings," *Thin Solid Films*, vol. 644, pp. 106–114, Dec. 2017.

[144] J. W. Dini, "Brush plating: Recent property data," *Met. Finish.*, vol. 95, no. 6, pp. 88–93, Jun. 1997.

[145] W. Wang and X. Liu, "Influences of brush plating solutions composition and technological parameters on the quality of rolled copper foil surface coatings," *J. Mater. Res.*, vol. 30, no. 24, pp. 3766–3775, Dec. 2015.

[146] J. Hu *et al.*, "Effect of strain rate on tensile properties of electric brush-plated nanocrystalline copper," *Mater. Sci. Eng. A*, vol. 618, pp. 621–628, Nov. 2014.

[147] N. Rajasekaran and S. Mohan, "Structure, microstructure and corrosion properties of brush-plated Cu–Ni alloy," *J. Appl. Electrochem.*, vol. 39, no. 10, p. 1911, Oct. 2009.

[148] Z. Jiang, X. Liu, G. Li, Q. Jiang, and J. Lian, "Strain rate sensitivity of a nanocrystalline Cu synthesized by electric brush plating," *Appl. Phys. Lett.*, vol. 88, no. 14, p. 143115, Apr. 2006.

[149] R. M. Krishnan, C. J. Kennedy, S. Jayakrishnan, S. Sriveeraraghavan, S. R. Natarajan, and P. G. Venkatakrishnan, "Electrodeposition of nickel-tungsten alloys," *Met. Finish.*, vol. 93, no. 7, pp. 33–39, Jul. 1995.

[150] E. Lewis, R. Koba, and R. L. Woodin, "Diamond electronic packages featuring bonded metal," WO1997005757A1, 13-Feb-1997.

[151] J. G. Swadener, E. P. George, and G. M. Pharr, "The correlation of the indentation size effect measured with indenters of various shapes," *J. Mech. Phys. Solids*, vol. 50, no. 4, pp. 681–694, Apr. 2002.

[152] V. A. Vas'ko, I. Tabakovic, S. C. Riemer, and M. T. Kief, "Effect of organic additives on structure, resistivity, and room-temperature recrystallization of electrodeposited copper," *Microelectron. Eng.*, vol. 75, no. 1, pp. 71–77, Jul. 2004.

[153] D. T. Read, Y. W. Cheng, and R. Geiss, "Morphology, microstructure, and mechanical properties of a copper electrodeposit," *Microelectron. Eng.*, vol. 75, no. 1, pp. 63–70, Jul. 2004.

[154] Y. Zhou *et al.*, "Measurement of Young's modulus and residual stress of copper film electroplated on silicon wafer," *Thin Solid Films*, vol. 460, no. 1, pp. 175–180, Jul. 2004.

[155] S. Zhang, M. Sakane, T. Nagasawa, and K. Kobayashi, "Mechanical Properties of Copper Thin Films Used in Electronic Devices," *Procedia Eng.*, vol. 10, no. Supplement C, pp. 1497–1502, Jan. 2011.

[156] A. Ibañez and E. Fatás, "Mechanical and structural properties of electrodeposited copper and their relation with the electrodeposition parameters," *Surf. Coat. Technol.*, vol. 191, no. 1, pp. 7–16, Feb. 2005.

[157] P. Dixit, L. Xu, J. Miao, J. H. L. Pang, and R. Preisser, "Mechanical and microstructural characterization of high aspect ratio through-wafer

electroplated copper interconnects," *J. Micromechanics Microengineering*, vol. 17, no. 9, p. 1749, 2007.

[158] A. A. Volinsky *et al.*, "Microstructure and Mechanical Properties of Electroplated Cu Thin Films," *MRS Online Proc. Libr. Arch.*, vol. 649, ed 2000.

[159] T. Pearson and J. K. Dennis, "Effect of pulsed reverse current on the structure and hardness of copper deposits obtained from acidic electrolytes containing organic additives," *Surf. Coat. Technol.*, vol. 42, no. 1, pp. 69–79, Oct. 1990.

[160] W. C. Oliver and G. M. Pharr, "An improved technique for determining hardness and elastic modulus using load and displacement sensing indentation experiments," *J. Mater. Res.*, vol. 7, no. 6, pp. 1564–1583, Jun. 1992.

[161] P. B. Lindley, "Effect of Poisson's ratio on compression modulus," *J. Strain Anal.*, vol. 3, no. 2, pp. 142–145, Apr. 1968.

[162] E. Barbarini, "SiC materials in EV/HEV Modules," p. 12.